AN-2103 LM25117 Evaluation Board

1 Introduction

The LM5117 evaluation board provides the design engineer with a fully functional synchronous buck converter based on Emulated Current Mode Control to evaluate the LM5117 controller IC. The evaluation board provides 12V output with a 9A current capability in addition with average output current information. The input voltage ranges from 15V to 55V.

2 Performance of the Evaluation Board

- Input Voltage Range: 15V to 55V
- Output Voltage: 12V
- Output Current: 9A
- Nominal Switching Frequency: 230 kHz
- Synchronous Buck Operation: Yes
- Diode Emulation Mode: Yes
- Hiccup Mode Overload Protection: Yes
- External VCC Sourcing: Yes
- Current Monitor Output: Yes

3 Powering and Loading Consideration

3.1 Proper Board Connection

When applying power to the LM5117 evaluation board certain precautions need to be followed. A misconnection can damage the assembly.

The input connection is made to the J1 (VIN+) and J2 (VIN-) connectors. The load is connected to the J3 (VOUT+) and J4 (VOUT-). Be sure to choose the correct connector and wire size when attaching the source power supply and the load. The average output current can be monitored at J5. Use RCA jack to remotely sense the current monitor output. TP5 is directly connected to UVLO and can be used as an input of the remote shutdown signal.

3.2 Source Power

The power supply and cabling must present low impedance to the evaluation board. Insufficient cabling or a high impedance power supply will droop during power supply application with the evaluation board inrush current. If large enough, this droop will cause a chattering condition upon power up. During power down, this insufficient cabling or a high impedance power supply will overshoot, results in a non-monotonic decay on the output.

An additional external bulk input capacitor may be required unless the output voltage droop/overshoot of the source power supply is less than 1V.

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3.3 Loading

When using an electronic load, it is strongly recommended to power up the evaluation board at light load and then slowly increase the load. If it is desired to power up the evaluation board at maximum load, resistor bank must be used. In general, electronic load is best suited for monitoring steady state waveforms.

3.4 Air Flow

Prolonged operation with high input voltage at full power will cause the MOSFETs to overheat. A fan with a minimum of 200LFM should be always provided.

3.4.1 Quick Start-Up Procedure

1. Set the power supply current limit to at least 16A. Connect the power supply to J1 and J2.
2. Connect the load with a 9A capacity between J3 and J4.
3. Set input voltage to 15V and turn it on.
4. Measure the output voltage. The output should be regulated at 12V.
5. Slowly increase the load current while monitoring the output voltage. The output should remain in regulation up to full load current.
6. Slowly sweep the input voltage from 15V to 55V while monitoring the output voltage. The output should remain in regulation.

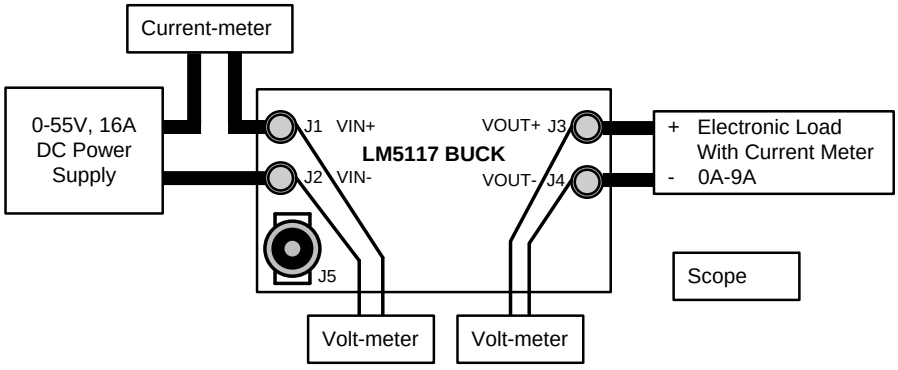

Figure 1. Typical Evaluation Setup

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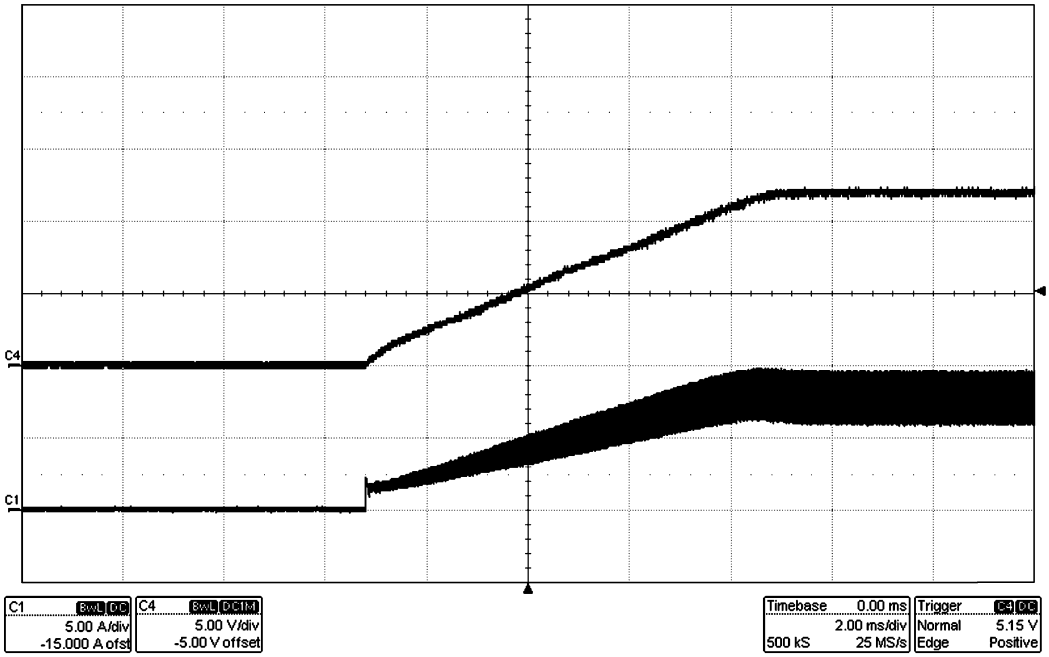
3.5 Waveforms

3.5.1 Soft Start

When applying power to the LM5117 evaluation board, a certain sequence of events occurs. Soft-start capacitor and other components allow for a linear increase in output voltage. Figure 2 shows the output voltage during a typical start-up with a load of 1.5Ω



Conditions:
Input Voltage = 48VDC
1.5Ω Load on the output
Traces:
Top Trace: Output Voltage, Volt/div = 5V
Bottom Trace: Inductor Current, Amp/div=5A
Horizontal Resolution = 2ms/div

Figure 2. Start-Up With Resistive Load

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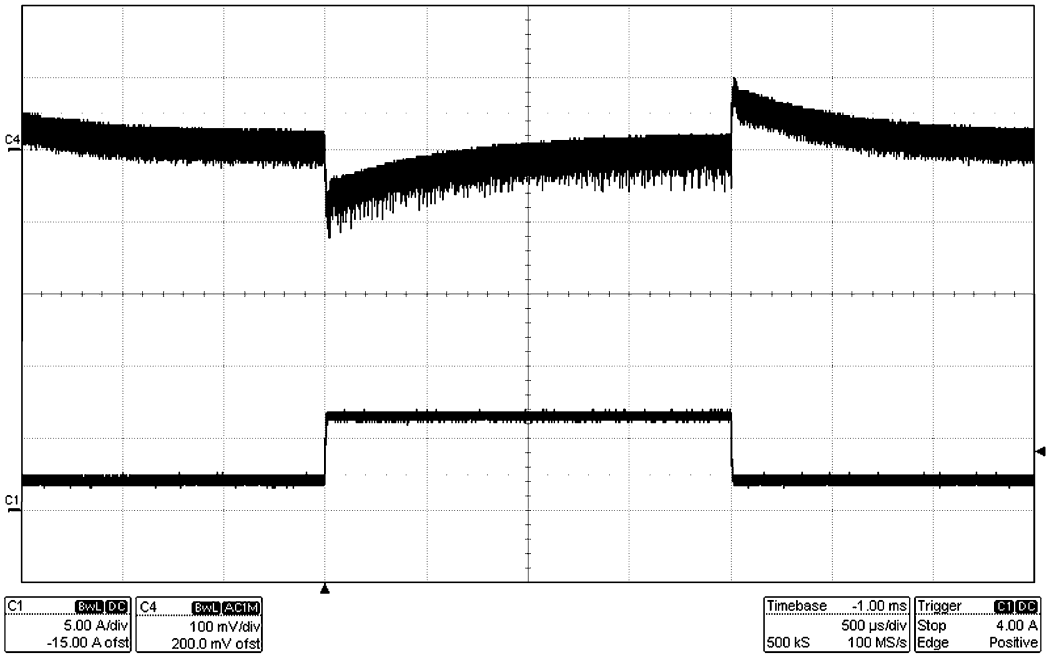
3.5.2 Load Transient

Figure 3 shows the transient response for a load of change from 2A to 6.5A. The upper waveform shows output voltage droop and overshoot during the sudden change in output current shown by the lower waveform.



Conditions:
Input Voltage = 48VDC
Output Current 2A to 6.5A
Traces:
Top Trace: Output Voltage
Volt/div = 100mV, AC coupled
Bottom Trace: Load Current, Amp/div = 5A
Horizontal Resolution = 0.5ms/div

Figure 3. Load Transient Response

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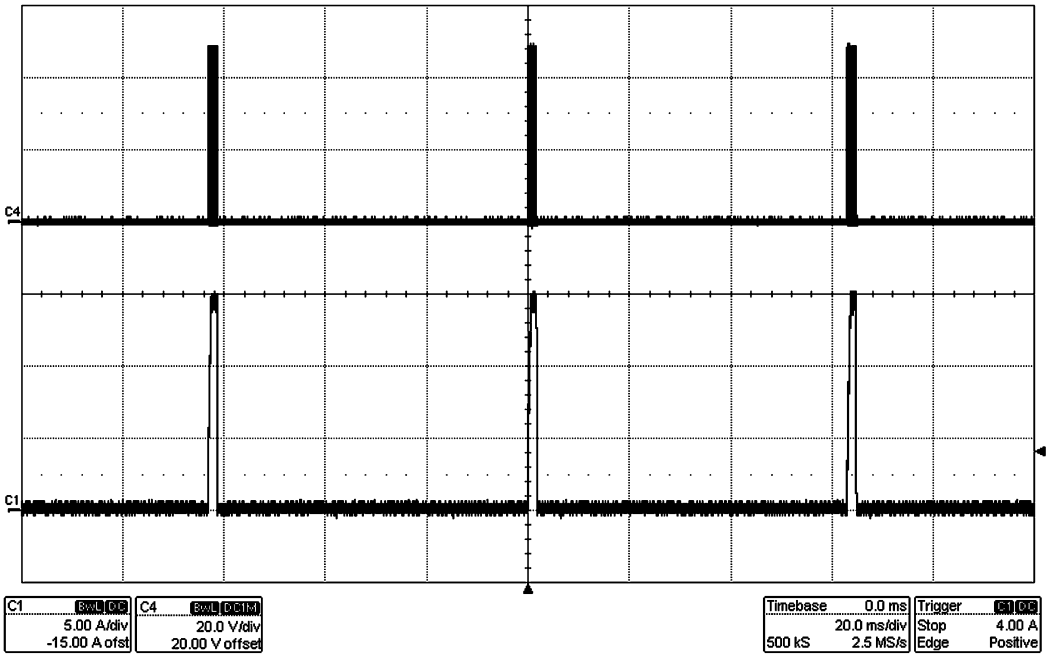
3.5.3 Overload Protection

The evaluation board is configured with hiccup mode overload protection. The restart time can be programmed by C20 restart capacitor. Figure 4 shows hiccup mode operation in the event of an output short.



Conditions:
Input Voltage = 48VDC
Output Short
Traces:
Top Trace: SW Voltage Volt/div = 20V
Bottom Trace: Inductor Current, Amp/div = 5A
Horizontal Resolution = 20ms/div

Figure 4. Short Circuit

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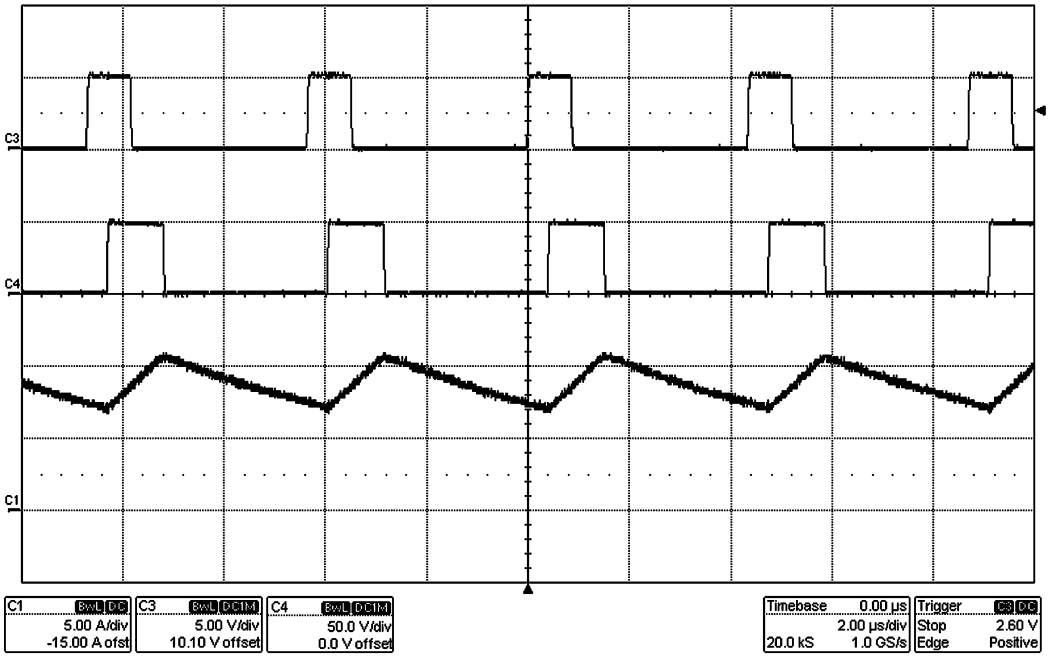
3.5.4 External Clock Synchronization

A TP3 (SYNC) test point has been provided on the evaluation board in order to synchronize the internal oscillator to the external clock. Figure 5 shows the synchronized switching operation.



Conditions:
Input Voltage = 48VDC
Load Current = 9A
Traces:
Top Trace: SYNC pulse, 20% duty cycle, Volt/div = 5V
Middle Trace: SW voltage, Volt/div = 50V
Bottom Trace: Inductor Current, Amp/div = 5A
Horizontal Resolution = 2µs/div

Figure 5. Clock Synchronization

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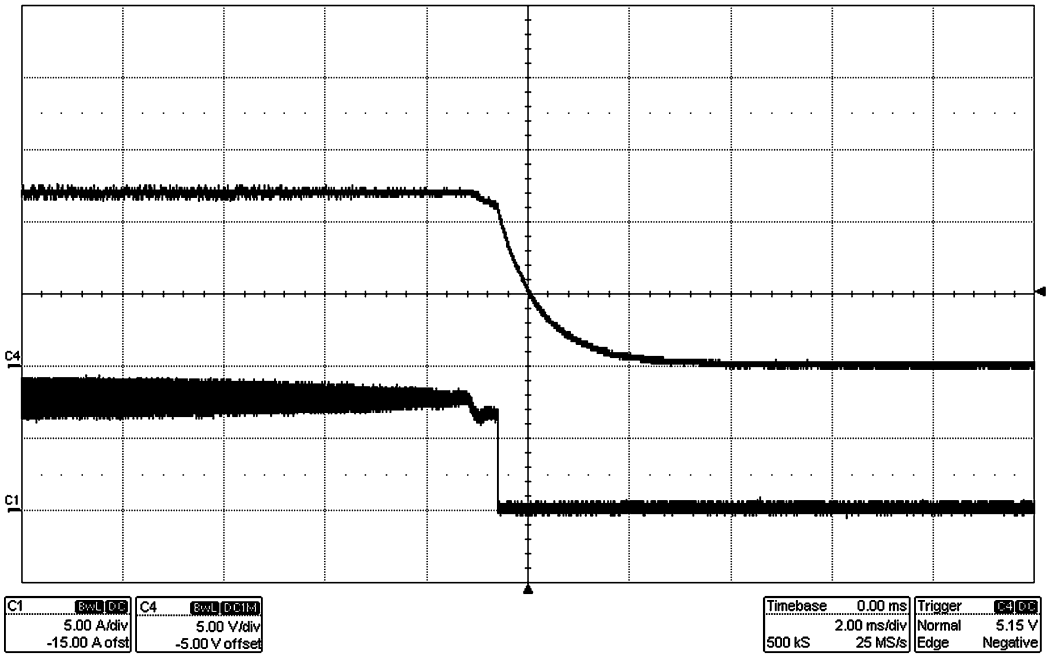
3.5.5 Shutdown

Figure 6 shows the shutdown procedure by powering off the source power. When UVLO pin voltage is less than 1.26V, the switching stops and soft-start capacitor is discharged by internal switches.



Conditions:
Input Voltage = 48VDC
1.5Ω Load on the Output
Traces:
Top Trace: Output Voltage, Volt/div = 5V
Bottom Trace: Inductor Current, Amp/div = 5A
Horizontal Resolution = 2ms/div

Figure 6. Shutdown

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3.6 Performance Characteristics

Figure 7 shows the efficiency curves. During the efficiency measurement, monitor the current into and out of the evaluation board and monitor the voltage directly at the input and output terminals of the evaluation board.

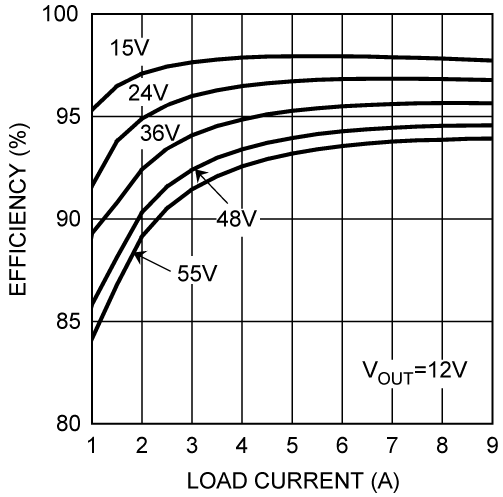

Figure 7. Typical Efficiency vs Load Current

3.7 Board Configuration

3.7.1 Loop Response

TP6 and TP7 have been provided in order to measure the loop transfer function. For detail information about the loop transfer function measurement, see *AN-1889 How to Measure the Loop Transfer Function of Power Supplies* (SNVA364).

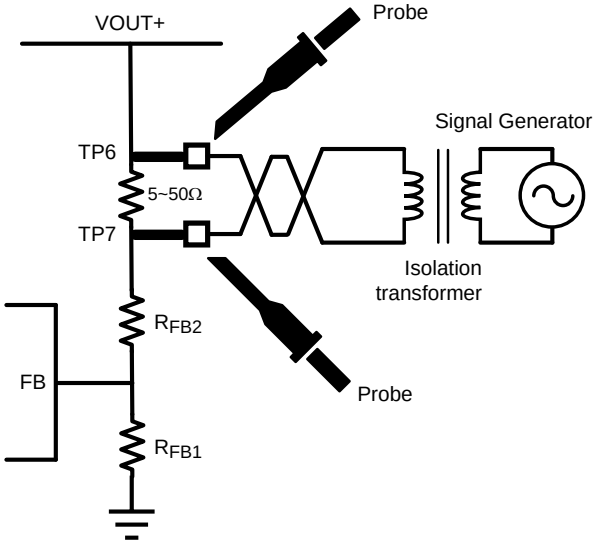

Figure 8. Loop Response Measurement Setup

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3.7.2 External VCC Supply

External VCC supply helps to reduce the temperature and the power loss of the LM5117 at high input voltage. By populating D1 and R7, VCC can be supplied from the output. In this evaluation board, VCC is supplied from 12V output to achieve high efficiency.

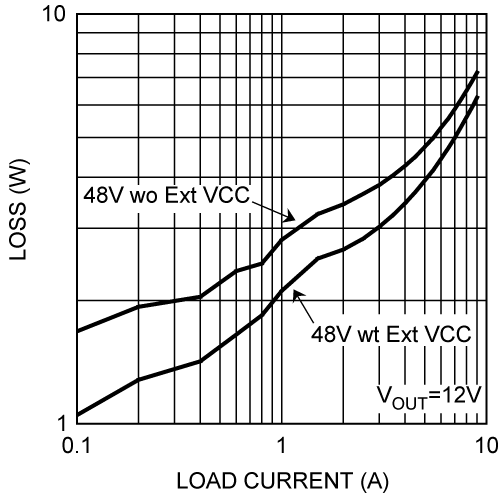

Figure 9. Loss Comparison at 48V; With External VCC vs Without External VCC

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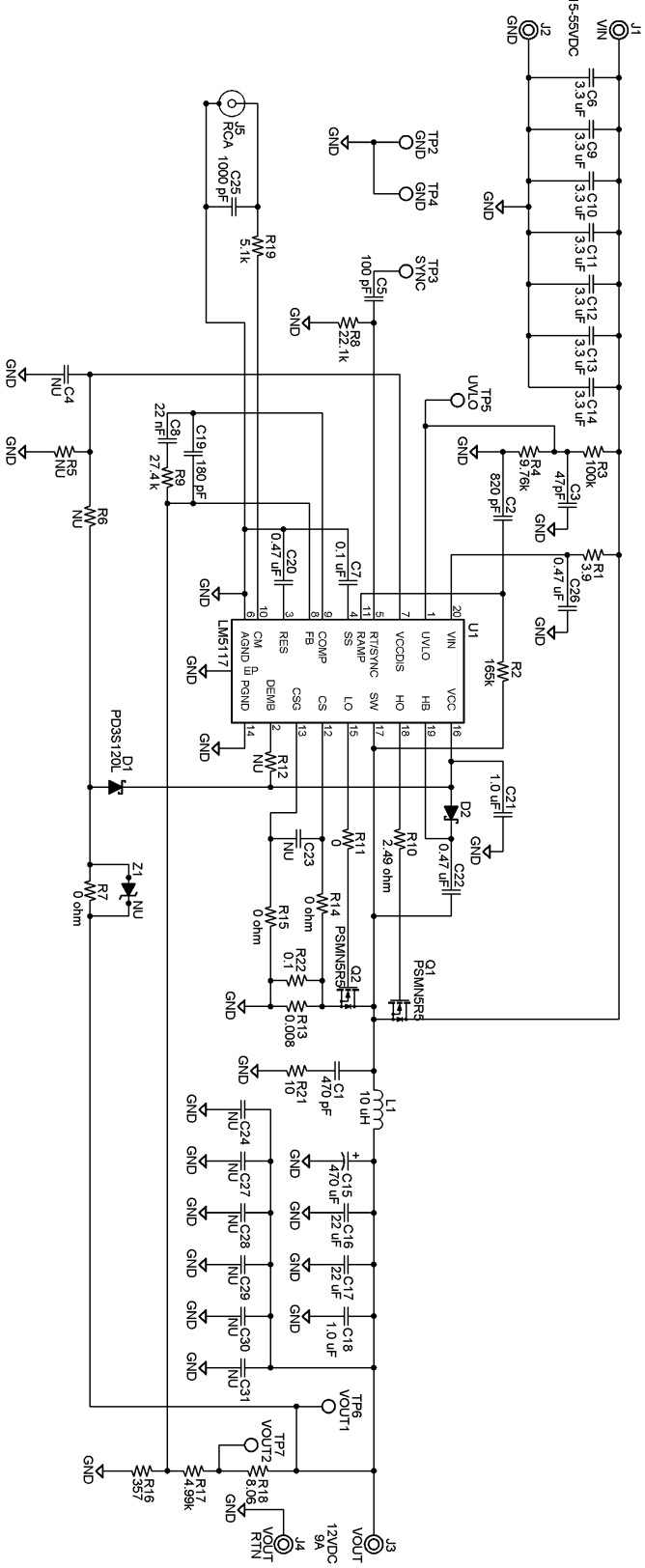
3.8 Evaluation Board Schematic



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3.9 Bill of Materials (BOM)

Part	Value	Package	Part Number	Manufacturer
C1	470pF, 100V, C0G	0805	C2012C0G2A471J	TDK
C2	820pF, 50V, C0G	0603	C1608C0G1H821J	TDK
C3	47p, 50V, C0G	0603	C1608C0G1H470J	TDK
C4, C23	NU	0603		
C5	100pF, 50V, C0G	0603	C1608C0G1H101J	TDK
C6, C9, C10, C11, C12, C13, C14	3.3µF, 100V, X7S	1210	C3225X7S2A335K	TDK
C7	0.1µF, 25V, X7R	0603	C1608X7R1E104K	TDK
C8	0.022µF, 50V, X7R	0603	06035C223JAT2A	AVX
C15	470µF, 16V, 20mΩ	Φ10	PCG1C471MCL1GS	NICHICON
C16, C17	22µF, 16V, X7R	2220	C5750X7R1C226M	TDK
C18, C21	1µF, 16V, X7R	0603	C1608X7R1C105K	TDK
C19	180pF, 50V, C0G	0603	C1608C0G1H181J	TDK
C20, C22	0.47µF, 25V, X7R	0603	GRM188R71E474KA12	MURATA
C24, C27, C28, C29, C30, C31	NU	2220		
C25	1000pF, 50V, X7R	0603	C1608X7R1H102K	TDK
C26	0.47µF, 100V, X7R	0805	GRM21BR72A474KA73	MURATA
R1	3.9 ohm, 5%	0805	CRCW08053R90JNEA	VISHAY
R2	165k, 1%	0805	MCR10EZPF1653	ROHM
R3	100k, 1%	0805	CRCW0805100KFKEA	VISHAY
R4	9.76k, 1%	0603	CRCW06039K76FKEA	VISHAY
R5, R6, R12	NU	0603		
R7, R11, R14, R15	0 ohm	0603	MCR03EZPJ000	ROHM
R8	22.1k, 1%	0603	CRCW060322K1FKEA	VISHAY
R9	27.4k, 1%	0603	CRCW060327K4FKEA	VISHAY
R10	2.49 ohm, 1%	0603	CRCW06032R49FKEA	VISHAY
R13	0.008 ohm, 1W, 1%	0815	RL3720WT-R008-F	SUSUMU
R16	357 ohm, 1%	0603	CRCW0603357RFKEA	VISHAY
R17	4.99k, 1%	0603	CRCW06034K99FKEA	VISHAY
R18	8.06 ohm, 1%	0805	CRCW08058R06FKEA	VISHAY
R19	5.1k, 5%	0603	CRCW06035K10JNEA	VISHAY
R21	10 ohm, 1%	2010	CRCW201010R0FKEF	VISHAY
R22	0.1 ohm, 1%	1206	MCR18EZHFLR100	ROHM
D1	20V, 1A	PowerDI323	PD3S120L	DIODES
D2	60V, 1A	SOD123F	PMEG6010CEH	NXP
Z1	NU	SOT89		
L1	10µH, 15A / 21.5A	18.2x18.3	74435561100	WE
Q1, Q2	60V, 100A	LFPAK SO-8	PSMN5R5-60YS	NXP
U1		HTSSOP-20	LM5117	TI
J1, J2, J3, J4	Terminal-Turret		1509	KEYSTONE
J5	RCA Jack, Blue		RCJ-025	CUI
TP2, TP3, TP4, TP5, TP6, TP7	Test Point		1040	KEYSTONE

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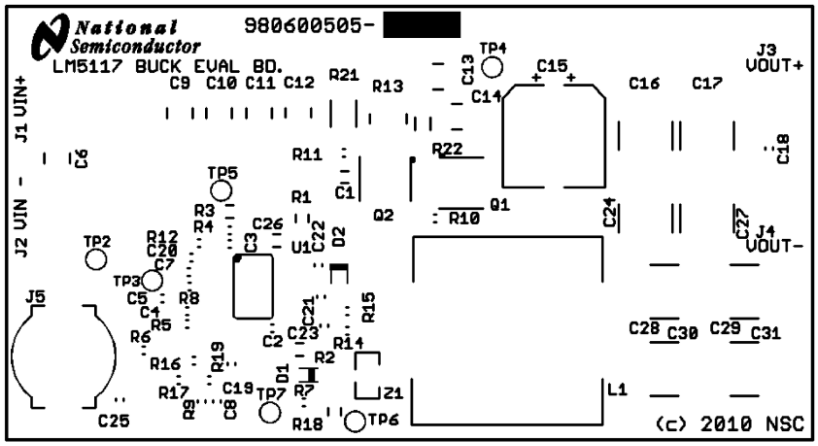
3.10 PC Board Layout



TOP SILKSCREEN (.PLC) LAYER AS VIEWED FROM TOP

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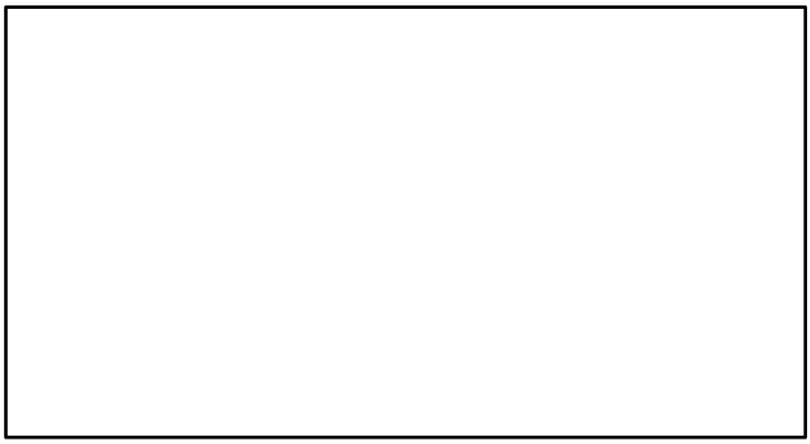

BOTTOM SILKSCREEN (.BPL) LAYER AS VIEWED FROM TOP

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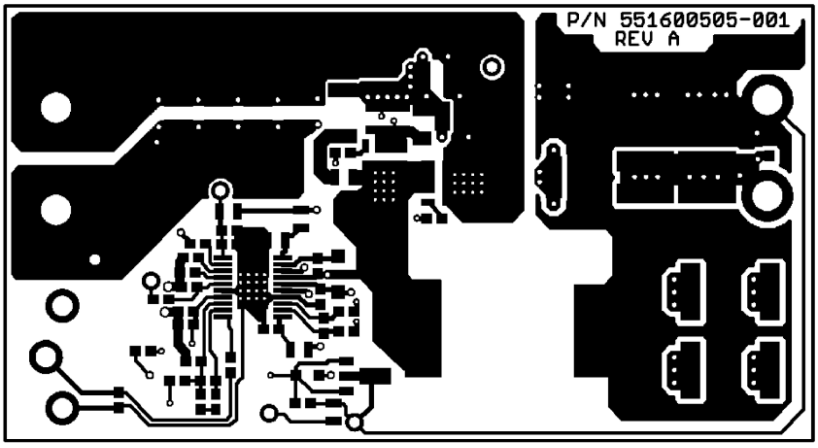

TOP (.CMP) LAYER AS VIEWED FROM TOP

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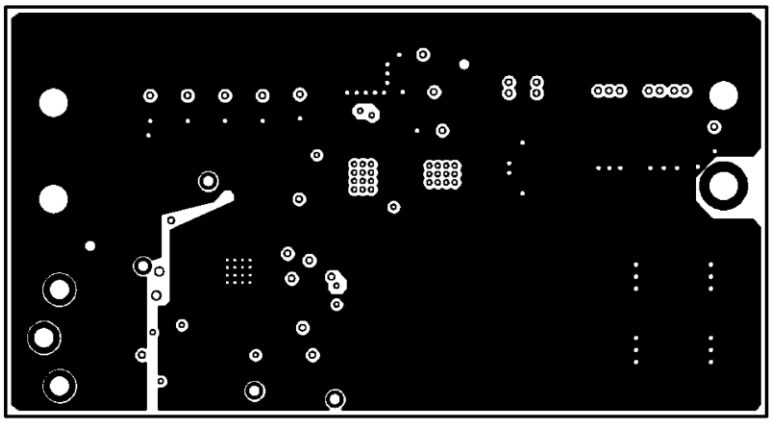

LAYER 2 (.LY2) AS VIEWED FROM TOP

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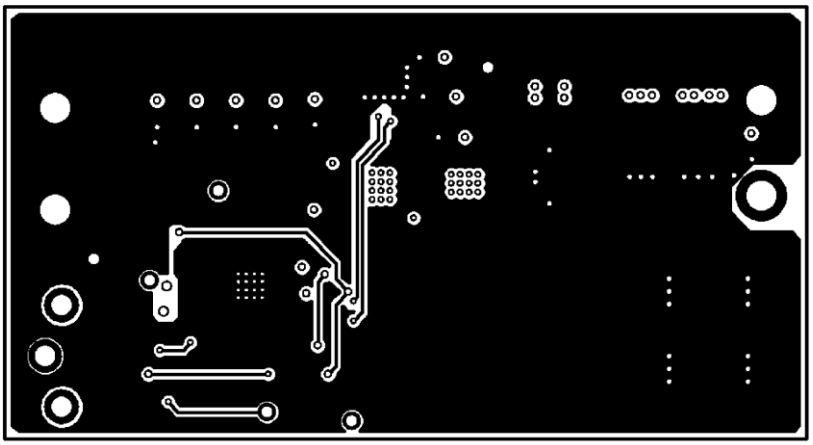

LAYER 3 (.LY3) AS VIEWED FROM TOP

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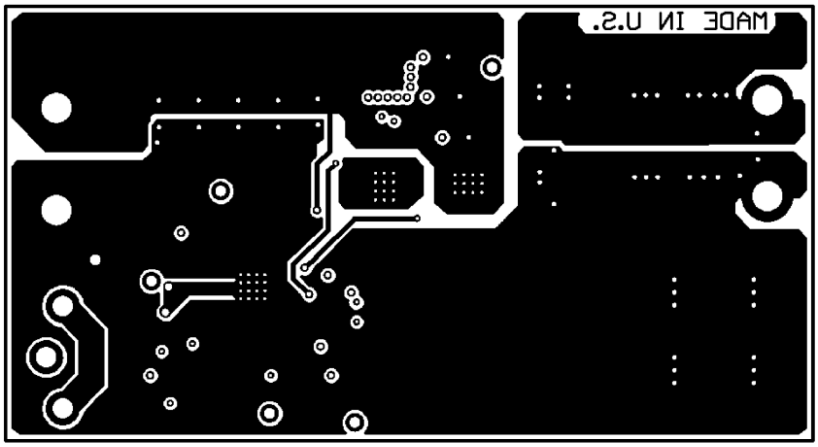

BOTTOM (.SOL) LAYER AS VIEWED FROM TOP

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