

SN54ALS874B, SN74ALS874B, SN74ALS876A SN74AS874, SN74AS876 DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

SDAS061C – APRIL 1982 – REVISED JANUARY 1995

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Choice of True or Inverting Logic
 - SN54ALS874B, SN74ALS874B, SN74AS874 Have True Outputs
 - SN74ALS876A, SN74AS876 Have Inverting Outputs
- Asynchronous Clear
- Package Options Include Plastic Small-Outline (DW) Packages, Plastic (FN) and Ceramic (FK) Chip Carriers, and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

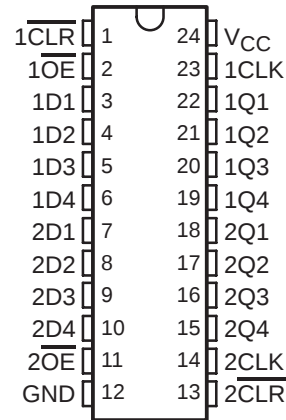
description

These dual 4-bit D-type edge-triggered flip-flops feature 3-state outputs designed specifically as bus drivers. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

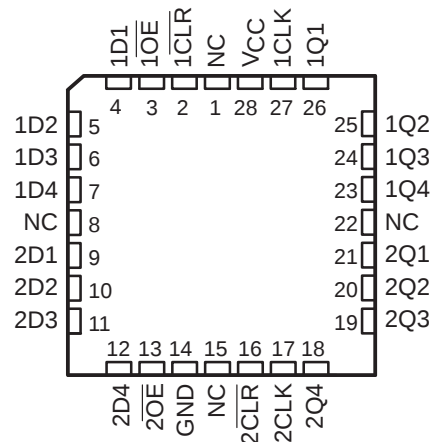
The edge-triggered flip-flops enter data on the low-to-high transition of the clock (CLK) input. The SN54ALS874B, SN74ALS874B, and SN74AS874 have clear ($\overline{\text{CLR}}$) inputs and noninverting Q outputs. The SN74ALS876A and SN74AS876 have preset ($\overline{\text{PRE}}$) inputs and inverting $\overline{\text{Q}}$ outputs; taking $\overline{\text{PRE}}$ low causes the four Q or $\overline{\text{Q}}$ outputs to go low independently of the clock.

The SN54ALS874B is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS874B, SN74ALS876A, SN74AS874, and SN74AS876 devices are characterized for operation from 0°C to 70°C .

SN54ALS874B . . . JT PACKAGE
SN74ALS874B, SN74AS874 . . . DW OR NT PACKAGE
(TOP VIEW)

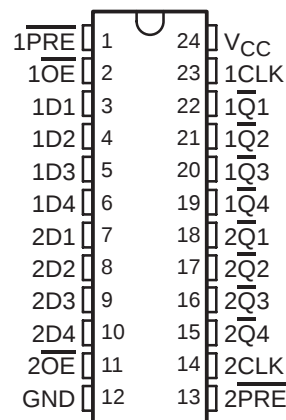


SN54ALS874B . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

SN74ALS876A, SN74AS876 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS874B, SN74ALS874B, SN74ALS876A SN74AS874, SN74AS876 DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

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Function Tables

SN54ALS874B, SN74ALS874B, SN74AS874
(each flip-flop)

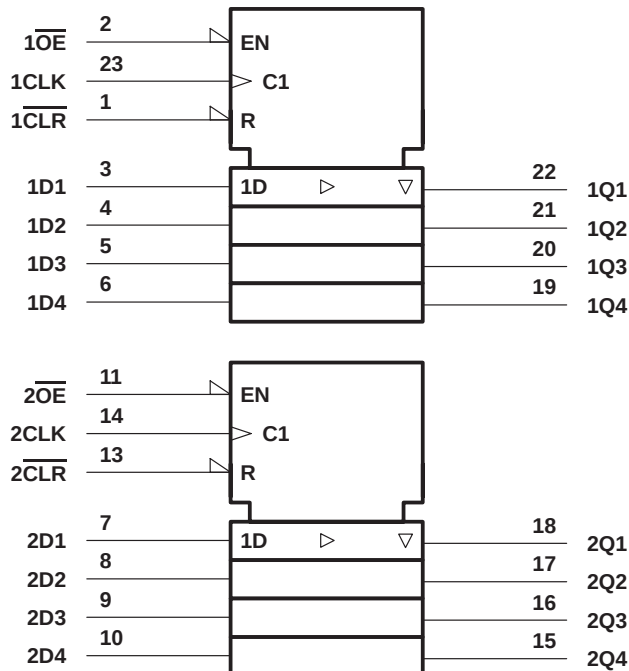
INPUTS				OUTPUT Q
$\overline{OE}$	$\overline{CLR}$	CLK	D	
L	L	X	X	L
L	H	$\uparrow$	H	H
L	H	$\uparrow$	L	L
L	H	L	X	Q_0
H	X	X	X	Z

SN74ALS876A, SN74AS876
(each flip-flop)

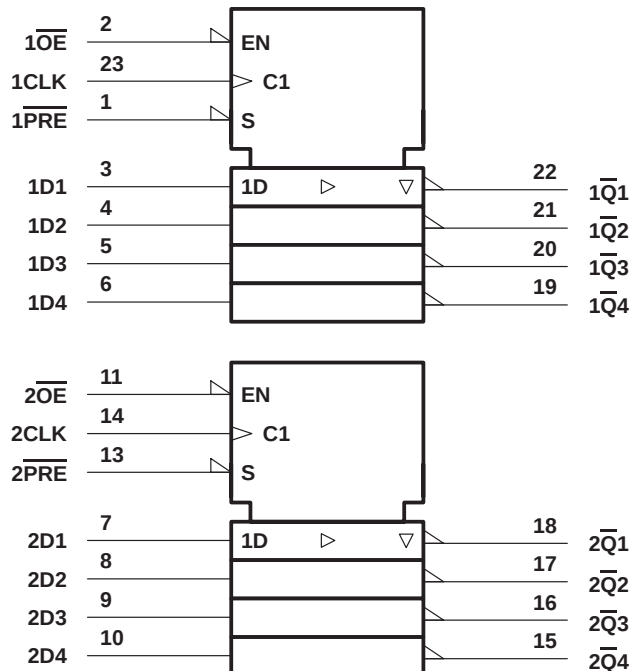
INPUTS				OUTPUT $\overline{Q}$
$\overline{OE}$	$\overline{PRE}$	CLK	D	
L	L	X	X	L
L	H	$\uparrow$	H	L
L	H	$\uparrow$	L	H
L	H	L	X	$\overline{Q_0}$
H	X	X	X	Z

logic symbols[†]

SN54ALS874B, SN74ALS874B, SN74AS874



SN74ALS876A, SN74AS876

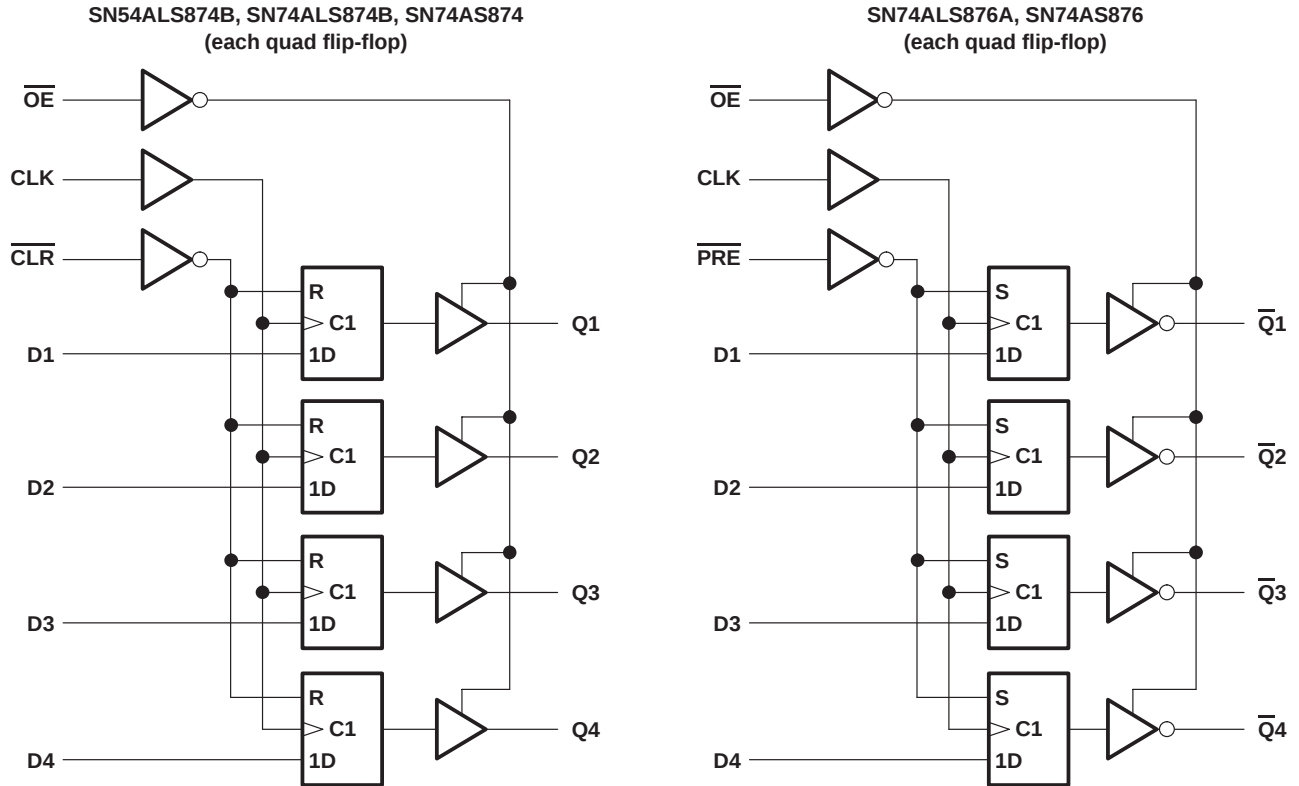


[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

SN54ALS874B, SN74ALS874B, SN74ALS876A
SN74AS874, SN74AS876
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

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logic diagrams (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A : SN54ALS874B	–55°C to 125°C
SN74ALS874B, SN74ALS876A	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



SN54ALS874B, SN74ALS874B, SN74ALS876A

SN74AS874, SN74AS876

DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

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recommended operating conditions

			SN54ALS874B			SN74ALS874B SN74ALS876A			UNIT		
			MIN	NOM	MAX	MIN	NOM	MAX			
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V		
V _{IH}	High-level input voltage		2			2			V		
V _{IL}	Low-level input voltage				0.7			0.8	V		
I _{OH}	High-level output current				−1			−2.6	mA		
I _{OL}	Low-level output current				12			24	mA		
f _{clock}	Clock frequency		0		25	0		30	MHz		
t _w	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	15			10			ns		
		CLK high	20			16.5					
		CLK low	20			16.5					
t _{su}	Setup time before CLK↑	Data	15			15			ns		
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	15			10					
t _h	Hold time, data after CLK↑		4			0			ns		
T _A	Operating free-air temperature		−55			125			0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS874B			SN74ALS874B SN74ALS876A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA				-1.2			-1.2	V
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA		V _{CC} - 2			V _{CC} - 2			V
		V _{CC} = 4.5 V, I _{OH} = -1 mA		2.4	3.3					
		V _{CC} = 4.5 V, I _{OH} = -2.6 mA					2.4	3.2		
V _{OL}		V _{CC} = 4.5 V, I _{OL} = 12 mA		0.25	0.4		0.25	0.4		V
		V _{CC} = 4.5 V, I _{OL} = 24 mA					0.35	0.5		
I _{OZH}		V _{CC} = 5.5 V, V _O = 2.7 V				20			20	μA
I _{OZL}		V _{CC} = 5.5 V, V _O = 0.4 V				-20			-20	μA
I _I		V _{CC} = 5.5 V, V _I = 7 V				0.1			0.1	mA
I _{IH}		V _{CC} = 5.5 V, V _I = 2.7 V				20			20	μA
I _{IL}		V _{CC} = 5.5 V, V _I = 0.4 V				-0.2			-0.2	mA
I _O ‡		V _{CC} = 5.5 V, V _O = 2.25 V		-20		-112	-30		-112	mA
I _{CC}	'ALS874B	V _{CC} = 5.5 V	Outputs high	14	21		14	21		mA
			Outputs low	19	30		19	30		
			Outputs disabled	20	32		20	32		
	SN74ALS876A	V _{CC} = 5.5 V	Outputs high				14	21		
			Outputs low				18	29		
			Outputs disabled				20	31		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS874B, SN74ALS874B, SN74ALS876A
SN74AS874, SN74AS876
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

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switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX†				UNIT
			SN54ALS874B		SN74ALS874B		
			MIN	MAX	MIN	MAX	
f _{max}			25		30		MHz
t _{PLH}	CLK	Any Q	4	18	4	14	ns
t _{PHL}			4	16	4	14	
t _{PHL}	$\overline{\text{CLR}}$	Any Q	5	23	5	17	ns
t _{PZH}	$\overline{\text{OE}}$	Any Q	4	24	4	18	ns
t _{PZL}			4	21	4	18	
t _{PHZ}	$\overline{\text{OE}}$	Any Q	2	15	2	10	ns
t _{PLZ}			3	22	3	12	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX†		UNIT
			SN74ALS876A		
			MIN	MAX	
f _{max}			30		MHz
t _{PLH}	CLK	Any $\overline{Q}$	4	14	ns
t _{PHL}			4	14	
t _{PHL}	$\overline{PRE}$	Any $\overline{Q}$	6	19	ns
t _{PZH}	$\overline{OE}$	Any $\overline{Q}$	4	18	ns
t _{PZL}			4	18	
t _{PHZ}	$\overline{OE}$	Any $\overline{Q}$	2	10	ns
t _{PLZ}			3	13	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V _{CC}	7 V
Input voltage, V _I	7 V
Operating free-air temperature range, T _A : SN74AS874, SN74AS876	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



SN54ALS874B, SN74ALS874B, SN74ALS876A

SN74AS874, SN74AS876

DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

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recommended operating conditions

			SN74AS874			SN74AS876			UNIT		
			MIN	NOM	MAX	MIN	NOM	MAX			
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V		
V _{IH}	High-level input voltage		2			2			V		
V _{IL}	Low-level input voltage		0.8			0.8			V		
I _{OH}	High-level output current		−15			−15			mA		
I _{OL}	Low-level output current		48			48			mA		
f _{clock}	Clock frequency		0	125		0	80		MHz		
t _w	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	2			4.5			ns		
		CLK high	3			6.2					
		CLK low	4			6.2					
t _{su}	Setup time before CLK↑	Data	2			4.5			ns		
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	4			5					
t _h	Hold time, data after CLK↑		1			2			ns		
T _A	Operating free-air temperature		0			70	0			70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74AS874 SN74AS876			UNIT
				MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = –18 mA				–1.2	V
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = –2 mA		V _{CC} – 2			V
		V _{CC} = 4.5 V, I _{OH} = –15 mA		2.4	3.3		
V _{OL}		V _{CC} = 4.5 V, I _{OL} = 48 mA		0.35	0.5		V
I _{OZH}		V _{CC} = 5.5 V, V _O = 2.7 V			50		μA
I _{OZL}		V _{CC} = 5.5 V, V _O = 0.4 V			–50		μA
I _I		V _{CC} = 5.5 V, V _I = 7 V			0.1		mA
I _{IH}		V _{CC} = 5.5 V, V _I = 2.7 V			20		μA
I _{IL}	D	V _{CC} = 5.5 V, V _I = 0.4 V			–2		mA
	All others				–0.5		
I _O ‡		V _{CC} = 5.5 V, V _O = 2.25 V		–30		–112	mA
I _{CC}	SN74AS874	V _{CC} = 5.5 V	Outputs high		82	133	mA
			Outputs low		92	149	
			Outputs disabled		100	160	
	SN74AS876	V _{CC} = 5.5 V	Outputs high		88	142	
			Outputs low		94	150	
			Outputs disabled		100	160	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS874B, SN74ALS874B, SN74ALS876A
SN74AS874, SN74AS876
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switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX†		UNIT
			SN74AS874		
			MIN	MAX	
f _{max}			125		MHz
t _{PLH}	CLK	Any Q	3	8.5	ns
t _{PHL}			4	10.5	
t _{PHL}	$\overline{\text{CLR}}$	Any Q	4	9.5	ns
t _{PZH}	$\overline{\text{OE}}$	Any Q	2	7	ns
t _{PZL}			3	10.5	
t _{PHZ}	$\overline{\text{OE}}$	Any Q	2	6	ns
t _{PLZ}			2	7.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX†		UNIT
			SN74AS876		
			MIN	MAX	
f _{max}			80		MHz
t _{PLH}	CLK	Any $\overline{Q}$	3	8.5	ns
t _{PHL}			4	10.5	
t _{PHL}	$\overline{PRE}$	Any $\overline{Q}$	4	9.5	ns
t _{PZH}	$\overline{OE}$	Any $\overline{Q}$	2	7	ns
t _{PZL}			3	11	
t _{PHZ}	$\overline{OE}$	Any $\overline{Q}$	2	7	ns
t _{PLZ}			2	7	

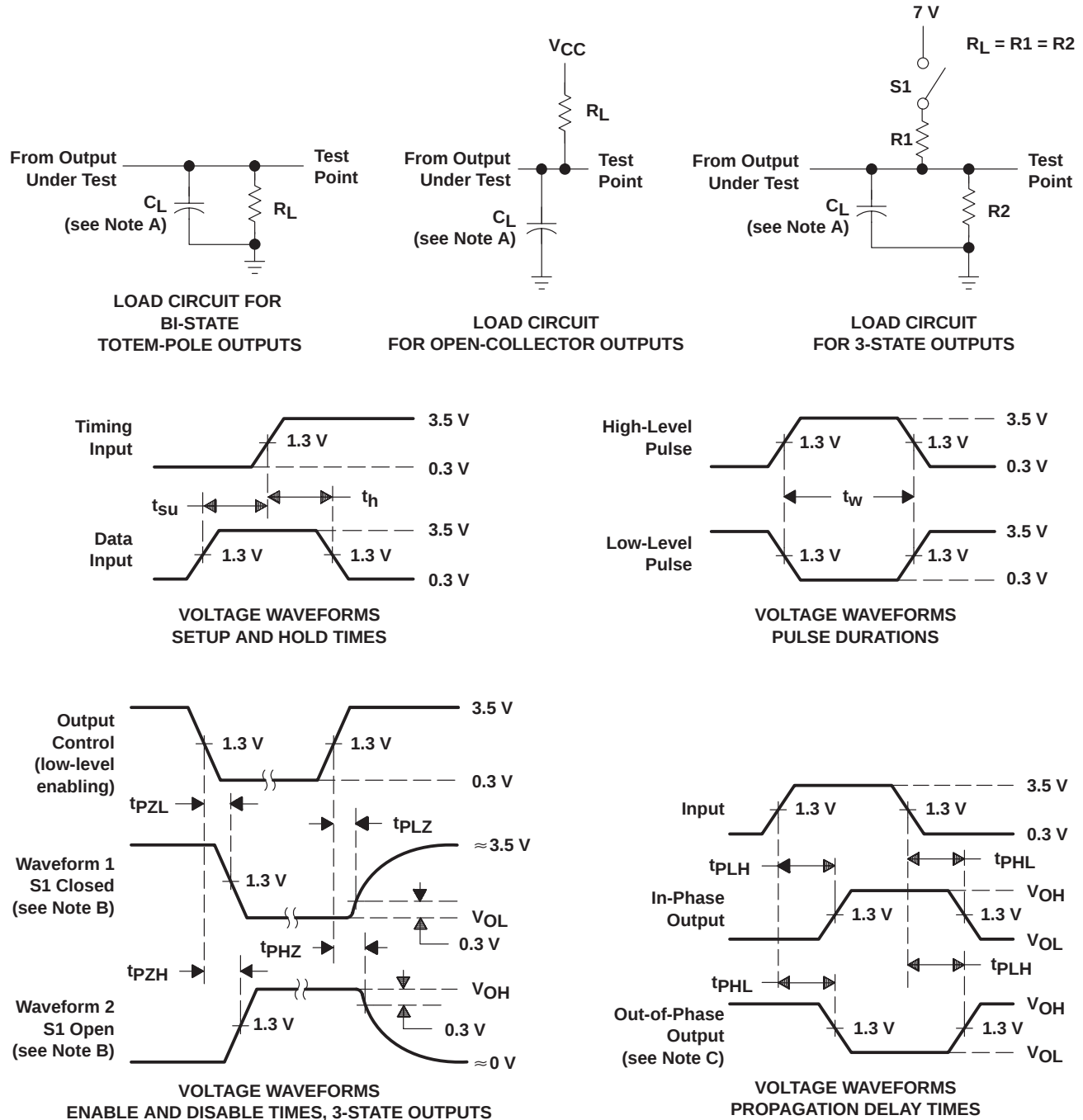
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS874B, SN74ALS874B, SN74ALS876A
SN74AS874, SN74AS876
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

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PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: PRR $\leq$ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
8401001LA	ACTIVE	CDIP	JT	24	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8401001LA SNJ54ALS874BJT	Samples
SN54ALS874BJT	ACTIVE	CDIP	JT	24	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SN54ALS874BJT	Samples
SN74ALS874BDW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS874B	Samples
SN74ALS874BDWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS874B	Samples
SN74ALS874BDWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS874B	Samples
SN74AS874DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS874	Samples
SNJ54ALS874BJT	ACTIVE	CDIP	JT	24	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8401001LA SNJ54ALS874BJT	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54ALS874B, SN74ALS874B :

- Catalog: [SN74ALS874B](#)
- Military: [SN54ALS874B](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS874BDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

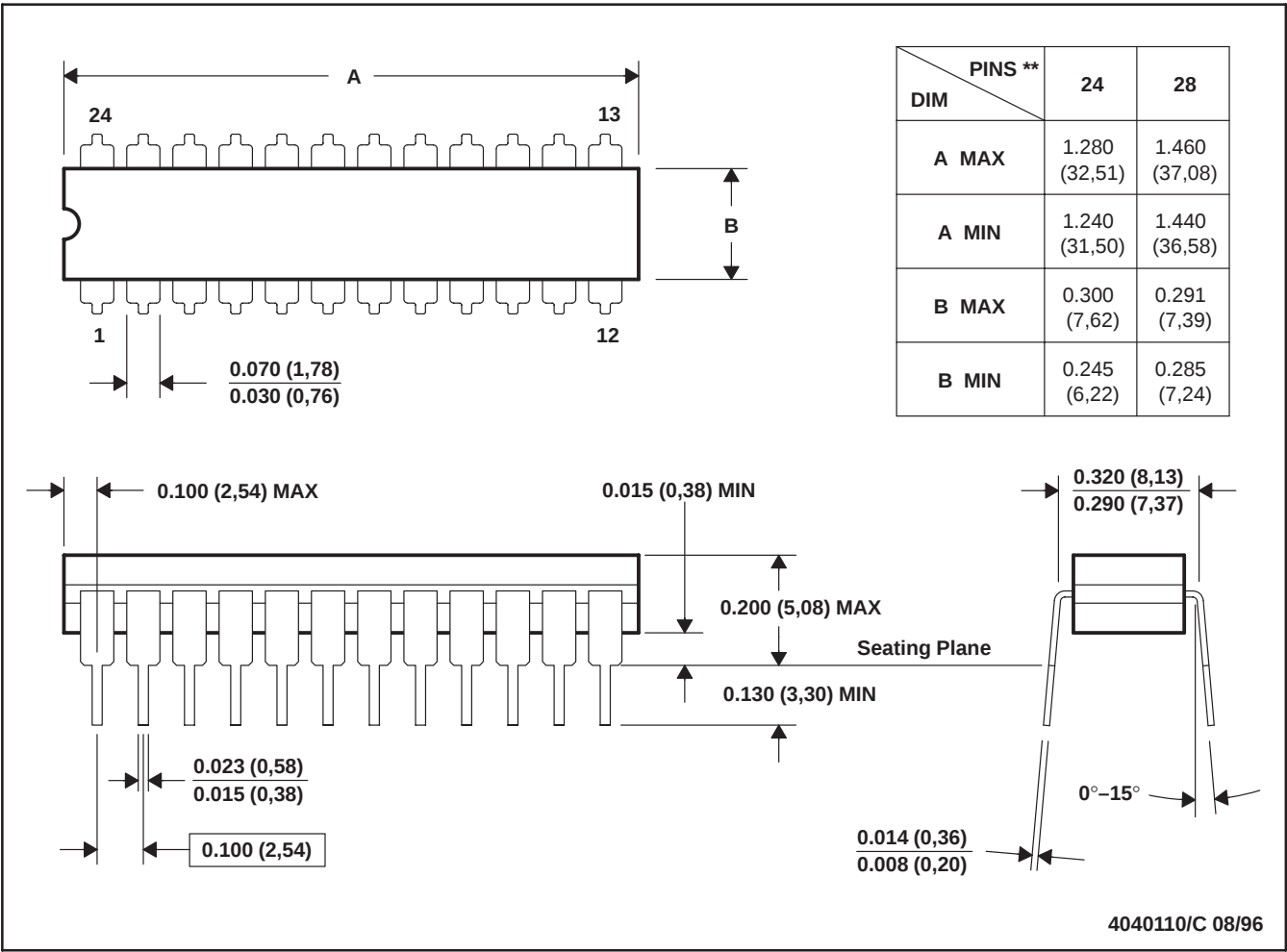


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS874BDWR	SOIC	DW	24	2000	350.0	350.0	43.0

JT (R-GDIP-T**)
24 LEADS SHOWN

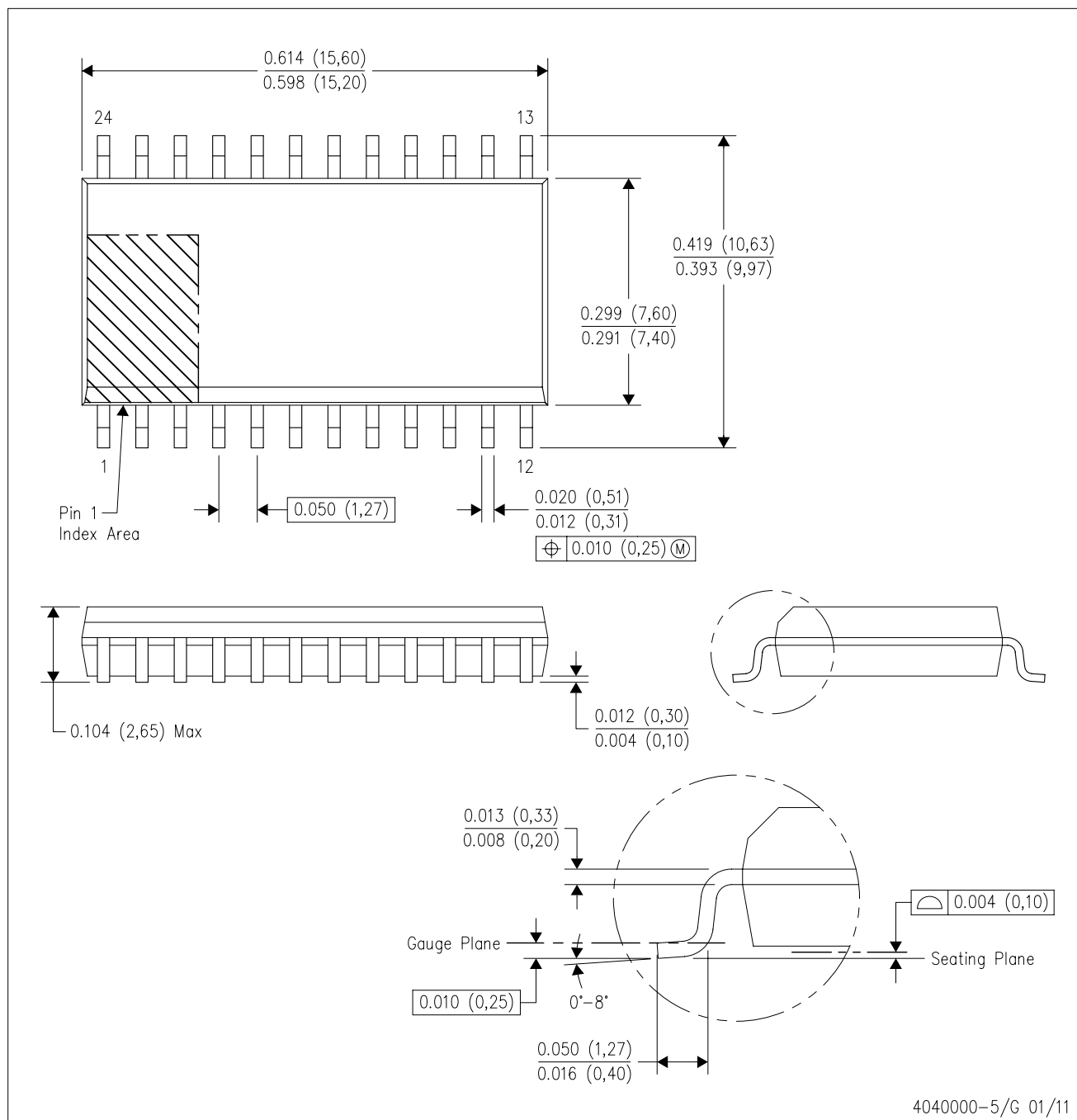
CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

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