CSD18536KTT 60 V N-Channel NexFET™ Power MOSFET

1 Features

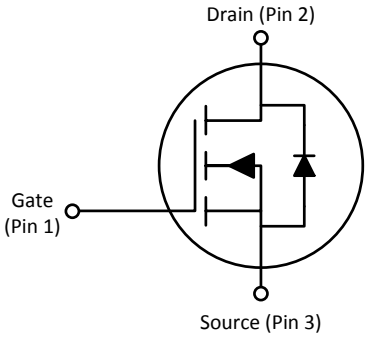
- Ultralow Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- D^2PAK Plastic Package

2 Applications

- Secondary Side Synchronous Rectifier
- Motor Control

3 Description

This 60-V, 1.3-mΩ, D^2PAK (TO-263) NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	60		V
Q_g	Gate Charge Total (10 V)	108		nC
Q_{gd}	Gate Charge Gate-to-Drain	14		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V	1.7	mΩ
		V_{GS} = 10 V	1.3	mΩ
$V_{GS(th)}$	Threshold Voltage	1.8		V

Ordering Information(1)

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD18536KTT	500	13-Inch Reel	D^2PAK Plastic Package	Tape & Reel
CSD18536KTTT	50			

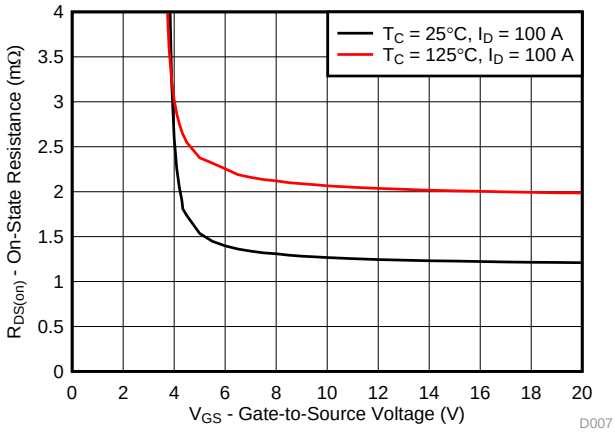
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package limited)	200	A
	Continuous Drain Current (Silicon limited), T_C = 25°C	349	A
	Continuous Drain Current (Silicon limited), T_C = 100°C	247	A
I_{DM}	Pulsed Drain Current (1)	400	A
P_D	Power Dissipation	375	W
T_J, T_{stg}	Operating Junction and Storage Temperature	–55 to 175	°C
E_{AS}	Avalanche Energy, Single Pulse I_D = 128 A, L = 0.1 mH, R_G = 25 Ω	819	mJ

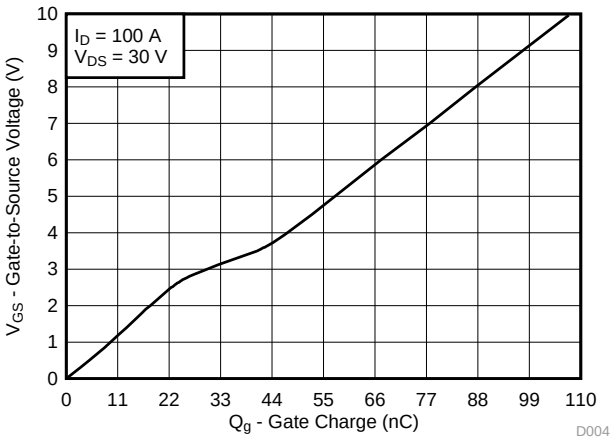
(1) Max $R_{\theta JC}$ = 0.4°C/W, pulse duration ≤100 µs, duty cycle ≤1%

$R_{DS(on)}$ vs V_{GS}



D007

Gate Charge



D004

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

DATE	REVISION	NOTES
March 2016	*	Initial release.

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5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 48 V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.4	1.8	2.2	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 4.5 V, I_D = 100 A		1.7	2.2	mΩ
		V_{GS} = 10 V, I_D = 100 A		1.3	1.6	mΩ
g_{fs}	Transconductance	V_{DS} = 6 V, I_D = 100 A		312		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 30 V, f = 1 MHz		8790	11430	pF
C_{oss}	Output capacitance			1410	1840	pF
C_{rss}	Reverse transfer capacitance			39	51	pF
R_G	Series gate resistance			0.7	1.4	Ω
Q_g	Gate charge total (10 V)	V_{DS} = 30 V, I_D = 100 A		108	140	nC
Q_{gd}	Gate charge gate-to-drain			14		nC
Q_{gs}	Gate charge gate-to-source			18		nC
$Q_{g(th)}$	Gate charge at V_{th}			17		nC
Q_{oss}	Output charge	V_{DS} = 30 V, V_{GS} = 0 V		230		nC
$t_{d(on)}$	Turn on delay time	V_{DS} = 30 V, V_{GS} = 10 V, I_{DS} = 100 A, R_G = 0 Ω		11		ns
t_r	Rise time			5		ns
$t_{d(off)}$	Turn off delay time			24		ns
t_f	Fall time			4		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 100 A, V_{GS} = 0 V		0.9	1.0	V
Q_{rr}	Reverse recovery charge	V_{DS}= 30 V, I_F = 100 A, di/dt = 300 A/µs		323		nC
t_{rr}	Reverse recovery time			86		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			0.4	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance			62	°C/W

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5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

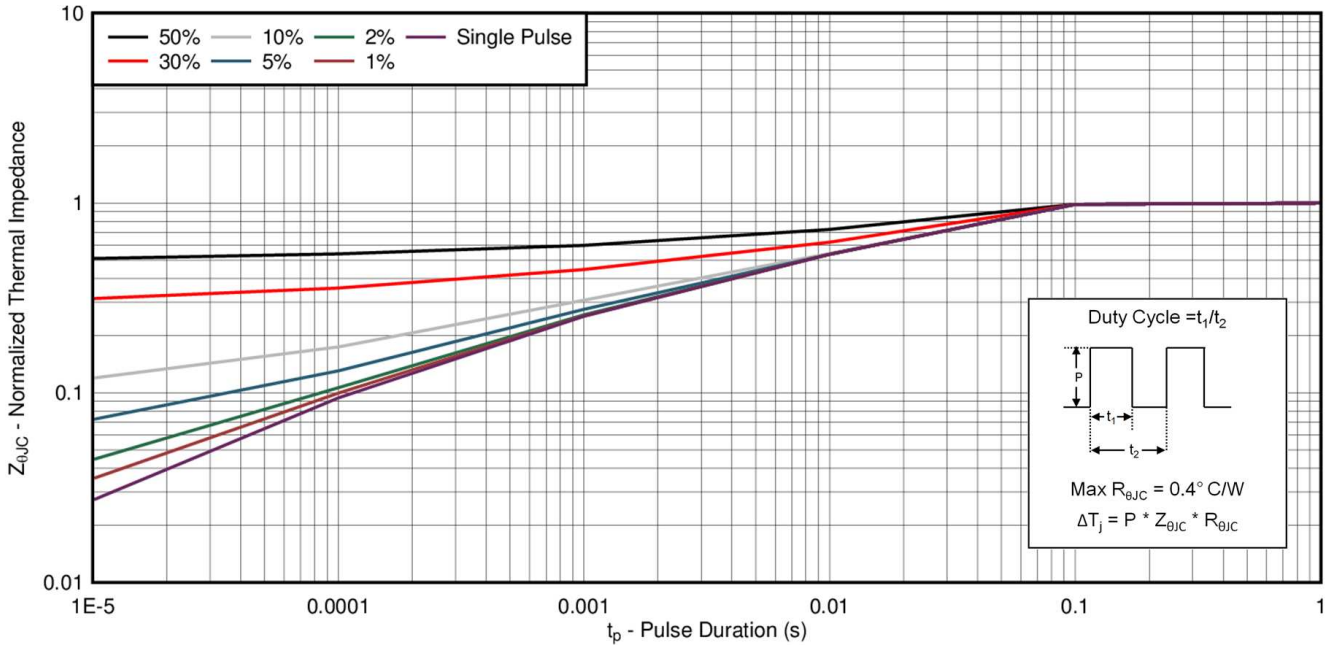


Figure 1. Transient Thermal Impedance

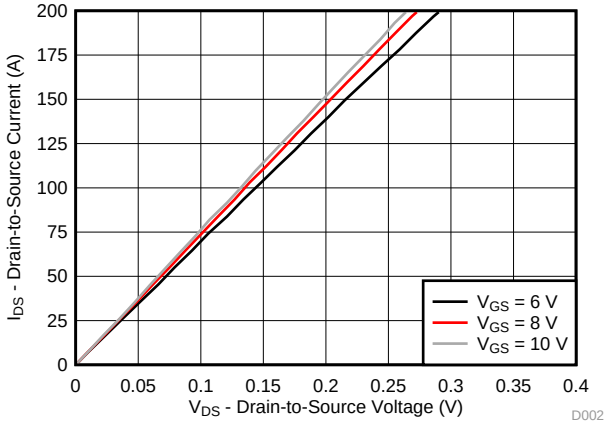


Figure 2. Saturation Characteristics

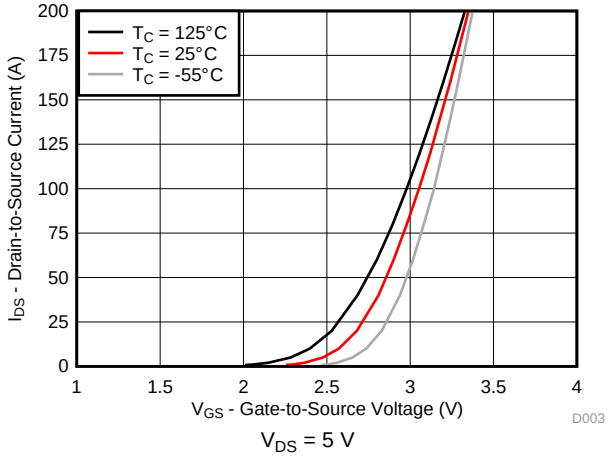


Figure 3. Transfer Characteristics

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Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

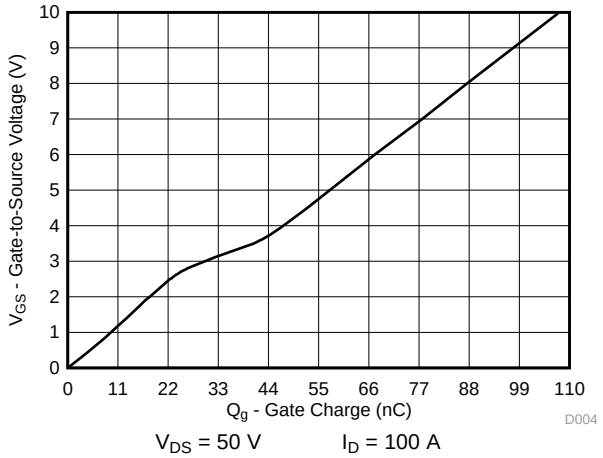


Figure 4. Gate Charge

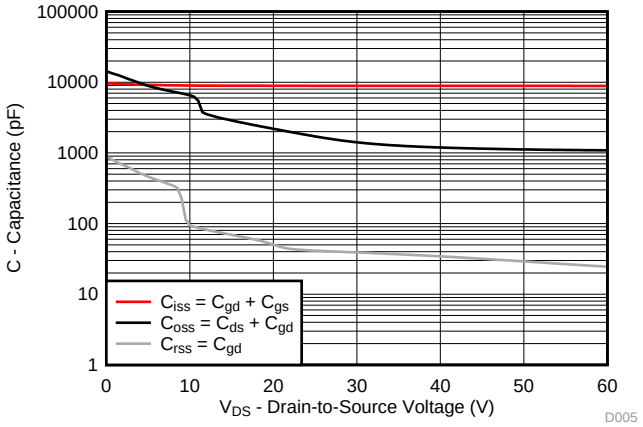


Figure 5. Capacitance

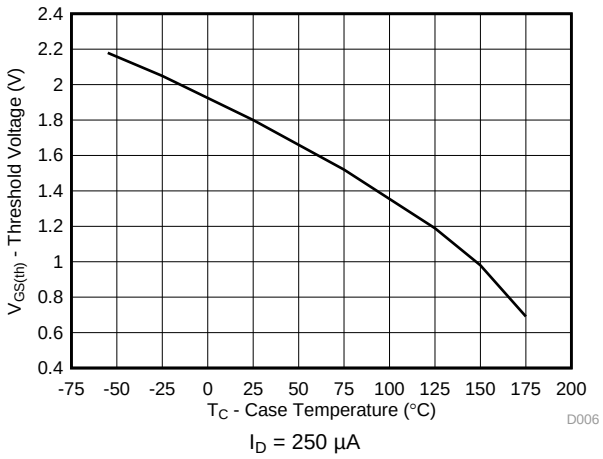


Figure 6. Threshold Voltage vs Temperature

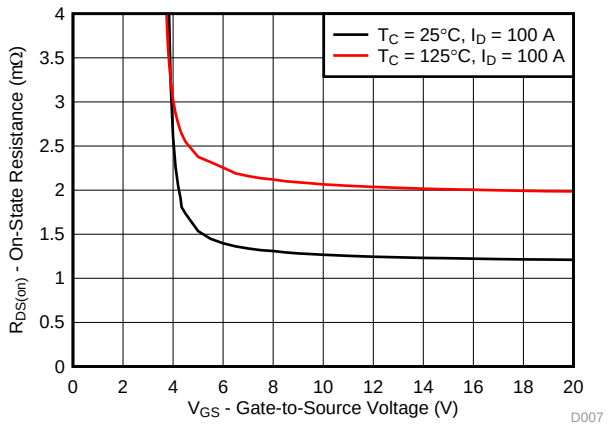


Figure 7. On-State Resistance vs Gate-to-Source Voltage

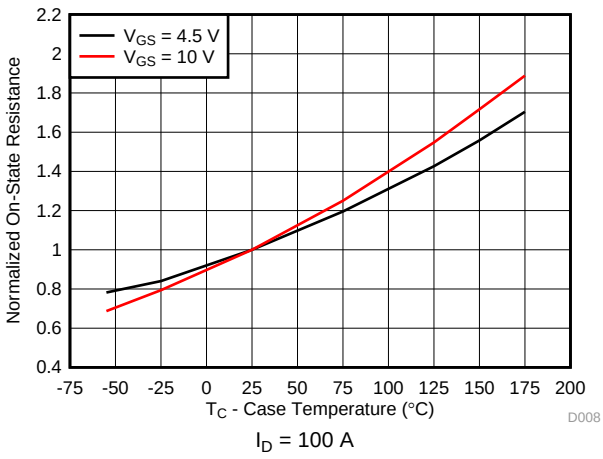


Figure 8. Normalized On-State Resistance vs Temperature

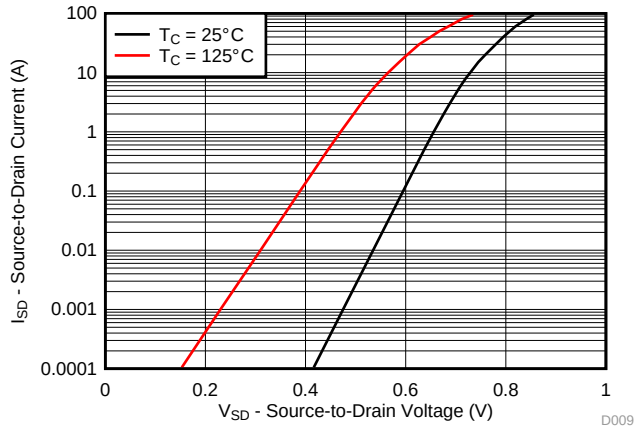


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

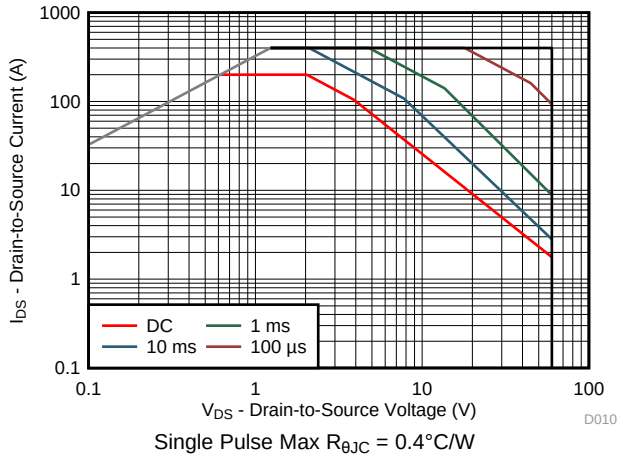


Figure 10. Maximum Safe Operating Area

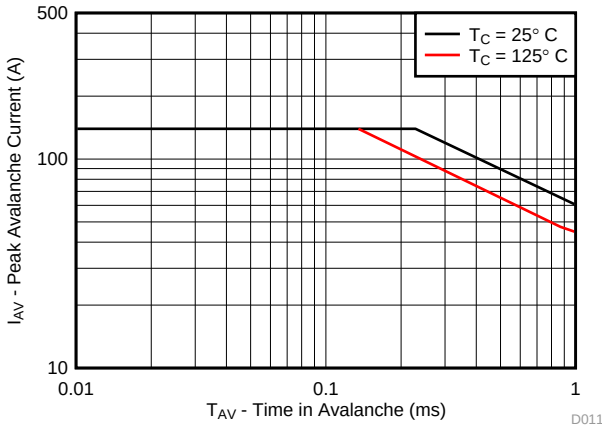


Figure 11. Single Pulse Unclamped Inductive Switching

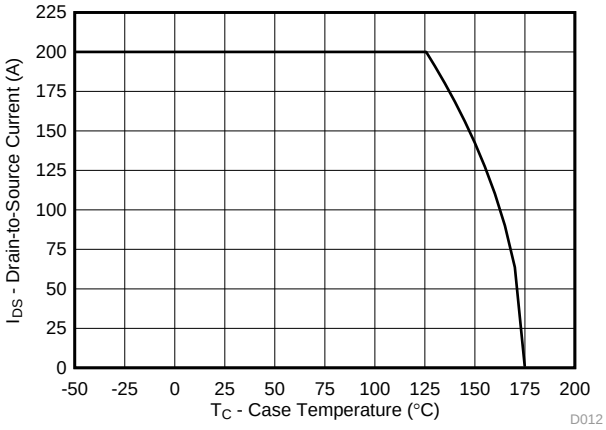


Figure 12. Maximum Drain Current vs Temperature

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6 Device and Documentation Support

6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.4 Glossary

SLYZ022 — *TI Glossary*.

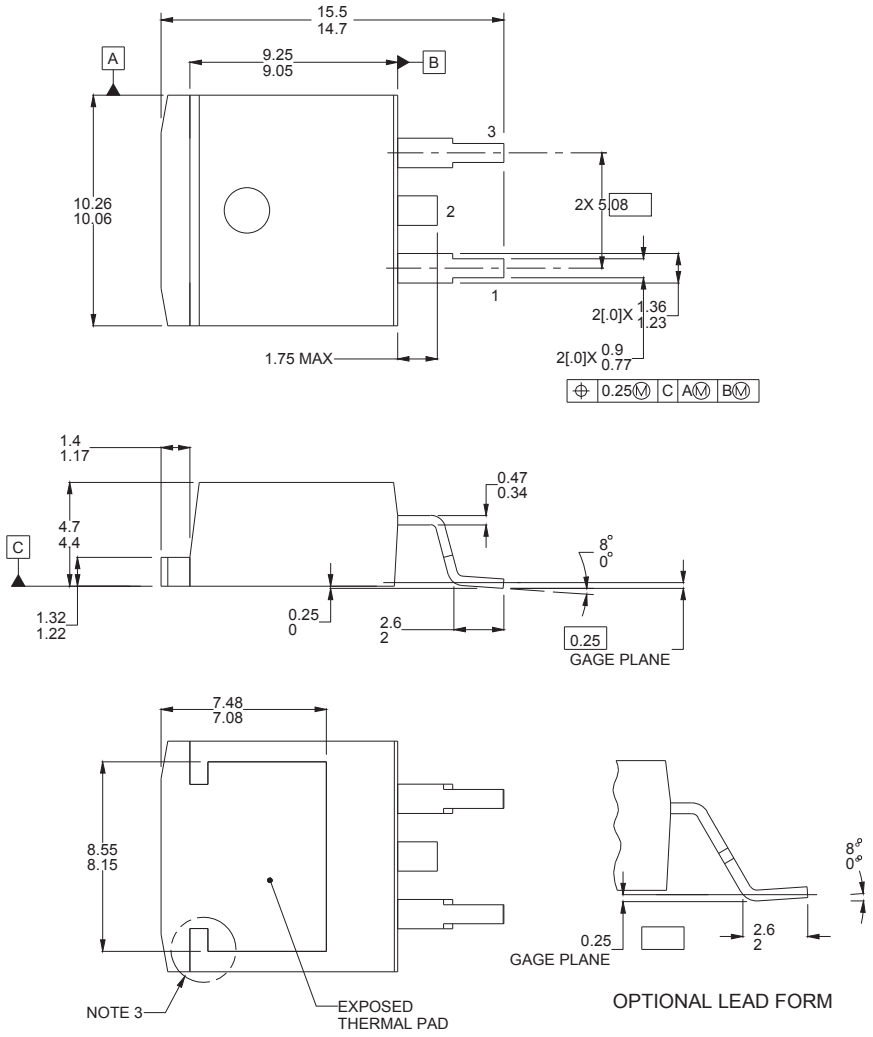
This glossary lists and explains terms, acronyms, and definitions.

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7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 KTT Package Dimensions



Notes:

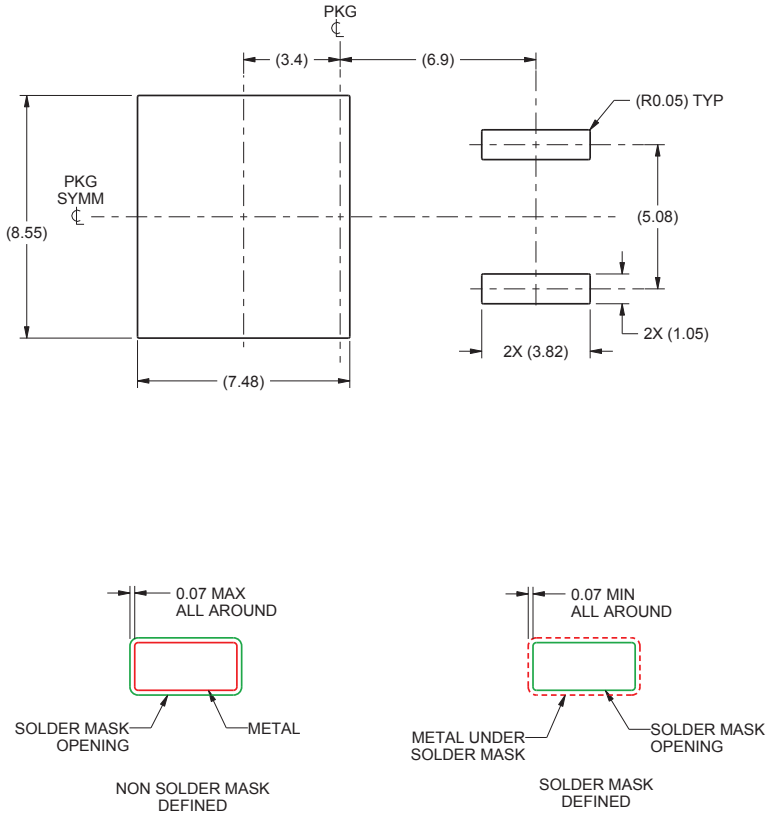
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Features may not exist and shape may vary per different assembly sites.

Pin Configuration

POSITION	DESIGNATION
Pin 1	Gate
Pin 2 / Tab	Drain
Pin 3	Source

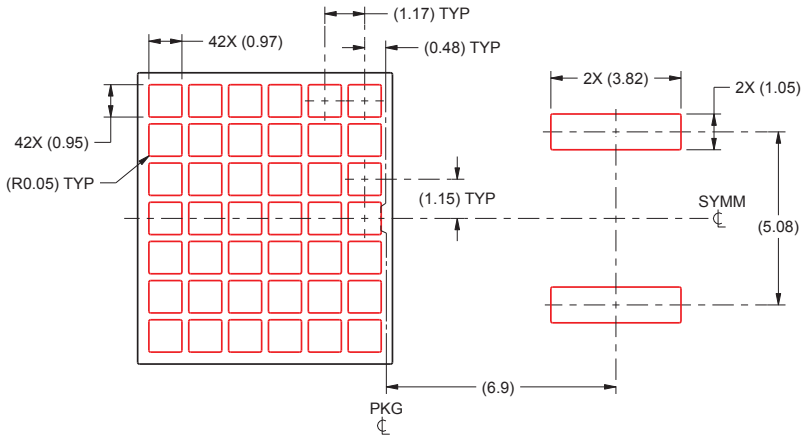
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7.2 Recommended PCB Pattern



For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

7.3 Recommended Stencil Opening (0.125 mm Stencil Thickness)



Notes:

1. This package is designed to be soldered to a thermal pad on the board. See application notes, *PowerPAD Thermally Enhanced Package* (SLMA002) and *PowerPAD Made Easy* (SLMA004) for more information.
2. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
3. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18536KTT	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-55 to 175	CSD18536KTT	Samples
CSD18536KTTT	ACTIVE	DDPAK/ TO-263	KTT	3	50	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-55 to 175	CSD18536KTT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

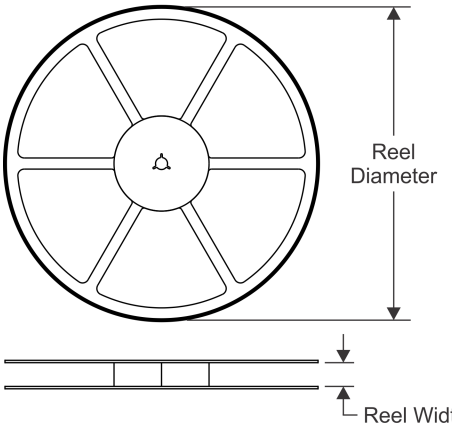
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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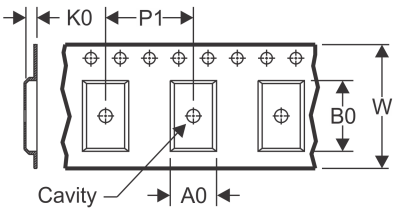
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

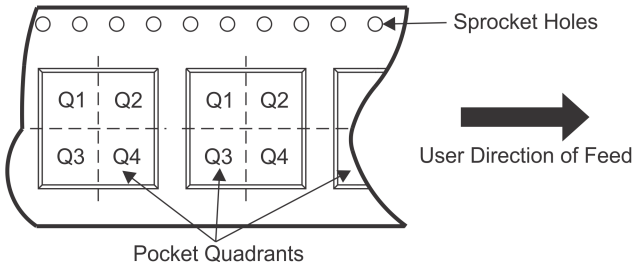


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

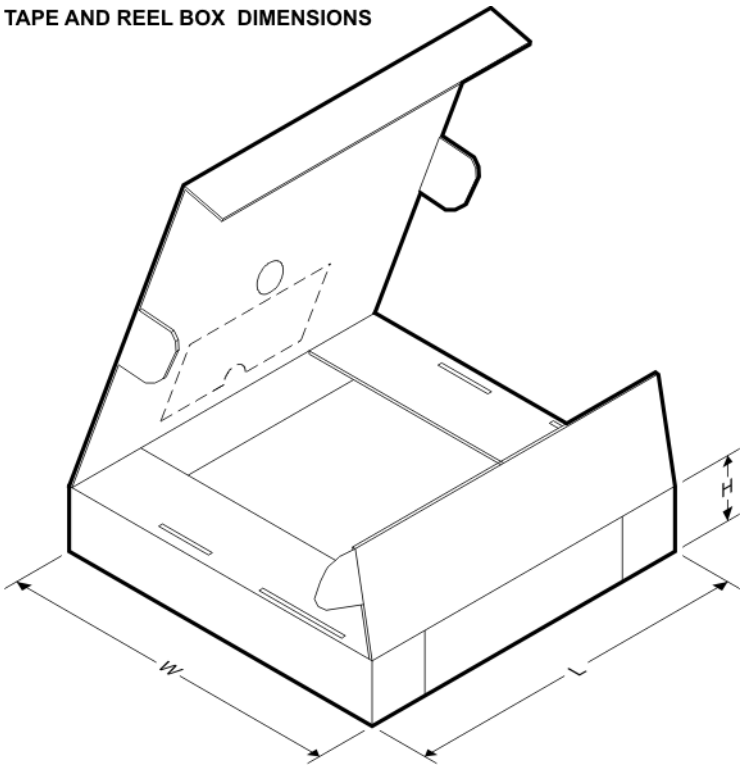
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD18536KTT	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
CSD18536KTTT	DDPAK/ TO-263	KTT	3	50	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD18536KTT	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
CSD18536KTTT	DDPAK/TO-263	KTT	3	50	340.0	340.0	38.0

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