PIC18F65/66K40 Family
Silicon Errata and Data Sheet Clarification

The PIC18F65/66K40 family devices that you have received conform functionally to the current Device Data Sheet (DS40001842**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F65/66K40 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F65/66K40 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	DEVICE ID<13:0>(1),(2)	Revision ID for Silicon Revision	
		A3	A4
PIC18F65K40	6B00h	A003	A004
PIC18LF65K40	6B60h	A003	A004
PIC18F66K40	6AE0h	A003	A004
PIC18LF66K40	6B40h	A003	A004

Note 1: The Device ID is located in addresses 3FFFFCh-3FFFFDh and 3FFFFEh-3FFFFFh.

2: Refer to the *"PIC18(L)F6xK40 Memory Programming Specification"* (DS40001822) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item No.	Issue Summary	Affected Revisions(1)	
				A3	A4
Analog-to-Digital Converter (ADC)	ADC Conversion	1.1	Delay of one instruction cycle required prior to setting the ADGO bit when using ADCRC as the ADCC clock source.	X	
Analog-to-Digital Converter (ADC)	Computation Overflow Bit	1.2	The Computation Overflow bit may be erroneously set by the ADFLTR.	X	
Analog-to-Digital Converter (ADC)	ADCRC Oscillator Operation in Sleep	1.3	The ADCRC oscillator does not stop after conversion is complete in Sleep mode.	X	X
Analog-to-Digital Converter (ADC)	ADC Conversion with FVR	1.4	Using the FVR as the ADC positive voltage reference can cause missing codes.	X	X
PIC18 Debug Executive	Data Write Match Breakpoints	2.1	Data write match breakpoints do not work when used on a location GPR space.	X	
PIC18 Core	TBLRD	3.1	TBLRD requires NVMREG value to point to appropriate memory.	X	
Program Flash Memory	Endurance of PFM Cell	4.1	Endurance of the PFM cell is lower than specified.	X	X
MSSP	SMBus 2.0 Voltage Level	5.1	Input low voltage threshold level is dependent on V_{DD}.	X	X
Electrical Specifications for LF Devices Only	Min V_{DD} Specification	6.1	V_{DDMIN} specifications are changed for LF devices only at -40°C and 0°C.		X
Electrical Specifications	FVR Specification	7.1	FVR specifications require use above -20°C.	X	X
Timer0	Clock Source	8.1	Operation of Timer0 is incorrect when $F_{OSC}/4$ is used as the clock source.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: Analog-to-Digital Converter (ADC)

1.1 ADC Conversion

When using the ADCRC as the clock source for ADCC, there is a delay of one instruction cycle between the user setting the ADGO bit and being able to read it set. This can lead to a false conversion complete scenario (i.e., ADGO being cleared), depending if the user code has a bit clear test (`BTFSC` instruction on the ADGO bit, immediately after setting the ADGO bit. See code example below.

e.g.

```
BSF ADCON0, ADGO      ; Start conversion
BTSFC ADCON0, ADGO    ; Is conversion done?
GOTO $-1              ; No, test again
```

The BTFSC will pass the very first time in this situation.

Work around

Add a `NOP` instruction after setting the ADGO bit and before testing the bit for completion of conversion. See code example below.

e.g.

```
BSF ADCON0, ADGO      ; Start conversion
NOP
BTSFC ADCON0, ADGO    ; Is conversion done?
GOTO $-1              ; No, test again
```

Affected Silicon Revisions

A3	A4						
X							

1.2 Computation Overflow Bit

If the sign bit of ADFLTR (bit 7 of ADFLTRH) is set, the Computation Overflow bit will also be set, even though this is not a legitimate case of an overflow event.

Work around

None.

Affected Silicon Revisions

A3	A4						
X							

1.3 ADCRC Oscillator Operation in Sleep

If the part is in Sleep and the ADCRC oscillator is used as the clock source to the ADC, the oscillator continues to run after the conversion is complete. This will increase the current consumption in Sleep mode. The oscillator will stop after the device exits Sleep mode and resumes normal code execution.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

1.4 ADC Conversion with FVR

Using the FVR as the positive voltage reference for the ADC can cause an increase in missing codes.

Work around

Increase the bit conversion time, known as TAD, to 8 µs or higher.

Affected Silicon Revisions

A3	A4						
X	X						

2. Module: PIC18 Debug Executive

2.1 Data Write Match Breakpoints

If the data in a GPR location is modified using any arithmetic instruction like INCF, ADDWF, SETF, CLRF, etc., the data write match breakpoint does not work. It works with MOVF, which moves the data into the same memory location.

e.g.

1.

```
MOVLB   0x00
CLRF    0x08
LOOP
INCF    0x08  ;Doesn't break when data
               breakpoint set @ 0x08
               with data match for 0xAA
GOTO    LOOP
```

2.

```
MOVLB   0x00
MOVLW   0xAA
MOVF    0x08  ;Breaks when data
               breakpoint set @ 0x08
               with data match for 0xAA
```

Work around

Use data write breakpoints without matching wherever possible.

Affected Silicon Revisions

A3	A4						
X							

3. Module: PIC18 Core

3.1 TBLRD requires NVMREG value to point to appropriate memory

The affected silicon revisions of the PIC18FXXK40 devices improperly require the NVMREG<1:0> bits in the NVMCON register to be set for TBLRD access of the various memory regions. The issue is most apparent in compiled C programs when the user defines a const type and the compiler uses TBLRD instructions to retrieve the data from program Flash memory (PFM). The issue is also apparent when the user defines an array in RAM for which the complier creates start-up code, executed before main(), that uses TBLRD instructions to initialize RAM from PFM.

Work around

Assembly code:

Set the NVMREG<1:0> bits to select the appropriate memory region before executing TBLRD instructions.

C code:

Create an assembly file named powerup.as and include this file with the other files in the project. This file will change the NVMREG<1:0> bits to point to program Flash before any code is executed.

Contents of the powerup.as file:

```
#include <xc.inc>
    GLOBAL  powerup, start
    PSECT   powerup, class=CODE, delta=1,
            reloc=2
powerup:
    BSF     NVMCON1, 7
    GOTO    start
    end
```

If there is a need to change the NVMREG<1:0> value to anything other than '10' and the Interrupt Service Routine uses constants or literal strings, then interrupts must be disabled before the change and restored to '10' before interrupts are enabled.

Affected Silicon Revisions

A3	A4						
X							

4. Module: Program Flash Memory

4.1 Endurance of PFM is Lower than Specified

The Flash memory cell endurance specification (Parameter MEM30) is 1K cycles.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

5. Module: MSSP

5.1 SMBus 2.0 Voltage Level

The input low-voltage threshold level (V_{IL}) depends on V_{DD}, as follows:

V_{IL} = 0.7 for V_{DD} < 4V

V_{IL} = 0.8 for V_{DD} > 4V

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

6. Module: Electrical Specifications for LF Devices Only

6.1 Min V_{DD} Specification

V_{DDMIN} specifications are changed for LF devices only.

V_{DDMIN} at -40°C to 0°C = 2.3V

V_{DDMIN} at 0°C to 25°C = 2.1V

Work around

None.

Affected Silicon Revisions

A3	A4						
	X						

7. Module: Electrical Specifications

7.1 Fixed Voltage Reference (FVR)

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings, (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

Affected Silicon Revisions

A3	A4						
X	X						

8. Module: Timer0

8.1 Clock Source

Clearing the T0ASYNC bit in the T0CON1 register when Timer0 is configured to use $F_{OSC}/4$ may cause incorrect behavior.

This issue is only valid when Fosc/4 is used as the clock source.

Work around

Set the T0ASYNC bit in the T0CON1 register when using Fosc/4 as the Timer0 clock.

Affected Silicon Revisions

A3	A4						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001842**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Core Features

1.1 Operating Speed on Pg.1

The bullet point mentioning the operating speed is incorrect. The correct text is shown below.

- Operating Speed:
  - **DC-64 MHz clock input**
  - 62.5 ns minimum instruction cycle

2. Module: Pin Allocation Tables

2.1 ADC Channel Selection

Table 1 on pg 8, incorrectly mentions that ANF0, ANF3 and ANF7 are possible ADC input channels. These are reserved connections and are not available as ADC inputs. The correct list of available ADC input channels can be found in "**Section 33.1.2 Channel Selection**" on pg. 627 and 628.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (09/2016)

Initial release of this document.

Rev B Document (12/2016)

Added modules 1.3. ADCRC Oscillator Operation in Sleep, 1.4. ADC Conversion with FVR, and 5. MSSP to the Silicon Errata Issues section. Other minor corrections.

Rev C Document (3/2017)

Added Module 6 to Silicon Errata Issues; other minor corrections.

Rev D Document (5/2018)

Added Module 7: Electrical Specifications (FVR) and Module 8: Timer0.

Data Sheet Clarifications: Added Module 1 (Core Features).

Rev E Document (6/2018)

Data Sheet Clarifications: Added Module 2 (ADC Channel Selection).

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