19-5310; Rev 0; 7/10

EVALUATION KIT AVAILABLE

Automotive, Two-Channel Proximity and Touch Sensor

MAX1441

General Description

The MAX1441 proximity and touch sensor IC is designed for capacitive proximity sensing in automotive passive remote keyless entry (PRKE) and other applications. This device provides signal processing to support two independent touch/proximity sensor channels. The device features two open-drain output pins with high-voltage capability up to 28V, as well as five digital I/Os to indicate sensing events. During manufacturing, JTAG programming uses four digital I/Os.

The device uses grounded electrode capacitive sensing to measure capacitance between one of the two sense pins and the ground. A hand approaching a sense electrode attached to these sense pins causes a change in measured capacitance indicating the presence (touch or proximity) of the object. Active-guard outputs shield the sense electrode from unwanted sources without adding parasitic capacitance. Spread-spectrum techniques in the sensor excitation circuit reduce both electromagnetic emissions and susceptibility to interfering signals. In addition, the sensing excitation frequency is programmable from 100kHz to 500kHz in 10kHz steps to avoid interference.

The sensor input signals are converted to a 12-bit digital data and are available to an on-chip microcontroller (µC). The device provides independent offset compensation of up to 63pF for each input channel. Each channel can be programmed to 5pF, 10pF, or 20pF full-scale range.

The device features an internal MAXQ® microcontroller with 2kword of flash for user programs and 128 bytes of SRAM. This feature provides the ability to implement customized signal processing and discrimination algorithms that optimize performance in the systems.

The device offers user-configurable general-purpose digital I/O lines. Power-on-reset (POR) circuitry provides consistent startup of the device, and a watchdog timer ensures long-term reliable operation of the user's software.

The device is available in a 20-pin TSSOP package and is specified over the -40°C to +105°C automotive temperature range.

Features

- **Low Average Operating Current (100µA at 14V)**
- **1.2fF LSB Capacitance-to-Digital Resolution (5pF Range)**
- **5V to 28V Operation**
- **45V Overvoltage Protection**
- **Sinusoidal Excitation for Reduced EMI Emissions**
- **Frequency Spreading Operation for Reduced EMI Susceptibility and Emissions**
- **Active-Guard-Sense Architecture Provides Increased Flexibility in System Packaging**
- **CMOS/LVCMOS-Compatible Outputs**
- **Embedded µC Supports User-Specified Adaptive Sense Algorithms**
- **2kwords Flash Memory**
- **128-Byte SRAM**
- **±2kV ESD Immunity on Sensor I/O Lines**
- **JTAG Serial Interface**
- **Supports Two Independent Grounded Capacitor Sensor Inputs**
- **-12V Reverse Voltage Protection with External Diode**

Applications

PRKE System Proximity Sensing

Object Detection Systems

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1441GUP/V+	-40°C to +105°C	20 TSSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.
/V Denotes an automotive qualified part.

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For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Automotive, Two-Channel Proximity and Touch Sensor

ABSOLUTE MAXIMUM RATINGS

(V_{DD} = V_{AA}, AGND = DGND, unless otherwise noted.)
V_{BATT} to AGND .....-0.3V to +45V
V_{AA}, V_{DD} to AGND .....-0.3V to +4V
SINPUT1, SINPUT2, AGUD1,
AGUD2 to AGND .....-0.3V to (V_{AA} + 0.3V)
$\overline{RESET}$, P0._, I.C. to DGND ..... -0.3V to (V_{DD} + 0.3V)
AGND to DGND .....-0.3V to +0.3V
OUT1, OUT2 to AGND .....-0.3V to +28V
OUT_, P0._ Continuous Output Current.....≤ 20mA
Continuous Power Dissipation (T_A = +70°C)
Single-Layer PCB
20-Lead TSSOP (derate 11mW/°C above +70°C).....879mW
Multilayer PCB
20-Lead TSSOP (derate 13.6mW/°C above +70°C)..1084mW
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 1)
20-Lead TSSOP ..... +20°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)
Single-Layer PCB
20-Lead TSSOP ..... +91°C/W
Multilayer PCB
20-Lead TSSOP ..... +73.8°C/W
Operating Temperature Range ..... -40°C to +105°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{BATT} = 5V to 28V, V_{AA} = V_{DD}, T_A = -40°C to +105°C. Typical values are at V_{BATT} = 14V, f_{EX} = 300kHz, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Average Power-Supply Current		16ms capacitance-to-digital (C2D) conversion time, two active channels; CPU in sleep mode		100	120	µA
CAPACITANCE-TO-DIGITAL CONVERTER						
Bit Resolution				12		Bits
Input Capacitance Range		CRNG_[1:0] = 10		20		pF
		CRNG_[1:0] = 01		10		
		CRNG_[1:0] = 00		5		
Input Capacitance LSB Resolution		20pF capacitance range		4.8		fF
		10pF capacitance range		2.4		
		5pF capacitance range		1.2		
Integral Nonlinearity	INL			1		%FS
Differential Nonlinearity	DNL			0.5		LSB
Sampling Time		f_{EX} = 300kHz (Note 3)	584	600	624	µs
Number of Effective Bits				11		Bits
DC Input Current of SINPUT1, SINPUT2				300		nA
INPUT CAPACITANCE EXCITATION SOURCE						
Source Peak-to-Peak Voltage		300kHz excitation frequency	0.96	1.0	1.21	V_{P-P}
Minimum Excitation Frequency	f_{EXMIN}	Frequency Control register = 0x0A (Note 3)		100		kHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{BATT} = 5V to 28V, V_{AA} = V_{DD}, T_A = -40°C to +105°C. Typical values are at V_{BATT} = 14V, f_{EX} = 300kHz, T_A = +25°C, unless otherwise noted.) (Note 2)

Maximum Excitation Frequency	f_{EXMAX}	Frequency Control register = 0x32 (Note 3)		500		kHz
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
CAPACITIVE OFFSET DACS						
Offset Adjustment Range		6 bits		63		pF
Offset Adjustment Resolution				1		pF
LOGIC INPUTS/OUTPUTS (P0._, $\overline{RESET}$)						
Output Logic Low	V_{OL}	I_{SINK} = 2mA			0.4	V
Output Logic High	V_{OH}	I_{SOURCE} = 2mA	V_{DD} - 0.5			V
Input Logic Low	V_{IL}	3.0V < V_{DD} < 3.6V			0.8	V
Input Logic High	V_{IH}	3.0V < V_{DD} < 3.6V	2.4			V
Leakage Current	I_L	I/O = high impedance		0.01	1	µA
Port 0 Interrupt Minimum Pulse Width		3.0V < V_{DD} < 3.6V		20		ns
HIGH-VOLTAGE OPEN-DRAIN OUTPUTS (OUT1, OUT2)						
Output Logic Low	V_{OL2}	I_{SINK} = 2mA			0.5	V
Leakage Current	I_L	V_{OUT1} = V_{OUT2} = 25V			1	µA
MICROCONTROLLER						
Flash Program Memory Size		16 bits wide		2k		Words
Program Memory Clear Time	t_{CPM}			38		ms
Page Write Time	t_W			10		ms
Maximum Flash Erase/Write Cycles	n_{CYC}			100k		Cycles
SRAM Size				128		Bytes
CPU Clock Frequency	f_{CPU}			1.25		MHz
INTERNAL OSCILLATOR						
Oscillator Frequency		Master oscillator	19.8	20.48	21.2	MHz
		RC oscillator	31.7	32	32.2	kHz
VOLTAGE REGULATOR						
Input Voltage	V_{BATT}		5	14	28	V
Maximum Dropout Voltage	V_{DROP}	I_{AA} = 10mA		0.6		V
Quiescent Current	I_Q			8		µA
Output Voltage	V_{AA}	5V < V_{BATT} < 28V, 0 < I_{AA} < 10mA	3.2	3.4	3.6	V

Note 2: All units are production tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range are guaranteed by design and characterization.

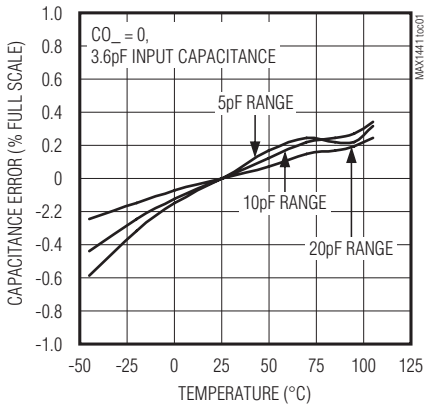
Note 3: Measured indirectly by testing the excitation signal frequency. The excitation signal frequency is determined by the master oscillator frequency, which in turn determines the sample time.

Automotive, Two-Channel Proximity and Touch Sensor

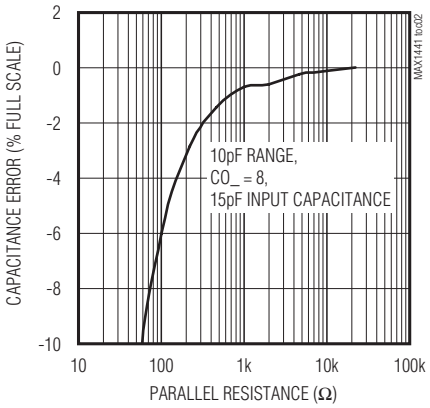
Typical Operating Characteristics

(V_{BATT} = 14V, V_{AA} = V_{DD} = 3.4V, T_A = +25°C, unless otherwise noted.)

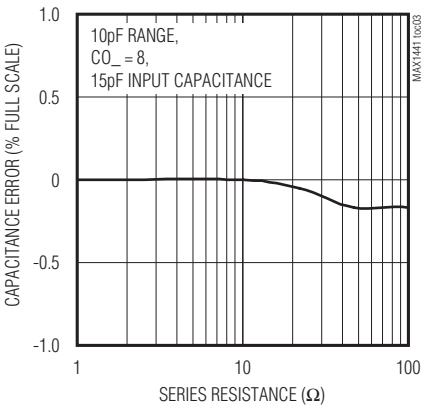
CAPACITANCE ERROR vs. TEMPERATURE



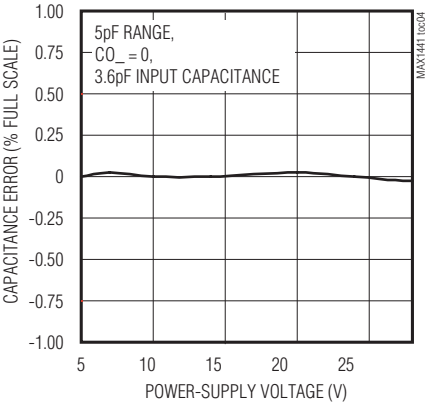
CAPACITANCE ERROR vs. PARALLEL RESISTANCE (SINPUT_ to AGUD_)



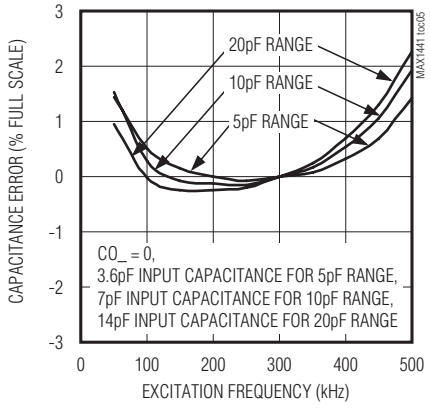
CAPACITANCE ERROR vs. SERIES RESISTANCE



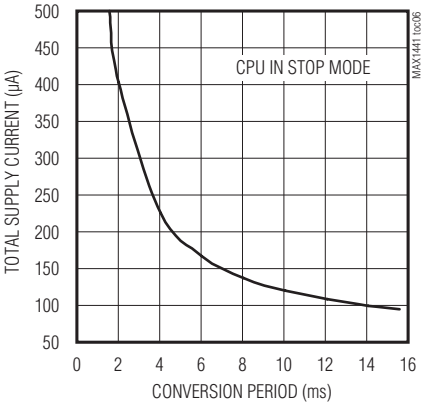
CAPACITANCE ERROR vs. POWER-SUPPLY VOLTAGE



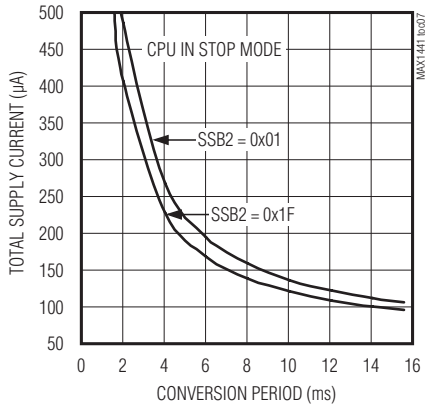
CAPACITANCE ERROR vs. EXCITATION FREQUENCY



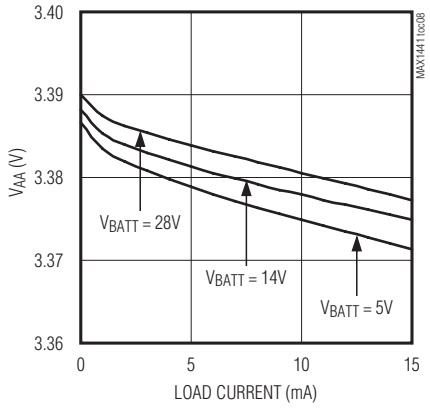
TOTAL SUPPLY CURRENT vs. CONVERSION PERIOD (ONE CHANNEL CONVERTING)



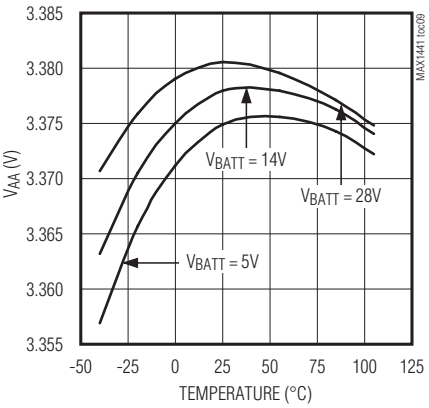
TOTAL SUPPLY CURRENT vs. CONVERSION PERIOD (TWO CHANNELS CONVERTING)



LDO OUTPUT VOLTAGE vs. LOAD CURRENT



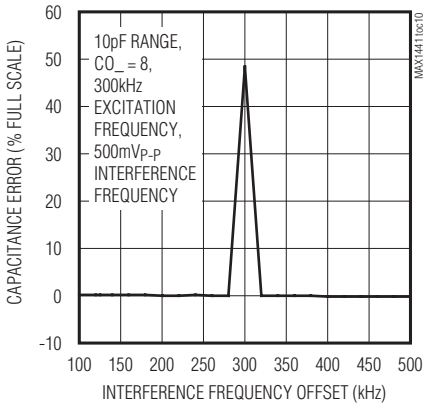
LDO OUTPUT VOLTAGE vs. TEMPERATURE



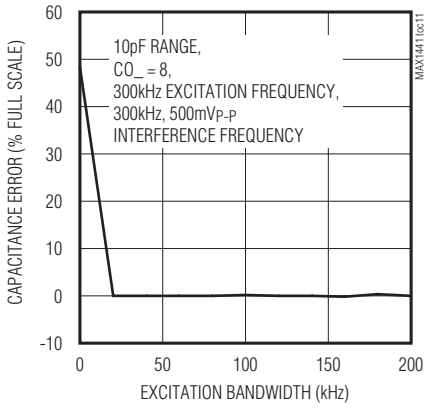
Typical Operating Characteristics (continued)

(V_{BATT} = 14V, V_{AA} = V_{DD} = 3.4V, T_A = +25°C, unless otherwise noted.)

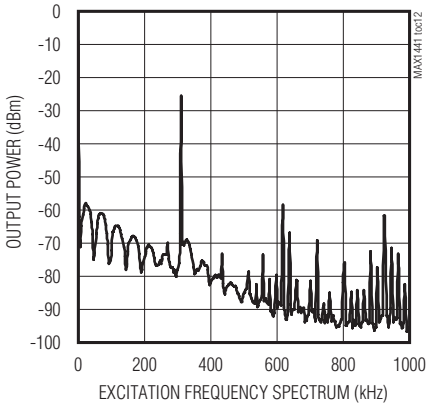
CAPACITANCE ERROR vs. INTERFERENCE FREQUENCY OFFSET



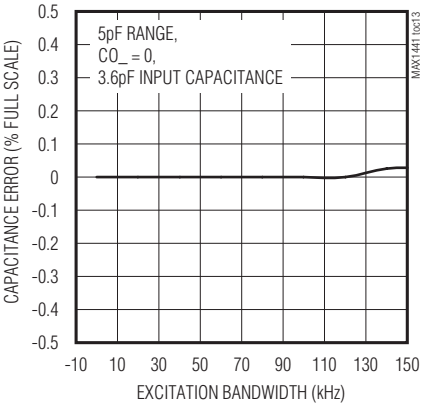
CAPACITANCE ERROR vs. EXCITATION BANDWIDTH (WITH IN-BAND INTERFERENCE)



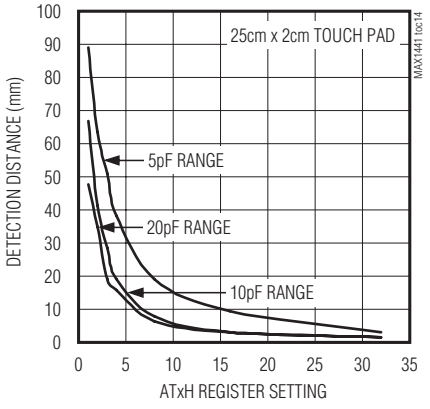
OUTPUT POWER vs. EXCITATION FREQUENCY SPECTRUM



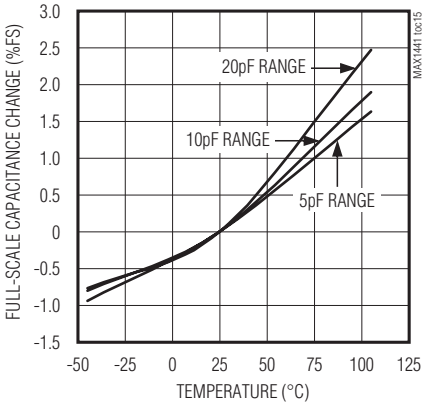
CAPACITANCE ERROR vs. EXCITATION BANDWIDTH



DETECTION DISTANCE vs. ATxH REGISTER SETTING

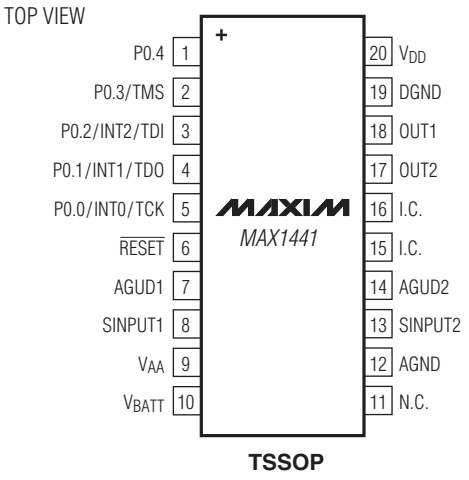


FULL-SCALE CAPACITANCE CHANGE vs. TEMPERATURE



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Pin Configuration

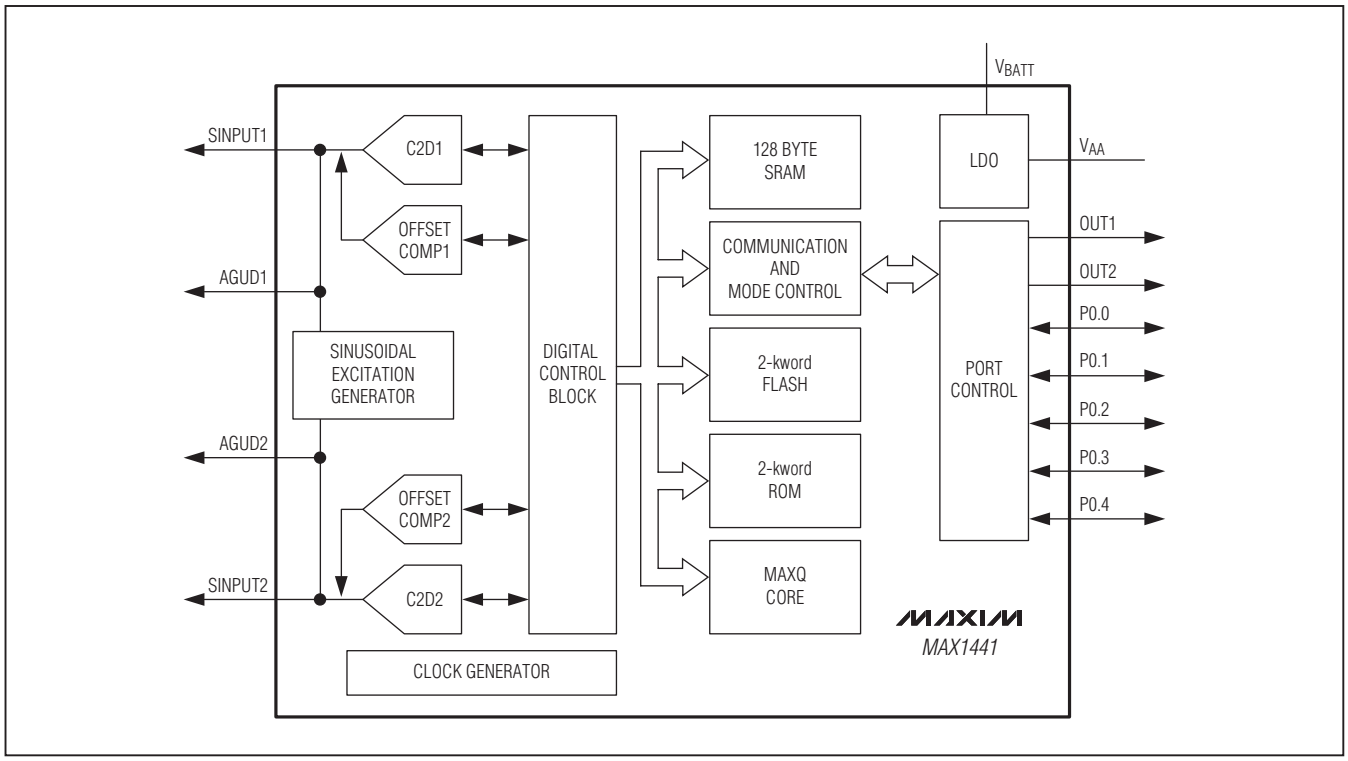


Pin Description

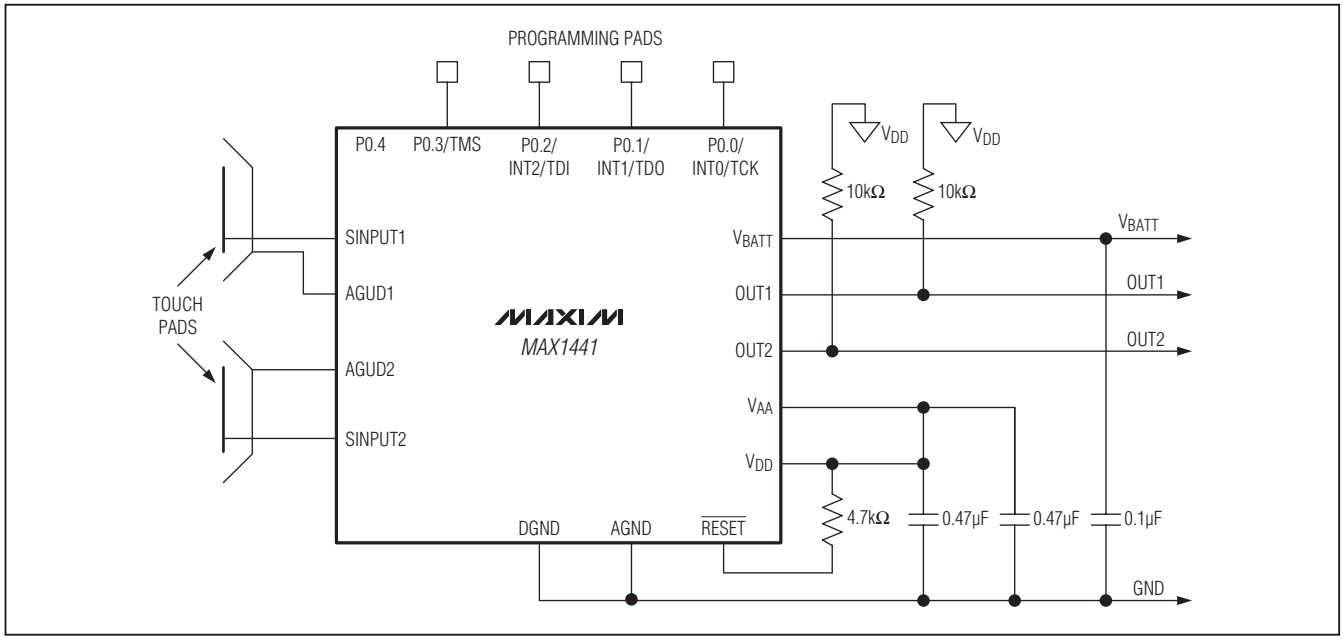
PIN	NAME	FUNCTION
1	P0.4	CPU Port 0 Bit 4. Digital input/output.
2	P0.3/TMS	CPU Port 0 Bit 3/TMS. Digital input/output.
3	P0.2/INT2/TDI	CPU Port 0 Bit 2/TDI. Digital input/output with configurable edge-triggered interrupt.
4	P0.1/INT1/TDO	CPU Port 0 Bit 1/TDO. Digital input/output with configurable edge-triggered interrupt.
5	P0.0/INT0/TCK	CPU Port 0 Bit 0/TCK. Digital input/output with configurable edge-triggered interrupt.
6	$\overline{\text{RESET}}$	Active-Low Reset Input. $\overline{\text{RESET}}$ requires an external pullup to V_{DD}.
7	AGUD1	Active Guard 1. Driven guard (active shield) output for channel 1.
8	SINPUT1	Sensor Input 1. Capacitive sensor electrode input for channel 1.
9	V_{AA}	Analog Power Supply. V_{AA} is internally connected to the output of an on-chip 3.4V linear regulator. Connect V_{AA} to V_{DD}. Bypass V_{AA} with a 0.47µF capacitor to AGND as close to V_{AA} as possible.
10	V_{BATT}	Power-Supply Voltage. Input to the 3.4V on-chip linear regulator. Bypass V_{BATT} to AGND with a 0.1µF capacitor as close to V_{BATT} as possible.
11	N.C.	No Connection. Not internally connected. Leave N.C. unconnected.
12	AGND	Analog Ground. Connect AGND to DGND.
13	SINPUT2	Sensor Input 2. Capacitive sensor electrode input for channel 2.
14	AGUD2	Active Guard 2. Driven guard (active shield) output for channel 2.
15, 16	I.C.	Internally Connected. Leave unconnected.
17	OUT2	Open-Drain Output 2. CPU port 0 bit 6.
18	OUT1	Open-Drain Output 1. CPU port 0 bit 5.
19	DGND	Digital Ground. Connect DGND to AGND.
20	V_{DD}	Digital Power Supply. Connect V_{DD} to V_{AA}. Bypass V_{DD} with a 0.47µF capacitor to DGND as close to V_{DD} as possible.

Automotive, Two-Channel Proximity and Touch Sensor

Functional Diagram



Typical Application Circuit



Automotive, Two-Channel Proximity and Touch Sensor

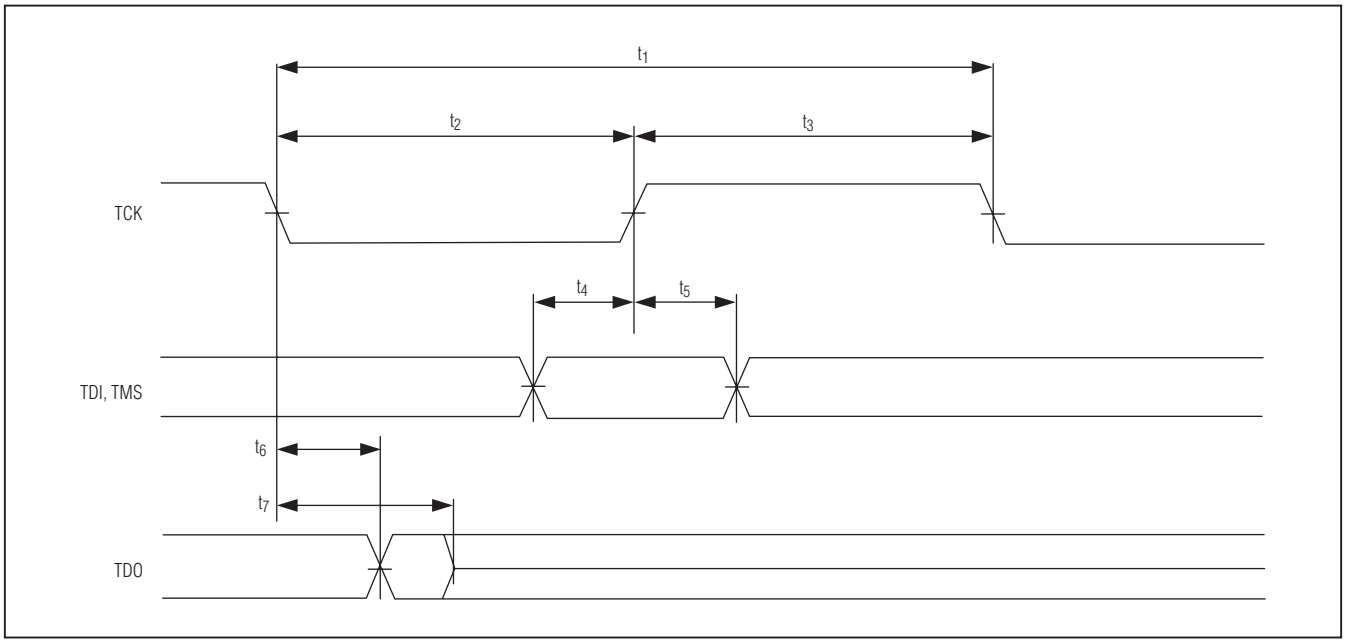


Figure 1. JTAG Timing Diagram

Detailed Description

The MAX1441 is a 2-channel proximity and touch sensor that contains all the functions necessary to implement a proximity/touch detection system for vehicle PRKE systems and other applications. There are four principal architectural components to the device: the capacitive sensing analog front-end (AFE), a programmable CPU system, vehicle power, and I/O interface. Figure 1 shows the JTAG timing diagram.

The AFE uses a 2-channel C2D converter to measure the capacitance present between sensor inputs SINPUT1 and SINPUT2 and the ambient ground (Figure 2). The AFE-sensing architecture converts approaching hand motion to 12-bit digital words that are operated by an algorithm in the CPU to ensure detection of positive events and minimizing false detections. The C2D converters can measure the input capacitance in three different ranges: 20pF, 10pF, and 5pF. Additionally, the C2Ds compensate up to 63pF of parasitic capacitance programmable in 1pF steps.

In addition to capacitive proximity and touch detection, the AFE contains POR and a watchdog timer for monitoring CPU operations. The CPU runs the input capacitive data through an algorithm to ensure detection of positive events and minimizing false detections. The CPU system includes Flash-based program memory, SRAM, clocks, and communications. The power input and signal outputs provide a complete interface to the vehicle power system and a robust communication signal to remote electronic control modules (ECUs).

Technical Function

Each C2D converter produces an AC excitation voltage at inputs SINPUT1 and SINPUT2. The excitation voltage forces current through the capacitance connected to the sensor input. The current amplitude is proportional to the measured capacitance. The circuit measures the input capacitance by measuring the current flowing through the sensor inputs. This excitation signal is a sine wave with a frequency programmable from 100kHz to 500kHz in 10kHz steps. The sinusoidal excitation allows for much lower EMI emissions compared to architectures that utilize simple square-wave excitation.

The device drives the guard outputs AGUD1 and AGUD2 with the same signal from the sinusoidal excitation and shields the sense electrodes without adding parasitic capacitance. The converter measures the amplitude of the current and converts it to 12-bit digital data by a 12-bit C2D. The maximum conversion rate in each of the sensor channels is 1.66kHz.

The microcontroller reads the input capacitance values and uses a user-supplied custom algorithm to detect the object proximity. Once the proximity is detected,

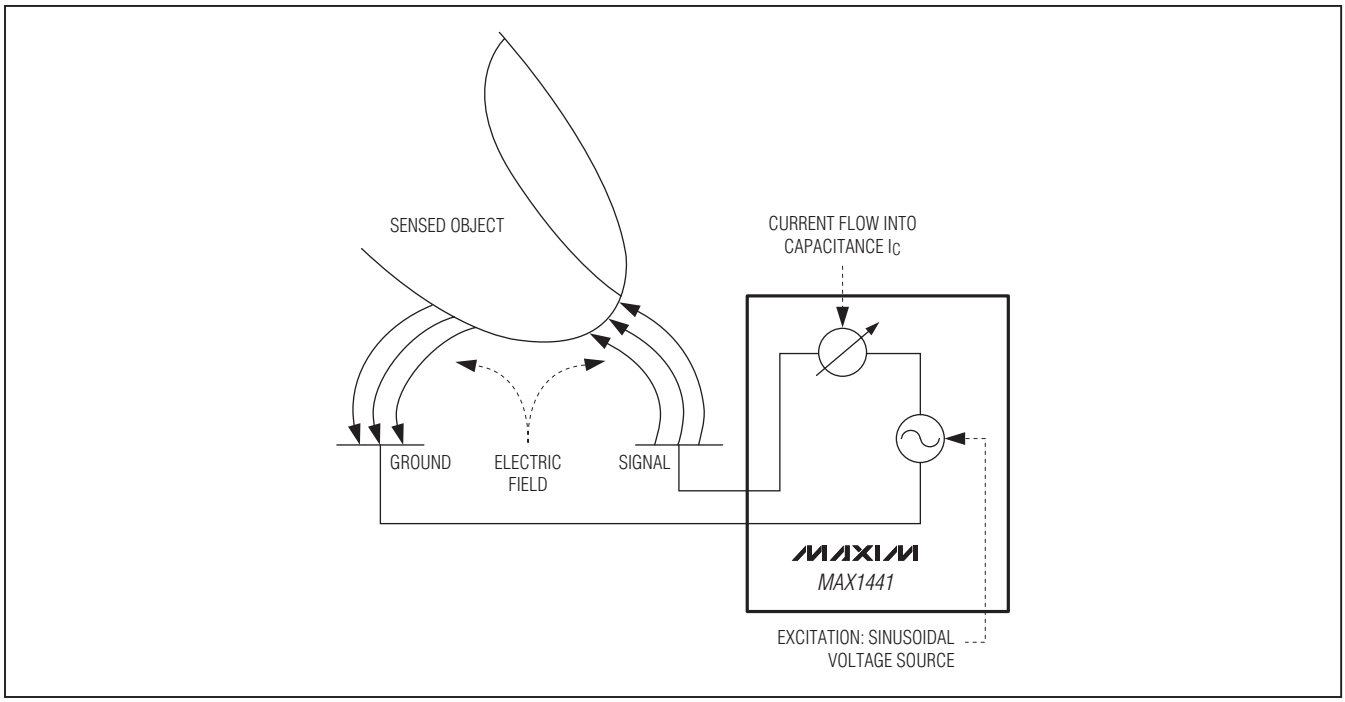


Figure 2. Capacitive-Sensing Function

the microcontroller can use the OUT1 or OUT2 pins to signal the event to external modules. The GPIOs can also provide system or configuration inputs to the microcontroller.

The device has a power-saving standby mode for power-sensitive applications. In the standby mode, the microcontroller is powered down (CPU stop mode) and the analog front-end runs conversions at a reduced and programmable rate. A programmable hardware discriminator monitors the C2D converters outputs and brings the device out of standby mode when a potential object-proximity event is detected. The microcontroller can then analyze the capacitance data and validate the object-proximity event.

The on-chip watchdog timer requires periodic servicing from the microcontroller to ensure proper and continuous operation. The watchdog timer resets the microcontroller if it is not serviced. This prevents the microcontroller from permanently hanging up due to unpredicted code behavior.

The device features an on-chip voltage regulator allowing the part to operate with a wide range of power-supply voltage inputs: 5V to 28V with protection up to 45V. The regulator provides power for all the circuits making the device a very compact single-chip solution.

Control Registers

The device's analog front-end is controlled by a number of control registers. The C2D conversion results and the AFE status are accessible through status and result registers. All AFE registers are available in the microcontroller data space. The control registers support read and write operations. The status and result registers are read-only registers.

Communication between the CPU and the external interface and AFE registers is performed using read/write operations to CPU special-function registers (SFRs).

The SFRs are organized in three sections (Section I–Section III); each section consists of six modules (M0–M5). Table 1 shows the location of each SFR within the SFR sections (see the *Detailed Description* for more details).

Sensed Capacitance Range

The sensed capacitance range can be set independently for both channels. After power-up, the range is set to 20pF in both channels.

Automotive, Two-Channel Proximity and Touch Sensor

Table 1. Important AFE Function Registers

REGISTER	FUNCTION
CRNG	Adjust the capacitance range
FEL	Set the frequency of excitation
FEB	Set the bandwidth of the spread-spectrum modulation
CO1, CO2	Set the capacitance offset
SCT	Put the device in single-conversion mode
DSB	Set the standby conversion rate
SSB2	Set the channel 2 standby conversion rate subdivider
PD	Put the AFE in power-down mode (does not affect CPU operation)
WU1, WU2	Select the wakeup criteria (rate-of-change and/or absolute capacitive change)
AT1H, AT2H	Set the absolute wake-up threshold
RT1H, RT2H	Set the capacitance rate-of-change threshold
CRSLT1L, CRSLT1H	Channel 1 conversion result
CRSLT2L, CRSLT2H	Channel 2 conversion result
AFEINTST	Interrupt status of the AFE

Excitation Frequency

To avoid interference, the excitation frequency can be adjusted to automatically spread within a frequency range. The lower frequency bound and spread-spectrum bandwidth registers determine this range. Spread spectrum continuously changes the excitation frequency so that the radiated power is distributed over a frequency range rather than a single frequency. This lowers the radiated energy density and thus leads to a cleaner spectrum. In addition, by changing the excitation frequency, the capacitance measurement becomes more immune against interference signals.

Offset Capacitance

In case the capacitance measurement permanently reaches the upper or lower limit, there is a likelihood of a parasitic capacitance on top of the touch pads. This could be an ice coating on the door handle for example. In this case, the offset capacitance is adjusted so that the capacitance reenters the measurement range. A parasitic capacitance up to 63pF is compensated for each channel independently by properly setting the offset registers, CO1/CO2.

Single Conversion Mode

The C2D converter can be placed into a single conversion mode. In the single conversion mode, the microcontroller triggers a single conversion by setting bit SCT. If the single conversion mode is enabled, the analog front-end powers up only during the conversion. SCEN controls the single conversion mode. SCEN = 1 enables the single conversion mode and SCEN = 0 disables the single conversion mode. When single conversion mode is enabled, set bit SCT to trigger a conversion. SCT bit automatically clears after the conversion is completed.

Standby Control

To save power, the analog front-end can be put in the standby state. During standby, the conversion rate is determined by the standby state conversion rate divider. SB controls the standby mode. SB = 1 enables the standby mode and SB = 0 disables the standby mode. There is only 1 SB bit common to both channels, so the channels cannot be placed in the standby state independently.

The following sequence of control register writes to the PD register is recommended for entering standby mode:

1) Set PD to 06h to put both AFE channels into reset state.
2) Write DSB and SSB2 registers to set standby rate (if not already set).
3) Set PD to 00h to release AFE reset.
4) Set PD to 01h to enter standby mode.

Standby State Conversion-Rate Divider

The maximum C2D conversion rate is 1.66kHz. Standby state uses conversion-rate reduction to save power. The conversion rate divider and conversion rate subdivider determine the final conversion rate. The DSB divider DSB[4:0] is common to both sensor channels. The conversion rate for channel 2 can be further reduced by the SSB2[4:0] divider. The conversion rate in kHz is determined by the equation:

$$f_{conv,channel1} = \frac{1}{D} \times 1.66kHz$$

$$f_{conv,channel2} = \frac{1}{D \times S} \times 1.66kHz$$

where D is an integer number determined by a 5-bit word DSB[4:0] and S is an integer number determined by a 5-bit word SSB2[4:0]. The default value of D and S is one. D > 1 when S > 1.

Power-Down Control

Each sensor channel independently powers down through the PD register. Bit value 1 powers down the channel and bit value 0 powers up the channel. The excitation source circuitry powers down if both channels are powered down. Powering down both channels also resets all AFE internal circuits except for the AFE's control registers.

Wake-Up Event Thresholds

The sensor wakes up when the measured capacitance exceeds a set capacitance threshold and/or a predefined rate of change in the capacitance. When an object approaches the sensor, the sensed capacitance starts changing. Once the capacitance value crosses the absolute value threshold and/or the capacitance rate of change crosses the rate-of-change threshold, the analog front-end is automatically put in the wake-up state and the SB bit is cleared. At the same time, the wake-up interrupt is sent to the microcontroller. The 8-bit word ATx[11:4] determines the absolute wake-up threshold and 8-bit word RTx[11:4] determines the rate-of-change threshold. Only the upper 8 bits are used in the threshold comparisons. Bit AOx determines if logical AND or OR operation is performed on the absolute and the rate-of-change threshold crossing events to produce the wake-up event. Bit value 1 sets the AND operation and bit value 0 sets OR operation. Both absolute and rate-of-change threshold crossing detection can be enabled or disabled using bits AEx and REx. AEx bit value 1 enables absolute value detection and REx bit value 1 enables rate-of-change detection. The thresholds can be independently programmed in channels 1 and 2.

Conversion Result Word

The 12-bit result of the C2D conversion is available in CRSLT1L and CRSLT1H for channel 1 and in CRSLT2L and CRSLT2H for channel 2. Bit OVRx is set to 1 if the current conversion caused overranging in the C2D converter.

Data Ready in Channel 1

The interrupt status bit IDR1 is set to 1 when a new conversion result is available in channel 1. If the microcontroller does not read the conversion result before the next conversion is completed, the old conversion result is overwritten.

Data Ready in Channel 2

The interrupt status bit IDR2 is set to 1 when a the new conversion result is available in channel 2. If the microcontroller does not read the conversion result before the next conversion is completed, the old conversion result is overwritten.

Wake-Up Event in Channel 1

The interrupt status bit IWUP1 is set to 1 when channel 1 detects a wake-up condition.

Wake-Up Event in Channel 2

The interrupt status bit IWUP2 is set to 1 when channel 2 detects a wake-up condition.

Detailed Controller Specification

Architecture

The device is based on the MAXQ RISC processor with Harvard memory architecture.

Specific MAXQ Special-Purpose Register Implementation

The device implements all other standard MAXQ special-purpose registers (SPRs). For details, see the SPR bit description in Table 5.

Special-Purpose Registers

Table 2 summarizes the SPRs and their address indexes. These registers can be accessed by user software.

Table 2. Special-Purpose Register Map

MODULE		INDEX OF SPECIAL-PURPOSE REGISTER															
MODULE	**SPECIFIER**	**00000**	**00001**	**00010**	**00011**	**00100**	**00101**	**00110**	**00111**	**01000**	**01001**	**01010**	**01011**	**01100**	**01101**	**01110**	**01111**
AP	01000	AP	APC	—	—	PSF	IC	IMR	—	SC	—	—	IIR	—	—	CKCN	WDCN
A	01001	A0	A1	A2	A3	—	—	—	—	—	—	—	—	—	—	—	—
PFX	01011	PFX	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
IP	01100	IP	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SP	01101	—	SP	IV	—	—	—	LC0	LC1	—	—	—	—	—	—	—	—
DPC	01110	—	—	—	Offs	DPC	GR	GRL	BP	GRS	GRH	GRXL	FP	—	—	—	—
DP	01111	—	—	—	DP0	—	—	—	DP1	—	—	—	CP	—	—	—	—

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Indexes not specified in this table are either reserved for hardware functional use or for future expansion; access to these locations has deterministic behavior that may not be the intention of the user. Register addresses highlighted in the table are reserved.

Table 3 lists the SPR registers' functional bits and their bit positions. Table 4 specifies the default reset condition for all SPR bits. The default value for unused SPR bit locations is 0. For registers in the accumulator and Loop module, all 16 bits are undetermined after a reset. Undetermined values are labeled as "i" in the table. Special default values are labeled as "s" in the table.

Table 5 details all SPRs and their bit description. Registers are also identified by their address in the form of (xxh, yyh), where xxh is the register index in hex and yyh is the module specifier in hex.

Table 3. Special-Purpose Register Bit Function

REGISTER		MSB							LSB
AP	[7:0]	—	—	—	—	—	—	AP1	AP0
APC	[7:0]	CLR	IDS	—	—	—	—	MOD1	MOD0
PSF	[7:0]	Z	S	—	GPF1	GPF0	OV	C	E
IC	[7:0]	—	—	—	—	—	—	INS	IGE
IMR	[7:0]	IMS	—	—	—	—	—	IM1	IM0
SC	[7:0]	TAP	—	—	—	—	ROD	PWL	—
IIR	[7:0]	IIS	—	—	—	—	—	—	—
CKCN	[7:0]	IDLE	—	—	—	—	—	—	—
WDCN	[7:0]	POR	EWDI	WD1	WD0	WDIF	WTRF	EWT	RWT
A0	[15:0]	A0[15:0]							
A1	[15:0]	A1[15:0]							
A2	[15:0]	A2[15:0]							
A3	[15:0]	A2[15:0]							
PFX	[15:0]	PFX[15:0]							
IP	[15:0]	IP[15:0]							
SP	[15:0]	SP[15:0]							
IV	[15:0]	IV[15:0]							
LC0	[15:0]	LC0[15:0]							
LC1	[15:0]	LC1[15:0]							
DPC	[7:0]	—	—	—	—	—	WBS0	—	—
GR	[15:0]	GR[15:0]							
GRL	[7:0]	GRL[7:0]							
GRS	[15:8]	GR7	GR6	GR5	GR4	GR3	GR2	GR1	GR0
	[7:0]	GR15	GR14	GR13	GR12	GR11	GR10	GR9	GR8
GRH	[7:0]	GRH[7:0]							
GRXL	[15:8]	GR7	GR7	GR7	GR7	GR7	GR7	GR7	GR7
	[7:0]	GR7	GR6	GR5	GR4	GR3	GR2	GR1	GR0
DP0	[15:0]	DP0[15:0]							

Table 4. Special-Purpose Registers' Reset Values

REGISTER	MSB			LSB
AP	—	—	0000	0000
APC	—	—	0000	0000
PSF	—	—	1000	0000
IC	—	—	0000	0000
IMR	—	—	0000	0000
SC	—	—	1000	00s0
IIR	—	—	0000	0000
CKCN	—	—	1110	0000
WDCN	—	—	ss11	0ss0
A0	0000	0000	0000	0000
A1	0000	0000	0000	0000
A2	0000	0000	0000	0000
A3	0000	0000	0000	0000

REGISTER	MSB			LSB
PFX	0000	0000	0000	0000
IP	1000	0000	0000	0000
SP	0000	0000	0010	1111
IV	0000	0111	1111	1101
LC0	0000	0000	0000	0000
LC1	0000	0000	0000	0000
DPC	0000	0000	0000	0100
GR	0000	0000	0000	0000
GRL	—	—	0000	0000
GRS	0000	0000	0000	0000
GRH	—	—	0000	0000
GRXL	0000	0000	0000	0000
DP0	0000	0000	0000	0000

Table 5. Special-Purpose Register Bit Description

REGISTER	DESCRIPTION	
AP (00h, 08h)	**Accumulator Pointer (8-Bit Register)**	
Initialization	This register is cleared to 00h on all forms of reset.	
Read/Write Access	Unrestricted read/write.	
AP[1:0]	**Active Accumulator Select Bits [1:0].** The setting of these bits activates one of the four accumulators in the accumulator module (A) to function as the active accumulator for arithmetic and logical operations. The setting of these bits can be automatically incremented/decremented in a modulo fashion according to the setting to the APC register.	
AP[7:2]	**Reserved. Read returns 0.**	
APC (01h, 08h)	**Accumulator Pointer Control (8-Bit Register)**	
Initialization	This register is cleared to 00h on all forms of reset.	
Read/Write Access	Unrestricted read/write.	
APC[1:0]–MOD[1:0]	**Modulo Bits [1:0].** The accumulator pointer autoincrement/decrement function is activated when these bits are set to a value other than 00b. The modulo is selected accordingly when active pointer autoincrement/decrement is active.	
	MOD[1:0]	**MODULO**
	00	Default, no AP autoincrement/decrement
	01	Modulo 2
	10	Modulo 4
	11	Reserved (modulo 4 if set)
APC[5:2]	**Reserved. Read returns 0.**	
APC.6–IDS	**Increment/Decrement Select.** When this bit is cleared to 0, the content of AP increments after an arithmetic or logical operation. When this bit is set to 1, the content of AP is decremented after arithmetic or logical operation.	
APC.7–CLR	**AP Clear.** When this bit is set to 1, the content of AP is cleared to 0. This bit automatically resets to 0 after clearing the AP register. Note if the MOVE APC, Acc instruction (980Ah) causes the CLR bit to set, the clear operation overrides other functions (i.e., the AP autoincrement/decrement does not happen).	

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Table 5. Special-Purpose Register Bit Description (continued)

REGISTER	DESCRIPTION
PSF (04h, 08h)	**Processor Status Flags Register (8-Bit Register)**
Initialization	This register is set to 80h on all forms of reset.
Read/Write Access	Unrestricted direct read. Write access to OV, E, C, GPF1, and GPF0 bits only.
PSF.0–E	**Equal Flag.** This flag reflects the state of the Equal bit of a compare operation. It is 1 when the two values are equal. It is 0 when the two values are different. Writing a 1 to this bit by software is effectively set by the Equal flag.
PSF.1–C	**Carry Flag.** This flag reflects the state of the Carry bit of the active accumulator. Its state may change after an arithmetic and logical operation. This flag is set to 1 if the last operation resulted in a carry/borrow. Otherwise, it is cleared to 0. Writing a 1 to this bit by software is effectively set by the Carry flag.
PSF.2–OV	**Overflow Flag.** This flag is set to 1 if there is a carry out of bit 14 but not out of bit 15, or a carry out of bit 15 bit not out of bit 14 from the last arithmetic operation; otherwise, the OV remains as 0. When adding signed numbers, OV indicates a negative number resulted as the sum of two positive operands, or a positive sum resulted from two negative operands. For subtraction, OV is set if a borrow is needed into bit 14 but not into bit 15, or into bit 15 but not into bit 14. This bit can be read and written by software to allow it to be restored after events such as interrupt servicing and debug operations.
PSF.3–GPF0	**General-Purpose Flag 0.** This is a general-purpose flag for software control.
PSF.4–GPF1	**General-Purpose Flag 1.** This is a general-purpose flag for software control.
PSF.5	**Reserved. Read returns 0.**
PSF.6–S	**Sign Flag.** This flag reflects the state of the Sign bit of the active accumulator (the most significant bit of the active accumulator). Its state may change after an arithmetic and logical operation or after the switch of the active accumulator. When it is set to 1, it indicates a negative value in the active accumulator from the last operation. When it is cleared to 0, it indicates a positive value.
PSF.7–Z	**Zero Flag.** This flag reflects the state of the Zero bit of the active accumulator (bit-wise NOR of the active accumulator). Its state may change after an arithmetic and logical operation or after the switch of the active accumulator. When it is set to 1, it indicates a zero value as a result of the last operation. When it is cleared to 0, it indicates a nonzero value.
IC (05h, 08h)	**Interrupt and Control Register (8-Bit Register)**
Initialization	This register is cleared to 00h on all forms of reset.
Read/Write Access	Unrestricted read/write.
IC.0–IGE	**Interrupt Global Enable.** The IGE bit enables the interrupt handler if set to 1. No interrupt to the CPU is allowed if this bit is cleared to 0.
IC.1–INS	**Interrupt In Service.** The INS is set by the interrupt handler automatically when an interrupt is acknowledged. No further interrupt occurs as long as the INS remains set. The interrupt service routine can clear the INS to allow interrupt nesting. Otherwise, at the execution of an RETI/POPI instruction, the INS is cleared automatically by the interrupt handler.
IC[7:2]	**Reserved. Read returns 0.**
IMR (06h, 08h)	**Interrupt Mask Register (8-Bit Register)**
Initialization	This register is cleared 80h on all forms of reset.
Read/Write Access	Unrestricted read. All bits have unrestricted write access, unless otherwise stated.
IMR.0–IM0	**Interrupt Mask 0.** This bit is the module level interrupt enable for register module 0. To activate the interrupt request from module 0, the IGE and IM0 must be set and the INS is not set. Clearing this bit to 0 disables all interrupt sources in module 0.

Table 5. Special-Purpose Register Bit Description (continued)

REGISTER	DESCRIPTION
IMR.1–IM1	**Interrupt Mask 1.** This bit is the module level interrupt enable for register module 1. To activate the interrupt request from module 1, the IGE and IM1 must be set and the INS is not set. Clearing this bit to 0 disables all interrupt sources in module 1.
IMR[6:2]	**Reserved. Read returns 0.**
IMR.7–IMS	**Interrupt Mask 7.** This bit is the module level interrupt enable for SPR modules. To activate the interrupt request from any SPR modules, the IGE and IMS must be set and the INS is not set. Clearing this bit to 0 disables all interrupt sources in all SPR modules. **This bit is read only and defaults to 1 on all forms of reset.**
SC (08h, 08h)	**System Control Register (8-Bit Register)**
Initialization	This register is set to 82h on POR and set to 1000 00s0b on all other forms of reset.
Read/Write Access	Unrestricted read. See the following bit definition for write restriction.
SC.0	**Reserved. Read returns 0.**
SC.1–PWL	**Password Lock.** This bit defaults to 1 on a power-on reset. When this bit is 1, it requires a 32-byte password to be matched with the password in the program space before allowing access to the ROM loader's utilities for read/write of program memory and debug functions.
SC.2–ROD	**ROM Operation Done.** This bit is used to signify completion of a ROM operation sequence to the control units. This allows the debug engine to determine the status of a ROM sequence. Setting this bit to logic 1 causes an internal system reset if the SPE bit is also set. Setting the ROD bit clears the SPE bit if it is set and the ROD bit is automatically cleared by hardware once the control unit acknowledges the done indication. **Setting this bit to 1 causes either an internal system reset or the debug engine to execute a command to clear this bit. Either way, the applicable code is never able to read a 1 from this bit.**
SC[6:3]	**Reserved. Read returns 0.**
SC.7–TAP	**Test Access (JTAG) Port Enable.** This bit controls whether the test access port special function pins are enabled. The TAP defaults to being enabled. Clearing this bit to 0 disables the TAP special function on the JTAG pins.
IIR (0Bh, 08h)	**Interrupt Identification Register (8-Bit Register)**
Initialization	This register is cleared to 00h on all forms of reset.
Read/Write Access	Unrestricted direct read. Write access is a no operation.
IIR.0–II0	**Interrupt ID 0.** When this bit is set to 1, it indicates that there is at least one pending interrupt in module 0. This bit is set only if the interrupt flag and its corresponding enable bit are set. The II0 is cleared by hardware when the interrupt source is disabled or the flag is cleared by software.
IIR.1–II1	**Interrupt ID 1.** When this bit is set to 1, it indicates that there is at least one pending interrupt in module 1. This bit is set only if the interrupt flag and its corresponding enable bit are set. The II1 is cleared by hardware when the interrupt source is disabled or the flag is cleared by software.
IIR[6:2]	**Reserved. Read returns 0.**
IIR.7–IIS	**Interrupt ID System.** When this bit is set to 1, it indicates that there is at least one pending interrupt in SPR modules. This bit is set only if the interrupt flag and its corresponding enable bit is set. The IIS is cleared by hardware when the interrupt source is disabled or the flag is cleared by software.
CKCN (0Eh, 08h)	**System Clock Control Register (8-Bit Register)**
Initialization	This register is set to 060h on all forms of resets.
Read/Write Access	Unrestricted read. See the following bit description for write restriction.

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Table 5. Special-Purpose Register Bit Description (continued)

<table>
<tr><th>REGISTER</th><th colspan="4">DESCRIPTION</th></tr>
<tr><td>CKCN[3:0]</td><td colspan="4">Reserved. These bits are read only. Read returns 0.</td></tr>
<tr><td>CKCN.4–STOP</td><td colspan="4">Stop Mode Select. Setting this bit to 1 stops program execution and commences low-power CPU operation. This bit is cleared by a reset or any of the enabled external interrupts. Setting and resetting the STOP bit does not change the system clock source and its divide ratio.</td></tr>
<tr><td>CKCN[6:5]</td><td colspan="4">Reserved. These bits are read only. Read returns 11b.</td></tr>
<tr><td>CKCN.7–IDLE</td><td colspan="4">IDLE Mode Select. Setting this bit to a 1 stops program execution by halting the instruction pointer and disabling the internal module selects (similar to a NOP operation). This provides a low-power mode that does not require a system warm-up on exit.</td></tr>
<tr><td>WDCN (0Fh, 08h)</td><td colspan="4">Watchdog Timer Control (8-Bit Register)</td></tr>
<tr><td>Initialization</td><td colspan="4">This register is set to B2h on POR and set to ss00 0ss0b on all other forms of reset.</td></tr>
<tr><td>Read/Write Access</td><td colspan="4">Unrestricted read. Unrestricted write access, unless stated otherwise.</td></tr>
<tr><td>WDCN.0–RWT</td><td colspan="4">Reset Watchdog Timer. Setting this bit resets the watchdog timer count. This bit must be set before the watchdog timer expires, or a watchdog timer reset and/or interrupt is generated if enabled. The timeout period is defined by WD1 and WD0. This bit is always 0 when read.</td></tr>
<tr><td>WDCN.1–EWT</td><td colspan="4">Enable Watchdog Timer Reset. Setting this bit to 1 enables the watchdog timer to reset the device; clearing this bit to 0 disables the watchdog timer reset. It has no effect on the timer itself and its ability to generate a watchdog interrupt. This bit is set to 1 following a power-on reset and is unaffected by all other resets. This bit can only be written once by software. Once written, the value of this bit is not altered by any subsequent write.</td></tr>
<tr><td>WDCN.2–WTRF</td><td colspan="4">Watchdog Timer Reset Flag. When set, this bit indicates that a watchdog timer reset has occurred. It is typically interrogated to determine if a reset was caused by the watchdog timer. It is cleared by power-on reset, but otherwise must be cleared by software before the next reset of any kind to allow software to work correctly. Setting this bit by software does not generate a watchdog timer reset. If the EWT bit is cleared, the watchdog timer has no effect on this bit.</td></tr>
<tr><td rowspan="8">WDCN.3–WDIF</td><td colspan="4">Watchdog Interrupt Flag. This bit is set to 1 by a watchdog timeout, which indicates a watchdog timer event has occurred if EWT and/or EWDI are set. When the WDIF is set, EWT and EWDI determine the action to take.
Setting this bit from 0 to 1 also activates the reset counter for the watchdog reset timeout, which allows 512 clock cycles for the system to reset the watchdog timer using the RWT bit.
Setting this bit in software generates a watchdog interrupt if enabled and triggers the reset counter. This bit must be cleared in software before exiting the interrupt service routine, or another interrupt is generated. The reset counter must be cleared by RWT once started.</td></tr>
<tr><td>EWT</td><td>EWDI</td><td>WDIF</td><td>ACTIONS</td></tr>
<tr><td>x</td><td>x</td><td>0</td><td>No interrupt has occurred.</td></tr>
<tr><td>0</td><td>0</td><td>x</td><td>Watchdog disable, clock is gated off.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Watchdog interrupt has occurred.</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>No interrupt has been generated. Watchdog reset occurs in 512 clock cycles if RWT is not set or WDIF not cleared.</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Watchdog interrupt has occurred. Watchdog reset occurs in 512 clock cycles if RWT is not set or WDIF not cleared.</td></tr>
<tr><td colspan="4">Note: Software cannot set this flag. Software can only clear this flag. This restriction is specific to the MAX1441 only and does not apply to other MAXQ products.</td></tr>
</table>

Table 5. Special-Purpose Register Bit Description (continued)

REGISTER	DESCRIPTION
WDCN[5:4]–WD[1:0]	**Watchdog Timer Mode Select Bits [1:0].** These bits are used to provide a user selection of watchdog timer interrupt periods, which determine the watchdog timer interrupt timeout when the watchdog timer is enabled. All watchdog timer reset timeouts follow the programmed interrupt timeouts by 512 times the clock divide ratio oscillator cycles. Mode select bit settings and the timeout values. Changing the WD1:0 bit settings resets the watchdog timer unless the 512 clock reset counter has already started, in which case, changing the WD1:0 bits does not affect the watchdog timer or reset counter. **These bits can only be written when simultaneously resetting the timer (RWT = 1). Otherwise, a write to these control bits is ignored (i.e., user software sets the RWT bit and changes the WD value in the same instruction).**
WDCN.6–EWDI	**Watchdog Interrupt Enable.** Setting this bit to 1 enables interrupt requests generated by the watchdog timer. Clearing this bit to 0 disables the interrupt requests. This bit is cleared following a power-on reset and unaffected by all other resets.
WDCN.7–POR	**Power-On Reset Flag.** This bit indicates whether the last reset was a power-on reset. This bit is typically interrogated following a reset. It must be cleared before the next reset of any kind for software to work correctly. This bit is set following a power-on reset and unaffected by all other resets.
A0 (00h, 09h)	**Accumulator 0 (16-Bit Register)**
Initialization	This register is cleared to 0000h on all forms of reset.
Read/Write Access	Unrestricted read/write.
A0[15:0]	**Accumulator 0 Bits [15:0].** This register serves as the accumulator for arithmetic and logical operation when activated by the accumulator pointer. Otherwise, it can be used as general-purpose working register.
A1 (01h, 09h)	**Accumulator 1 (16-Bit Register)**
Initialization	This register is cleared to 0000h on all forms of reset.
Read/Write Access	Unrestricted read/write.
A1[15:0]	**Accumulator 1 Bits [15:0].** This register serves as the accumulator for arithmetic and logical operation when activated by the accumulator pointer. Otherwise, it can be used as a general-purpose working register.
A2 (02h, 09h)	**Accumulator 2 (16-Bit Register)**
Initialization	This register is cleared to 0000h on all forms of reset.
Read/Write Access	Unrestricted read/write.
A2[15:0]	**Accumulator 2 Bits [15:0].** This register serves as the accumulator for arithmetic and logical operation when activated by the accumulator pointer. Otherwise, it can be used as a general-purpose working register.
A3 (03h, 09h)	**Accumulator 3 (16-Bit Register)**
Initialization	This register is cleared to 0000h on all forms of reset.
Read/Write Access	Unrestricted read/write.
A3[15:0]	**Accumulator 3 Bits [15:0].** This register serves as the accumulator for arithmetic and logical operation when activated by the accumulator pointer. Otherwise, it can be used as a general-purpose working register.

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Table 5. Special-Purpose Register Bit Description (continued)

REGISTER	DESCRIPTION
PFX (00h–07h, 0Bh)	**Prefix Register (16-Bit Register)**
Initialization	This register is cleared to 0000h on all forms of reset.
Read/Write Access	Unrestricted read/write.
PFX[7:0]	**Prefix Register Bits [7:0].** This register provides a means to supply the high-order byte of data to a 16-bit destination register with 8-bit sources. To transfer 8-bit source data to a 16-bit destination, the high-order byte must first transfer to the PFX register. This activates the PFX for the next instruction cycle, which concatenates PFX data with the source operand to form a 16-bit data for the target destination. The PFX holds data for only one cycle before resetting all its bits to 0. When PFX is used as a source, it basically transfers a zero value to the destination when PFX has not been activated in the preceding instruction.
PFX[15:8]	**Prefix Register Bits [15:8].** Reserved. Read returns 0. **Note:** Subdecodes (1h–7h) function as extension bits for source/destination indexing.
IP (00h, 0Ch)	**Instruction Pointer (16-Bit Register)**
Initialization	This register is set to 8000h on all forms of reset.
Read/Write Access	Unrestricted read/write.
IP[15:0]	**Instruction Pointer Bits [15:0].** This register contains the next program address to be fetched by the fetch unit. The content of IP is automatically incremented by 1 after each fetch. New data written to this register causes the program flow to branch to the new location. Read access to the IP register does not affect the program flow.
SP (01h, 0Dh)	**Stack Pointer (16-Bit Register)**
Initialization	This register is cleared to 002Fh on all forms of reset.
Read/Write Access	Unrestricted read/write.
SP[5:0]	**Stack Pointer Bits [5:0].** The SP designates the memory location that is at the top of the stack, which is the storage location of the last word. The contents of the SP is postdecremented for a POP operation, and is preincremented for a PUSH operation.
SP[15:6]	**Reserved. Read returns 0.**
IV (02h, 0Dh)	**Interrupt Vector Register (16-Bit Register)**
Initialization	This register is set to 07FDh on all forms of reset.
Read/Write Access	Unrestricted read only.
IV[15:0]	**Interrupt Vector Bits [15:0].** This register contains the interrupt vector address. The interrupt handler forces a hardware call to this vector location when there is an enabled interrupt request pending.
LC0 (06h, 0Dh)	**Loop Counter 0 (16-Bit Register)**
Initialization	This register is cleared to 0000h on all forms of reset.
Read/Write Access	Unrestricted read/write.
LC0[15:0]	**Loop Counter 0 Bits [15:0].** This register contains the loop count for a loop operation. The content of LC0 is automatically decremented by 1 after each loop. This register is normally used as a loop control for conditional branch to a new location.
LC1 (07h, 0Dh)	**Loop Counter 1 (16-Bit Register)**
Initialization	This register is cleared to 0000h on all forms of reset.
Read/Write Access	Unrestricted read/write.
LC1[15:0]	**Loop Counter 1 Bits [15:0].** This register contains the loop count for a loop operation. The content of LC1 is automatically decremented by 1 after each loop. This register is normally used as loop control for conditional branch to a new location.

Table 5. Special-Purpose Register Bit Description (continued)

REGISTER	DESCRIPTION
DPC (04h, 0Eh)	**Data Pointer Control Register (16-Bit Register)**
Initialization	This register is set to 0004h on all forms of reset.
Read/Write Access	Unrestricted read/write.
DPC[1:0]–SDPS[1:0]	**Reserved. Read returns 0.**
DPC.2–WBS0	**Word/Byte Select 0.** This bit selects access mode for DP[0]. When WBS0 is set to logic 1, the DP[0] is operated in word mode for data-memory access; when WBS0 is cleared to logic 0, DP[0] is operated in byte mode for data-memory access.
DPC[15:3]	**Reserved. Read returns 0.**
GR (05h, 0Eh)	**General Register (16-Bit Register)**
Initialization	This register is cleared to 0000h on all forms of reset.
Read/Write Access	Unrestricted read/write.
GR[15:0]	**General Register Bits [15:0].** This register is intended primarily for supporting byte operation on 16-bit data. GR can be used as a 16-bit general-purpose register and allows byte-readable and byte-writable operations through the corresponding GRL and GRH register locations. It also supports byte-swap operation when read through the GRS register location.
GRL (06h, 0Eh)	**General Register Low Byte (8-Bit Location)**
Initialization	This register is cleared to 00h on all forms of reset.
Read/Write Access	Unrestricted read/write.
GRL[7:0]	**General Register Low Byte Bits [7:0].** This register location reflects the low byte of the GR register and is intended primarily for supporting byte operation on 16-bit data. Any data written to this location stores in the low byte of the GR register, and a read in this location returns the least significant data byte of the GR register.
GRS (08h, 0Eh)	**General Register Byte Swap (16-Bit Location)**
Initialization	This register is cleared to 0000h on all forms of reset.
Read/Write Access	Unrestricted read only.
GRS[15:0]	**General Register Byte Swap Bits [15:0].** This read-only register location reflects the byte-swapped data of the GR register and is intended primarily for supporting byte operation on 16-bit data. Reading this register location returns the byte-swapped data from the GR register.
GRH (09h, 0Eh)	**General Register High Byte (8-Bit Location)**
Initialization	This register is cleared to 00h on all forms of reset.
Read/Write Access	Unrestricted read/write.
GRH[7:0]	**General Register High Byte Bits [7:0].** This register location reflects the high byte of the GR register and is intended primarily for supporting byte operation on 16-bit data. Any data written to this location stores in the high byte of the GR register, and read this location returns the most significant data byte of the GR register.
GRXL (0Ah, 0Eh)	**General Register Sign Extended Low Byte (16-Bit Location)**
Initialization	This register is cleared to 0000h on all forms of reset.
Read/Write Access	Unrestricted read only.
GRXL[15:0]	**General Register Sign Extended Byte Bits [15:0].** This read-only register location reflects the sign extended low byte of the GR register. When read, the upper 8 bits contain the logic value of bit 7 of the GR register, and the lower 8 bits are the low byte of the GR register.

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Table 5. Special-Purpose Register Bit Description (continued)

REGISTER	DESCRIPTION
DP0 (03h, 0Fh)	**Data Pointer 0 (16-Bit Register)**
Initialization	This register is cleared to 0000h on all forms of reset.
Read/Write Access	Unrestricted read/write.
DP0[15:0]	**Data Pointer 0 Bits [15:0].** This register contains the data address for data memory access. The contents of DP0 can be automatically incremented/decremented for read/write data-memory operation.

Special-Function Registers

All peripherals and operations that are not explicit instructions in the device are controlled using special-function registers (SFRs). These registers allow communication and data exchange between the CPU and the peripherals. Normally, interaction between a peripheral and the processor is initiated through the interrupt handler. SFRs can be 8-bit or 16-bit registers and most of the SFRs are accessible by user software (Tables 6, 7, 8). All undefined or unallocated registers should be treated as reserved registers.

Table 6. Special-Function Register Map Section I

MODULE		INDEX OF SPECIAL-FUNCTION REGISTER (SECTION I)							
M[x]	**SPECIFIER**	**00000**	**00001**	**00010**	**00011**	**00100**	**00101**	**00110**	**00111**
M0	00000	PO0	EIF0	EIE0	EIES0	TCON	TFRQ	TCNT	—
M1	00001	AFEINTST	SCT	CRNG	PD	WU1	WU2	FEL	FEB
M2	00010	—	—	—	—	—	—	—	—
M3	00011	—	—	—	—	—	—	—	—
M4	00100	—	—	—	—	—	—	—	—
M5	00101	—	—	—	—	—	—	—	—

Table 7. Special-Function Register Map Section II

MODULE		INDEX OF SPECIAL-FUNCTION REGISTER (SECTION II)							
M[x]	**SPECIFIER**	**01000**	**01001**	**01010**	**01011**	**01100**	**01101**	**01110**	**01111**
M0	00000	PI0	PD0	—	—	TM2	—	—	BRKP
M1	00001	CRSLT1L	CRSLT1H	CRSLT2L	CRSLT2H	AT1H	RT1H	AT2H	RT2H
M2	00010	—	—	—	—	—	—	—	—
M3	00011	—	—	—	—	—	—	—	—
M4	00100	—	—	—	—	—	—	—	—
M5	00101	—	—	—	—	—	—	—	—

Table 8. Special-Function Register Map (Section III)

MODULE		INDEX OF SPECIAL-FUNCTION REGISTER (SECTION III)															
M[x]	**SPECIFIER**	**10000**	**10001**	**10010**	**10011**	**10100**	**10101**	**10110**	**10111**	**11000**	**11001**	**11010**	**11011**	**11100**	**11101**	**11110**	**11111**
M0	00000	—	—	—	—	—	—	—	LOCK	ICDT0	ICDT1	ICDC	ICDF	ICDB	ICDA	ICDD	—
M1	00001	CO1	CO2	DSB	SSB2	AFEIE	—	—	—	—	—	—	—	—	—	—	—
M2	00010	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
M3	00011	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
M4	00100	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
M5	00101	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Table 9 lists the SFR register's functional bits and their bit positions. Table 10 specifies the default reset condition for all SFR bits. Special default values are labeled as "s" in the table. The default value for unused SFR bit locations is 0. Table 11 details all SFRs and their bit description. Registers are also identified by their address in the form of (xxh, yyh), where xxh is the register index in hex and yyh is the module specifier in hex.

Table 9. Special-Function Register Bit Function

REGISTER		MSB							LSB
MODULE 0									
PO0	[7:0]	—	PO0[6:0]						
EIF0	[7:0]	—	—	—	—	—	IE[2:0]		
EIE0	[7:0]	—	—	—	—	—	EX[2:0]		
EIES0	[7:0]	—	—	—	—	—	IT[2:0]		
TCON	[7:0]	TMRIE	TMRIF	TVALID	TMREN	TCLK	TPSS[2:0]		
TFRQ	[7:0]	TFRQ[7:0]							
TCNT	[7:0]	TCNT[7:0]							
PI0	[7:0]	—	PI0[6:0]						
PD0	[7:0]	—	PD0[6:0]						
BRKP	[15:0]	—	—	—	—	—	—	—	BREAK
ICDT0	[15:0]	ICDT0[15:0]							
ICDT1	[15:0]	ICDT1[15:0]							
ICDC	[7:0]	DME	TE	REGE	—	CMD3	CMD2	CMD1	CMD0
ICDF	[7:0]	—	—	—	—	—	—	SPE	TXC
ICDB	[7:0]	ICDB[7:0]							
ICDA	[15:0]	ICDA[15:0]							
ICDD	[15:0]	ICDD[15:0]							
MODULE 1									
AFEINTST	[7:0]	—	—	—	—	IWUP2	IWUP1	IDR2	IDR1
SCT	[7:0]	—	—	—	—	—	—	SCEN	SCT
CRNG	[7:0]	—	—	CRNG2[1:0]		—	—	CRNG1[1:0]	
PD	[7:0]	—	—	—	—	—	PD2	PD1	SB
WU1	[7:0]	—	—	—	—	—	AO1	RE1	AE1
WU2	[7:0]	—	—	—	—	—	AO2	RE2	AE2
FEL	[7:0]	—	—	FEL[5:0]					
FEB	[7:0]	—	—	—	FEB[4:0]				
CRSLT1L	[7:0]	CRSLT1[3:0]				—	—	—	OVR1
CRSLT1H	[7:0]	CRSLT1[11:4]							
CRSLT2L	[7:0]	CRSLT2[3:0]				—	—	—	OVR2
CRSLT2H	[7:0]	CRSLT2[11:4]							
AT1H	[7:0]	AT1[11:4]							
RT1H	[7:0]	RT1[11:4]							
AT2H	[7:0]	AT2[11:4]							
RT2H	[7:0]	RT2[11:4]							
CO1	[7:0]	—	—	CO1[5:0]					
CO2	[7:0]	—	—	CO2[5:0]					
DSB	[7:0]	—	—	—	DSB[4:0]				
SSB2	[7:0]	—	—	—	SSB2[4:0]				
AFEIE	[7:0]	—	—	—	—	EIWUP2	EIWUP1	EDR2	EDR1

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Table 10. Special-Function Register Reset Values

MODULE 0					MODULE 1				
REGISTER	MSB			LSB	REGISTER	MSB			LSB
PO0	—	—	0111	1111	AFEINTST	—	—	0000	0000
EIF0	—	—	0000	0000	SCT	—	—	0000	0010
EIE0	—	—	0000	0000	CRNG	—	—	0010	0010
EIES0	—	—	0000	0000	PD	—	—	0000	0000
TCON	—	—	0000	0000	WU1	—	—	0000	0100
TFRQ	—	—	0000	0000	WU2	—	—	0000	0100
TCNT	—	—	0000	0000	FEL	—	—	0001	1110
PI0	—	—	ssss	ssss	FEB	—	—	0000	0000
PD0	—	—	0000	0000	CRSLT1L	—	—	0000	0000
BRKP	0000	0000	0000	0000	CRSLT1H	—	—	0000	0000
ICDT0	0000	0000	0000	0000	CRSLT2L	—	—	0000	0000
ICDT1	0000	0000	0000	0000	CRSLT2H	—	—	0000	0000
ICDC	—	—	0000	0000	AT1H	—	—	0000	0000
ICDF	—	—	0000	0000	RT1H	—	—	0000	0000
ICDB	—	—	0000	0000	AT2H	—	—	0000	0000
ICDA	0000	0000	0000	0000	RT2H	—	—	0000	0000
ICDD	0000	0000	0000	0000	CO1	—	—	0000	0000
—	—	—	—	—	CO2	—	—	0000	0000
—	—	—	—	—	DSB	—	—	0000	0001
—	—	—	—	—	SSB2	—	—	0000	0001
—	—	—	—	—	AFEIE	—	—	0000	0000

Table 11. Special-Function Register Bit Description

REGISTER	DESCRIPTION
PO0 (00h, 00h)	**Port 0 Output Register (8-Bit Register)**
Initialization	This register is set to 7Fh on all forms of reset.
Read/Write Access	Unrestricted read/write.
PO0[6:0]	**Port 0 Output Register Bits [6:0].** This register stores output data for this port when it is defined as an output port. Reading from the register returns the contents of the register and does not necessarily reflect the true state of the port pins. Changing the direction of this port does not change the data contents of the register.
PO0.7	**Reserved. Read returns 0.**
EIF0 (01h, 00h)	**External Interrupt Flag 0 Register (8-Bit Register)**
Initialization	This register is cleared to 00h on all forms of reset.
Read/Write Access	Unrestricted read/write.
EIF0[2:0]–IE[2:0]	**Interrupt Edge Detect Bits [2:0].** These bits are set when the edge selected by ITx is detected on the interrupt pin, INTx. Setting any of the bits to 1 generates an interrupt to the CPU if the corresponding interrupt is enabled. These bits remain set until cleared by software or a reset. It must be cleared by software before exiting the interrupt source routine or another interrupt is generated as long as the bit remains set.
EIF0[7:3]	**Reserved. Read returns 0.**

Table 11. Special-Function Register Bit Description (continued)

REGISTER	DESCRIPTION	
EIE0 (02h, 00h)	**External Interrupt Enable 0 Register (8-Bit Register)**	
Initialization	This register is cleared to 00h on all forms of reset.	
Read/Write Access	Unrestricted read/write.	
EIE0[2:0]–EX[2:0]	**Enable External Interrupt Bits [2:0].** Setting any of these bits to 1 enables the corresponding external interrupt, INTx. Clearing any of the bits to 0 disables the corresponding interrupt function.	
EIE0[7:3]	**Reserved. Read returns 0.**	
EIES0 (03h, 00h)	**External Interrupt Edge Select 0 Register (8-Bit Register)**	
Initialization	This register is cleared to 00h on all forms of reset.	
Read/Write Access	Unrestricted read/write.	
EIES0[2:0]–IT[2:0]	**Edge Select for External Interrupt Bits [2:0]:** ITx = 0 – External Interrupt INTx is positive edge triggered. ITx = 1 – External Interrupt INTx is negative edge triggered.	
EIS0[7:3]	**Reserved. Read returns 0.**	
TCON (04h, 00h)	**Timer Control Register (8-Bit Register)**	
Initialization	This register is cleared to 00h on all forms of reset.	
Read/Write Access	Unrestricted read. Write is unrestricted, unless otherwise stated in the following bit description.	
TCON[2:0]–TPSS[2:0]	**Timer Prescaler Select Bits [2:0].** The following bits select the prescaler value that apply to the select source clock.	
	TPSS[2:0]	**PRESCALE VALUE**
	000	/1
	001	/4
	010	/16
	011	/64
	100	/256
	101	/512
	110	/1024
	111	/2048
	These bits can only be written to when the timer is disabled (TMREN = 0).	
TCON.3–TCLK	**Timer Clock Select.** This bit selects the clock source used by the Timer. When this bit is cleared to 0, the system clock is used as the clock source. When this bit is set to 1, the 32kHz is used. This bit can only be written to when the timer is disabled (TMREN = 0).	
TCON.4–TMREN	**Timer Enable.** Setting this bit to 1 enables the Timer. Clearing this bit halts the Timer. The Timer continues to run in Stop mode if TMREN = 1.	
TCON.5–TVALID	**Timer Value Valid.** This bit indicates whether TCNT returns the valid value when 32kHz is selected as the clock source. When this bit is set to 1, TCNT returns the valid value. When this bit is cleared to 0, TCNT returns 0000h. This bit has no meaning when the system clock is used as a clock source. In this case, TCNT always returns valid value.	
TCON.6–TMRIF	**Timer Interrupt Flag.** This bit is set to 1 when the Timer count matches the timer frequency value. It is cleared either by software or a reset. A 0 on this bit indicates no Timer overflow has been detected.	
TCON.7–TMRIE	**Timer Interrupt Enable.** Setting this bit to 1 enables the Timer interrupt. Clearing this bit to 0 disables the Timer interrupt.	

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Table 11. Special-Function Register Bit Description (continued)

REGISTER	DESCRIPTION
TFRQ (05h, 00h)	**Timer Frequency Register (8-Bit Register)**
Initialization	This register is cleared to 00h on all forms of reset.
Read/Write Access	Unrestricted read. This register can only be written when TCLK = 0; otherwise, a write to this register is ignored.
TFRQ[7:0]	**Timer Reload Register Bits [7:0].** This register is used to store Timer overflow value.
TCNT (06h, 00h)	**Timer Count Register (8-Bit Register)**
Initialization	This register is cleared to 00h on all forms of reset.
Read/Write Access	Unrestricted read. This register can only be written when TCLK = 0; otherwise, a write to this register is ignored.
TCNT[7:0]	**Timer Count Register Bits [7:0].** This register is used to load and read a value to/from the Timer.
PI0 (08h, 00h)	**Port 0 Input Register (8-Bit Register)**
Initialization	The reset value for this register is dependent on the logical states of the pins.
Read/Write Access	Unrestricted read only
PI0[6:0]	**Port 0 Input Register Bits [6:0].** This register reflects the logic state of its port pins when read.
PI0.7	**Reserved. Read returns 0.**
PD0 (09h, 00h)	**Port 0 Direction Register (8-Bit Register)**
Initialization	This register is cleared to 00h on all forms of reset.
Read/Write Access	Unrestricted read/write.
PD0[6:0]	**Port 0 Direction Register Bits [6:0].** This register is used to determine the direction of the Port 0 function. The port pins are independently controlled by their direction bits. When a bit is set to 1, its corresponding pin is used as an output; data in the PO register is driven on the pin. When a bit is cleared to 0, its corresponding pin is used as an input, and allows an external signal to drive the pin. Note that when functioning as an input, the port pin is driven to a high-impedance state.
PD0.7	**Reserved. Read returns 0.**
BRKP (0Fh, 00h)	**Software Breakpoint Register (8-Bit Register)**
Initialization	This register is cleared to 00h on all forms of reset.
Read/Write Access	Unrestricted read/write.
BRKP.0–BREAK	**BREAK.** Setting this bit causes an emulation breakpoint to activate and halt the system on the instruction, which sets the bit. This bit is connected directly to the SBPE input on the emulation block and is self-clearing. A read of this bit always returns zero.
BRKP[7:1]	**Reserved. Read returns 0.**
ICDT0 (18h, 00h)	**In-Circuit Debug Temp 0 Register (16-Bit Register)**
Initialization	This register is cleared to 0000h after a power-on reset or a Test-Logic-Reset TAP state.
Read/Write Access	Unrestricted read/write access by the CPU from background or debug mode.
ICDT0[15:0]	**In-Circuit Debug Temp 0 Register Bits [15:0].** This register is intended for use by the utility ROM in-circuit debug or test routines as temporary storage to save registers that might otherwise have to be placed in the stack (e.g., DPC, DP[n]).
ICDT1 (19h, 00h)	**In-Circuit Debug Temp 1 Register (16-Bit Register)**
Initialization	This register is cleared to 0000h after a power-on reset or a Test-Logic-Reset TAP state.
Read/Write Access	Unrestricted read/write access by the CPU from background or debug mode.
ICDT1[15:0]	**In-Circuit Debug Temp 1 Register Bits [15:0].** This register is intended for use by the utility ROM in-circuit debug or test routines as temporary storage to save registers that might otherwise have to be placed in the stack (e.g., DPC, DP[n]).

Table 11. Special-Function Register Bit Description (continued)

REGISTER	DESCRIPTION	
ICDC (1Ah, 00h)	**In-Circuit Debug Control Register (8-Bit Register)**	
Initialization	This register is cleared to 00h after a power-on reset or a Test-Logic-Reset TAP state.	
Read/Write Access	Unrestricted read; all bits are set and cleared by the debug engine only. This register can be accessed using a valid JTAG debug engine command.	
ICDC[3:0]–CMD[3:0]	**Command Bits [3:0].** These bits reflect the current host command in debug mode. These bits are set by the debug engine and allow the ROM code to determine the course of action.	
	CMD[3:0]	**ACTION**
	0000	No operation
	0001	Read register
	0010	Read data memory
	0011	Read stack memory
	0100	Write register
	0101	Write data memory
	0110	Trace, single step the CPU
	0111	Return, return to background mode
	1000	Unlock password
	1001	Read selected register
	1010	Execute Test Execute Test (only supported when TME = 1)
	Other	Reserved
ICDC.4	**Reserved. Read returns 0.**	
ICDC.5–REGE	**Break-On Register Enable.** **This bit always returns 0. Therefore, BP4 and BP5 breakpoints are not supported.**	
ICDC.6–TE	**Timer Enabled.** **This bit always returns 0 and the timer is automatically disabled in debug mode.**	
ICDC.7–DME	**Debug Mode Enable.** When this bit is cleared to 0, background mode commands can be executed but breakpoints are disabled. When this bit is set to 1, breakpoints are enabled while background mode commands can still be entered. This bit is only set or cleared from background mode. This bit has no meaning for the ROM code.	
ICDF (1Bh, 00h)	**In-Circuit Debug Flag Register (8-Bit Register)**	
Initialization	This register is cleared to 00h after a power-on reset or a Test-Logic-Reset TAP state.	
Read/Write Access	Unrestricted read; only bit 0 is writable by the CPU.	
ICDF.0–TXC	**Serial Transfer Complete.** This bit is set by the hardware at the end of a transfer cycle at the TAP communication link. The TXC helps the debug engine to recognize host requests, either command or data. This bit is normally set by ROM code to signify/request sending or receiving data; the TXC must be cleared by the debug engine once set. CPU writes to the TXC bit result in clearing the JTAG PSS1:0 bits.	
ICDF.1–SPE	**System Program Enable.** The SPE bit used for in-system programming support and its logical state, when read by the CPU, always reflects the logical-OR of the SPE bit and the SPE bit of the System Programming Buffer (SPB) register in the TAP module (which is accessible using JTAG). The logical state of this bit determines the program flow after a reset. When it is set to logic 1, in-system programming is executed by the utility ROM. When it is cleared to 0, execution is transferred to user code. This bit allows read access by the CPU and is cleared to 0 only on a power-on reset or Test-Logic-Reset. The JTAG SPE bit is cleared by hardware when the ROD bit is set. **The SPE bit is read only.**	

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Table 11. Special-Function Register Bit Description (continued)

REGISTER	DESCRIPTION
ICDF[7:2]	**Reserved. Read returns 0.**
ICDB (1Ch, 00h)	**In-Circuit Debug Buffer Register (8-Bit Register)**
Initialization	This register is cleared to 00h after a power-on reset or a Test-Logic-Reset TAP state.
Read/Write Access	Unrestricted read/write by CPU.
ICDB[7:0]	**In-Circuit Debug Buffer Bits [7:0].** ICDB serves as the parallel holding buffer for the debug shift register of the TAP. Data is read from or written to ICDB for serial communication between the debug function and the external host. This register is mapped to the SFR space for read/write access by the CPU.
ICDA (1Dh, 00h)	**In-Circuit Debug Address Register (16-Bit Register)**
Initialization	This register is cleared to FFFFh after a power-on reset or a Test-Logic-Reset TAP state.
Read/Write Access	Unrestricted read by the CPU. This register can be accessed using a valid JTAG debug engine command.
ICDA[15:0]	**In-Circuit Debug Address Bits [15:0].** This register serves as the address register for the debug engine to store a specific location for the ROM code execution. This register is also used by the debug engine as a mask register to mask out don't care bits in the ICDD register when BP5 is used as a register breakpoint. When a bit in this register is set to 1, the corresponding bit location in the ICDD register is compared to the updating destination data to determine if a break should be generated. When a bit in this register is cleared, the corresponding bit in the ICDD register becomes a don't care and is not compared against the updating data. When all bits in this register are cleared, any updated data pattern causes a break when the BP5 register matches the destination register address of the current instruction.
ICDD (1Eh, 00h)	**In-Circuit Debug Data Register (16-Bit Register)**
Initialization	This register is cleared to 0000h after a power-on reset or a Test-Logic-Reset TAP state.
Read/Write Access	Unrestricted read by the CPU. This register can be accessed using a valid JTAG debug engine command.
ICDD[15:0]	**In-Circuit Debug Data Bits [15:0].** This register serves as the data/count register for the debug engine to store data or read count for ROM code execution. This register is also used by the debug engine as a data register for content matching when BP5 is used as a register breakpoint. In this case, only data bits in this register with their corresponding mask bits in the ICDA register set is compared with the updated destination data to determine if a break should be generated.
AFEINTST (00h, 01h)	**AFE Interrupt Status Register (8-Bit Register)**
Initialization	This register is cleared to 00h on all forms of reset.
Read/Write Access	Unrestricted read/write. See the following individual bit definitions for write restriction.
AFEINTST.0–IDR1	**CH1 Data Ready Interrupt Flag.** This bit is set to 1 when a new conversion result is available. This bit remains set unless cleared by software.
AFEINTST.1–IDR2	**CH2 Data Ready Interrupt Flag.** This bit is set to 1 when a new conversion result is available. This bit remains set unless cleared by software.
AFEINTST.2–IWUP1	**CH1 Wake-Up Event Interrupt Flag.** This bit is set to 1 when a wake-up condition is detected. This bit remains set unless cleared by software.
AFEINTST.3–IWUP2	**CH2 Wake-Up Event Interrupt Flag.** This bit is set to 1 when a wake-up condition is detected. This bit remains set unless cleared by software.
AFEINTST[7:4]	**Reserved. Read returns 0.**

Table 11. Special-Function Register Bit Description (continued)

REGISTER	DESCRIPTION	
SCT (01h, 01h)	**Single Conversion Register (8-Bit Register)**	
Initialization	This register is cleared to 02h on all forms of reset.	
Read/Write Access	Unrestricted read/write. See the following individual bit definitions for write restriction.	
SCT.0–SCT	**Single Conversion Trigger.** Setting this bit to 1 initiates a conversion to an enabled channel (PDx = 0) when the single conversion mode is enabled. Once set to 1, a write to this bit is ignored. This bit is automatically cleared to 0 at the end of the conversion.	
SCT.1–SCEN	**Single Conversion Enable.** Setting this bit to 1 enables the single conversion mode. Clearing this bit to 0 disables the single conversion mode.	
SCT[7:2]	**Reserved. Read returns 0.**	
CRNG (02h, 01h)	**Input Range Register (8-Bit Register)**	
Initialization	This register is cleared to 22h on all forms of reset.	
Read/Write Access	Unrestricted read/write.	
CRNG[1:0]–CRNG1[1:0]	**CH1 Capacitance Input Range Bits [1:0].** These bits set the capacitance input range.	
	CRNG1[1:0]	**CAPACITANCE RANGE (pF)**
	00	5
	01	10
	10	20
	11	20
CRNG[3:2]	**Reserved. Read returns 0.**	
CRNG[5:4]–CRNG2[1:0]	**CH2 Capacitance Input Range Bits [1:0].** These bits set the capacitance input range.	
	CRNG2[1:0]	**CAPACITANCE RANGE (pF)**
	00	5
	01	10
	10	20
	11	20
CRNG[7:6]	**Reserved. Read returns 0.**	
PD (03h, 01h)	**Power-Down Register (8-Bit Register)**	
Initialization	This register is cleared to 0000h on all forms of reset.	
Read/Write Access	Unrestricted read. Write to this register is unrestricted, unless otherwise stated in the following bit definition.	
PD.0–SB	**Standby Enable.** Setting this bit to 1 enables the standby mode for both channels. Clearing this bit to 0 disables the standby mode. When standby mode is enabled, the conversion occurs at a divided-down rate as defined by DSB and SSB. Once set, this bit can be cleared by software. This bit is automatically cleared to 0 if a wake-up event occurs.	
PD.1–PD1	**CH1 Power-Down.** Setting this bit to 1 powers down CH1. Clearing this bit to 0 powers up CH1.	
PD.2–PD2	**CH2 Power-Down.** Setting this bit to 1 powers down CH2. Clearing this bit to 0 powers up CH2.	
PD[7:3]	**Reserved. Read returns 0.**	
WU1 (04h, 01h)	**CH1 Wake-Up Control Register (8-Bit Register)**	
Initialization	This register is cleared to 04h on all forms of reset.	
Read/Write Access	Unrestricted read/write.	
WU1.0–AE1	**CH1 Absolute Wake-Up Threshold Enable.** Setting this bit to 1 enables the absolute wake-up threshold detection. Clearing this bit to 0 disables the absolute wake-up threshold detection.	

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Table 11. Special-Function Register Bit Description (continued)

REGISTER	DESCRIPTION
WU1.1–RE1	**CH1 Rate-of-Change Wake-Up Threshold Enable.** Setting this bit to 1 enables the rate-of-change wake-up threshold detection. Clearing this bit to 0 disables the rate-of-change wake-up threshold detection.
WU1.2–AO1	**CH1 AND/OR Mode Enable.** Setting this bit to 1 causes an interrupt to the CPU when both the absolute and rate-of-change threshold are exceeded. Both AEI and REI must be enabled when AO1 is set to 1. Clearing this bit to 0 causes an interrupt to the CPU when either the absolute threshold or rate-of-change threshold is exceeded.
WU1[7:3]	**Reserved. Read returns 0.**
WU2 (05h, 01h)	**Channel 2 Wake-Up Control Register (8-Bit Register)**
Initialization	This register is cleared to 04h on all forms of reset.
Read/Write Access	Unrestricted read/write.
WU2.0–AE2	**CH2 Absolute Wake-Up Threshold Enable.** Setting this bit to 1 enables the absolute wake-up threshold detection. Clearing this bit to 0 disables the absolute wake-up threshold detection.
WU2.1–RE2	**CH2 Rate-of-Change Wake-Up Threshold Enable.** Setting this bit to 1 enables the rate-of-change wake-up threshold detection. Clearing this bit to 0 disables the rate-of-change wake-up threshold detection.
WU2.2–AO2	**CH2 AND/OR Mode Enable.** Setting this bit to 1 causes an interrupt to the CPU when both the absolute and rate-of-change threshold are exceeded. Clearing this bit to 0 causes an interrupt to the CPU when either the absolute or rate-of-change threshold is exceeded.
WU2[7:3]	**Reserved. Read returns 0.**
FEL (06h, 01h)	**Excitation Frequency Low-Limit Register (8-Bit Register)**
Initialization	This register is set to 1Eh on all forms of reset.
Read/Write Access	Unrestricted read/write.
FEL[5:0]	**Excitation Frequency Low-Limit Bits [5:0].** These bits set the lower end of the excitation frequency (FEL x 10kHz).
FEL[7:6]	**Reserved. Read returns 0.**
FEB (07h, 01h)	**Excitation Frequency Spread-Spectrum Bandwidth Register (8-Bit Register)**
Initialization	This register is cleared to 00h on all forms of reset.
Read/Write Access	Unrestricted read/write.
FEB[4:0]	**Excitation Frequency Spread-Spectrum Bandwidth Bits [4:0].** These bits set the excitation frequency bandwidth (FEB x 20kHz).
FEB[7:5]	**Reserved. Read returns 0.**
CRSLT1L (08h, 01h)	**Channel 1 Conversion Result Register (8-Bit Register)**
Initialization	This register is cleared to 00h on all forms of reset.
Read/Write Access	This register is read only.
CRSLT1L.0–OVR1	**CH1 Overrange Flag.** The overrange flag is set to 1 by hardware if the current conversion causes overranging of the C–to–D conversion. This bit is cleared to 0 if the current conversion does not cause overranging.
CRSLT1L[3:1]	**Reserved. Read returns 0.**
CRSLT1L[7:4]	**Channel 1 Conversion Result Bits [3:0].** This register contains the lower 4 bits of the C–to–D conversion.

Table 11. Special-Function Register Bit Description (continued)

REGISTER	DESCRIPTION
CRSLT1H (09h, 01h)	**Channel 1 Conversion Result Register (8-Bit Register)**
Initialization	This register is cleared to 00h on all forms of reset.
Read/Write Access	This register is read-only.
CRSLT1H[7:0]	**Channel 1 Conversion Result Bits [11:4].** This register contains the upper 8 bits of the C–to–D conversion.
CRSLT2L (0Ah, 01h)	**Channel 2 Conversion Result Register (8-Bit Register)**
Initialization	This register is cleared to 00h on all forms of reset.
Read/Write Access	This register is read-only.
CRSLT2L.0–OVR2	**CH2 Overrange Flag.** The overrange flag is set to 1 by hardware if the current conversion causes overranging of the C–to–D conversion. This bit is cleared to 0 if the current conversion does not cause overranging.
CRSLT2L[3:0]	**Reserved. Read returns 0.**
CRSLT2L[7:4]	**Channel 2 Conversion Result Bits [3:0].** This register contains the lower 4 bits of the C–to–D conversion.
CRSLT2H (0Bh, 01h)	**Channel 2 Conversion Result Register (8-Bit Register)**
Initialization	This register is cleared to 00h on all forms of reset.
Read/Write Access	This register is read only.
CRSLT2H[7:0]	**Channel 2 Conversion Result Bits [11:4].** This register contains the upper 8 bits of the C–to–D conversion.
AT1H (0Ch, 01h)	**CH1 Absolute Wake-Up Threshold Register (8-Bit Register)**
Initialization	This register is cleared to 00h on all forms of reset.
Read/Write Access	Unrestricted read/write.
AT1H[7:0]	**CH1 Absolute Wake-Up Threshold Bits [11:4].** This register contains the threshold value against which a wake-up event is generated in standby mode. This register has no effect if the absolute threshold is not enabled.
RT1H (0Dh, 01h)	**CH1 Rate-of-Change Wake-Up Threshold Register (8-Bit Register)**
Initialization	This register is cleared to 0000h on all forms of reset.
Read/Write Access	Unrestricted read/write.
RT1H[7:0]	**CH1 Rate-of-Change Wake-Up Threshold Bits [11:4].** This register contains the threshold value against which a wake-up event is generated in standby mode. This register has no effect if the rate-of-change threshold is not enabled.
AT2H (0Eh, 01h)	**CH2 Absolute Wake-Up Threshold Register (8-Bit Register)**
Initialization	This register is cleared to 0000h on all forms of reset.
Read/Write Access	Unrestricted read/write.
AT2H[7:0]	**CH2 Absolute Wake-Up Threshold Bits [11:4].** This register contains the threshold value against which a wake-up event is generated in standby mode. This register has no effect if the absolute threshold is not enabled.
RT2H (0Fh, 01h)	**CH2 Rate-of-Change Wake-Up Threshold Register (8-Bit Register)**
Initialization	This register is cleared to 0000h on all forms of reset.
Read/Write Access	Unrestricted read/write.
RT2H[7:0]	**CH2 Rate-of-Change Wake-Up Threshold Bits [11:4].** This register contains the threshold value against which a wake-up event is generated in standby mode. This register has no effect if the rate-of-change threshold is not enabled.

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Table 11. Special-Function Register Bit Description (continued)

REGISTER	DESCRIPTION
CO1 (10h, 01h)	**Channel 1 Capacitance Offset Register (8-Bit Register)**
Initialization	This register is cleared to 00h on all forms of reset.
Read/Write Access	Unrestricted read/write.
CO1[5:0]	**Channel 1 Capacitance Offset Bits [5:0].** These bits select the amount of capacitance compensation to be applied. Capacitance can be adjusted in a 1pF increment up to 63pF.
CO1[7:6]	**Reserved. Read returns 0.**
CO2 (11h, 01h)	**Channel 2 Capacitance Offset Register (8-Bit Register)**
Initialization	This register is cleared to 00h on all forms of reset.
Read/Write Access	Unrestricted read/write.
CO2[5:0]	**Channel 2 Capacitance Offset Bits [5:0].** These bits select the amount of capacitance compensation to be applied. Capacitance can be adjusted in a 1pF increment up to 63pF.
CO2[7:6]	**Reserved. Read returns 0.**
DSB (12h, 01h)	**Standby State Conversion Rate Divider Register (8-Bit Register)**
Initialization	This register is cleared to 01h on all forms of reset.
Read/Write Access	Unrestricted read/write.
DSB[4:0]	**Standby State Conversion Rate Divider Bits [4:0].** These bits set the conversion rate divider for both channels 1 and 2 in the standby state. The conversion rate is reduced by DSB[4:0].
DSB[7:5]	**Reserved. Read returns 0.**
SSB2 (13h, 01h)	**Channel 2 Standby State Conversion Rate Subdivider Register (8-Bit Register)**
Initialization	This register is cleared to 01h on all forms of reset.
Read/Write Access	Unrestricted read/write.
SSB2[4:0]	**Channel 2 Standby State Conversion Rate Divider Bits [4:0].** These bits set the additional channel 2 conversion rate divider that is applied, in addition to the DSB divide ratio in the standby state. The conversion rate for channel 2 is divided by DSB[4:0] x SSB2[4:0].
SSB2[7:5]	**Reserved. Read returns 0.**
AFEIE (14h, 01h)	**AFE Interrupt Enable Register (8-Bit Register)**
Initialization	This register is cleared to 00h on all forms of reset.
Read/Write Access	Unrestricted read/write.
AFEIE.0–EDR1	**CH1 Data Ready Interrupt Enable.** Setting this bit to 1 generates an interrupt to the CPU when the IDR1 bit is set to 1. Clearing this bit to 0 disables an interrupt from generating.
AFEIE.1–EDR2	**CH2 Data Ready Interrupt Enable.** Setting this bit to 1 generates an interrupt to the CPU when the IDR2 bit is set to 1. Clearing this bit to 0 disables an interrupt from generating.
AFEIE.2–EIWUP1	**CH1 Wake-Up Event Interrupt Enable.** Setting this bit to 1 generates an interrupt to the CPU when EIWUP1 = 1. Clearing this bit to 0 disables an interrupt from generating.
AFEIE.3–EIWUP2	**CH2 Wake-Up Event Interrupt Enable.** Setting this bit to 1 generates an interrupt to the CPU when EIWUP2 = 1. Clearing this bit to 0 disables an interrupt from generating.
AFEIE[7:4]	**Reserved. Read returns 0.**

Memory Organization

There are three distinct memory areas in the IC's registers, program memory, and data memory. All memories are located on-chip.

Data memory is realized by SRAM memory, which allows both read and write access; program memory is implemented with nonvolatile Flash memory. The user application codes are programmed using a bootstrap loader. The bootstrap loader program is located in the utility code space. From a user perspective, the utility code segment is a program segment in the program memory map.

As illustrated in Figure 3, the device incorporates 4KB program memory, 4KB Utility ROM, and 128 bytes SRAM data memory.

Data memory is contiguous from 0000h to 03Fh words. Programmable memory begins at address 0000h and is contiguous through a maximum of 7FFh words.

The device also incorporates a soft stack using data RAM for the stack.

The MMU provides access controls for program and data memories. The built-in bootstrap loader is used to support Flash memory erase/program operations.

Register Space

Two of the register modules (M0/M1) are used by the device.

Data Memory

On-chip data memory begins at address 0000h and is contiguous through the internal data memory space to 03Fh words (128 bytes).

Data memory mapping and access control are handled by the MMU. Read/write access to the data memory can be in word or in byte.

Program Memory

The program memory is implemented using nonvolatile Flash memory. Flash memory provides in-system programming capability but this memory technology requires erase operation before a write operation and the time required to carry out write access is extremely long. Write access to nonvolatile memory is actually performed by utility ROM code for the device.

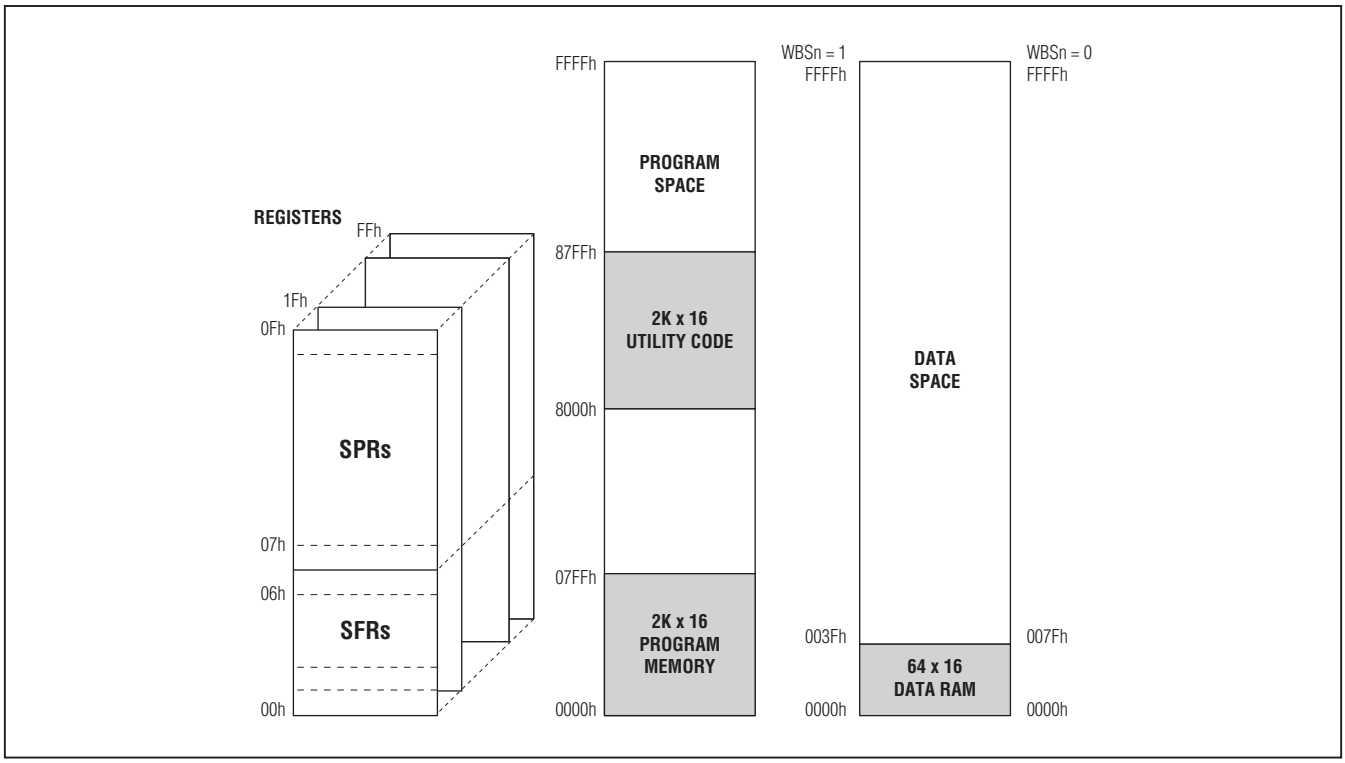


Figure 3. Memory Map

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Utility Code

A program segment on top of the 32K program memory space is realized by ROM, which provides system utility functions:

- Reset vector
- Bootstrap function for system initialization
- In-circuit debug

Reset vector is located in the utility code, starting at 8000h. Following each reset, the processor automatically starts execution from the utility code, allowing the utility code to perform any necessary system-support functions.

Note that the default value for the instruction pointer is effectively set to the lowest address of the program memory; a reset forces the program address to 8000h directly and activates the utility code for code fetch. The most significant bit of the address bus continues to be held high until the program flow is first progressed outside the utility code memory range.

The SPE bit can be used to force the processor to bypass the utility code reset routine and start execution from the user code after a reset. The device is always reset to 8000h after a reset. If the SPE bit is cleared to logic 0, the processor vectors out of the utility code segment immediately and starts standard user-program execution at location 0000h of the program memory. However, if the SPE bit is set to logic 1, the processor starts execution from the utility code, entering to the bootstrap loader mode. The SPE bit is defaulted to 0. To enter the bootstrap loader mode, the SPE bit can be set during POR using the JTAG interface. The bootstrap loader should clear the SPE bit to 0 after program initialization.

If the utility code is bypassed during reset, the initialization vector should be stored in the lower bytes of the program memory.

Nonvolatile Memory Programming

The program memory is realized in the Flash memory, which provides a storage area for critical code/data that must be maintained in case of power-down.

Write access to the nonvolatile memory is performed by a utility code routine that is initiated by a user call to the subroutine. The ROM routine can perform the write to the Flash.

Program Stack

The device supports only a software stack that is located in the normal data memory space and its contents are fixed as 16-bit words. The program stack supports subroutine calls and system interrupts. The stack can also be used to store variables by the user software. The program stack is addressed by the stack pointer (SP).

The SP designates the stack location at the top of the stack, which is the location of the last word stored. The SP register is a 16-bit register but only the lower bits are implemented as per C_SP_LEN configuration. The SP is defaulted to 02F0h and the content of the SP is predecremented for write and postincremented for read. The SP value is automatically decreased before a write operation, and automatically increased after a read operation.

Note that the PUSH and POP instructions are provided for the convenience of programmers who prefer to use these traditional stack-related instructions. From the assembly and the hardware point of view, the PUSH and POP instructions are equivalent to the MOVE @++SP, XXX and MOVE XXX, @SP-- instruction, respectively. These MOVE instructions involved with indirect SP predecrement/postincrement the SP register value accordingly.

Memory Management Unit

Memory allocation and access control for program and data memories are managed by the MMU. Program stack is controlled by a dedicated state machine for fast stack operation.

The instruction pointer is fully decoded. Access to any nonexisting physical memory returns NOP. The instruction pointer keeps increasing until it reaches 0FFFFh (top of IP), then it wraps around to 0000h.

The data pointer is fully decoded. Access to any nonexisting physical memory returns a value of 0. If an instruction requests the data pointer to be increased, it keeps increasing until it reaches 0FFFFh (top of DP), then it wraps around to 0000h. If an instruction requests the data pointer to be decreased, it keeps decreasing until it reaches 0000h, then it wraps around to 0FFFFh.

The last word in sector 1 (07FFh) is used as a security lock. When content of the security word[15:0] is equal to FFFFh, the memory is unsecured and program and erase operations are allowed. When security word[15:0] is any other value, all memory write operations are blocked by the hardware.

CAUTION: Do not write any value other than FFFFh in memory location 07FFh (last word of the Flash memory). Any value other than FFFFh in this location PERMANENTLY secures the Flash memory and no further Flash write or erase operations are allowed.

All erase/program operations are under the control of the Flash controller and assisted by the ROM code.

The device does not support individual word programming. A whole page must be programmed at the same time. In attempts to write to an individual word, the data intended for the individual word is copied to the entire page.

CAUTION: It is the user's responsibility to ensure that a Flash high-voltage operation (erase or write) is allowed to complete without external intervention. When an external intervention such as POR, or asserting the reset pin, is applied during a Flash high-voltage operation, the Flash operation is aborted. This can cause irreversible damage to the Flash and make the Flash inoperable.

Instruction Set

The device supports all the standard MAXQ20 instructions when executing from Flash and the utility ROM (Table 12).

For a complete list of instructions and detailed descriptions, refer to the *MAXQ Family Instruction Set Summary* in the MAXQ Family User's Guide.

Table 12. MAXQ Family Instruction Set Summary

	MNEMONIC	DESCRIPTION	16-BIT INSTRUCTION WORD	STATUS BITS AFFECTED	AP INC/DEC	NOTES
LOGICAL OPERATIONS	AND src	Acc ← Acc AND src	f001 1010 ssss ssss	S, Z	Y	4
	OR src	Acc ← Acc OR src	f010 1010 ssss ssss	S, Z	Y	4
	XOR src	Acc ← Acc XOR src	f011 1010 ssss ssss	S, Z	Y	4
	CPL	Acc ← ~Acc	1000 1010 0001 1010	S, Z	Y	—
	NEG	Acc ← ~Acc + 1	1000 1010 1001 1010	S, Z	Y	—
	SLA	Shift Acc left arithmetically	1000 1010 0010 1010	C, S, Z	Y	—
	SLA2	Shift Acc left arithmetically twice	1000 1010 0011 1010	C, S, Z	Y	—
	SLA4	Shift Acc left arithmetically four times	1000 1010 0110 1010	C, S, Z	Y	—
	RL	Rotate Acc left (w/o C)	1000 1010 0100 1010	S	Y	—
	RLC	Rotate Acc left (through C)	1000 1010 0101 1010	C, S, Z	Y	—
	SRA	Shift Acc right arithmetically	1000 1010 1111 1010	C, Z	Y	—
	SRA2	Shift Acc right arithmetically twice	1000 1010 1110 1010	C, Z	Y	—
	SRA4	Shift Acc right arithmetically four times	1000 1010 1011 1010	C, Z	Y	—
	SR	Shift Acc right (0 → msbit)	1000 1010 1010 1010	C, S, Z	Y	—
	RR	Rotate Acc right (w/o C)	1000 1010 1100 1010	S	Y	—
	RRC	Rotate Acc right (though C)	1000 1010 1101 1010	C, S, Z	Y	—
BIT OPERATIONS	MOVE C, Acc.<b>	C ← Acc.<b>	1110 1010 bbbb 1010	C	—	—
	MOVE C, #0	C ← 0	1101 1010 0000 1010	C	—	—
	MOVE C, #1	C ← 1	1101 1010 0001 1010	C	—	—
	CPL C	C ← ~C	1101 1010 0010 1010	C	—	—
	MOVE Acc.<b>, C	Acc.<b> ← C	1111 1010 bbbb 1010	S, Z	—	—
	AND Acc.<b>	C ← C AND Acc.<b>	1001 1010 bbbb 1010	C	—	—
	OR Acc.<b>	C ← C OR Acc.<b>	1010 1010 bbbb 1010	C	—	—
	XOR Acc.<b>	C ← C XOR Acc.<b>	1011 1010 bbbb 1010	C	—	—
	MOVE dst.<b>, #1	dst.<b> ← 1	1ddd dddd 1bbb 0111	C, S, E, Z	—	5
	MOVE dst.<b>, #0	dst.<b> ← 0	1ddd dddd 0bbb 0111	C, S, E, Z	—	5
	MOVE C, src.<b>	C ← src.<b>	fbbb 0111 ssss ssss	C	—	
MATH	ADD src	Acc ← Acc + src	f100 1010 ssss ssss	C, S, Z, OV	Y	4
	ADDC src	Acc ← Acc + (src + C)	f110 1010 ssss ssss	C, S, Z, OV	Y	4
	SUB src	Acc ← Acc – src	f101 1010 ssss ssss	C, S, Z, OV	Y	4
	SUBB src	Acc ← Acc – (src + C)	f111 1010 ssss ssss	C, S, Z, OV	Y	4

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Table 12. MAXQ Family Instruction Set Summary (continued)

	MNEMONIC	DESCRIPTION	16-BIT INSTRUCTION WORD	STATUS BITS AFFECTED	AP INC/DEC	NOTES
BRANCHING	{L/S}JUMP src	IP ← IP + src or src	f000 1100 ssss ssss	—	—	6
	{L/S}JUMP C, src	If C=1, IP ← (IP + src) or src	f010 1100 ssss ssss	—	—	6
	{L/S}JUMP NC, src	If C=0, IP ← (IP + src) or src	f110 1100 ssss ssss	—	—	6
	{L/S}JUMP Z, src	If Z=1, IP ← (IP + src) or src	f001 1100 ssss ssss	—	—	6
	{L/S}JUMP NZ, src	If Z=0, IP ← (IP + src) or src	f101 1100 ssss ssss	—	—	6
	{L/S}JUMP E, src	If E=1, IP ← (IP + src) or src	0011 1100 ssss ssss	—	—	6
	{L/S}JUMP NE, src	If E=0, IP ← (IP + src) or src	0111 1100 ssss ssss	—	—	6
	{L/S}JUMP S, src	If S=1, IP ← (IP + src) or src	f100 1100 ssss ssss	—	—	6
	{L/S}DJNZ LC[n], src	If --LC[n] <> 0, IP ← (IP + src) or src	f10n 1101 ssss ssss	—	—	6
	{L/S}CALL src	@++SP ← IP+1; IP ← (IP+src) or src	f011 1101 ssss ssss	—	—	6, 7
	RET	IP ← @SP--	1000 1100 0000 1101	—	—	—
	RET C	If C=1, IP ← @SP--	1010 1100 0000 1101	—	—	—
	RET NC	If C=0, IP ← @SP--	1110 1100 0000 1101	—	—	—
	RET Z	If Z=1, IP ← @SP--	1001 1100 0000 1101	—	—	—
	RET NZ	If Z=0, IP ← @SP--	1101 1100 0000 1101	—	—	—
	RET S	If S=1, IP ← @SP--	1100 1100 0000 1101	—	—	—
	RETI	IP ← @SP--; INS ← 0	1000 1100 1000 1101	—	—	—
	RETI C	If C=1, IP ← @SP--; INS ← 0	1010 1100 1000 1101	—	—	—
	RETI NC	If C=0, IP ← @SP--; INS ← 0	1110 1100 1000 1101	—	—	—
	RETI Z	If Z=1, IP ← @SP--; INS ← 0	1001 1100 1000 1101	—	—	—
	RETI NZ	If Z=0, IP ← @SP--; INS ← 0	1101 1100 1000 1101	—	—	—
	RETI S	If S=1, IP ← @SP--; INS ← 0	1100 1100 1000 1101	—	—	—
DATA TRANSFER	XCH (MAXQ20 only)	Swap Acc bytes	1000 1010 1000 1010	S	Y	—
	XCHN	Swap nibbles in each Acc byte	1000 1010 0111 1010	S	Y	—
	MOVE dst, src	dst ← src	fddd dddd ssss ssss	C, S, Z, E	(Note 8)	7, 8
	PUSH src	@++SP ← src	f000 1101 ssss ssss	—	—	7
	POP dst	dst ← @SP--	1ddd dddd 0000 1101	C, S, Z, E	—	7
	POPI dst	dst ← @SP--; INS ← 0	1ddd dddd 1000 1101	C, S, Z, E	—	7
	CMP src	E ← (Acc = src)	f111 1000 ssss ssss	E	—	—
	NOP	No operation	1101 1010 0011 1010	—	—	—

Note 4: The active accumulator (Acc) is not allowed as the src in operations where it is the implicit destination.

Note 5: Bit operation. Potentially affects C or E if the PSF register is the destination. Potentially affects S and/or Z if AP or APC is the destination.

Note 6: The '{L/S}' prefix is optional.

Note 7: Instructions that attempt to simultaneously push/pop the stack (e.g., PUSH @SP--, PUSH @SPI--, POP @++SP, POPI @++SP) or modify SP in a conflicting manner (e.g., MOVE SP, @SP--) are invalid.

Note 8: Special cases: If 'MOVE APC, Acc' sets the APC.CLR bit, AP is cleared, overriding any auto-inc/dec/modulo operation specified for AP. If 'MOVE AP, Acc' causes an auto-inc/dec/modulo operation on AP, this overrides the specified data transfer (i.e., Acc is not transferred to AP).

Special System Functions

Interrupt

The device supports interrupt through the Interrupt Vector (IV) register and the Interrupt Control (IC) register. The IV register allows the user program to set a preferred vector location to any program memory address. The IV register is fixed at 07FDh. Since the reset location can also be at 0000h, the user program must take care of any potential conflict between the reset and interrupt vector function.

Interrupt Sources

Interrupt sources can be classified into two categories:

- Asynchronous interrupt
- Synchronous interrupt

The device supports the following asynchronous interrupts:

- External interrupts
- Watchdog interrupt
- Timer interrupts
- AFE interrupts

All the other internal interrupts are synchronous interrupts. Synchronous internal interrupt is directly routed to the interrupt handler that can be recognized in one cycle.

Clock Generation

All functional units in the device are synchronized to the system clock that is generated from the 20MHz oscillator. The basic unit of time in the device is the system clock period. All storage logic blocks are triggered by the rising edge of the system clock.

Clock Sources

The internal clock circuitry generates the system clock from an internal 5MHz, which is derived from the 20MHz oscillator (Figure 4).

Each time-code execution must start or restart (e.g., exiting stop mode), the following sequence occurs:

1) Remove clock gating of internal 5MHz.
2) Reset the warm-up counter.
3) Wait for Flash to power up (about 10µs).
4) Allow the required warm-up delay of eight oscillator cycles of the 5MHz input.

The only time 20MHz turns off is if the CPU is in stop mode and AFE is in standby mode or powered down (PD register = 6). During stop mode, if the AFE is in standby mode, the oscillator is periodically turned off and on to allow the AFE to sample inputs. This causes an interrupt to the CPU if an enabled threshold condition is met.

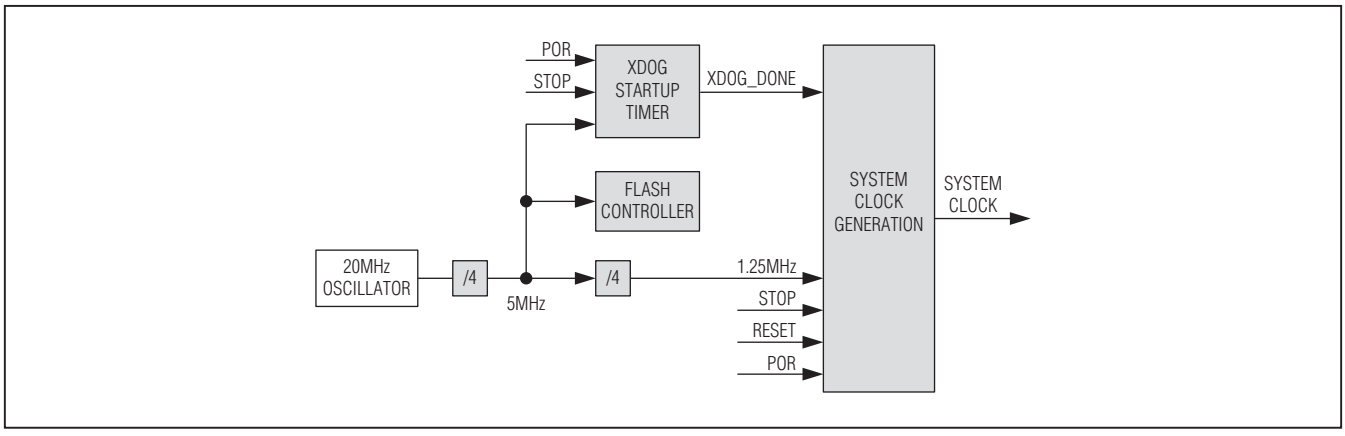


Figure 4. Clock Sources

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Table 13. Watchdog Timer Timeout Interval

WD[1:0]	TIMEOUT COUNT	TIMEOUT (s)
00	16384	0.5
01	32768	1.0
10	65536	2.0
11	131072	4.0

Watchdog Timer

The watchdog timer is clocked by the internal 32kHz oscillator (Table 13). All timing reference for the watchdog is based on the 32kHz.

In addition, the watchdog is disabled in debug mode and when SPE is set to 1. Clock to the watchdog is gated off in the conditions mentioned in the *Clock Sources* section.

Startup Timer

An independent startup timer (X-dog timer) functions:

- When the device is first powered up (POR)
- Exit from stop mode

The X-dog counter is used to count eight oscillator cycles of the 5MHz after the power supply is stable.

The power supply is stable after three-to-four 32kHz oscillator cycles.

The AFE circuit is released at least one 32kHz oscillator cycle before the CPU to allow for the 5MHz clock startup to properly occur.

The X-dog timer is active only for startup count; during normal operation, it is completely shut off.

Idle Mode

The device supports idle mode. Idle mode suspends the processor by holding the instruction pointer (IP) in a static state. No instructions are fetched and no processing occurs. Setting the IDLE bit in the SC register to logic 1 invokes the idle mode. The instruction that executes this step is the last instruction prior to freezing the program counter. Once in idle mode, all resources are preserved and all clocks remain active with the enabled peripherals. The power monitor continues to work, so the processor can exit the idle state using any of the interrupt sources that are enabled. The IDLE bit is cleared automatically once the idle state is exited, allowing the processor to execute the instruction that immediately follows the instruction that sets the IDLE bit.

Resetting the processor also removes the idle mode. Reset places the processor in a reset state and clears the IDLE bit.

Stop Mode

The stop mode disables all circuits within the processor, unless explicitly stated otherwise. All microcontroller system clocks, timers, and serial communication are stopped and no processing is possible. However, the AFE can be left in the standby mode and remain functional.

Once in stop mode, the CPU is in a static state. Its power consumption is mostly limited by the leakage current.

Stop mode is invoked by setting the STOP bit to logic 1. The processor enters the stop mode on the instruction that sets the STOP bit. Entering the stop mode does not affect the setting of the clock control bits. This allows the system to return to its original operating frequency following the stop mode removal, except if the removal is caused by RST or a power loss, which resets the clock generation to its default condition.

The processor can exit stop mode by:

- Any of the external interrupts that are enabled.
- External reset using the RST pin.
- Timer interrupt.
- Watchdog timeout.
- AFE interrupts that are enabled.

When the stop mode is removed, the device executes the following procedure:

1) Remove clock gating of internal 5MHz.
2) Reset the warm-up counter.
3) Wait for Flash to power up (about 10µs).
4) Allow the required warm-up delay of eight oscillator cycles of the 5MHz input.
5) Resume normal operation.

During stop mode, the following peripherals can be operational:

- Timer (TMREN = 1)
- Watchdog timer (WDCN.EWDI = 1)
- AFE

Reset Conditions

The device has four ways of entering a reset state:

- Power-on reset
- Watchdog timer reset
- External reset
- Internal system reset

If the reset is caused by watchdog or external sources, the clock source (5MHz oscillator) remains running, but no program execution is allowed. When the reset source is external, the user must remove the reset stimulus. When power is applied to the device, the power-on delay removes the stimulus automatically.

Power-On Reset Generation

The device incorporates an internal voltage reference and comparator to monitor V_{DD} and hold the device in reset if the supply is out of tolerance. Once V_{DD} has risen above the V_{POR} threshold, the device generates a power-on reset, starts the internal 20MHz, and counts eight cycles of the derived 5MHz to ensure that Flash is powered up and the system clock source has had time to stabilize. The processor then exits the reset state automatically and starts executing the program at location 8000h.

Software can determine that a POR has occurred by checking the power-on reset flag, POR in the WDCN register. Software should clear the POR flag after having read it. The POR is an asynchronous reset source.

Watchdog Timer Reset

The watchdog timer is a free-running timer with a programmable interval. The watchdog supervises the processor operation by requiring software to clear the timer counter before the timeout expires. If the timer is enabled and software fails to clear it before this interval expires, the device is placed into a reset state. The reset state maintains for about 90 system clock cycles. Once the reset is removed, the processor resumes execution at address 8000h. Software can determine if a reset is caused by a watchdog timeout by checking the watchdog timer reset flag, WTRF in the WDCN register. This flag is cleared by software only.

External Reset

If the $\overline{\text{RESET}}$ input is taken to logic 0, the device is forced into a reset state. An external reset is accomplished by holding the $\overline{\text{RESET}}$ pin low at least four clock cycles while the internal 5MHz clock is running. Once the reset state is invoked, it is maintained as long as $\overline{\text{RESET}}$ is pulled to logic 0. When the reset state is removed, the processor exits the reset state within four clock cycles and begin execution at address 8000h.

If a reset state is applied while the processor is in the stop mode, the reset causes the processor to exit the stop mode and forces the program counter to 8000h. The reset delay is four clock cycles.

The $\overline{\text{RESET}}$ is a bidirectional I/O. If a reset is caused by a watchdog timer reset or an internal system reset, an output reset pulse is also generated at the $\overline{\text{RESET}}$ pin. This reset pulse is asserted as long as a reset source is asserted and may not be able to drive the reset signal out if the $\overline{\text{RESET}}$ pin is connected to an RC reset circuitry. Connecting the $\overline{\text{RESET}}$ pin to a capacitor would not affect the internal reset condition.

Internal System Reset

An internal system reset can occur in system programming mode when the ROD bit is set to logic 1 while the SPE bit is 1.

Timer

The device has implemented an 8-bit timer with an 11-bit prescaler. The operation of the timer is configurable using the Timer Control register (TCON), Timer Frequency register (TFRQ), and the Timer Counter register (TCNT).

The timer is enabled by setting the Timer Enable Bit (TCON.TMREN) to 1. Once enabled, the timer starts counting from the initial TCNT value up to the TFRQ limit. When TCNT = TFRQ, the timer interrupt flag (TMRIF) is set to 1. This can cause an interrupt to the CPU if the timer interrupt is enabled (TMRIE = 1). Once the frequency limit is reached, TCNT is reset to 0 and continue to count up again.

The timer has two clock sources: system clock and the 32kHz clock. The selection is made using the Timer Clock Select (TCLK) bit. Due to different clock domains, when running off the 32kHz clock, reading of the TCNT register is only valid when the Timer Valid Flag (TVALID) is set to 1. When running the system clock, there is no restriction on running from TCLK. In addition, a write to TMREN when running off the 32kHz clock can be delayed due to synchronization between the two domains.

To increase the period between subsequent interrupts, an 11-bit prescaler is provided to prescale the input clock from 1 to 2048.

If the timer is enabled and running off the 32kHz clock source prior to the stop mode entry, the timer continues to run and invoke a stop mode exit if the interrupt is enabled.

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I/O Ports

The device implements an I/O port that is slightly different from those found in other MAXQ products.

The I/O port is still governed by the PI0, PO0, and PD0 registers.

When a PD0 register is cleared to 0, the port pin is operating as input and the pin is high impedance. The PI register contains the input value. PI is read only. PI may not always immediately equal PO due to capacitance at the output.

When a PD0 bit is set to 1, the output is enabled and the port pin output data corresponds to the PO value. In addition, OUT1 and OUT2 can ONLY be used as open-drain outputs. To use OUT1 and OUT2, clear PO bit to 0 and drive PD bit with inverted data.

When used as inputs, do not leave the port unconnected. Program unused port pins as outputs.

The external interrupt flag (EIF) is set to 1 when either a rising or falling edge is detected on a port pin regardless of its PD0 value. An interrupt is generated if it is enabled (EIE = 1).

At power-up, weak pullups are enabled on pin P0.[4:0]. To disable a pullup, clear the associated bit in the PO0 register.

The external interrupts are asynchronous.

Peripheral Prioritization

In the discussion that follows, priority only has meaning when two peripherals are both configured to drive outputs at the same time. Then one of the named peripheral's output has priority over the other, thus making the other's output disabled. Note that the lower priority peripheral can still be running and trying to output value onto the pad. However, since it has lower priority, its output is not driven onto the pad. For inputs, all peripherals have equal priority—even though the inputs may not be desirable. This means that if two input peripherals sharing the same pin are enabled, both of them receive the same input concurrently.

When a pin operates as input (whether it is a GPIO or special-function input), its behavior is governed by PO0 and PD0. Anytime a pin behaves as an output (because one of its special functions is configured as output), PO0 and PD0 are no longer used.

Port 0 supports the following functions: JTAG and GPIO.

All special functions have priority over GPIO.

JTAG Pin Special Function

The following apply when port pins are multiplexed with the JTAG function:

- The Special-Function Enable (SF Enable) signal for these JTAG pins must be active during reset so that the JTAG port is accessible during this time. SF enable is controlled by the TAP register bit, which is set to 1 on all resets.
- The Special-Function Input, when disabled, should be gated high for TMS. This disables the JTAG interface and forces the TAP into the Test-Logic-Reset state if the TCK pin has been toggled for more than five times.
- The TDO Special-Function Enable requires not only that TAP = 1, but also that the TAP be in the Shift-IR or Shift-DR state. The debug engine already produces a control signal (TDONZ) to denote when the TAP is in a shift state.

System Operating Modes

Following each system reset, the device automatically activates the utility ROM at 8000h. The reset vector in the utility ROM determines whether the program flow is to start in the user mode or the ROM bootstrap mode. The factor that determines which program is executed is the System Programming Enable (SPE) bit in the ICDF register. The SPE can be set/cleared with the debug mode command using the TAP interface.

The device supports various modes of system operations. Normally, the device is running in user mode to support user applications. The ROM bootstrap loader mode is used for initializing memory and system configuration. The debug mode is intended to provide real-time in-circuit debugging/emulation. The debug mode is supported through a test access port (TAP) and the TAP controller, which is compatible to the JTAG standard.

The TAP and the TAP controller are enabled after any reset, but remain inactive until a valid command is entered into the instruction register so as not to disrupt normal user-mode operation. If the TAP is not used, or the TAP interface pins are needed to serve another purpose, the TAP can be disabled by clearing the TAP enable (TAP) bit located in the SC system register.

Depending upon the mode desired, the instruction register should be loaded with the associated "debug" or "in-system programming" instruction. The method for loading the instruction register is described in the subsequent sections. These modes can be established anytime the digital supply voltage is above the POR threshold (e.g., during system reset both are acceptable).

JTAG Port

The device supports a TAP and TAP controller for communication with a bus master that can be either an automatic test equipment or a component that interfaces to a higher level test bus as part of a complete system. The communication operates across a 4-wire serial interface from a dedicated TAP, which is compatible to the JTAG IEEE® Standard 1149. The TAP is a general-purpose port, which allows access to many debug and test functions built into the core.

For detailed information on the TAP and TAP controller, refer to IEEE Standard 1149.1 *IEEE Standard Test Access Port and Boundary-Scan Architecture*.

Bootstrap Loader Mode

Internal nonvolatile memory can be initialized by the bootstrap loader in bootstrap loader mode. The bootstrap loader mode is enabled by an external host device using the TAP in the system programming instruction.

The system programming function is supported using the system programming buffer (SPB):

1) SPB.0–System programming enable (SPE)

   When it is set, the bootstrap loader program is activated to perform a bootstrap loader function.

   When it is cleared, the reset vector forces the IP to 8000h and starts normal user-program execution.

2) SPB.2:1–Programming source select (PSS[1:0])

   These bits allow the host to select programming interface sources:

PSS1	PSS0	PROGRAMMING SOURCE
0	0	JTAG
0	1	Reserved
1	0	Reserved
1	1	Reserved

User Mode

User applications are executed in user mode. In user mode, the processor can execute program routines in any memory segments. Normally, data is loaded and stored from/to the data memory. The device contains three memory segments among the program and the data spaces:

- Program segment
- Data segment
- Utility ROM segment

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Password-Protected Access

Some applications require preventive measures to protect against simple access and viewing of program code memory. To address this need for code protection, the device grants full access to in-system programming or in-circuit debugging utilities only after a password has been supplied. The password is defined as the 16 words of physical program memory at addresses 0010h to 001Fh. Note that using these memory locations for a password does not exclude their usage for general code space if a unique password is not needed. Also, if addresses 0010h to 001Fh contain all zeros or all FFFFs, the password function is effectively disabled and a password is not needed to gain access.

A single password lock bit (PWL) is implemented in the SC register. When the PWL is set to 1, a password is required to access the ROM loader utilities, which support read/write accessing of internal memory and debug functions. When PWL is cleared to 0, these utilities are fully accessible through the utility ROM without a password.

The PWL bit defaults to 1 by a POR. To access the ROM utilities, a correct password is needed; otherwise, access of ROM utilities is denied. Once the correct password has been supplied by the user, the ROM utility clears the password lock. The PWL remains clear until one of the following occurs:

- A power-on reset

OR

- Set to logic 1 by user software.

Entering Password

A password can be entered:

- Using the interface established by the PSS1 and PSS0 bits in system programming when the SPE bit is set to logic 1; the ROM loader must establish a suitable protocol for that interface to recognize the multibyte password.

OR

- Through the TAP interface directly in debug mode or test mode by issuing a password-unlock command; this command requires 32 follow-on transfer cycles, each containing a byte value compared with the password.

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Applications Information

Layout, Grounding, and Bypassing

For best performance, use PCBs. Ensure to separate digital and analog signal lines from each other. Do not run analog and digital signals parallel to one another (especially clock signals) or do not run digital lines underneath the IC package. High-frequency noise in the power-supply lines can affect performance. Bypass the V_{AA} and V_{DD} supplies with 0.47µF capacitors close to V_{AA} and V_{DD}. Bypass the V_{BATT} supply with a 0.1µF capacitor close to the V_{DD} pin. Minimize capacitor lead lengths for best supply-noise rejection. Refer to the MAX1441 Evaluation Kit for an example of proper layout.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TSSOP	U20M+2	21-0066	90-0116

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/10	Initial release	—

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