60V Low I_Q Buck Controller Plus 4-Channel 8A Configurable Buck DC/DCs

FEATURES

- **HV Buck Controller: V_{IN} = 4.5V to 60V, V_{OUT} = 5V/3.3V**
- **LV Buck Regulators: V_{INA-H} = 2.25V to 5.5V, $V_{OUT1-4} \geq$ 0.8V**
- **8×1A LV Buck Integrated Power Stages, Configurable as 2, 3 or 4 Output Channels**
- **8 Unique Output Configurations (1A to 4A Per Channel)**
- **Low Total No-Load Input Supply Current (I_Q)**
  - **15µA HV Controller Only ($5V_{OUT}$)**
  - **23µA HV Controller Only ($3.3V_{OUT}$)**
  - **33µA HV Controller ($3.3V_{OUT}$) Plus One LV Regulator**
  - **9µA Per Additional LV Regulator Channel**
- 1MHz to 3MHz Operation (HV Runs at 1/6 Frequency)
- Programmable or Synchronizable to External Clock
- Programmable Watchdog and Power-On Reset Delay
- IC Die Temperature Monitor Output
- Thermally Enhanced 48-Pin 7mm × 7mm QFN Package

APPLICATIONS

- Automotive and Industrial Always-On Systems
- General Purpose Multi-Channel Power Supplies

DESCRIPTION

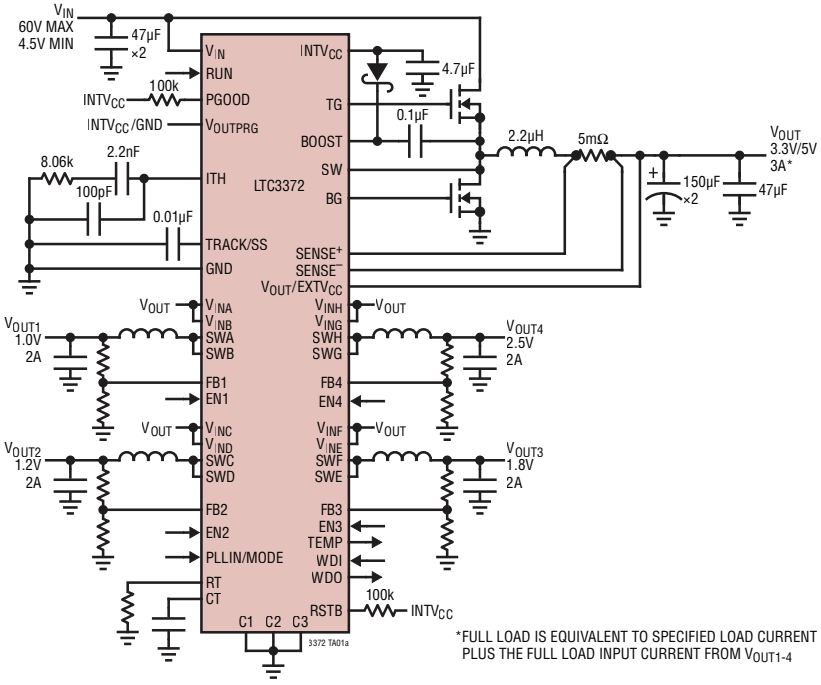
The LTC®3372 is a highly flexible multioutput power supply IC. The device includes a high-performance, high voltage (HV) step-down DC/DC switching regulator controller that drives an all N-channel synchronous power FET stage from a 4.5V to 60V input.

The LTC3372 also includes four low voltage (LV) synchronous buck regulators that can be programmed by the C1-C3 pins to share eight 1A integrated power stages in one of eight possible configurations. Each power stage is powered from independent inputs which may be connected to the HV buck's V_{OUT} or to other 2.25V to 5.5V supplies.

The CT pin programs timing parameters of the watchdog timer and LV outputs' Power-On Reset ($\overline{RST}$). Precision enable thresholds facilitate reliable power-up sequencing.

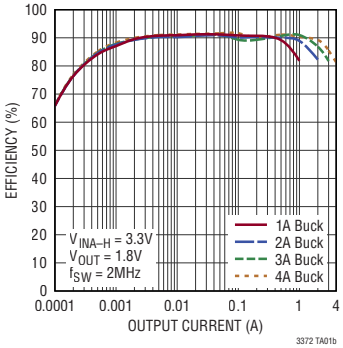
The LTC3372 is available in a 48-pin 7mm × 7mm QFN package.

TYPICAL APPLICATION



*FULL LOAD IS EQUIVALENT TO SPECIFIED LOAD CURRENT PLUS THE FULL LOAD INPUT CURRENT FROM V_{OUT1-4}

LV Efficiency vs Output Current



Low Voltage Buck Regulator Configurations

C3	C2	C1	BUCK1	BUCK2	BUCK3	BUCK4
0	0	0	2A	2A	2A	2A
0	0	1	3A	1A	2A	2A
0	1	0	3A	1A	1A	3A
0	1	1	4A	1A	1A	2A
1	0	0	3A	2A	–	3A
1	0	1	4A	–	2A	2A
1	1	0	4A	–	1A	3A
1	1	1	4A	–	–	4A

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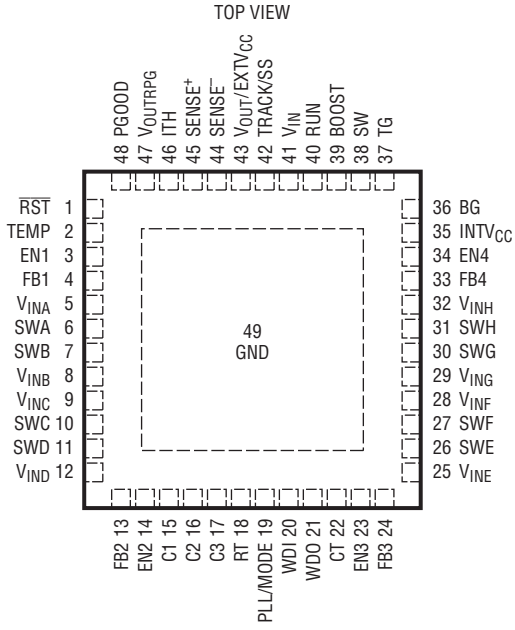
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply (V_{IN}) Voltage ..... –0.3V to 65V
Topside Driver (BOOST) Voltage ..... –0.3V to 71V
Switch (SW) Voltage ..... –5V to 65V
(BOOST-SW) Voltage ..... –0.3V to 6V
RUN Voltage ..... –0.3V to 65V
TRACK/SS, V_{OUT}/EXTV_{CC}, SENSE$^+$, SENSE$^-$, PGOOD, RT, PLL/MODE, FB1-4, EN1-4, C1-3, WDI, WDO, $\overline{RST}$, V_{INA-H} Voltages ..... –0.3V to 6V
TG, BG ..... (Note 11)
ITH, V_{OUTPRG}, CT, TEMP Voltages ..... –0.3V to (INTV_{CC} + 0.3V)
$I_{\overline{RST}}$, I_{WDO} 5mA
Operating Junction Temperature Range (Notes 2, 3) ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UK PACKAGE
48-LEAD (7mm × 7mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 49) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3372EUK#PBF	LTC3372EUK#TRPBF	LTC3372UK	48-Lead (7mm × 7mm) Plastic QFN	–40°C to 125°C
LTC3372IUK#PBF	LTC3372IUK#TRPBF	LTC3372UK	48-Lead (7mm × 7mm) Plastic QFN	–40°C to 125°C
LTC3372HUK#PBF	LTC3372HUK#TRPBF	LTC3372UK	48-Lead (7mm × 7mm) Plastic QFN	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN} = 12V, V_{RUN} = 5V, V_{OUT} = V_{INA-H} = 3.3V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{IN}	V_{IN} Pin Operating Voltage Range				4.5		60	V
I_Q (Forced Continuous/ Pulse-Skipping Mode)	No-Load V_{IN} Pin DC Current No-Load V_{OUT}/$EXTV_{CC}$ Pin + $SENSE^-$ Pin DC Current	PLL/MODE = $INTV_{CC}$ or $INTV_{CC}$/2 Run = V_{IN} EN1-4 = GND	V_{OUTPRG} = $INTV_{CC}$ (5V V_{OUT})			7 1450		µA µA
	No-Load V_{IN} Pin DC Current No-Load V_{OUT}/$EXTV_{CC}$ Pin + $SENSE^-$ Pin DC Current		V_{OUTPRG} = GND (3.3V V_{OUT})			1300 130		µA µA
I_Q (Burst Mode)	No-Load V_{IN} Pin DC Current No-Load V_{OUT}/$EXTV_{CC}$ Pin DC Current HV Controller On Only HV Controller and One LV Regulator On Additional I_Q, per LV Regulator On Additional I_Q, Watchdog On (Float CT Pin) Additional I_Q, TEMP On (Float TEMP Pin) No-Load $SENSE^-$ Pin DC Current	PLL/MODE = GND (Burst Mode) V_{IN} = 12V, V_{INA-H} = V_{OUT} (LV Regulators Powered from HV Regulator's Output), No Load on V_{OUT} or V_{OUT1-4}.	V_{OUTPRG} = $INTV_{CC}$ (5V V_{OUT})	● ● ●		4 20 52 +26 +7 +15 0.5	10 46 74 +39 +12 2	µA µA µA µA µA µA µA
	No-Load V_{IN} Pin DC Current HV Controller On Only HV Controller and LV Regulator On Additional I_Q, Watchdog On (Float CT Pin) Additional I_Q, TEMP On (Float TEMP Pin) No-Load V_{OUT}/$EXTV_{CC}$ Pin DC Current HV Controller On Only HV Controller and One LV Regulator On Additional I_Q, per LV Regulator On Additional I_Q, Watchdog On (Float CT Pin) Additional I_Q, TEMP On (Float TEMP Pin)	CT = TEMP = $INTV_{CC}$ (Watchdog and TEMP Monitor Off, Unless Otherwise Specified)	V_{OUTPRG} = GND (3.3V V_{OUT})	 ● ● 	 22 23 +1 +2 4 29 +23 +6 +13	 42 33 +4.2 8.5 39 +33 +8 	 µA µA µA µA µA µA µA µA µA
I_Q (Note 4) (Burst Mode)	Total No-Load Input Supply Current HV Controller On Only HV Controller and One LV Regulator On Additional I_Q, per LV Regulator On Additional I_Q, Watchdog On (Float CT Pin) Additional I_Q, TEMP On (Float TEMP Pin)	PLL/MODE = GND V_{IN} = 12V, V_{INA-H} = V_{OUT} (LV Regulators Powered from HV Regulator's Output), No Load on V_{OUT} or V_{OUT1-4}	V_{OUTPRG} = $INTV_{CC}$ (5V V_{OUT})	●		15 31 +14 +4 +8	35 45 +20 +6 	µA µA µA µA µA
	Total No-Load Input Supply Current HV Controller On Only HV Controller and One LV Regulator On Additional I_Q, per LV Regulator On Additional I_Q, Watchdog On (Float CT Pin) Additional I_Q, TEMP On (Float TEMP Pin)	CT = TEMP = $INTV_{CC}$ (Watchdog and TEMP Monitor Off, unless otherwise specified)	V_{OUTPRG} = GND (3.3V V_{OUT})	●		23 33 +9 +3 +7	46 46 +12 +7 	µA µA µA µA µA
I_{SD}	V_{IN} Pin Current in Shutdown	RUN = EN1-4 = GND				3.5	8	µA

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
High Voltage Buck Controller							
V_{OUT}	Regulated Output Voltage	(Note 5) I_{TH} = 0.7V to 2V V_{OUTPRG} = $INTV_{CC}$, V_{IN} = 6V to 60V V_{OUTPRG} = GND, V_{IN} = 4.5V to 60V	 ● ●	 4.875 3.217	 5.000 3.300	 5.125 3.383	 V V
V_{RUN}	RUN Pin Controller Enable Threshold	RUN Pin Voltage Rising Hysteresis		1.17	1.22 50	1.27	V mV
I_{RUN}	RUN Pin Pull-Up Current	RUN = 0V			0.5		µA
g_m	Error Amplifier Transconductance	(Note 5) ITH = 1.2V, Sink/Source 5µA			2		mS
$I_{TRACK/SS}$	Soft-Start Charge Current	TRACK/SS = 0V		7	10	14	µA
I_{SENSE^+}	$SENSE^+$ Pin Current					±1	µA
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	$SENSE^-$ = 3.3V	●	68	75	82	mV
$D_{MAX(HV)}$	Maximum Duty Cycle In Dropout	R_{RT} = 400k		97.5	98		%
TG	Top Gate Pull-Up On-Resistance Top Gate Pull-Down On-Resistance				2.3 1.5		Ω Ω
BG	Bottom Gate Pull-Up On-Resistance Bottom Gate Pull-Down On-Resistance				2.4 1.1		Ω Ω
$t_{D(TG/BG)}$	Delay Time, Top Gate Off to Bottom Gate On	(Note 6)			40		ns
$t_{D(BG/TG)}$	Delay Time, Bottom Gate Off to Top Gate On	(Note 6)			18		ns
$t_{ON(MIN)}$	Minimum On-Time (Top Gate)	(Note 7)			60		ns
PGOOD	PGOOD Pin Voltage When Low PGOOD Pin Leakage Current When High	I_{PGOOD} = 2mA PGOOD = 5V			0.2	0.4 1	V µA
UV	V_{OUT}/$EXTV_{CC}$ Pin Undervoltage Threshold	Falling, Relative to Regulated V_{OUT} Hysteresis		–5	–7.5 2.5	–10	% %
OV	V_{OUT}/$EXTV_{CC}$ Pin Overvoltage Threshold	Rising, Relative to Regulated V_{OUT} Hysteresis		+5	+7.5 2.5	+10	% %
	$SENSE^-$ Pin Overvoltage Threshold	Rising, Relative to Regulated V_{OUT} Hysteresis			+15 2.5		% %
t_{PGOOD}	PGOOD Delay for Reporting OV/UV Fault	PGOOD High to Low			40		µs
$INTV_{CC}$	No Load Internal V_{CC} Regulated Voltage $INTV_{CC}$ Voltage Load Regulation	6V < V_{IN} < 60V, V_{OUT} = 3.3V I_{INTVCC} = 0mA to 50mA		4.9	5.1 –1	5.3 –2	V %
	No Load Internal V_{CC} Voltage Source Resistance	V_{OUT} = 5V I_{INTVCC} = 0mA to 50mA			5 –2.5		V Ω
	V_{OUT} Threshold for $INTV_{CC}$ Switchover from V_{IN} to V_{OUT}	V_{OUT} Rising Hysteresis		4.5	4.7 0.25	4.9	V V
	Undervoltage Lockout (UVLO) Threshold on $INTV_{CC}$	$INTV_{CC}$ Voltage Rising $INTV_{CC}$ Voltage Falling	● ●	 3.6	4.0 3.8	4.25 4.0	V V
	Internal Bias Start Up Time	V_{OUT} = 0V			1.2		ms
Oscillator and Phase-Locked Loop							
f_{OSC}	Frequency of Internal Oscillator (LV Regulators' Switching Frequency)	V_{RT} = $INTV_{CC}$ V_{RT} = $INTV_{CC}$ R_{RT} = 400k	 ● ●	1.9 1.75 1.85	2 2 2	2.1 2.25 2.15	MHz MHz MHz
f_{SW}	HV Controller Switching Frequency				1/6•f_{OSC}		kHz
$f_{PLL/MODE}$	Synchronization Frequency Range	t_{LOW}, t_{HIGH} > 60ns	●	1		3	MHz
$V_{PLL/MODE}$	PLL/MODE Level High PLL/MODE Level Low	For Synchronization For Synchronization	● ●	1.3		 0.25	V V
V_{RT}	RT Servo Voltage	R_{RT} = 400k	●	770	800	825	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN} = 12V, V_{RUN} = 5V, V_{OUT} = V_{INA-H} = 3.3V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Temperature Monitor							
$V_{TEMP(ROOM)}$	TEMP Voltage at 25°C			200	220	240	mV
ΔV_{TEMP}/°C	V_{TEMP} Slope				7		mV/°C
OT	Overtemperature Shutdown				170		°C
OT Hyst	Overtemperature Hysteresis				10		°C
Low Voltage (LV) Buck Regulators							
V_{INA-H}	Input Operating Voltage		●	2.25		5.5	V
V_{OUT1-4}	Regulated Output Voltage Set Point		●	0.8		V_{INA-H}	V
UVLO	Undervoltage Lockout Threshold on V_{INA-H}	V_{INA-H} Falling V_{INA-H} Rising	● ●	1.95 2.05	2.05 2.15	2.15 2.25	V V
$I_{Q(VINA-H)}$	Quiescent Current into V_{INA-H} Pins, Per Enabled LV Regulator (Note 8)	Burst Mode, FB1-4 = 0.82V Forced Continuous Mode, FB1-4 = 0V			25 400	35 550	µA µA
$I_{SD(VINA-H)}$	Shutdown Current into V_{INA-H} Pins				0	1	µA
V_{FB1}	Regulated Feedback Voltage for Regulator 1		●	792	800	808	mV
V_{FB2-4}	Regulated Feedback Voltage for Regulators 2-4		●	780	800	820	mV
I_{FB1-4}	Feedback Leakage Current	FB1-4 = 0.85V		–50		50	nA
D_{MAX}	Maximum Duty Cycle	FB1-4 = 0V	●	100			%
R_{PMOS}	PMOS On-Resistance	I_{SW} = 100mA, 1A – Per Power Stage			290		mΩ
R_{NMOS}	NMOS On-Resistance	I_{SW} = –100mA, 1A – Per Power Stage			180		mΩ
I_{LEAKP}	PMOS Leakage Current	EN1-4 = GND		–1		1	µA
I_{LEAKN}	NMOS Leakage Current	EN1-4 = GND		–1		1	µA
t_{SS}	Soft-Start Time	(Note 10)		0.25	1.5	3	ms
UV	Rising Undervoltage $\overline{RST}$ Threshold Regulator 1	% Relative to Regulated V_{FB} Hysteresis	●	–4	–2 1	–1	% %
	Rising $\overline{RST}$ Undervoltage Threshold Regulators 2-4	% Relative to Regulated V_{FB} Hysteresis	●	–7	–5 1	–3	% %
OV	$\overline{RST}$ Overvoltage Threshold of Regulators 1-4	% Relative to Regulated V_{FB} Hysteresis	●	+5	+7.5 –3	+10	% %
I_{LIM}	PMOS Current Limit	1 Buck with 1 Power Stage (Note 9)		1.4	1.8	2.2	A
		1 Buck with 2 Power Stages (Note 9)			3.6		A
		1 Buck with 3 Power Stages (Note 9)			5.4		A
		1 Buck with 4 Power Stages (Note 9)			7.2		A
Interface Logic Pins ($\overline{RST}$, WDO, WDI, CT, C1, C2, C3)							
I_{OH}	Output High Leakage Current	$\overline{RST}$, WDO 5.5V at Pin				1	µA
V_{OL}	Output Low Voltage	$\overline{RST}$, WDO 3mA at Pin			0.1	0.4	V
V_{IH}	WDI Input High Threshold		●	1.2			V
	CT, C1, C2, C3 Input High Threshold		●	$INTV_{CC}$ – 0.4			V
V_{IL}	WDI, C1, C2, C3 Input Low Threshold		●			0.4	V
$t_{WDI(WIDTH)}$	WDI Pulse Width		●	80			ns

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Interface Logic Pins (EN1, EN2, EN3, EN4)							
V_{EN}	Enable Rising Threshold	All LV Regulators Disabled	●	400	730	1200	mV
	Enable Rising Threshold	At Least One LV Regulator Enabled	●	380	400	420	mV
	Enable Falling Threshold		●	290	315	340	mV
I_{EN}	Enable Pin Leakage Current	EN = 3.3V				1	µA
CT Timing Parameters; C_T = 10nF							
t_{WDIO}	Time from WDO Low Until Next WDO Low	C_T = 10nF		9.7	12.9	16.1	s
t_{WDI}	Time from Last WDI Until Next WDO Low	C_T = 10nF		1.22	1.62	2.03	s
t_{WDO}	WDO Low Time Absent a Transition at WDI	C_T = 10nF		160	202	280	ms
$t_{\overline{RST}}$	$\overline{RST}$ Assertion Delay	C_T = 10nF		160	202	280	ms
t_{WDL}	Watchdog Lower Boundary	C_T = 10nF		38	50.6	63	ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3372 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3372E is guaranteed to meet specifications from 0°C to 85°C operating junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3372I is guaranteed over the –40°C to 125°C operating junction temperature range. The LTC3372H is guaranteed over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: This IC includes overtemperature protection which protects the device during momentary overload conditions. Junction temperatures will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: The I_Q (Total Input Supply Quiescent Current) is the total average current drawn from the input power supply by a typical application in Burst Mode with no load currents (from either the HV Controller V_{OUT} or the LV Regulators' V_{OUT1-4}).

Note 5: The HV Controller's output regulation is tested in a feedback loop that servos the ITH pin to a specified voltage and measures the resulted voltage at V_{OUT}/EXTV_{CC} pin.

Note 6: Delays are measured using 50% levels, with TG and BG driving minimum capacitive load.

Note 7: The minimum on-time conditions is specified for an inductor peak-to-peak ripple current ≥40% of I_{MAX} (see Minimum On-Time Considerations in the Applications Information section).

Note 8: The $I_{Q(VINA-H)}$ (Quiescent Current into V_{INA-H} Pins) are measured with power switches not switching. Dynamic supply current when switching may be higher due to the gate charge being delivered.

Note 9: The current limit features are intended to protect the IC from short term or intermittent fault conditions. Continuous operation above the maximum specified pin current rating may result in device degradation over time.

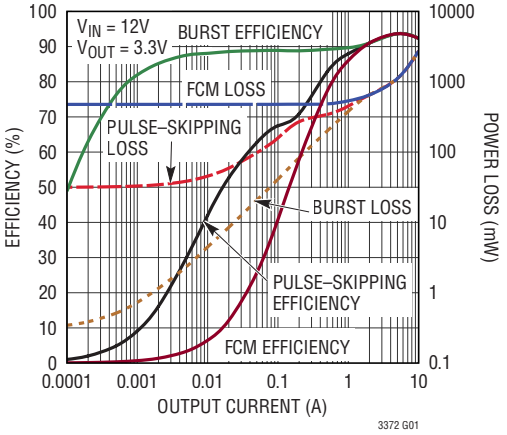
Note 10: The soft-start is the time from the first top switch turn on, after an enable rising, until the feedback has reached 90% of its nominal regulation voltage.

Note 11: Do not apply a voltage or current source to these pins. They must be connected to the gates of the external power MOSFETs, otherwise permanent damage may occur.

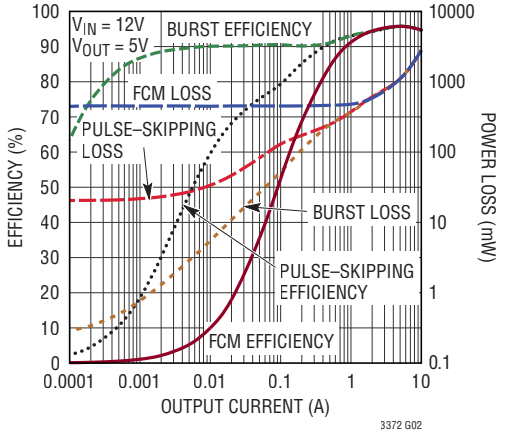
TYPICAL PERFORMANCE CHARACTERISTICS

(HV Controller) T_A = 25°C, unless otherwise noted.

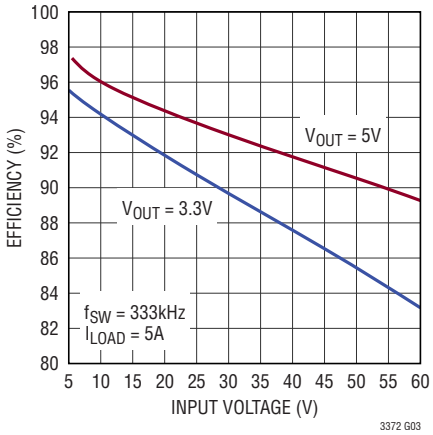
Efficiency and Power Loss vs Output Current



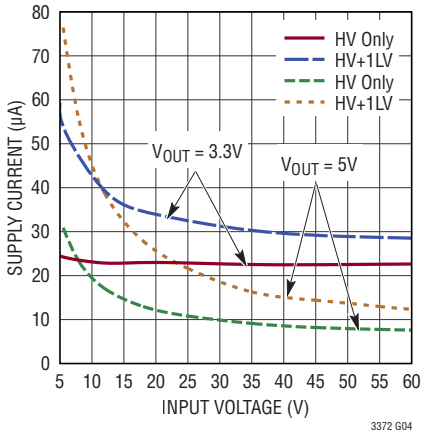
Efficiency and Power Loss vs Output Current



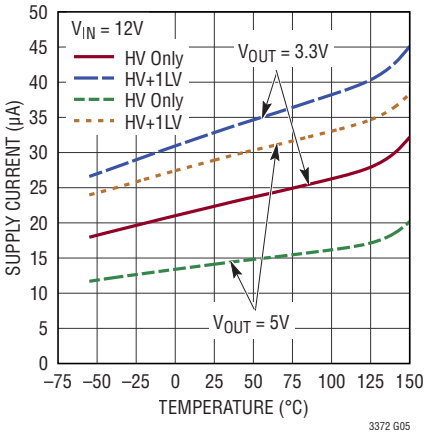
Efficiency vs V_{IN}



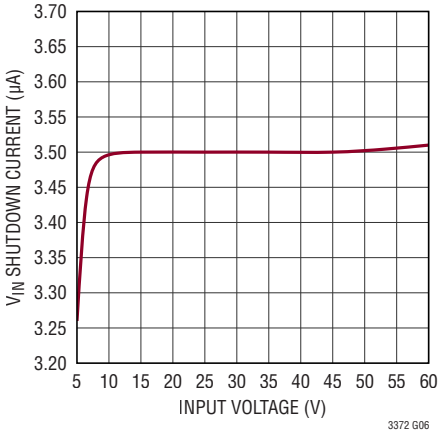
Burst Mode Quiescent Current vs V_{IN}



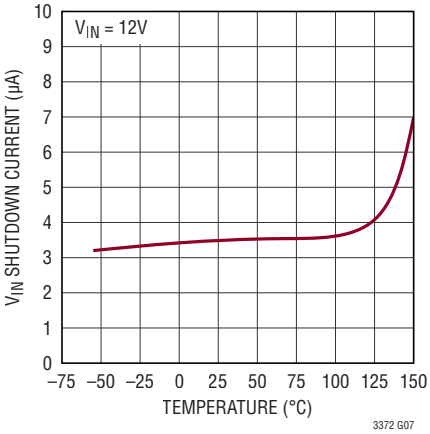
Burst Mode Quiescent Current vs Temperature



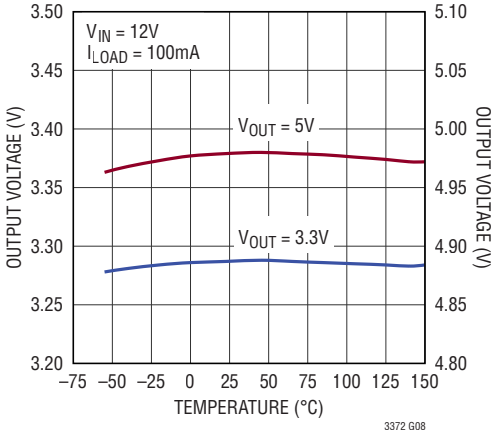
Shutdown Current vs V_{IN}



Shutdown Current vs Temperature



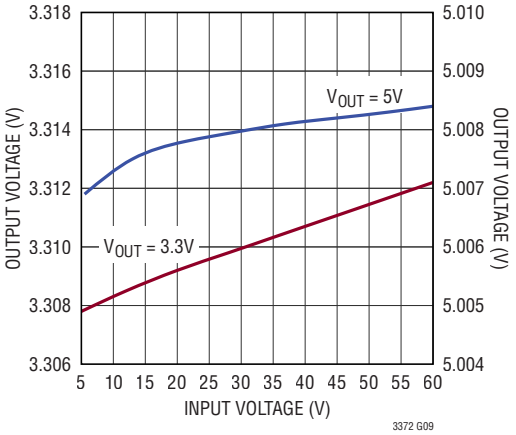
Output Voltage vs Temperature Forced Continuous Mode



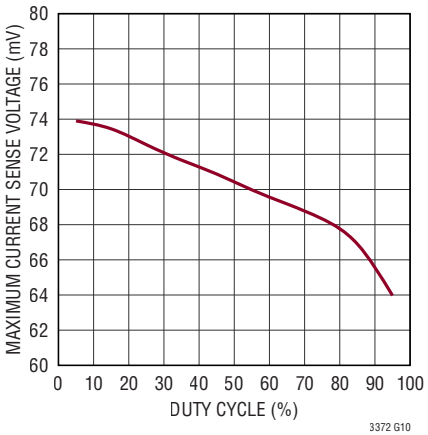
TYPICAL PERFORMANCE CHARACTERISTICS

(HV Controller) T_A = 25°C, unless otherwise noted.

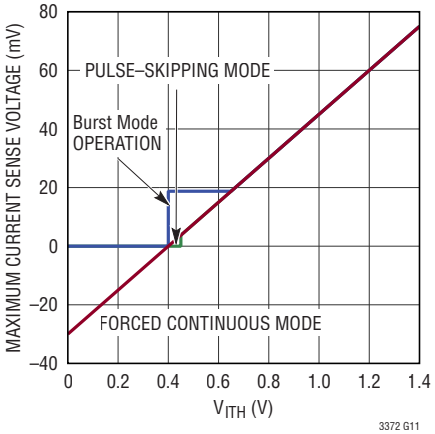
Output Voltage Line Regulation Forced Continuous Mode



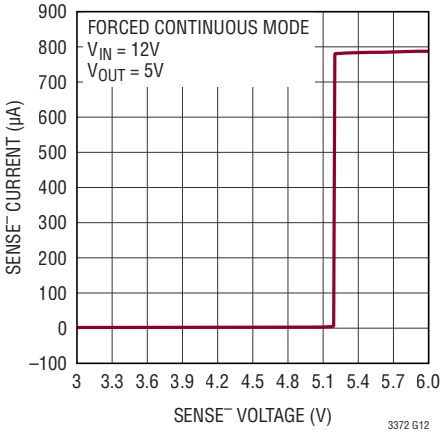
Maximum Current Sense Threshold vs Duty Cycle



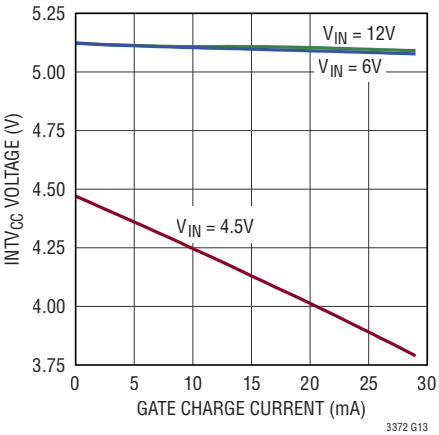
Maximum Current Sense Voltage vs I_{TH} Voltage



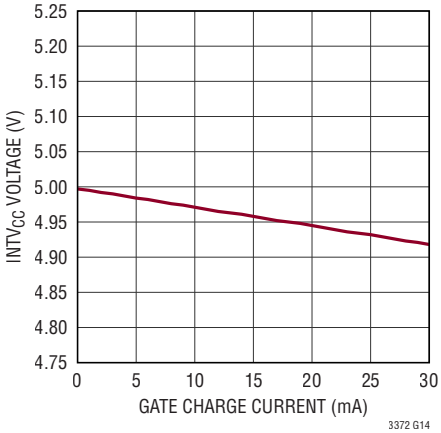
SENSE⁻ Pin Input Bias Current



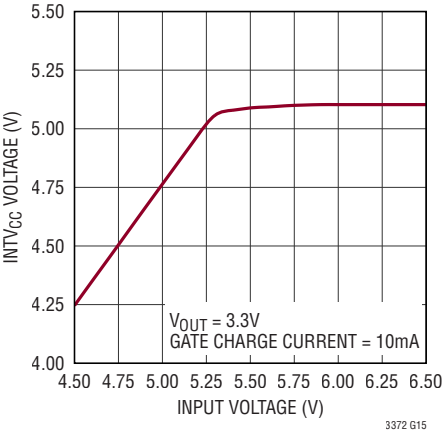
$INTV_{CC}$ Voltage vs Gate Charge Current V_{OUT} = 3.3V



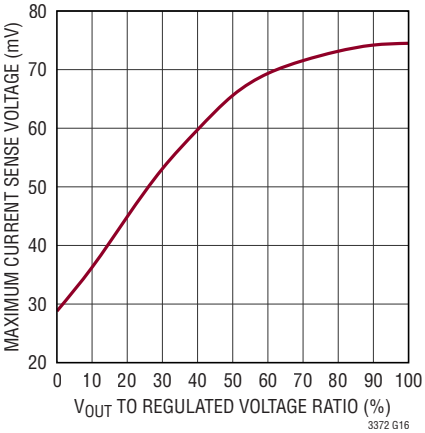
$INTV_{CC}$ Voltage vs Gate Charge Current V_{OUT} = 5V



$INTV_{CC}$ Line Regulation in Dropout



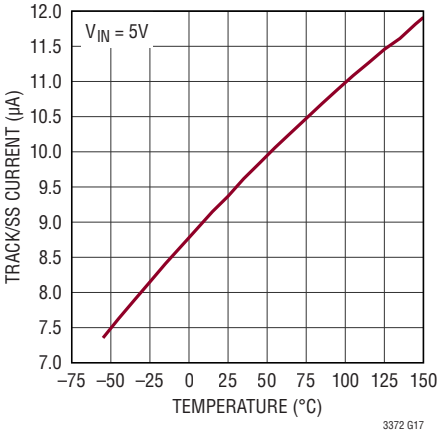
Current Limit in Foldback



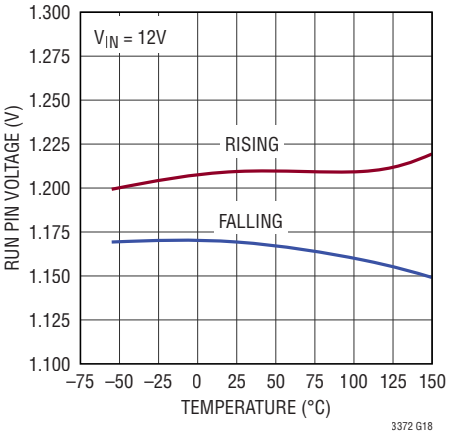
TYPICAL PERFORMANCE CHARACTERISTICS

(HV Controller) T_A = 25°C, unless otherwise noted.

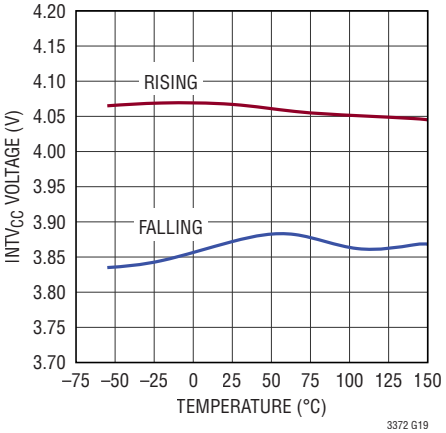
TRACK/SS Pull-Up Current vs Temperature



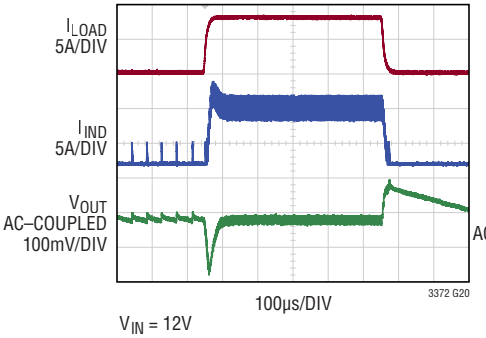
Shutdown (RUN) Threshold vs Temperature



Undervoltage Lockout Threshold vs Temperature

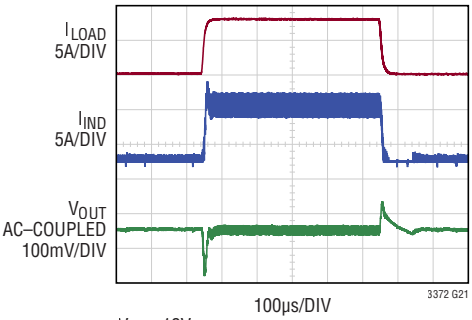


Load Step Burst Mode Operation



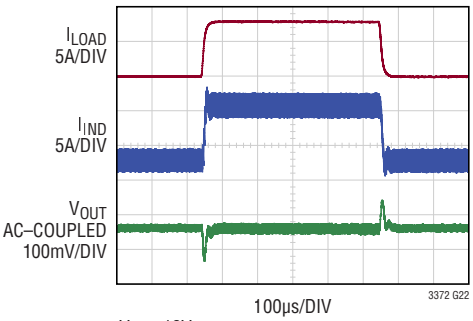
V_{IN} = 12V
V_{OUT} = 3.3V
I_{LOAD} = 100mA to 8A

Load Step Pulse-Skipping Mode



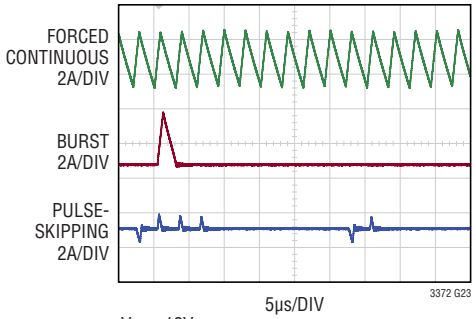
V_{IN} = 12V
V_{OUT} = 3.3V
I_{LOAD} = 100mA to 8A

Load Step Forced Continuous Mode



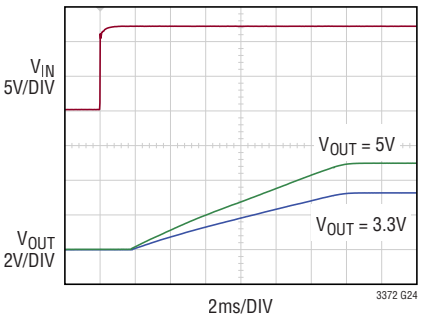
V_{IN} = 12V
V_{OUT} = 3.3V
I_{LOAD} = 100mA to 8A

Inductor Current at Light Load



V_{IN} = 12V
V_{OUT} = 3.3V
I_{LOAD} = 200µA

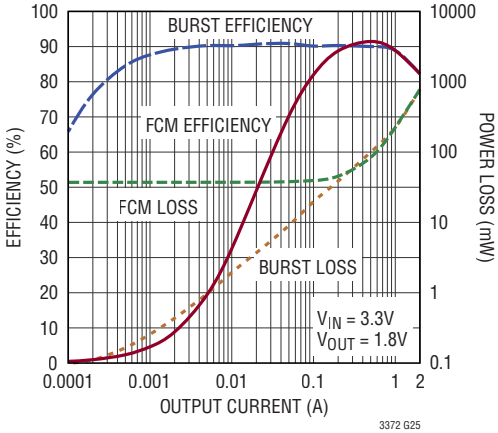
Soft Start-Up



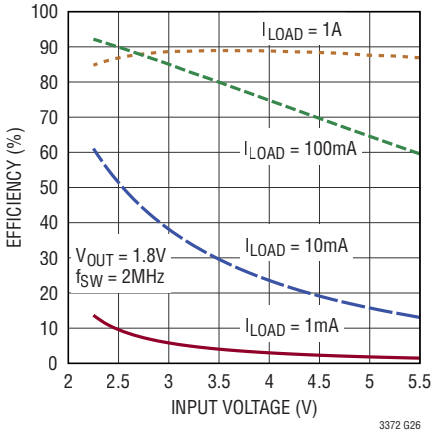
TYPICAL PERFORMANCE CHARACTERISTICS

(LV Buck Regulator) T_A = 25°C, unless otherwise noted.

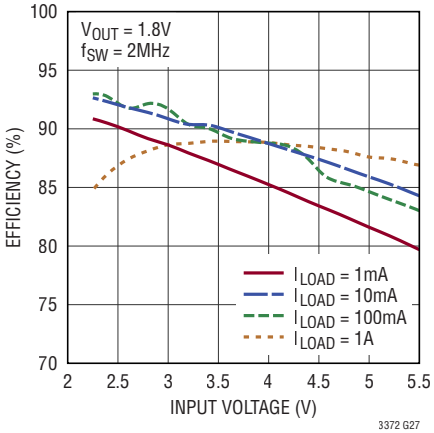
2A Buck Efficiency and Power Loss vs Output Current



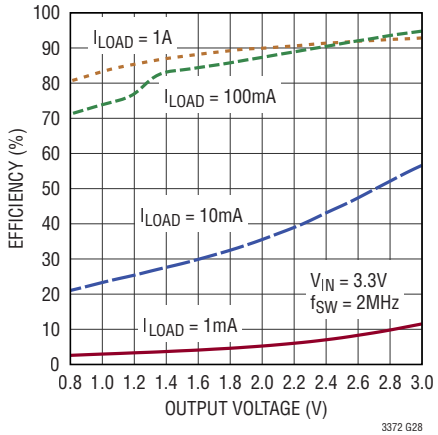
2A Buck Efficiency vs V_{IN} Forced Continuous Mode



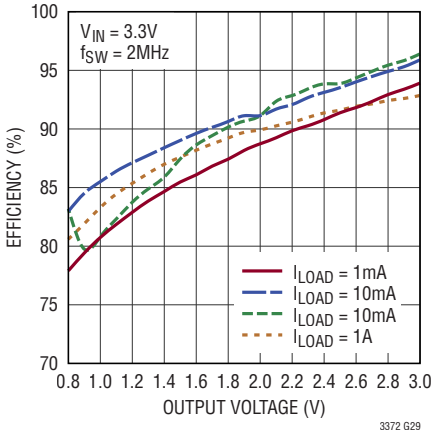
2A Buck Efficiency vs V_{IN} Burst Mode



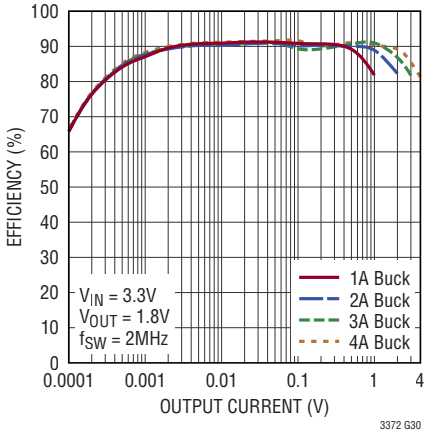
2A Buck Efficiency vs V_{OUT} Forced Continuous Mode



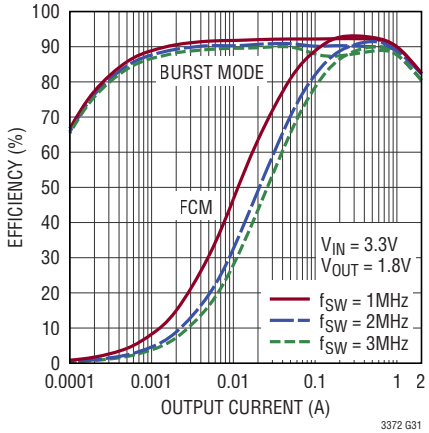
2A Buck Efficiency vs V_{OUT} Burst Mode Operation



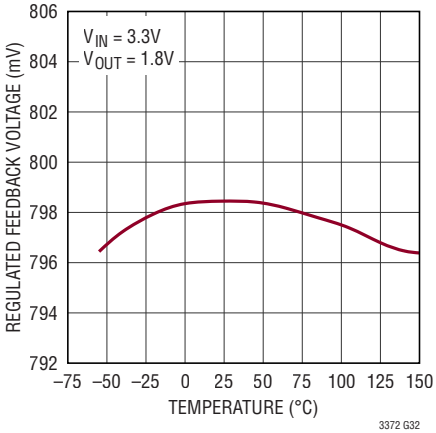
Efficiency vs Output Current Burst Mode Operation



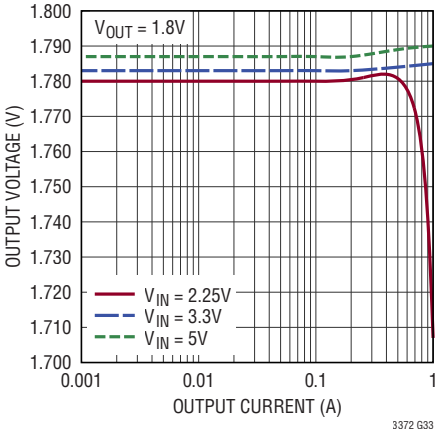
2A Buck Efficiency vs Output Current Across Switching Frequency



2A Buck Regulator Feedback Voltage vs Temperature



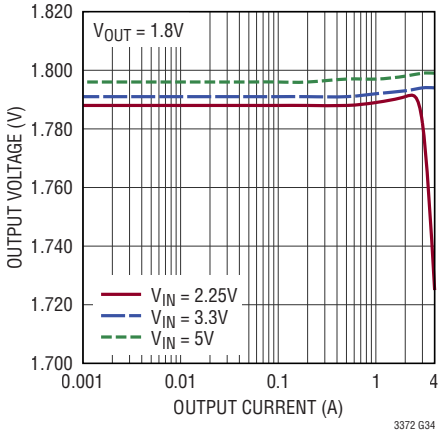
1A Buck Load Regulation Across V_{IN} Forced Continuous Mode



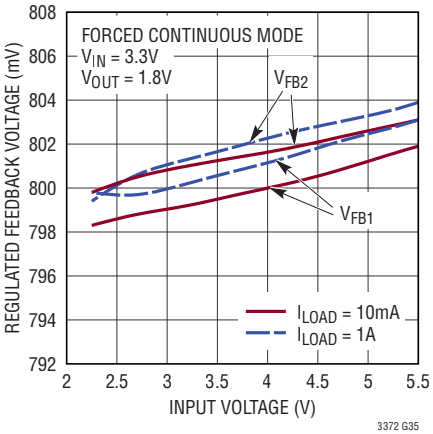
TYPICAL PERFORMANCE CHARACTERISTICS

(LV Buck Regulator) T_A = 25°C, unless otherwise noted.

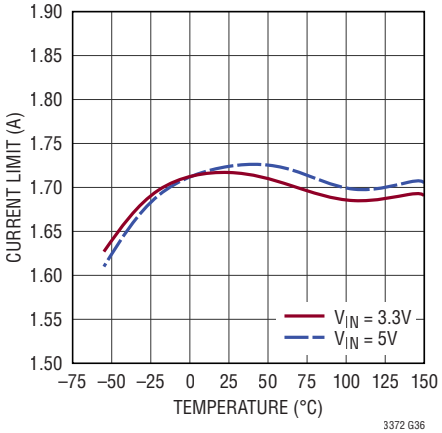
4A Buck Output Voltage vs Output Current



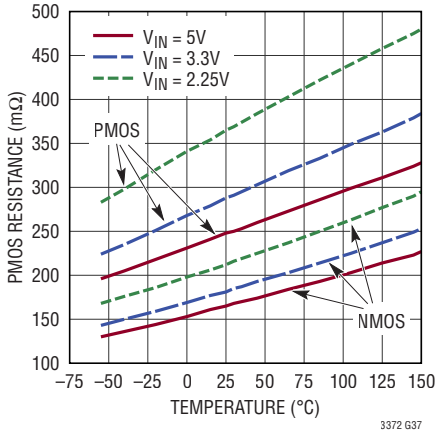
2A Buck Regulated Feedback Voltage vs V_{INA-H}



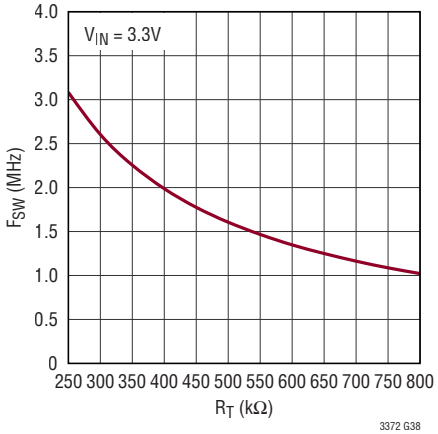
1A Buck PMOS Current Limit vs Temperature



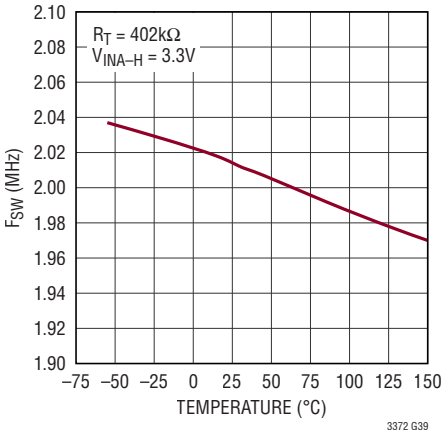
1A Buck NMOS and PMOS $R_{DS(ON)}$ vs Temperature Across V_{IN}



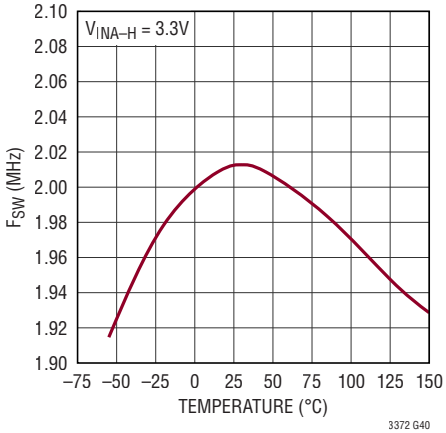
Oscillator Frequency vs R_T



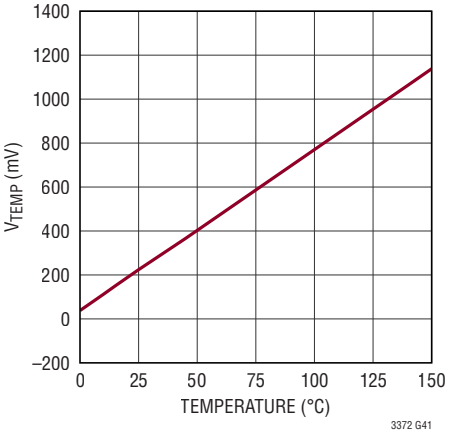
R_T Programmed Oscillator Frequency vs Temperature



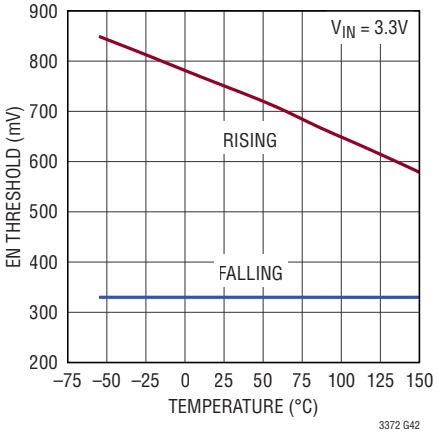
Default Oscillator Frequency vs Temperature



V_{TEMP} vs Temperature



Enable Threshold vs Temperature

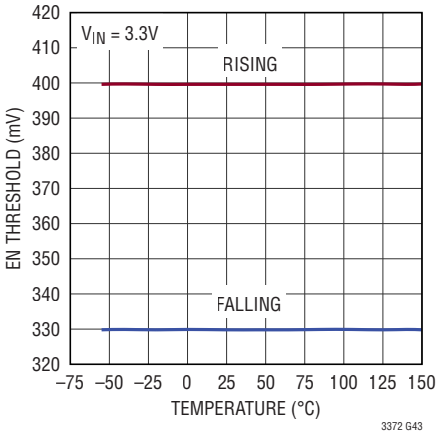


Rev. A

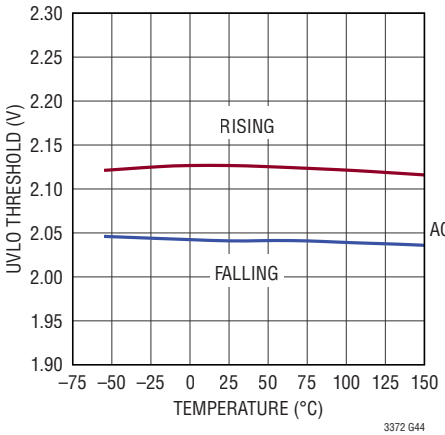
TYPICAL PERFORMANCE CHARACTERISTICS

(LV Buck Regulator) T_A = 25°C, unless otherwise noted.

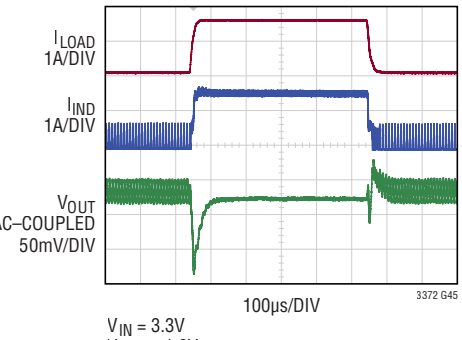
Precise Enable Threshold vs Temperature



V_{INA-H} UVLO Threshold vs Temperature

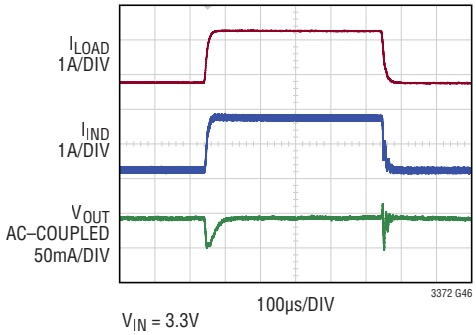


2A Buck Load Step Burst Mode



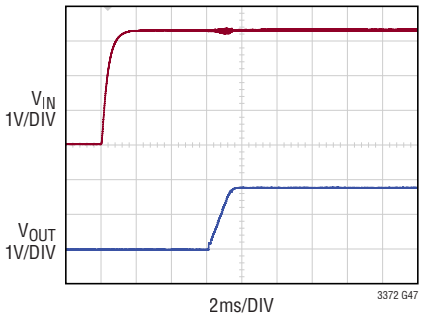
V_{IN} = 3.3V
V_{OUT} = 1.8V
I_{LOAD} = 100mA to 1.6A

2A Buck Load Step Forced Continuous Mode



V_{IN} = 3.3V
V_{OUT} = 1.8V
I_{LOAD} = 100mA to 1.6A

2A Buck Start-Up



V_{IN} = 3.3V
V_{OUT} = 1.8V

PIN FUNCTIONS

$\overline{RST}$ (Pin 1): LV Regulator Reset Logic Output. This pin is pulled low when the feedback pin (FB1-4) voltage of any enabled LV regulator is outside of its power good window. The window is –2% to +7.5% (typical) for regulator 1, and –5% to +7.5% (typical) for regulators 2-4, around the regulated 0.8V level. This pin is pulled low when all LV regulators are disabled. Assertion (the pin goes high) delay is scaled by the C_T capacitor.

TEMP (Pin 2): Temperature Indication Pin. TEMP outputs a voltage of 220mV (typical) at 25°C. The TEMP voltage will increase by 7mV/°C (typical) at higher temperatures giving an external indication of the IC's internal die temperature. The temperature monitor can be shut down by tying the TEMP pin to $INTV_{CC}$ to reduce quiescent current. If all LV regulators are disabled, the temperature monitor shuts down and the TEMP pin becomes high impedance.

EN1 (Pin 3): LV Buck Regulator 1 Enable Input. Active high. Do not float.

FB1 (Pin 4): LV Buck Regulator 1 Feedback Pin. Receives feedback by a resistor divider connected across the output.

V_{INA} (Pin 5): LV Power Stage A Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor.

SWA (Pin 6): LV Power Stage A Switch Node. External inductor connects to this pin.

SWB (Pin 7): LV Power Stage B Switch Node. External inductor connects to this pin.

V_{INB} (Pin 8): LV Power Stage B Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor.

V_{INC} (Pin 9): LV Power Stage C Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor.

SWC (Pin 10): LV Power Stage C Switch Node. External inductor connects to this pin.

SWD (Pin 11): LV Power Stage D Switch Node. External inductor connects to this pin.

V_{IND} (Pin 12): LV Power Stage D Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor.

FB2 (Pin 13): LV Buck Regulator 2 Feedback Pin. Receives feedback by a resistor divider connected across the output. In configurations where LV Regulator 2 is not used, FB2 should be tied to ground.

EN2 (Pin 14): LV Buck Regulator 2 Enable Input. Active high. In configurations where LV Regulator 2 is not used, tie EN2 to ground. Do not float.

C1 (Pin 15): LV Regulator Configuration Control Input Bit. With C2 and C3, C1 configures the buck output current power stage combinations. C1 should either be tied to $INTV_{CC}$ or ground. Do not float.

C2 (Pin 16): LV Regulator Configuration Control Input Bit. With C1 and C3, C2 configures the buck output current power stage combinations. C2 should either be tied to $INTV_{CC}$ or ground. Do not float.

C3 (Pin 17): LV Regulator Configuration Control Input Bit. With C1 and C2, C3 configures the buck output control power stage combinations. C3 should either be tied to $INTV_{CC}$ or ground. Do not float.

RT (Pin 18): Oscillator Frequency Pin. This pin provides two modes of setting the switching frequency. Connecting a resistor from RT to ground will set the switching frequency based on the resistor value. If RT is tied to $INTV_{CC}$ the internal 2MHz oscillator will be used. Do not float.

PLL/MODE (Pin 19): Oscillator Synchronization Input and Mode Select Pin. Driving this pin with an external clock signal synchronizes the internal oscillator to the applied clock. The LV bucks synchronize to the oscillator frequency and HV buck synchronizes to 1/6th frequency when in forced continuous mode. When no external clock is applied the oscillator frequency is programmed by the RT pin. When not synchronizing to an external clock this input determines how the controller and regulators operate at light load. Floating or grounding this pin selects Burst Mode operation, and tying this pin to $INTV_{CC}$ forces continuous inductor current mode operation for all the converters and the controller. Tying this pin to a voltage greater than 1.2V and less than $INTV_{CC}$–1.3V selects pulse-skipping mode operation for the controller, but Burst Mode operation for the low voltage converters. This pin has a 100k internal resistor to ground.

PIN FUNCTIONS

WDI (Pin 20): Watchdog Timer Input. The WDI pin must be toggled either low to high or high to low every 1.62 seconds. Failure to toggle WDI results in the WDO pin being pulled low for 202ms. All times correspond to a 10nF capacitor on the CT pin.

WDO (Pin 21): Watchdog Timer. Open-drain output. WDO is pulled low for 202ms during a watchdog timeout period. The WDO pin pulls low if the WDI input does not transition in less than 1.62 seconds since its last transition or 12.9 seconds after a watchdog timeout period. An UVLO event resets the watchdog timer and WDO asserts itself low for the 202ms watchdog timeout period. All times correspond to a 10nF capacitor on the CT pin.

CT (Pin 22): Timing Capacitor Pin. A capacitor connected to GND sets a time constant which is scaled for use by the WDI, WDO, and $\overline{RST}$ pins. Tying the CT pin to $INTV_{CC}$ disables the watchdog timer to reduce quiescent current.

EN3 (Pin 23): LV Buck Regulator 3 Enable Input. Active high. In configurations where LV Regulator 3 is not used, tie EN3 to ground. Do not float.

FB3 (Pin 24): LV Buck Regulator 3 Feedback Pin. Receives feedback by a resistor divider connected across the output. In configurations where LV Regulator 3 is not used, FB3 should be tied to ground.

V_{INE} (Pin 25): LV Power Stage E Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor.

SWE (Pin 26): LV Power Stage E Switch Node. External inductor connects to this pin.

SWF (Pin 27): LV Power Stage F Switch Node. External inductor connects to this pin.

V_{INF} (Pin 28): LV Power Stage F Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor.

V_{ING} (Pin 29): LV Power Stage G Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor.

SWG (Pin 30): LV Power Stage G Switch Node. External inductor connects to this pin.

SWH (Pin 31): LV Power Stage H Switch Node. External inductor connects to this pin.

V_{INH} (Pin 32): LV Power Stage H Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor.

FB4 (Pin 33): LV Buck Regulator 4 Feedback Pin. Receives feedback by a resistor divider connected across the output.

EN4 (Pin 34): LV Buck Regulator 4 Enable Input. Active high. Do not float.

$INTV_{CC}$ (Pin 35): Internal V_{CC} Pin. Output of an internal linear low-dropout (LDO) regulator powered from V_{IN}. The HV buck gate drive and control circuits are powered from this voltage source when V_{OUT} is < 4.7V. When V_{OUT} > 4.7V the bias connects to Vout and the LDO is shutdown. Must be de-coupled to GND pin with a minimum of 4.7µF low ESR (ceramic) capacitor.

BG (Pin 36): HV Controller High Current Gate Drive for Bottom (Synchronous) N-channel MOSFET. Voltage swing at this pin is from ground to $INTV_{CC}$.

TG (Pin 37): HV Controller High Current Gate Drive for Top N-channel MOSFET. This is the output of floating driver with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage SW.

SW (Pin 38): HV Controller Switch Node Connection to Inductor.

BOOST (Pin 39): HV Controller Bootstrapped Supply to the Topside Floating Driver. A capacitor should be connected between the BOOST and SW pin and a Schottky diode should be connected between the BOOST and $INTV_{CC}$ pins. Voltage swing at the BOOST pin is from $INTV_{CC}$ to (V_{IN} + $INTV_{CC}$).

RUN (Pin 40): HV Controller Enable Input. Forcing this pin above 1.2V turns on the HV controller. This pin has a 0.5µA internal pull-up current from ground to around 4V, and can be forced up to 65V (absolute maximum).

V_{IN} (Pin 41): HV Input Supply Pin. A bypass capacitor should be tied between this pin and the GND pin.

TRACK/SS (Pin 42): HV Controller External Tracking and Soft-Start Input. When this pin is above 1.2V, the controller regulates the output voltage V_{OUT} to the programed 5V or 3.3V level. When this pin is below 1.2V, the output voltage

PIN FUNCTIONS

is regulated proportionally lower. An internal 10µA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to the final regulated output voltage. Alternatively, a resistor divider on another voltage supply connected to this pin allows the controller's output to track another supply during start-up.

V_{OUT}/EXTV_{CC} (Pin 43): HV Controller Output Voltage Sensing and External V_{CC} Power Input. Connect this pin to the HV controller's regulated output voltage. The HV controller V_{OUT} is regulated to either 3.3V or 5V by an internal resistor divider selected by the V_{PROG} pin. This pin is also provides an external V_{CC} connection and supplies internal bias voltages from V_{OUT} to improve low I_Q performance and reduce power loss.

SENSE$^-$ (Pin 44): HV Controller Negative (–) Input to Differential Current Comparator. This SENSE$^-$ pin also functions as the output voltage sense pin for a secondary 15% overvoltage protection in addition to the 7.5% overvoltage protection at the V_{OUT}/EXTV_{CC} pin. In the situation that SENSE$^-$ pin is separated from V_{OUT}/EXTV_{CC} pin to achieve point-of-load (POL) regulation, SENSE$^-$ can begin drawing a >500µA current when SENSE$^-$ is 200mV greater than V_{OUT} (V_{OUT} = 5V) or INTV_{CC} (V_{OUT} = 3.3V). When voltage on SENSE$^-$ pin is close to INTV_{CC}, SENSE$^-$ can begin drawing >500µA current. Do not connect a filtering resistor in series with SENSE$^-$ pin unless SENSE$^-$ stays close to ground in the application.

SENSE$^+$ (Pin 45): HV Controller Positive (+) Input to Differential Current Comparator. The ITH pin voltage and controlled offsets between the SENSE$^-$ and SENSE$^+$ pins set the current trip threshold. The current comparator can be used for either inductor DCR sensing or traditional current sensing resistor (R_{SENSE}) sensing.

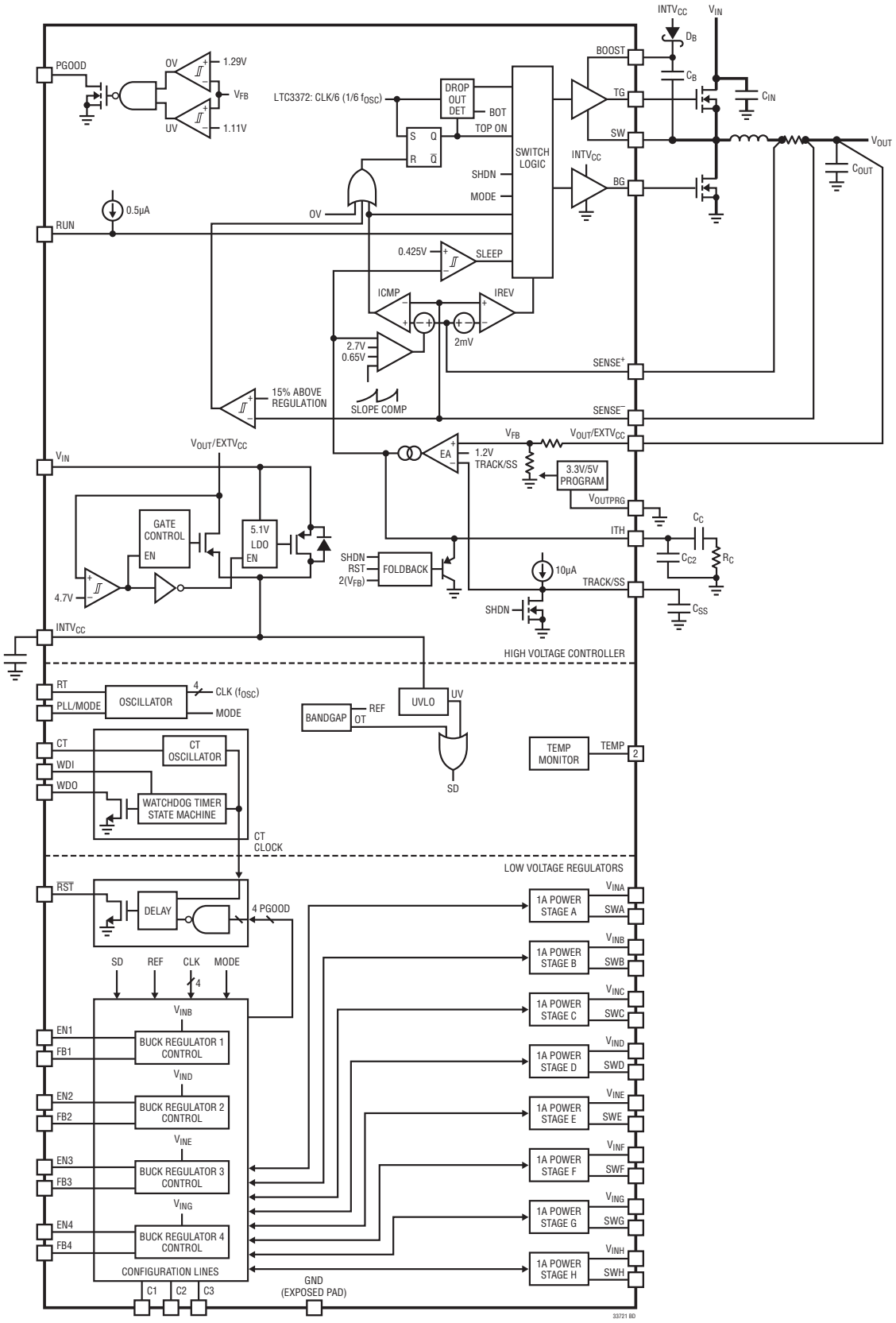
ITH (Pin 46): HV Controller Error Amplifier Output and Compensation Point. The current comparator threshold increases with this control voltage.

V_{OUTPRG} (Pin 47): HV Controller Output Voltage Programming Pin. When this pin is tied to INTV_{CC}, the output voltage is regulated to 5V. When tied to ground, the output voltage is regulated to 3.3V.

PGOOD (Pin 48): HV Controller Power Good Open-Drain Logic Output. This pin is pulled low when the voltage at the V_{OUT}/EXTV_{CC} pin is outside of the ±7.5% window around the regulated level, or voltage at SENSE$^-$ pin is more than 15% above the regulated level of V_{OUT}.

GND (Exposed Pad Pin 49): Ground. The exposed pad must be soldered to a continuous printed circuit board ground plane directly under the IC package for rated thermal performance. The exposed pad is a shared ground for signal grounds, driver ground and power stage grounds of all HV and LV buck regulators.

BLOCK DIAGRAM



OPERATION

The LTC3372 is a single IC that combines a high voltage (HV) buck (step-down) DC/DC switching regulator controller and a total of four configurable low voltage (LV) buck regulators.

Main Control Loop of HV Buck Controller

The HV controller uses a constant frequency, current mode buck (step-down) architecture. During normal operation, the external top MOSFET is turned on when the clock sets the RS latch, and is turned off when the main current comparator, ICMP, resets the RS latch. The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier, EA. The error amplifier compares an internal 1.2V reference voltage to the feedback voltage generated by an internal resistor divider connected to the $V_{OUT}/EXTV_{CC}$ pin. The divider can be selected to program an output of either 3.3V to 5V. When the load current increases, it causes a slight decrease in V_{FB} relative to the reference, which causes the EA to increase the ITH voltage until the average inductor current matches the new load current.

After the top MOSFET is turned off each cycle, the bottom MOSFET is turned on until either the beginning of the next clock cycle, or the inductor current starts to reverse, as indicated by the reverse current comparator IREV (at light load in pulse-skipping mode or Burst Mode).

$INTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and some other internal circuitry is derived from the $INTV_{CC}$ pin. When the $V_{OUT}/EXTV_{CC}$ pin is tied to a voltage less than 4.7V, the V_{IN} LDO (low dropout linear regulator) supplies 5.1V from V_{IN} to $INTV_{CC}$. If $V_{OUT}/EXTV_{CC}$ is taken above 4.7V, the V_{IN} LDO is turned off and an internal PMOS switch connects $V_{OUT}/EXTV_{CC}$ to $INTV_{CC}$. Using the $V_{OUT}/EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from the high efficiency HV buck regulator output.

The top MOSFET driver is biased from the floating bootstrap capacitor, C_B, which normally recharges during each cycle through an external diode, D_B, when the top MOSFET turns off. If the input voltage, V_{IN}, decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for a short time every tenth cycle to allow C_B to recharge, resulting in an effective duty cycle of 98%.

Shutdown and Start-Up (RUN, TRACK/SS Pins)

It typically takes 1.2ms for the internal bias circuits (including $INTV_{CC}$) to be ready after the first time either the RUN pin or any of the EN1-4 pins rises above 730mV. During the 1ms internal bias circuit startup time, neither the HV or LV regulators are enabled. The HV controller is enabled when the RUN pin is pulled above 1.2V and the internal bias is enabled. Pulling RUN pin below 1.16V disables the HV controller.

The RUN pin has an internal 0.5µA current that pulls up the pin to enable the HV controller. Alternatively, the RUN pin may be externally pulled up or driven by logic. The RUN pin can tolerate up to 65V (absolute maximum), so it can be conveniently tied to V_{IN} in an always-on application in which the controller is enabled continuously and never shut down.

The RUN pin can also be used as an undervoltage lockout (UVLO) by connecting it to the midpoint of an external resistor divider network of V_{IN} (see Applications Information section).

The start-up of the controller's output voltage V_{OUT} is controlled by the voltage on the TRACK/SS pin. When the voltage on the TRACK/SS pin is less than the 1.2V internal reference, the HV controller regulates the V_{FB} voltage to the TRACK/SS pin voltage instead of the 1.2V reference. This allows the TRACK/SS pin to be used to program a soft-start by connecting an external capacitor from the TRACK/SS pin to GND. An internal 10µA pull-up current charges this capacitor creating a voltage ramp on the TRACK/SS pin. As the TRACK/SS voltage rises linearly from 0V to 1.2V and beyond, the output voltage V_{OUT} rises smoothly from zero to its final value. Alternatively the TRACK/SS pin can be used to cause the start-up of V_{OUT} to track that of another supply. Typically, this requires connecting to the TRACK/SS pin an external resistor divider from the other supply to ground (see the Applications Information section).

OPERATION

Output Overvoltage Protection

Overvoltage comparators guard against transient overshoots as well as other more serious conditions that may overvoltage the output.

When the $V_{OUT}/EXTV_{CC}$ pin voltage rises by more than 7.5% above its regulation set point, the top power MOSFET gate (TG) is turned off and the bottom power MOSFET gate (BG) is turned on until the overvoltage condition is cleared.

The $SENSE^-$ pin functions as the output voltage sense pin for a secondary +15% overvoltage protection in addition to the +7.5% overvoltage protection at $V_{OUT}/EXTV_{CC}$ pin. When voltage at this pin is over 15% higher than the regulated output voltage set point, the HV controller will turn TG off and BG on. This provides an additional layer of protection when point-of-load (POL) regulation is desired.

Power Good Indicator (PGOOD) Pin

The PGOOD pin is connected to the open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the $V_{OUT}/EXTV_{CC}$ voltage is outside of the ±7.5% window around the regulated level. The PGOOD pin is also pulled low when the RUN pin is low (shut down). When the $V_{OUT}/EXTV_{CC}$ voltage is within the ±7.5% window, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source no greater than 6V.

Foldback Current Limit

When the output voltage falls to less than 70% of its nominal level, foldback current limiting is activated. Foldback progressively lowers the peak current limit as the output drops in a sustained overcurrent or short-circuit condition. Foldback current limiting is disabled during the soft-start interval (as long as the V_{FB} voltage is keeping up with the TRACK/SS voltage).

Light Load Current Operation

The HV buck controller can be enabled to enter one of the three modes at light load current: (a) high efficiency Burst Mode, (b) forced continuous conduction mode, or (c) pulse-skipping mode operations at light load currents.

The LTC3372's PLL/MODE pin selects the light load operation modes for both the HV controller and LV buck regulators. To select Burst Mode operation, tie the PLL/MODE pin to SGND. To select forced continuous mode operation, tie the PLL/MODE pin to $INTV_{CC}$. When PLL/MODE pin is connected to an external clock, both HV controller and the LV buck regulators are synchronized to the external clock in forced continuous mode operation. To select pulse-skipping mode for the HV controller, tie the PLL/MODE pin to a DC voltage greater than 1.2V but less than $INTV_{CC}$ – 3.3V. The LV buck regulators will operate in Burst Mode operation.

When the controller is enabled for Burst Mode operation, the minimum peak current in the inductor is set to approximately 25% of the maximum sense voltage even though the voltage on the ITH pin indicates a lower value. If the average inductor current is higher than the load current, the error amplifier, EA, will decrease the voltage on the ITH pin. When the ITH voltage drops below 0.425V, the internal sleep signal goes high (enabling sleep mode) and both external MOSFETs are turned off. The ITH pin is then disconnected from the output of the EA and parked at 0.450V.

In sleep, much of the internal circuitry is turned off, reducing the quiescent currents that the controllers draws. The load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the ITH pin is reconnected to the output of the EA, the sleep signal goes low, and the controller resumes normal operation by turning on the top external MOSFET on the next cycle of the internal oscillator.

When the controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator, I_{REV}, turns off the bottom external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous operation.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITH pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in

OPERATION

Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to other circuitry. In forced continuous mode, the output ripple is independent of load current. Clocking the LTC3372 from an external source enables forced continuous mode (see the Programming the Operating Frequency section.)

When the PLL/MODE pin is connected for pulse-skipping mode, the HV controller operates in PWM pulse-skipping mode at light loads. In this mode, constant frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the current comparator, ICMP, may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

LOW VOLTAGE REGULATORS

Low Voltage Buck Switching Regulator

The LTC3372 contains eight low voltage (LV) monolithic 1A synchronous buck switching power stages. Each power stage contains an integrated PMOS top-side switch and a NMOS bottom-side switch. The eight power stages are controlled by up to four constant frequency peak current mode controllers. All of the switching regulators are internally compensated and need only external feedback resistors to set their output voltages.

Each LV buck switching regulator can operate with an independent input voltage and has its own FB and EN pins to maximize flexibility. The enable pins have two different enable thresholds that depend on the operating state of the other LV regulators. When all of the LV regulators are disabled, the EN pin threshold is 0.73V . Once any LV regulator is enabled, the EN pin thresholds of the remaining LV regulators are set to a precision internal-reference-based 400mV. This precision EN threshold may be used to provide event based sequencing via feedback from other previously enabled regulators.

It typically takes 1ms for the internal bias circuits (including $INTV_{CC}$) to be ready after the first time RUN or any EN pin rises above 0.73V. All regulators are disabled during internal circuit start-up time. When a LV regulator is enabled there is an additional 150µs delay before the soft start ramp begins. All LV regulators have soft start and forward and reverse current limiting to control inrush current during start-up and to provide short-circuit protection in normal operation.

The LV buck switching regulators are phased in 90° steps to reduce noise and input ripple. The phase step determines the fixed edge of the switching sequence, which is when the PMOS turns on. The PMOS off (NMOS on) phase is subject to the duty cycle demanded by the regulator. Buck 1 is set to 0°, Buck 2 is set to 90°, Buck 3 is set to 270°, and Buck 4 is set to 180°. In shutdown all SW nodes are high impedance. The buck regulator enable pins may be tied to V_{OUT} voltages through a resistor divider, to program power-up sequencing.

LV Buck Regulators with Combined Power Stages

Up to four adjacent LV buck regulators may be combined in a master-slave configuration by setting the configuration via the C1, C2, and C3 pins. These pins should either be tied to ground or pin strapped to $INTV_{CC}$ in accordance with the desired configuration code (Table 1). Any combined SW pins must be tied together, as must any of the combined V_{IN} pins. EN1 and FB1 are utilized by Buck 1, EN2 and FB2 by Buck 2, EN3 and FB3 by Buck 3, and EN4 and FB4 by Buck 4. If any buck is not used or is not available in the desired configuration, then the associated FB and EN pins must be tied to ground.

Any available combination of 2, 3, or 4 adjacent buck regulators serves to provide up to either 2A, 3A, or 4A of average output load current. For example, code 110 (C3C2C1) configures Buck 1 to operate as a 4A regulator through V_{INA-H}/SWA-H pairs A, B, C, and D, while Buck 2 is disabled, Buck 3 operates as a 1A regulator through V_{INA-H}/SWA-H pair E, and Buck 4 operates as a 3A regulator through V_{INA-H}/SWA-H pairs F, G, and H.

OPERATION

Table 1. Master Slave Program Combinations (Each Letter Corresponds to a Low Voltage Power Stage)

PROGRAM CODE C3C2C1	BUCK 1	BUCK 2	BUCK 3	BUCK 4
000	AB	CD	EF	GH
001	ABC	D	EF	GH
010	ABC	D	E	FGH
011	ABCH	D	E	FG
100	ABC	DE	Not Used	FGH
101	ABCD	Not Used	EF	GH
110	ABCD	Not Used	E	FGH
111	ABCD	Not Used	Not Used	EFGH

Power Failure Reporting via $\overline{RST}$ Pin

Power failure conditions of all LV buck regulators are reported by the single $\overline{RST}$ pin. Each LV regulator has an internal power good signal. If LV Buck 1 output voltage falls below 98%, or any of the Buck 2-4 outputs falls below 95%, of its programmed value, or if any LV regulator's output rises above 107.5% of its programmed value, its internal power good signal is pulled low. If any internal power good signal stays low for greater than 100µs, then the $\overline{RST}$ pin is pulled low. The $\overline{RST}$ low signal indicates to a microprocessor that a power failure fault has occurred. The 100µs filter time prevents a false fault indication low due to a output/load transient.

The internal power good comparators have hysteresis, so the regulated output voltage of an enabled regulator has to move back into the power good window by more than the hysteresis for its power good signal to transition high. Once all enabled LV regulator outputs are power good for 202ms (typical, C_T = 10nF), the $\overline{RST}$ output goes high impedance (pulled high by external resistor/current). If all LV buck regulators are disabled, $\overline{RST}$ pulls low.

Temperature Monitoring and Overtemperature Protection

To prevent thermal damage to the IC and its surrounding components, the LV regulators have an overtemperature (OT) function. When the LTC3372 die temperature reaches 170°C (typical) all LV buck switching regulators are shut down and remain in shutdown until the die temperature falls to 160°C (typical).

The temperature may be read back by the user by sampling the TEMP pin analog voltage. The temperature, T, indicated by the TEMP pin voltage is given by:

$$T = \frac{V_{TEMP} - 45mV}{7mV} \bullet 1°C$$

To reduce quiescent current (I_Q), if all the LV buck regulators are shut down, the temperature monitor also shuts down and the TEMP pin becomes high impedance. The temperature monitor can be disabled by tying the TEMP pin to $INTV_{CC}$ to save I_Q.

Programming the Operating Frequency

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output voltage ripple.

The frequency of the internal oscillator (system clock) is determined by an external resistor that is connected between the RT pin and ground. The operating frequency can be calculated using the following equation:

$$f_{OSC} = \frac{8 \bullet 10^{11} \bullet \Omega Hz}{R_T}$$

The oscillator is designed to function with operating frequencies between 1MHz and 3MHz, it has safety clamps that prevent the oscillator from running faster than 4MHz (typical) or slower than 250kHz (typical). Tying the RT pin to $INTV_{CC}$ sets the oscillator to the default internal operating frequency of 2MHz (typical).

The internal oscillator can be synchronized through an internal PLL circuit to an external frequency by applying a square wave clock signal to the PLL/MODE pin. During synchronization, the top MOSFET turn-on of LV buck regulator 1 is phase-locked to the rising edge of the external frequency source. All other LV regulators are locked to the appropriate phase of the external frequency source.

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The synchronization frequency range is 1MHz to 3MHz. A synchronization signal on the PLL/MODE pin will force all low voltage (LV) active buck switching regulators to operate in forced continuous mode PWM.

The LV regulators switch directly off the internal oscillator in 90-degree phase increments. The LTC3372 HV controller switches at one-sixth (1/6) of the internal oscillator frequency with a range of between 166kHz to 500kHz.

Windowed Watchdog Timer

A standard watchdog function is used to ensure that the system is in a valid state by continuously monitoring the microprocessor's activity. The microprocessor must toggle the logic state of the WDI pin periodically in order to clear the watchdog timer. The WDI pin reset is read only on a WDI falling edge, such that a single reset signal may be asserted by pulsing the WDI pin for a time greater than the minimum pulse width. If timeout occurs, a WDO low is asserted for the reset timeout period, issuing a system reset. Once the reset timeout completes, WDO is released to go high and the watchdog timer starts again.

During power-up, the watchdog timer initiates in the timeout state with WDO asserted low. As soon as the reset timer times out, WDO goes high and the watchdog timer is started.

A windowed watchdog function is implemented by adding a lower boundary condition to the standard watchdog function. If the WDI input receives a falling edge prior to the watchdog lower boundary, the part considers this a watchdog failure, and asserts WDO low (releasing again after the reset timeout period as described above). This will again be followed by another lower boundary time period.

The watchdog timer shuts down when RUN and EN1-4 are off (all HV and LV regulators are shut down). Tying the CT pin to $INTV_{CC}$ disables the watchdog timer regardless of the RUN and EN1-4 pins (HV and LV regulators either on or off).

Choosing the C_T Capacitor

The watchdog timeout period is adjustable and can be optimized for software execution. The watchdog timeout period is adjusted by connecting a capacitor between CT and ground. Given a specified watchdog timeout period, the capacitor is determined by:

$$C_T = t_{WDO} \bullet 49.39\ [nF/s]$$

For example, using a standard capacitor value of 10nF gives a 202ms watchdog timeout period. Further, the other watchdog timing periods scale with t_{WDO}. The watchdog lower boundary time (t_{WDL}) scales as precisely 1/4 of t_{WDO}, the watchdog upper boundary time following the previous WDI pulse scales as eight times that of t_{WDO}, and the watchdog upper boundary time following a watchdog timeout scales as 64 times that of t_{WDO}. Finally the RST assertion delay will scale to the same time as t_{WDO}.

These timing periods are illustrated in Figure 1. Each WDO low period is equal to the time period t_2-t_1 (202ms for a 10nF C_T capacitor, typical). If a WDI falling edge occurs before the watchdog lower boundary, indicated by t_3-t_2 (50.6ms for a 10nF C_T capacitor, typical), then another watchdog timeout period occurs. If a WDI falling edge occurs after the watchdog lower boundary (t_4), then the watchdog counter resets, beginning with another watchdog lower boundary period. In the case where a WDI low transition is not detected by the specified time another watchdog timeout period is initiated. This time is indicated by t_5-t_4 (1.62s for a 10nF C_T capacitor, typical). If a WDI low transition is not detected within the specified time following a watchdog timeout period, then another watchdog timeout period is initiated. This time is indicated by t_7-t_6 (12.9s for a 10nF C_T capacitor, typical).

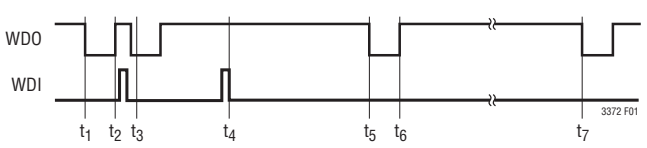


Figure 1. WDO Timing Parameters

APPLICATIONS INFORMATION High Voltage Buck Controller

HIGH VOLTAGE BUCK CONTROLLER

The Typical Application on the first page is a basic application circuit. The HV controller inductor current sensing can be configured to use either DCR (inductor resistance) or a low value sense resistor. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing has become popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value. Next, the power MOSFETs. Finally, input and output capacitors are selected.

Current Sense Pins (SENSE+ and SENSE–)

The SENSE+ and SENSE– pins are the inputs to the current comparators. The common mode voltage range on these pins is 0V to 6V (abs max), allowing margin for tolerances and transients for the HV regulator's regulated 5V or 3.3V output.

The SENSE+ pin is high impedance over the full common mode range, drawing at most ±1µA. This high impedance allows the current comparators to be used in inductor DCR sensing.

Connect the SENSE– pin directly to the sense point at the V_{OUT} side of the inductor (in DCR sensing) or the current sense resistor (R_{SENSE}), without adding any resistor in series. The impedance of the SENSE– pin changes depending on its voltage. When SENSE– is less than $INTV_{CC}$ – 0.5V, a small current of less than 1µA flows out of the pin. As SENSE– approaches $INTV_{CC}$, the current transitions higher to close to 1mA.

Filter components mutual to the sense lines should be placed close to the IC, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 2). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If inductor DCR sensing is used (Figure 3b), resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes.

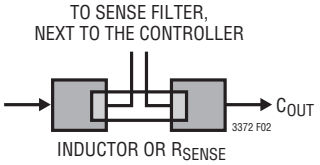
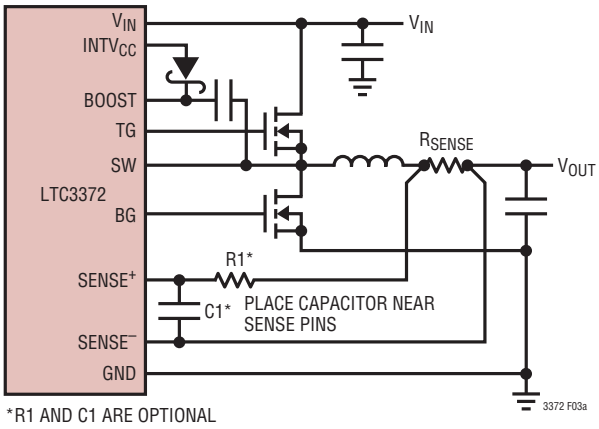
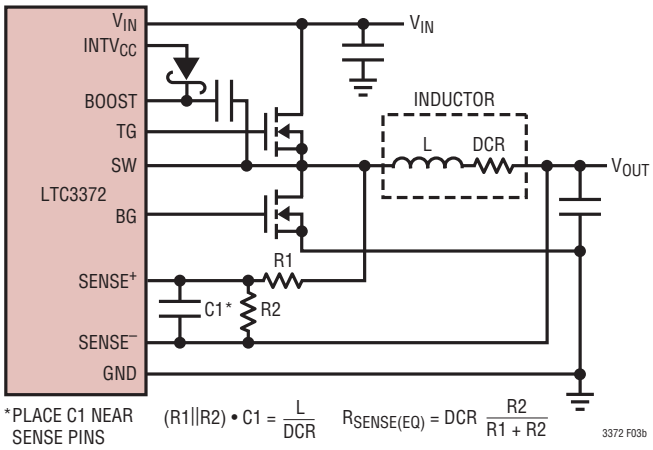


Figure 2. Sense Lines Placement with Inductor or Sense Resistor



(3a) Using a Resistor to Sense Current



(3b) Using the Inductor DCR to Sense Current

Figure 3. Current Sensing Methods

APPLICATIONS INFORMATION High Voltage Buck Controller

Resistor Current Sensing

A typical sensing circuit using a discrete resistor is shown in Figure 3a. R_{SENSE} is chosen based on the required output current.

This LTC3372's current comparator has a fixed maximum current limit threshold of 75mV (typical). The current comparator threshold voltage sets the peak of the inductor current, yielding a maximum average output current, I_{MAX}, equal to the peak value less half the peak-to-peak ripple current, ΔI_L. To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value (68mV) for the Maximum Current Sense Threshold ($V_{SENSE(MAX)}$) in the Electrical Characteristics table.

When using the controller in very low dropout conditions, the maximum output current level will be reduced due to the internal compensation required to meet stability criterion for buck regulators operating at greater than 50% duty factor. The maximum current sense threshold vs duty cycle curve is provided in the Typical Performance Characteristics section to estimate this reduction in peak inductor current depending upon the operating duty factor.

Inductor DCR Current Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC3372's HV controller is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 3b. The DCR of the inductor represents the small amount of DC resistance of the copper wire, which can be less than 1mΩ for today's low value, high current inductors. In a high current application requiring such an inductor, power loss through a sense resistor would cost several points of efficiency compared to inductor DCR sensing.

If the external (R1||R2) • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' data sheets for detailed information.

Using the inductor ripple current value from the Inductor Value Calculation section, the target sense resistor value is:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value (68mV) for the Maximum Current Sense Threshold ($V_{SENSE(MAX)}$) in the Electrical Characteristics table.

Next, determine the DCR of the inductor. When provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of copper resistance, which is approximately 0.4%/°C. A conservative value for $T_{L(MAX)}$ is 100°C.

To scale the maximum inductor DCR to the desired sense resistor value, use the divider ratio (R_D):

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX} \text{ at } T_{L(MAX)}}$$

C1 is usually selected to be in the range of 0.1µF to 0.47µF. This forces R1 || R2 to around 2k, reducing error that might have been caused by the $SENSE^+$ pin's ±1µA current.

The equivalent resistance R1 || R2 is scaled to the room temperature inductance and maximum DCR:

$$R1||R2 = \frac{L}{(DCR \text{ at } 20°C) \bullet C1}$$

APPLICATIONS INFORMATION High Voltage Buck Controller

The sense resistor values are:

$$R1 = \frac{R1||R2}{R_D};\ R2 = \frac{R1 \bullet R_D}{1 - R_D}$$

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS}\ R1 = \frac{(V_{IN(MAX)} - V_{OUT}) \bullet V_{OUT}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET switching and gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current, ΔI_L, decreases with higher inductance or higher frequency and increases with higher V_{IN}:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3(I_{MAX})$. The maximum ΔI_L occurs at the maximum input voltage.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance value selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred for high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Power MOSFET and Schottky Diode (Optional) Selection

Two external power MOSFETs must be selected for the HV controller: one N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5.1V during start-up (see V_{OUT} Pin Connection). Consequently, logic-level threshold MOSFETs must be used in most applications. Pay close attention to the BV_{DSS} specification for the MOSFETs as well.

Selection criteria for the power MOSFETs include the on-resistance, $R_{DS(ON)}$, Miller capacitance, C_{MILLER}, input

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voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{MAX}}{2}\right)(R_{DR})(C_{MILLER})\bullet\left[\frac{1}{V_{INTVCC} - V_{THMIN}} + \frac{1}{V_{THMIN}}\right](f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and R_{DR} (approximately 2Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. V_{THMIN} is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For $V_{IN} < 20V$ the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$ the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term $(1+\delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs.

A Schottky diode can be placed in parallel with the bottom MOSFET to conduct during the dead-time between the conduction of the two power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on, storing charge during the dead-time and requiring a reverse recovery period that could cost as much as 3% in efficiency at high V_{IN}. A 1A to 3A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance.

Another consideration is the losses due to the gate charge of the MOSFETs. Each cycle, the bottom FET gate driver draws a pulse of current from the $INTV_{CC}$ pin when turning on the bottom FET gate. Another pulse of current is drawn by the boost capacitor as the bottom FET turns on. This energy is used by the floating high side driver to turn on the top MOSFET. The $INTV_{CC}$ decoupling capacitor smooths the current flowing through the LDO. The resulting DC current can be estimated as:

$$I_{GQ} = f(Q_{GT} + Q_{GB})$$

The LDO losses will then become:

$$P_{LDO} = (V_{IN} - V_{INTVCC}) \bullet I_{GQ}$$

To avoid the LDO losses, program V_{OUT} for 5V with the VOUTPRG pin. With this setting, the $INTV_{CC}$ LDO is shut down and the $INTV_{CC}$ pin is tied to V_{OUT} with an internal switch. This will provide significant power loss reductions for high input voltages.

The losses in the gate driver are also affected by the MOSFET gate charge. A conservative estimate of the these losses is:

$$P_{GATE\_DRIVE} = I_{GQ} \bullet V_{INTVCC}$$

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C_{IN} and C_{OUT} Selection

The selection of C_{IN} is usually based off the worst-case RMS input current. The highest $(V_{OUT})(I_{OUT})$ product needs to be used in the formula to determine the maximum RMS capacitor current requirement.

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left[(V_{OUT})(V_{IN}-V_{OUT})\right]^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than size or height requirements in the design. Due to the high operating frequency, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

A small (0.1µF to 1µF) bypass capacitor between the chip V_{IN} pin and ground, placed close to the IC, is also suggested. A small (<10Ω) resistor placed between C_{IN} (C1) and the V_{IN} pin provides further isolation.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (V_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L\left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}}\right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and ΔI_L is the ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Setting Output Voltage (HV Controller)

The HV controller output voltage is set by the V_{OUTPRG} pin through an internal resistor voltage divider. When the V_{OUTPRG} pin is tied to $INTV_{CC}$, the output voltage is regulated to 5V. When tied to ground, the output voltage is regulated to 3.3V.

RUN Pin

The HV controller is enabled using the RUN pin. It has a rising threshold of 1.2V with 50mV of hysteresis. Pulling the RUN pin below 1.15V shuts down the main control loop. Pulling it below 0.7V disables the controller and most internal circuits, including the $INTV_{CC}$ LDOs.

Releasing the RUN pin allows a 0.5µA internal current to pull up the pin to enable the controller. The RUN pin may be externally pulled up to up to 60V (65V Abs Max).

The RUN pin can be implemented as a UVLO by connecting it to the output of an external resistor divider network off V_{IN}, as shown in Figure 4.

The rising and falling UVLO thresholds are calculated using the RUN pin thresholds:

$$V_{UVLO(RISING)} = 1.2V\left(1+\frac{R_B}{R_A}\right)$$

$$V_{UVLO(FALLING)} = 1.15V\left(1+\frac{R_B}{R_A}\right)$$

The resistor values should be carefully chosen such that the absolute maximum ratings of the RUN pin do not get violated over the entire V_{IN} voltage range.

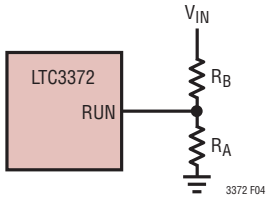

Figure 4. Using the RUN Pin as a UVLO

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Tracking and Soft-Start (TRACK/SS Pin)

The start-up of V_{OUT} is controlled by the voltage on the TRACK/SS pin. When the voltage on the TRACK/SS pin is less than the internal 1.2V reference, it regulates the internal V_{FB} voltage to the voltage on the TRACK/SS pin instead of 1.2V. The TRACK/SS pin can be used to program an external soft-start function or to allow V_{OUT} to track another supply during start-up.

Soft-start is enabled by simply connecting a capacitor from the TRACK/SS pin to ground, as shown in Figure 5. An internal 10µA current source charges the capacitor, providing a linear ramping voltage at the TRACK/SS pin. The HV controller will regulate the V_{FB} (and hence V_{OUT}) according to the voltage on the TRACK/SS pin, allowing $V_{OUT}/EXTV_{CC}$ to rise smoothly from 0V to its final regulated value. The total soft-start time will be approximately:

$$t_{SS} = C_{SS} \bullet \frac{1.2V}{10\mu A}$$

Alternatively, the TRACK/SS pin can be used to track another supply during start-up, as shown qualitatively in Figures 6a and 6b. To do this, a resistor divider should be connected from the master supply (V_X) to the TRACK/SS pin of the slave supply ($V_{OUT}/EXTV_{CC}$) as shown in Figure 7. During start-up $V_{OUT}/EXTV_{CC}$ will track V_X according to the ratio set by the resistor divider:

$$\frac{V_X}{V_{OUT}} = \frac{1.2V}{V_{OUT(REG)}} \bullet \frac{R_{TRACKA} + R_{TRACKB}}{R_{TRACKA}}$$

$V_{OUT(REG)}$ is the programmed output regulation voltage. If the V_{OUTPRG} pin it tied to $INTV_{CC}$ pin, $V_{OUT(REG)}$ = 5V. If the V_{OUTPRG} pin is tied to ground, $V_{OUT(REG)}$ = 3.3V.

$INTV_{CC}$ Regulation

$INTV_{CC}$ powers the gate drivers and much of the internal circuitry. Power to the $INTV_{CC}$ pin is supplied either from the V_{IN} pin through an internal low dropout linear regulator (LDO), or from the $V_{OUT}/EXTV_{CC}$ pin through an internal switch, depending on the voltage at $V_{OUT}/EXTV_{CC}$. The V_{IN} LDO regulates $INTV_{CC}$ to 5.1V. The $INTV_{CC}$ can supply a peak current of at least 50mA and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor. Good

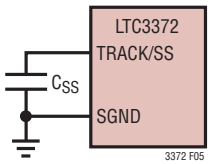
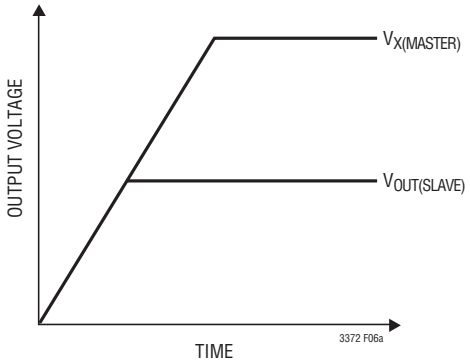
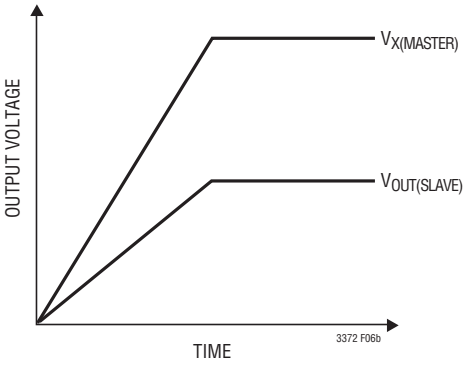


Figure 5. Using the TRACK/SS Pin to Program Soft-Start



(6a) Coincident Tracking



(6b) Ratiometric Tracking

Figure 6. Two Different Modes of Output Voltage Tracking

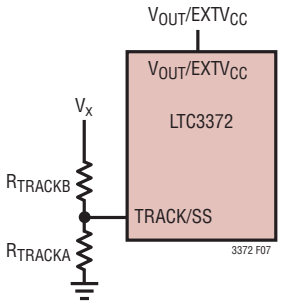


Figure 7. Using the TRACK/SS Pin for Tracking

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bypassing is needed to supply the high transient currents required by the MOSFET gate drivers and to prevent interaction between the channels.

The $INTV_{CC}$ load current (I_{INTVCC}) is dominated by the gate charge current and may be supplied by either the V_{IN} LDO or the $V_{OUT}/EXTV_{CC}$ pin. The gate charge current is dependent on operating frequency and NMOS size as discussed in the Efficiency Considerations section.

When the $V_{OUT}/EXTV_{CC}$ regulation is set to 3.3V, the V_{IN} LDO is always enabled as the voltage on the $V_{OUT}/EXTV_{CC}$ pin is never above the 4.7V threshold. Power dissipation for the IC in this case is highest and is equal to $V_{IN} \bullet I_{INTVCC}$.

High input voltage applications in which large power MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the IC to be exceeded. For example, a 30mA $INTV_{CC}$ current from a 48V input supply will result in a junction temperature (T_J) increase (rise) of:

$$\Delta T_J = (30mA)(48V)(34°C/W \text{ for QFN}) = 48°C$$

The power dissipation due to I_{INTVCC} from V_{IN} should be checked at the maximum V_{IN} of the application operating in forced continuous mode.

When the V_{OUT} regulation is set to 5V and V_{OUT} rises above 4.7V, $INTV_{CC}$ is connected to V_{OUT} through an internal switch. Significant efficiency and thermal gains can be realized by powering $INTV_{CC}$ from the output, since the input supply current resulting from $INTV_{CC}$ current is scaled by a factor of $(V_{OUT}/V_{IN})/(\text{efficiency})$. In this case, power dissipation in the LTC3372 due to the $INTV_{CC}$ current is $V_{INTVCC} \bullet I_{INTVCC}$, and the junction temperature (T_J) increase (rise) of:

$$\Delta T_J = (30mA)(5V)(34°C/W \text{ for QFN}) = 5°C$$

The LTC3372 junction temperature (T_J) can be estimated from ambient temperature (T_A) and total power dissipation (P_D) using the equations given in Note 2 of the Electrical Characteristics. To prevent the maximum junction temperature from being exceeded, all power dissipations from the HV controller's $INTV_{CC}$ current and the LV buck power stages must be considered.

Topside MOSFET Driver Supply (C_B, D_B)

An external bootstrap capacitor, C_B, connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. Capacitor C_B in the Block Diagram is charged though external diode D_B from $INTV_{CC}$ when the SW pin is low. When the topside MOSFET is to be turned on, the driver places the C_B voltage across the gate-source of the MOSFET. This enhances the top MOSFET switch and turns it on. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{INTVCC}$. The value of the boost capacitor, C_B, needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of the external Schottky diode must be greater than $V_{IN(MAX)}$.

Fault Conditions: Current Limit and Current Foldback

The HV controller includes current foldback to help limit load current when the output is shorted to ground. If the output voltage falls below 70% of its nominal output level, then the maximum sense voltage is progressively lowered from 100% to 45% of its maximum selected value. Under short-circuit conditions with very low duty cycles, cycle skipping will begin in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power. The short-circuit ripple current is determined by the minimum on-time, $t_{ON(MIN)}$ (see Electrical Characteristics), the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \left(\frac{V_{IN}}{L} \right)$$

The resulting average short-circuit current is:

$$I_{SC} = 45\% \bullet I_{LIM(MAX)} - \frac{1}{2} \Delta I_{L(SC)}$$

Fault Conditions: Overvoltage Protection (Crowbar)

The overvoltage crowbar is designed to blow a system input fuse when the output voltage of the regulator rises much higher than nominal levels. The crowbar causes huge currents to flow, that blow the fuse to protect against a shorted top MOSFET if the short occurs while the controller is operating.

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Both the V_{OUT} and SENSE$^-$ pins are monitored for overvoltage conditions. An overvoltage condition is detected when either pin is 7.5% above the nominal output voltage. When this condition is sensed, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared. The bottom MOSFET remains on continuously for as long as the overvoltage condition persists; if V_{OUT} returns to a safe level, normal operation automatically resumes.

A shorted top MOSFET will result in a high current condition which will open the system fuse. The switching regulator will regulate properly with a leaky top MOSFET by altering the duty cycle to accommodate the leakage.

Minimum On-Time Considerations

The minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the HV controller is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time of top FET is typically 60ns. However, as the peak sense voltage decreases the minimum on-time gradually increases. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%Efficiency = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in HV regulator: 1) IC V_{IN} current, 2) $INTV_{CC}$ regulator current, 3) I^2R losses, 4) topside MOSFET transition losses.

1. The V_{IN} current is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents. V_{IN} current typically results in a small (<0.1%) loss.

2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge, dQ, moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

   In applications when $V_{OUT}/EXTV_{CC}$ is set to 5V, $INTV_{CC}$ is supplied through $V_{OUT}/EXTV_{CC}$. This scales the V_{IN} current required for the driver and control circuits by a factor of (Duty Cycle)/(Efficiency). For example, in a 20V to 5V application, 10mA of $INTV_{CC}$ current results in approximately 2.5mA of V_{IN} current. This reduces the midcurrent loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

3. I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, current sense resistor and input and output capacitor ESR. In continuous mode the average output current flows through L and R_{SENSE}, but is chopped between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L, R_{SENSE} and ESR to obtain I2R

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losses. For example, if each $R_{DS(ON)}$ = 30mΩ, R_L = 50mΩ, R_{SENSE}= 10mΩ and R_{ESR} = 40mΩ (sum of both input and output capacitance losses), then the total resistance is 130mΩ. This results in losses ranging from 3% to 13% as the output current increases from 1A to 5A for a 5V output, or a 4% to 20% loss for a 3.3V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

4. Transition losses apply only to the topside MOSFET(s), and become significant only when operating at high input voltages (typically 15V or greater). Transition losses can be estimated from:

   Transition Loss = (1.7) • V_{IN} • 2 • $I_{O(MAX)}$ • C_{RSS} • f

   Other hidden losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these system level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of 20mΩ to 50mΩ of ESR. Other losses including body diode conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the ITH pin not only allows optimization of control loop behavior, but it also provides a DC coupled and AC filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components in Typical Applications will provide an adequate starting point for most applications.

The ITH series RC-CC filter sets the dominant pole-zero loop compensation. The values can be modified slightly to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response.

The gain of the loop will be increased by increasing RC and the bandwidth of the loop will be increased by decreasing CC. If RC is increased by the same factor that CC is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

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A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}/$EXTV_{CC}$. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Design Example

As a design example, assume V_{IN} = 12V (nominal), V_{IN} = 60V (max) for transient voltages, V_{OUT} = 3.3V, I_{MAX} = 10A, $V_{SENSE(MAX)}$ = 75mV and f = 333kHz. The inductance value is chosen first based on a 30% ripple current assumption. The highest value of ripple current occurs at the maximum input voltage. Tie the R_T pin to $INTV_{CC}$ (for better frequency accuracy over temperature, use an external R_T = 400k to ground), generating 333kHz operation for LTC3372's HV controller (1/6 of f_{OSC} at 2MHz). The maximum ripple current is:

$$\Delta I_L = \frac{V_{OUT}}{(f)(L)}\left(1-\frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

A 2.2µH inductor will produce 43% ripple current which is sufficiently close. The peak inductor current will be the maximum DC value plus one half the ripple current, or 12.1A. Increasing the ripple current will also help ensure that the minimum on-time of 60ns is not violated. The minimum on-time occurs at maximum V_{IN}:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}(f)} = \frac{3.3V}{60V(333kHz)} = 165ns$$

The equivalent R_{SENSE} resistor value can be calculated by using the minimum value for the maximum current sense threshold (68mV):

$$R_{SENSE} \le \frac{68mV}{12.1A} \approx 5.6m\Omega$$

Rounding down to the next standard value yields a sense resistor value of 5mΩ.

For a 3.3V/10A 333kHz converter operating with a nominal 12V input and a 60V surge rating, a reasonable MOSFET selection is:

Top: RJK0651DPB

$R_{DS(ON)}$ = 0.018Ω, Q_G = 15nC,

C_{MILLER} = 148pF, V_{THMIN} = 1.2V, V_{DSS} = 60V

Bottom: RJK0652DPB

$R_{DS(ON)}$ = 0.009Ω, Q_G = 29nC, V_{DSS} = 60V

At the nominal input voltage of 12V with T(estimated) = 50°C, the losses become:

$$P_{MAIN} = \frac{3.3V}{12V}(10A)^2\left[1+(0.005)(50°C-25°C)\right](0.018\Omega) + (12V)^2\frac{10A}{2}(2\Omega)(148pF)\bullet\left[\frac{1}{5.1V-1.2V}+\frac{1}{1.2V}\right](333kHz)$$

$$= 557mW + 77mW$$

$$= 643mW$$

$$P_{SYNC} = \frac{12V-3.3V}{12V}(10A)^2\bullet\left[1+(0.005)(50°C-25°C)\right](0.009\Omega)$$

$$= 734mW$$

Other losses include the gate drive and $INTV_{CC}$ LDO losses. These can be estimated from the gate charge and switching frequency:

I_{GQ} = 333kHz (15nC + 29nC)

= 14.7mA

P_{LDO} = (12V – 5.1V) 14.7mA

= 101mW

P_{GATE_DRIVE} = 5.1V • 14.7mA

P_{GATE_DRIVE} = 75mW

APPLICATIONS INFORMATION Low Voltage Buck Regulators

With the input voltage at a sustained 60V and full load on the output, the estimated power losses in the main FET will be 2.0W and the LDO losses inside the chip will be 0.8W. Airflow will likely be required. A lower switching frequency will reduce these losses and setting V_{OUT} to 5V will avoid the LDO losses.

A short-circuit to ground will result in a folded back current of:

$$I_{SC} = \frac{0.45(75mV)}{0.005\Omega} - \frac{1}{2}\left(\frac{60ns(22V)}{2.2\mu H}\right) = 6.6A$$

with a maximum value of $R_{DS(ON)}$ and = (0.005/°C)(25°C) = 0.125. The resulting power dissipated in the bottom MOSFET is:

$$P_{SYNC} = (6.6A)^2(1.125)(0.009\Omega)$$
$$= 441mW$$

which is less than under full-load conditions. C_{IN} is chosen for an RMS current rating of at least 5A at temperature assuming only this channel is on. C_{OUT} is chosen with an ESR of 0.01Ω for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$$V_{ORIPPLE} = R_{ESR}(\Delta I_L) = 0.1\Omega(4.3A) = 43mV_{P-P}$$

LOW VOLTAGE BUCK REGULATORS

Output Voltage and Feedback Network

The output voltage of each LV buck switching regulators is programmed by a resistor divider connected from the switching regulator's output to its feedback pin and is given by $V_{OUT} = V_{FB}(1 + R2/R1)$ as shown in Figure 8. Typical values for R1 range from 40k to 1M. The buck regulator transient response may improve with an optional capacitor, C_{FF}, that helps cancel the pole created by the feedback resistors and the input capacitance of the FB pin. Experimentation with capacitor values between 2.2pF and 22pF may improve transient response.

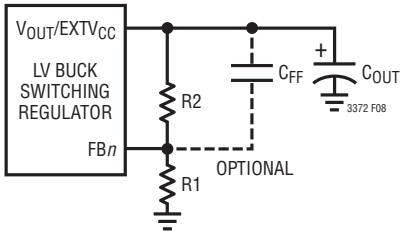


Figure 8. Feedback Components

Input and Output Decoupling Capacitor Selection

The LTC3372 buck regulators have individual input supply pins for each buck power stage. Each of these pins must be decoupled with low ESR capacitors to GND. These capacitors must be placed as close to the pins as possible. Ceramic dielectric capacitors are a good compromise between high dielectric constant and stability versus temperature and DC bias. Note that the capacitance of a capacitor deteriorates at higher DC bias. It is important to consult manufacturer data sheets and obtain the true capacitance of a capacitor at the DC bias voltage that it will be operated at. For this reason, avoid the use of Y5V dielectric capacitors. The X5R/X7R dielectric capacitors offer good overall performance.

Each low voltage input power supply voltage $V_{IN,A-H}$ Pins 5, 8, 9, 12, 25, 28, 29 and 32 all need to be de-coupled with at least 10µF capacitors. If power stages are combined the supplies should be shorted with as short of a trace as possible. Additionally, all LV buck regulator outputs should be bypassed with a capacitor to ground of at least 22µF for 1A, 47µF for 2A, 68µF for 3A and 100µF for 4A configurations.

Combined Buck Power Stages

The LTC3372 has eight power stages that can handle average load currents of 1A each. These power stages may be combined in any one of eight possible combinations, via the C1, C2, and C3 pins (see Table 1). Table 3, Table 4, and Table 5 show recommended inductors for the combined power stage configurations.

For a 2A combined buck regulator, the input supply should be de-coupled with a 22µF capacitor while the output should be de-coupled with a 47µF capacitor. Similarly, for 3A and 4A configurations the input and output capacitance must be scaled up to account for the increased load.

APPLICATIONS INFORMATION Low Voltage Buck Regulators

Table 2. Recommended Inductors for 1A Buck Regulators

f_{OSC}	PART NUMBER	L (µH)	MAX I_{DC} (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
1MHz	XFL4020-472ME	4.7	2.7	57.4	4 × 4 × 2.1	CoilCraft
	74408943047	4.7	2.2	52	4.8 × 4.8 × 3.8	Wurth Elektronik
2MHz	XFL4020-222ME	2.2	3.7	23.5	4 × 4 × 2.1	CoilCraft
	DFE252012P-2R2M	2.2	2.2	84	2.5 × 2.0 × 1.2	Toko
	IHLP1212BZER2R2M-11	2.2	3	46	3 × 3.65 × 2.0	Vishay
3MHz	74438336015	1.5	3.7	39	3 × 3 × 2	Wurth Elektronik
	DFE252012F-1R5M	1.5	2.7	58	2.5 × 2 ×1.2	Toko

Table 3. Recommended Inductors for 2A Buck Regulators

f_{OSC}	PART NUMBER	L (µH)	MAX I_{DC} (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
1MHz	XEL4020-222ME	2.2	5.5	38.7	4 × 4 × 2.1	CoilCraft
	74438356022	2.2	4.7	35	4.1 × 4.1 × 2.1	Wurth Elektronik
2MHz	XFL4020-102ME	1	5.4	11.9	4 × 4 × 2.1	CoilCraft
	IHLP1212BZER1R0M-11	1	4.5	24	3 × 3.65 × 2.0	Vishay
	SPM4020T-1R0M-LR	1	5.6	28.1	4.1 × 4.4 × 2	TDK
3MHz	744383360068	0.68	4.5	27	3 × 3 × 2	Wurth Elektronik
	IHLP1212AEERR68M-11	0.68	5.4	22	3 × 3.65 × 1.5	Vishay

Table 4. Recommended Inductors for 3A Buck Regulators

f_{OSC}	PART NUMBER	L (µH)	MAX I_{DC} (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
1MHz	XEL4020-152ME	1.5	7.4	23.6	4 × 4 × 2.1	CoilCraft
	IHLP2020CZER1R5M11	1.5	7	18.5	5.18 × 5.49 × 3	Vishay
2MHz	XEL4020-821ME	0.82	10.2	13	4 × 4 × 2	CoilCraft
	FDV0530-H-R75M	0.75	9.7	7.6	6.2 × 5.8 × 3	Toko
	744383560068	0.68	8.2	9	4.1 × 4.1 × 2.1	Wurth Elektronik
3MHz	FDSD0420D-R47M	0.47	6.8	18	4.2 × 4.2 × 2	Toko
	IHLP1212AEERR47M-11	0.47	6.7	15	3 × 3.65 × 1.5	Vishay

Table 5. Recommended Inductors for 4A Buck Regulators

f_{OSC}	PART NUMBER	L (µH)	MAX I_{DC} (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
1MHz	XEL4020-102ME	1	9	14.6	4 × 4 × 2.1	CoilCraft
	744316100	1	11.5	5.225	5.3 × 5.5 × 4.0	Wurth Elektronik
2MHz	XEL4020-561ME	0.56	11.3	8.8	4 × 4 × 2.1	CoilCraft
	FDV0530-H-R56M	0.56	11.1	6.3	6.2 × 5.8 × 3	Toko
	SPM4020T-R47M-LR	0.47	8.7	11.8	4.1 × 4.4 × 2	TDK
3MHz	XEL4014-331ME	0.33	9	12	4 × 4 × 1.4	CoilCraft
	744383560033	0.33	9.6	7.2	4.1 × 4.1 × 2.1	Wurth Elektronik

APPLICATIONS INFORMATION

Efficiency can be increased by combining more power stages than are required to meet output current requirements. Conduction loss will decrease by adding power stages. The overall efficiency will improve provided the switching loss of the added power stage does not exceed the reduction in conduction loss. For example, a buck running at 900mA load may have a higher efficiency when two power stages are combined to make a 2A buck. In this example, the 900mA load is closer to the peak efficiency power of the 2A buck this it is for a 1A buck. In addition to efficiency concerns, combining additional power stages provides increased margin and transient capability. It is therefore a good idea to explore combining any unused power stages with active bucks in any given application. Otherwise, any unused buck regulator should have it's FB and EN pins tied to ground. The V_{IN} pin may be tied to ground and the SW pin can float.

PRINTED CIRCUIT BOARD PCB LAYOUT CONSIDERATIONS

PCB Layout Considerations for HV Regulator

1. The path formed by the top N-channel MOSFET, the bottom N-channel MOSFET, and the C_{INTVCC} capacitor should have short leads and (PCB) trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitor and kept away from the loop described above.

   For proper operation of the gate drivers, the BG and TG traces should maintain low impedance. The length of the BG and TG traces should be 1.0" or less and the number of via should be kept minimum.

2. Kelvin connect the V_{OUT}/$EXTV_{CC}$ pin directly to the (+) terminal of C_{OUT}, or where the regulation needs to be. The connection should not be along the high current input feeds from the input capacitor(s).

3. Route the $SENSE^-$ and $SENSE^+$ signals together with minimum PCB trace spacing. The filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the current sense resistor. Don't connect the current sensing leads backwards! The output voltage may still be maintained but the current mode control will not be realized.

4. Place the $INTV_{CC}$ decoupling capacitor close to the IC, between the $INTV_{CC}$ pin and power ground plane. This capacitor carries the MOSFET drivers' current peaks. A ceramic capacitor placed immediately next to the $INTV_{CC}$ pin can help improve noise performance substantially.

5. Kelvin connect the return of the ITH network to an isolated shape (ground copper "island") tied to the GND pad of the IC (refer to the ground copper "island(s)" discussed in the Ground Planes section).

6. Keep the SW, TG, and BOOST nodes away from sensitive control signals (I_{TH}, $SENSE^+$, $SENSE^-$, RT, etc.). These nodes have very large and fast moving signals and therefore should be kept on the output side of the HV regulator and occupy minimum PCB trace area.

Debugging HV Buck Controller on PCB

1. Probe and synchronize the oscilloscope to the switching nodes (SW, SWA-H pins). It is helpful to use an oscilloscope current probe to monitor the currents in the inductors.

2. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to near dropout and until the peak of inductor current drops below the low current operation threshold—typically 25% of the maximum designed current level in Burst Mode operation.

   In pulse-skipping mode, the frequency should maintain at even lower peak inductor current compared to Burst Mode until a pulse is skipped to maintain the regulation. The frequency in forced continuous mode should not change with load current.

APPLICATIONS INFORMATION

The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation.

3. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PCB layout if regulator bandwidth optimization is not required.

4. Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation.

5. Investigate if any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins.

   If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, bottom MOSFET, and the top MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the exposed ground pad of the IC.

6. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling.

7. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, Schottky and the top MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the exposed ground pad of the IC.

PCB Layout Considerations for LV Regulators

1. Each of the V_{INA-H} input supply pins should have a decoupling capacitor. The connections of the decoupling capacitors to their respective V_{INA-H} pins should be kept as short as possible. The GND side of these capacitors should connect directly to the ground plane of the part. These capacitors provide the AC current to the internal power MOSFETs and their drivers. It is important to minimize inductance from these capacitors to the V_{IN} pins of the V_{INA-H} pins.

2. The switching power traces connecting SWA-H to the inductors should be minimized to reduce radiated EMI and parasitic coupling. Due to the fast voltage swing of the switching nodes, high input impedance sensitive nodes, such as the feedback nodes, should be shielded or kept far away from the switching nodes.

3. The return (GND side) of the switching regulators' output capacitors should be connected to the exposed pad (Pin 49, GND) of the IC through a ground plane. Minimize the trace length from the output capacitors to the inductor(s)/pin(s).

4. In a multiple power stage buck regulator application, the trace length of switch nodes to the inductor must be kept equal to ensure proper operation.

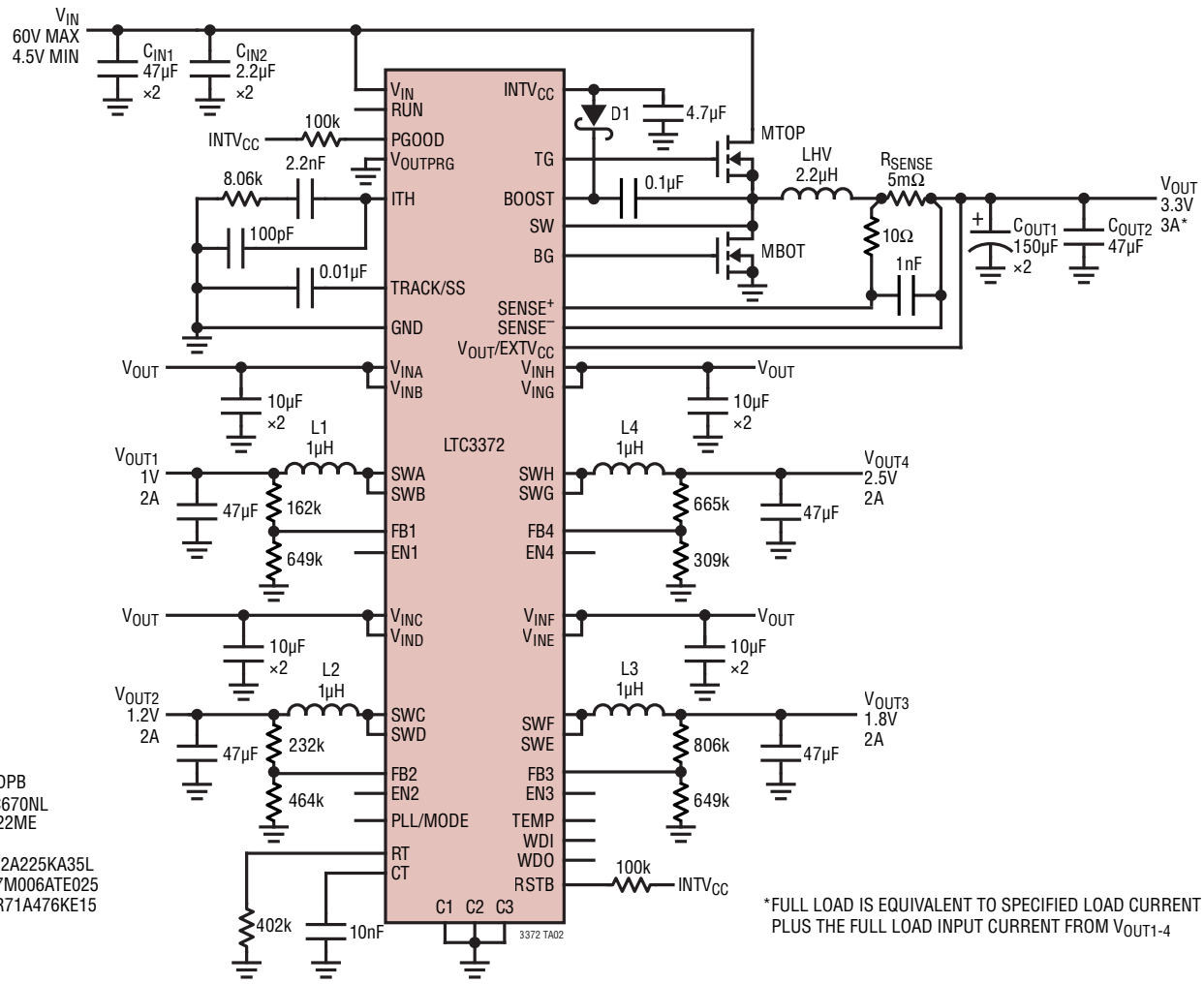
5. Kelvin connect the returns for RT, CT and the feedback dividers to an isolated shape (ground copper "island") tied to the GND pad of the IC.

Other PCB Layout Considerations

Care should be taken to minimize capacitance on the TEMP pin. If the TEMP voltage must drive more than ~30pF, then the pin should be isolated with a resistor placed close to the pin of a value between 10k and 100k. Keep in mind that any load on the isolation resistor will create a proportional error.

TYPICAL APPLICATIONS

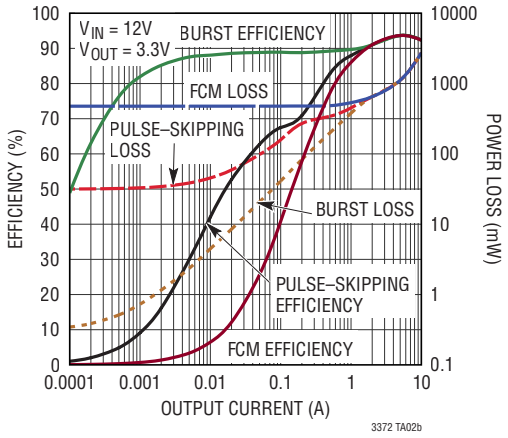
4.5V to 60V Input 3.3V/3A Output HV Buck Converter Plus Quad 1V/1.2V/1.8V/2.5V LV Regulators



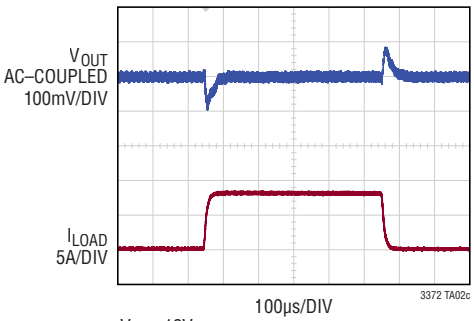
MTOP: RJK0651DPB
MTOP: NTMFS5C670NL
LHV: XAL1010-222ME
C_{IN1}: 63HVH47M
C_{IN2}: GRM32ER72A225KA35L
C_{OUT1}: T520B157M006ATE025
C_{OUT2}: GRM32ER71A476KE15
D1: DFLS1100

*FULL LOAD IS EQUIVALENT TO SPECIFIED LOAD CURRENT PLUS THE FULL LOAD INPUT CURRENT FROM V_{OUT1-4}

HV Controller Efficiency and Power Loss vs Output Current



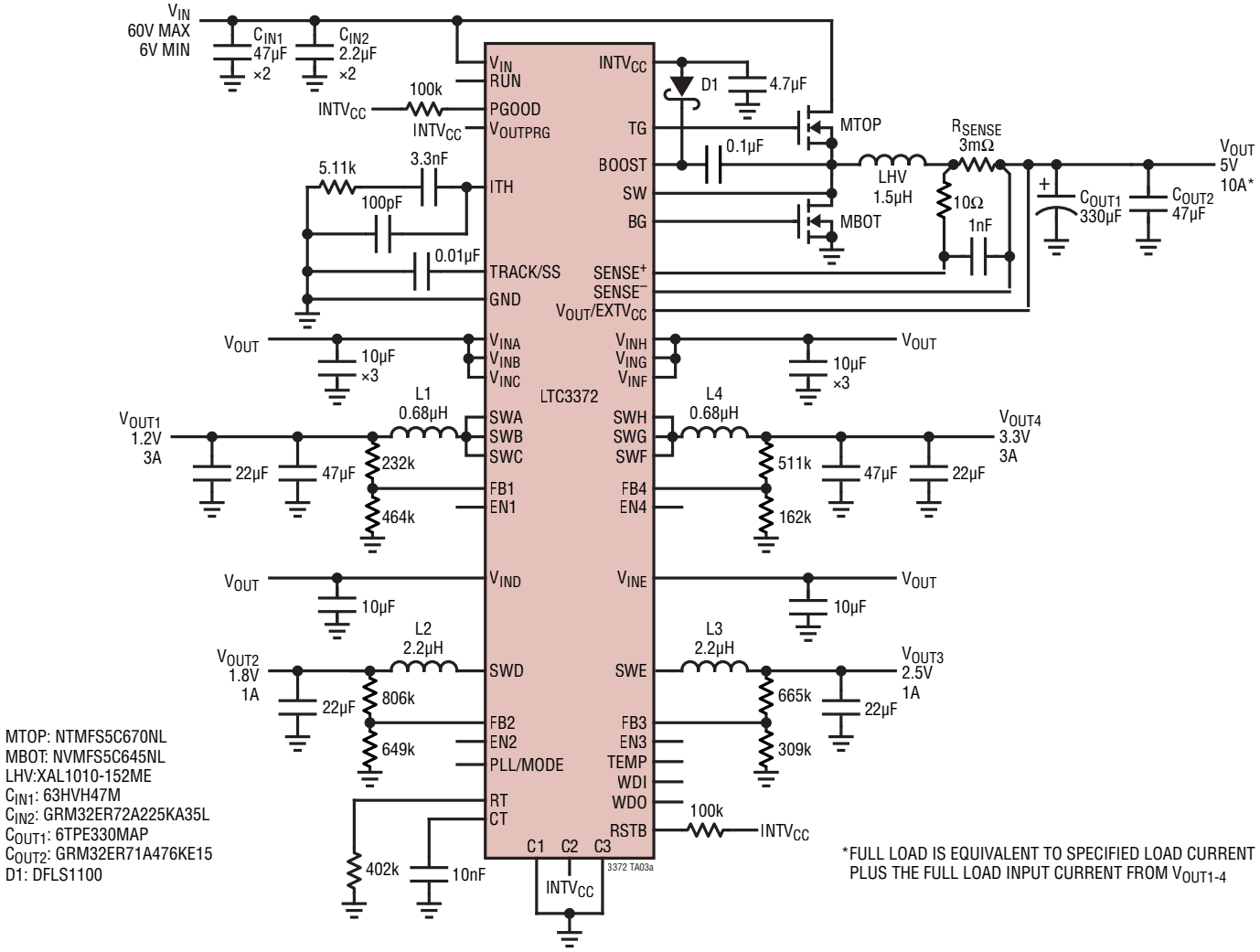
HV Controller Forced Continuous Mode Load Step



V_{IN} = 12V
V_{OUT} = 3.3V
I_{LOAD} = 200mA to 8A

TYPICAL APPLICATIONS

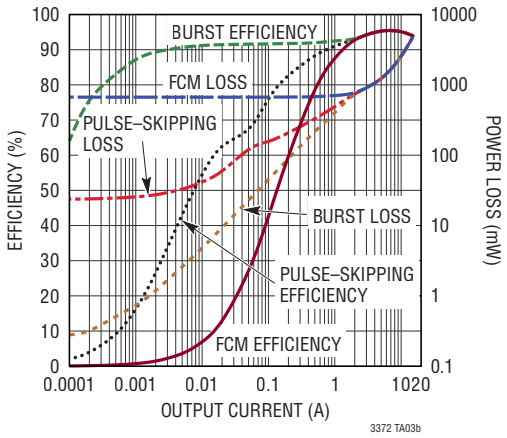
6V to 60V Input 5V/10A Output HV Buck Converter Plus Quad 1.2V/3A, 1.8V/1A, 2.5V/1A, and 3.3V/3A LV Regulators



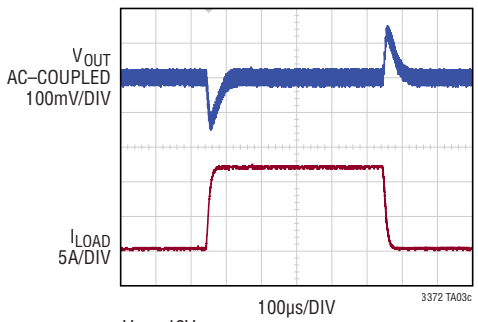
MTOP: NTMFS5C670NL
MBOT: NVMFS5C645NL
LHV:XAL1010-152ME
C_{IN1}: 63HVH47M
C_{IN2}: GRM32ER72A225KA35L
C_{OUT1}: 6TPE330MAP
C_{OUT2}: GRM32ER71A476KE15
D1: DFLS1100

*FULL LOAD IS EQUIVALENT TO SPECIFIED LOAD CURRENT PLUS THE FULL LOAD INPUT CURRENT FROM V_{OUT1-4}

HV Controller Efficiency and Power Loss vs Output Current



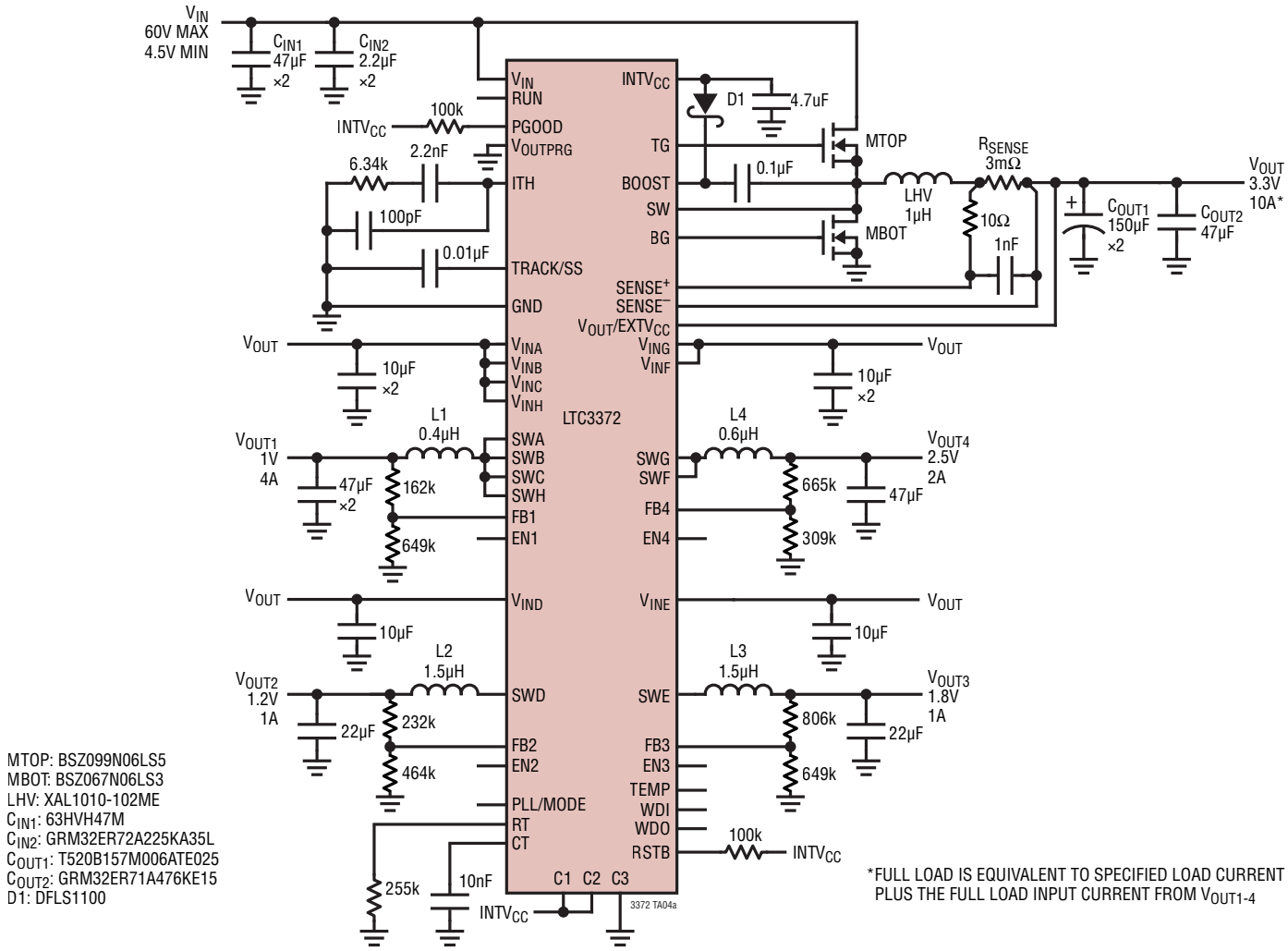
HV Controller Forced Continuous Mode Load Step



V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 200mA to 12A

TYPICAL APPLICATIONS

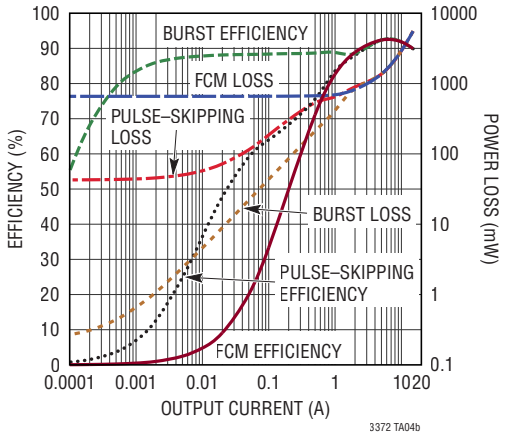
4.5V to 60V Input 3.3V/10A Output HV Buck Converter Plus Quad 1V/4A, 1.2V/1A, 1.8V/1A and 2.5V/2A LV Regulators



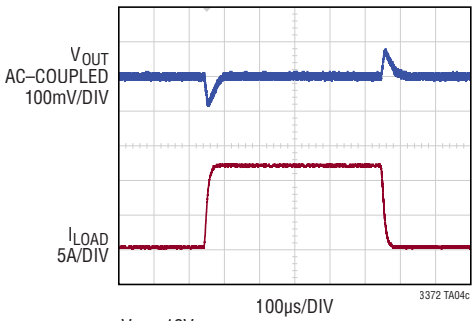
MTOP: BSZ099N06LS5
MBOT: BSZ067N06LS3
LHV: XAL1010-102ME
C_{IN1}: 63HVH47M
C_{IN2}: GRM32ER72A225KA35L
C_{OUT1}: T520B157M006ATE025
C_{OUT2}: GRM32ER71A476KE15
D1: DFLS1100

*FULL LOAD IS EQUIVALENT TO SPECIFIED LOAD CURRENT PLUS THE FULL LOAD INPUT CURRENT FROM V_{OUT1-4}

HV Controller Efficiency and Power Loss vs Output Current



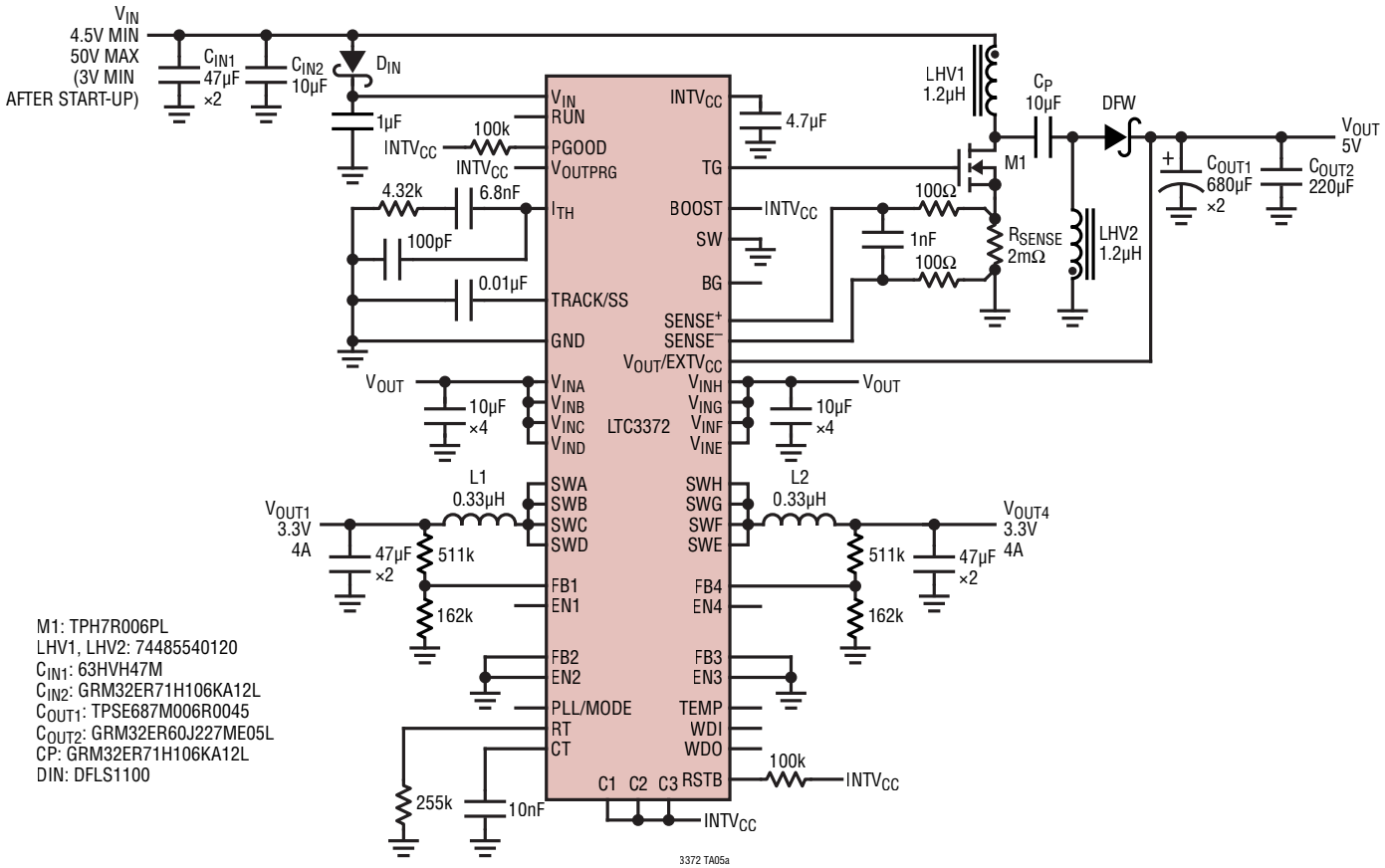
HV Controller Forced Continuous Mode Load Step



V_{IN} = 12V
V_{OUT} = 3.3V
I_{LOAD} = 200mA to 12A

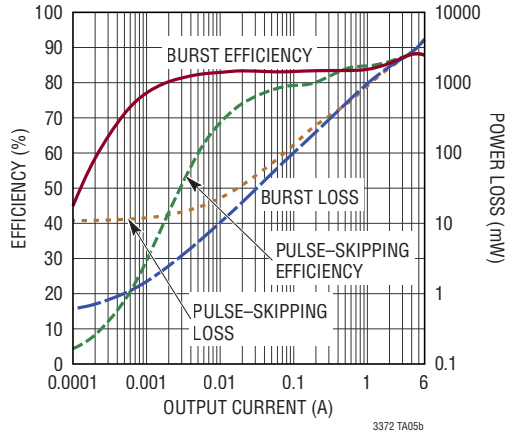
TYPICAL APPLICATIONS

4.5V (3V Minimum After Start-Up) to 50V Input HV SEPIC Converter Feeding Dual 3.3V/4A LV Regulators

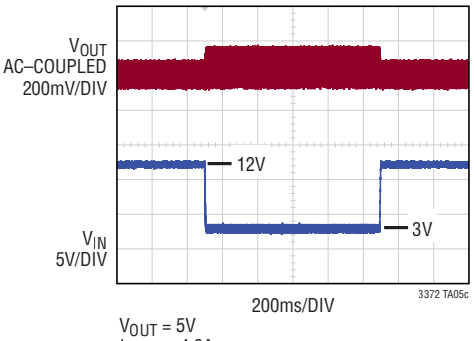


M1: TPH7R006PL
LHV1, LHV2: 74485540120
C_{IN1}: 63HVH47M
C_{IN2}: GRM32ER71H106KA12L
C_{OUT1}: TPSE687M006R0045
C_{OUT2}: GRM32ER60J227ME05L
CP: GRM32ER71H106KA12L
DIN: DFLS1100

HV Controller Efficiency and Power Loss vs Output Current



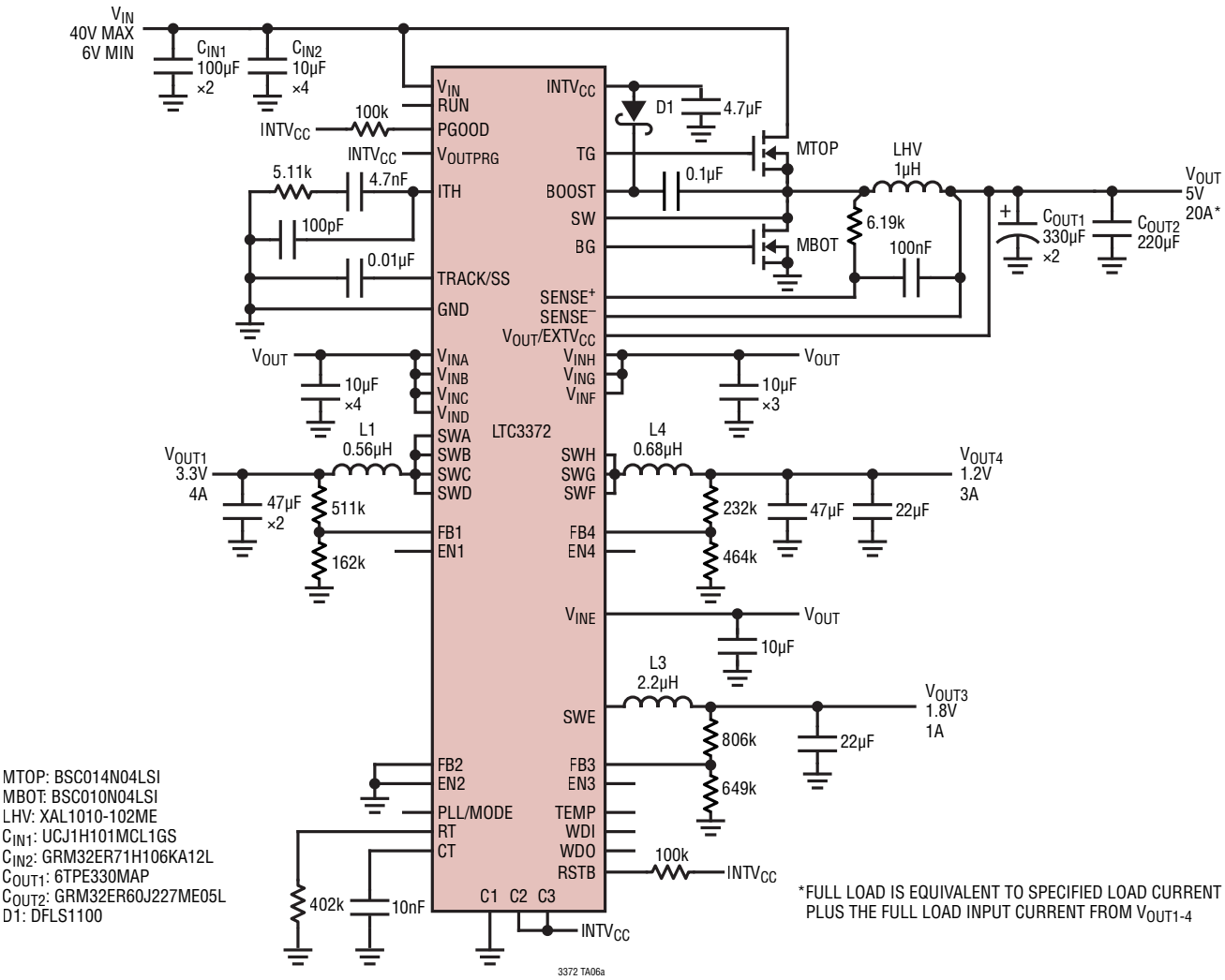
HV Controller V_{IN} Step Response



V_{OUT} = 5V
I_{LOAD} = 4.8A

TYPICAL APPLICATIONS

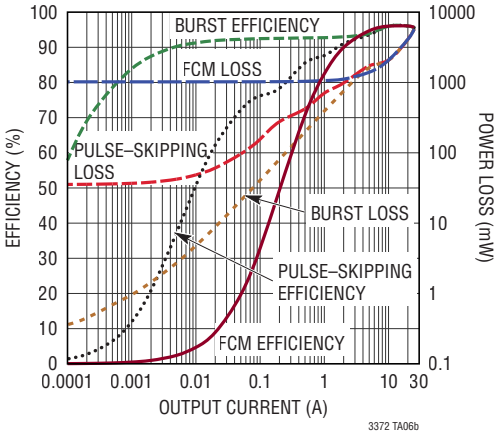
6V to 60V Input 5V/20A Output HV Buck Converter Plus Triple 3.3V/4A, 1.8V/1A and 1.2V/3A LV Regulators



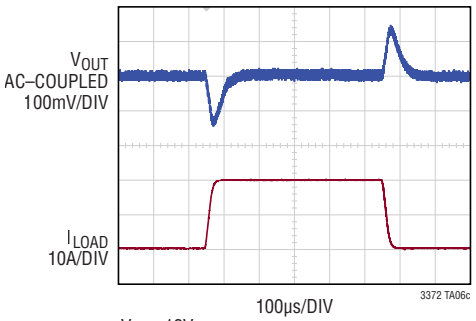
MTOP: BSC014N04LSI
MBOT: BSC010N04LSI
LHV: XAL1010-102ME
C_{IN1}: UCJ1H101MCL1GS
C_{IN2}: GRM32ER71H106KA12L
C_{OUT1}: 6TPE330MAP
C_{OUT2}: GRM32ER60J227ME05L
D1: DFLS1100

*FULL LOAD IS EQUIVALENT TO SPECIFIED LOAD CURRENT PLUS THE FULL LOAD INPUT CURRENT FROM V_{OUT1-4}

HV Controller Efficiency and Power Loss vs Output Current



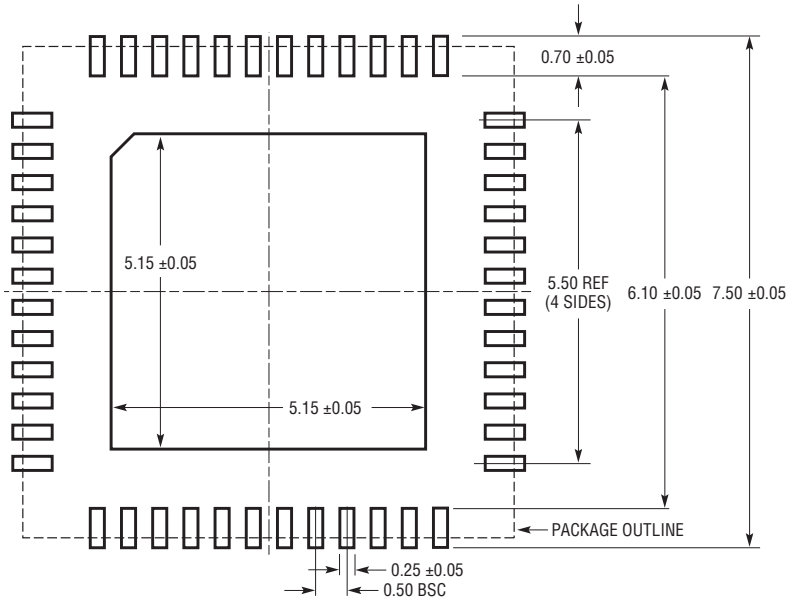
HV Controller Forced Continuous Mode Load Step



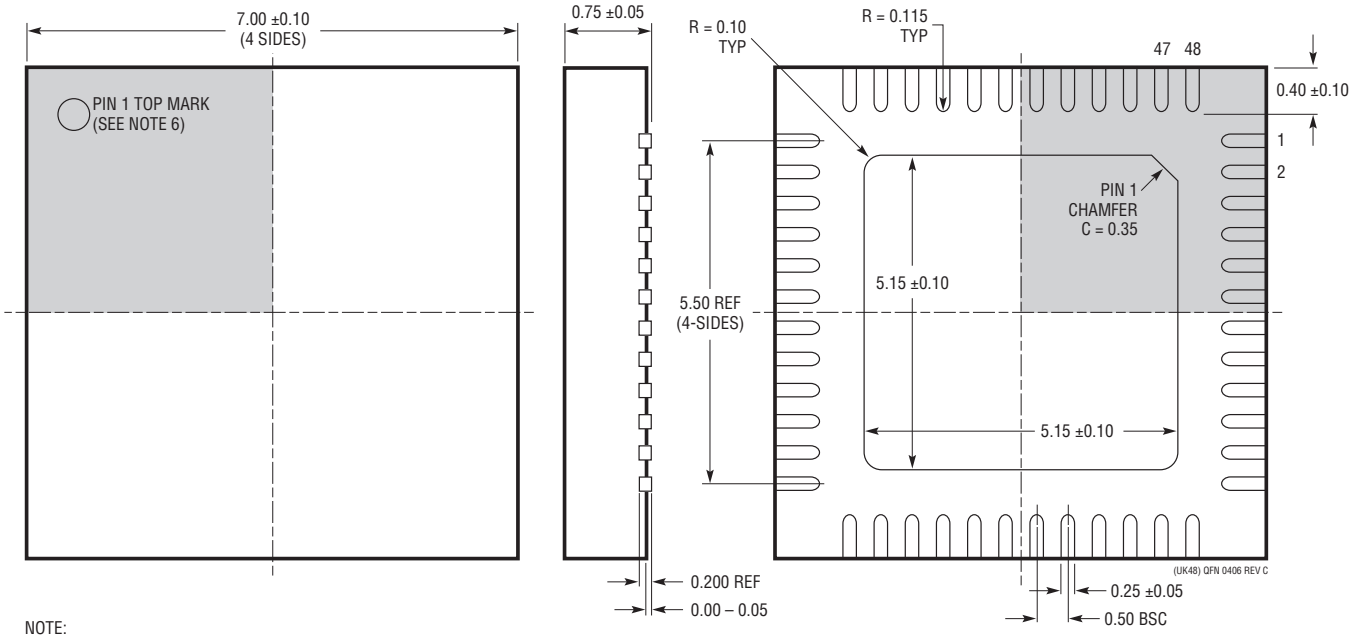
V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 200mA to 20A

PACKAGE DESCRIPTION

UK Package
48-Lead Plastic QFN (7mm × 7mm)
(Reference LTC DWG # 05-08-1704 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



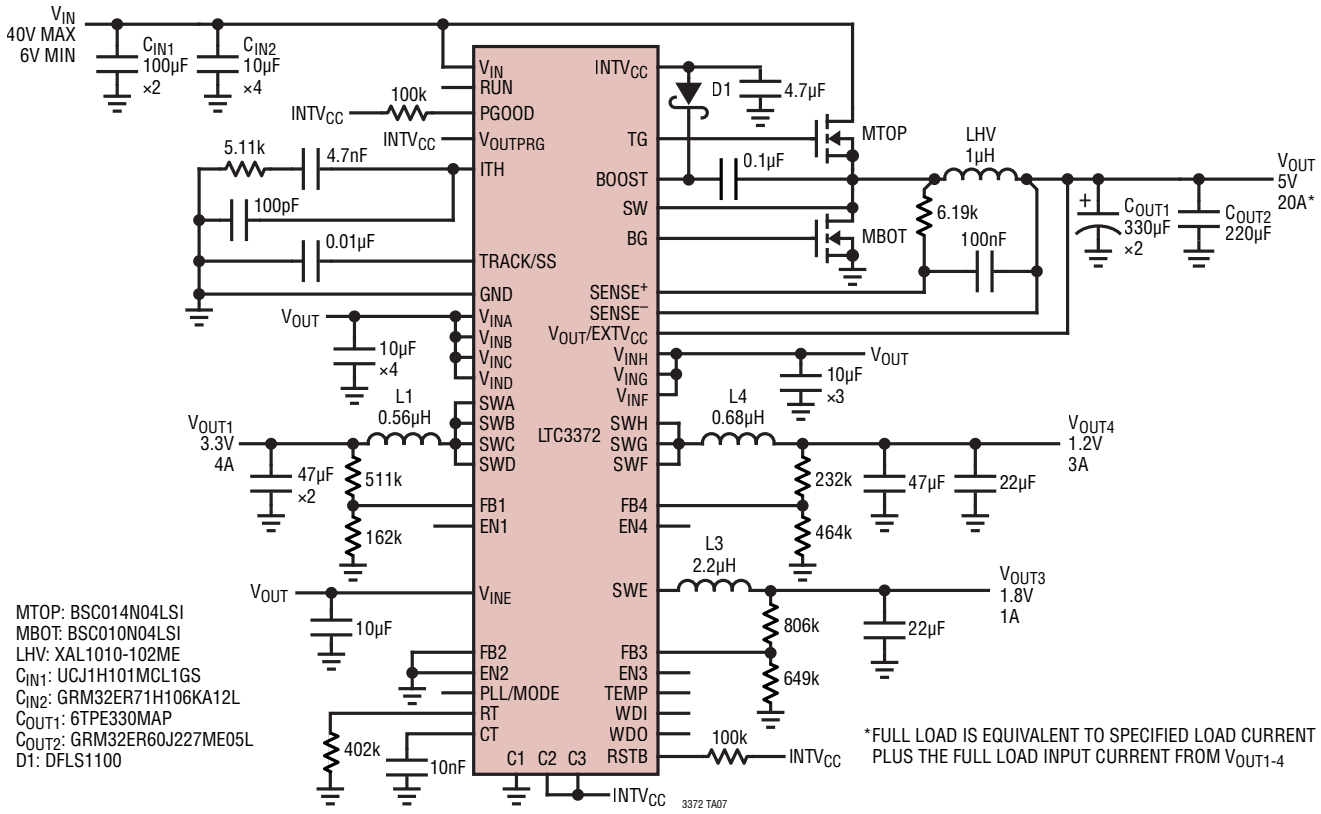
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WKKD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	03/19	Updated conditions in the Electrical Characteristics tables	4, 6

TYPICAL APPLICATION



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3891/LTC3890/ LTC3890-1/LTC3890-2/ LTC3890-3	60V, Low I_Q, Single/Dual Synchronous Step-Down DC/ DC Controller	Phase-Lockable Frequency 75kHz to 750kHz, 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q =50µA LTC3891: Single Channel; LTC3890/LTC3890-1/LTC3890-2/LTC3890-3
LTC3371/LTC3370	4-Channel Configurable DC/DC with 8 × 1A Power Stages	4 Synchronous Buck Regulators with 8 × 1A Power Stages. Can Connect Up to Four Power Stages in Parallel, 8 Output Configurations Possible. LTC3370: Precision PGOODALL Indication, 32-Lead (5mm × 5mm × 0.75mm) QFN Package. LTC3371: Precision $\overline{RST}$ Monitoring with Windowed Watchdog Timer (CT Programmable), 38-Lead (5mm × 7mm × 0.75mm) QFN and TSSOP Packages
LTC3892/LTC3892-1/ LTC3892-2	60V, Low I_Q, Dual, 2-Phase Synchronous Step-Down DC/ DC Controller	Phase-Lockable Frequency 75kHz to 850kHz, 4.5V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 99% V_{IN}, I_Q = 29µA, Adjustable 5V to 10V Gate Drive, No External Bootstrap Diode
LTC3589	8-Output Regulator with Sequencing and I^2C	Triple I^2C Adjustable High Efficiency Step-Down DC/DC Converters: 1.6A, 1A, 1A. High Efficiency 1.2A Buck-Boost DC/DC Converter, Triple 250mA LDO Regulators, 40-Lead (6mm × 6mm × 0.75mm) QFN.
LTC3675	7-Channel Configurable High Power PMIC	Quad Synchronous Buck Regulators (1A, 1A, 500mA, 500mA). Buck DC/DCs Can be Paralleled to Deliver Up to 2× Current with a Single Inductor. 1A Boost, 1A Buck- Boost, 40V LED Driver. 44-Lead (4mm × 7mm × 0.75mm) QFN Package.
LTC3676	8-Channel Power Management Solution for Application Processor	Quad Synchronous Buck Regulators (2.5A, 2.5A, 1.5A, 1.5A). Quad LDO Regulators (300mA, 300mA, 300mA, 25mA). 40-Lead (6mm × 6mm × 0.75mm) QFN Package.
LTC3375/LTC3374/ LTC3374A	8-Channel Programmable Configurable 1A DC/DC	8 × 1A Synchronous Buck Regulators. Can Connect Up to Four Power Stages in Parallel with a Single Inductor, 15 Output Configurations Possible, 48-Lead (7mm × 7mm × 0.75mm) QFN Package (LTC3375) 38-Lead (5mm × 7mm × 0.75mm) QFN and TSSOP Packages (LTC3374A)