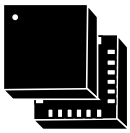
IIS328DQ

High-performance ultra-low-power 3-axis accelerometer with digital output for industrial applications

Datasheet - production data



QFN 24 (4 x 4 x 1.8 mm^3)

Features

- Wide supply voltage range: 2.16 V to 3.6 V
- Low voltage compatible IOs: 1.8 V
- Ultra-low power consumption: down to 10 µA
- ±2*g*/±4*g*/±8*g* dynamically selectable full-scale
- SPI / I^{2}C digital output interface
- 16-bit data output
- 2 independent programmable interrupt generators
- System sleep/wakeup function
- Extended temperature range: -40 °C to 105 °C
- Embedded self-test
- High shock survivability: up to 10000 *g*
- ECOPACK®, RoHS and “Green” compliant

Applications

- Anti-tampering devices
- Impact recognition and logging
- Vibration monitoring and compensation
- Robotics
- Platform/antenna stabilization
- Tilt/inclination measurements
- Motion-activated functions
- Intelligent power saving

Description

The IIS328DQ is an ultra-low-power high-performance 3-axis linear accelerometer with a digital serial interface, SPI or I^{2}C compatible. Recommended for industrial applications requiring an extended temperature range and long lifespan, the device features ultra-low-power operational modes that allow advanced power saving and smart sleep-to-wakeup functions. The IIS328DQ has dynamic user-selectable full-scales of ±2*g*/±4*g*/±8*g* and is capable of measuring accelerations with output data rates from 0.5 Hz to 1 kHz. The self-test capability allows the user to check the functioning of the sensor in the final application. The device may be configured to generate an interrupt signal through inertial wakeup events, or by the position of the device itself. Interrupt generators are programmable by the end user on-the-fly. Available in a small, quad, flat pack no-lead package (QFPN) with a 4x4 mm footprint, the IIS328DQ corresponds to the trend towards application miniaturization, and is guaranteed to operate over a temperature range from -40 °C to +105 °C.

Table 1. Device summary

Order codes	Temperature range [°C]	Package	Packaging
IIS328DQ	-40 to +105	QFPN 4x4x1.8 24L	Tray
IIS328DQTR	-40 to +105	QFPN 4x4x1.8 24L	Tape and reel

This is information on a product in full production. www.st.com

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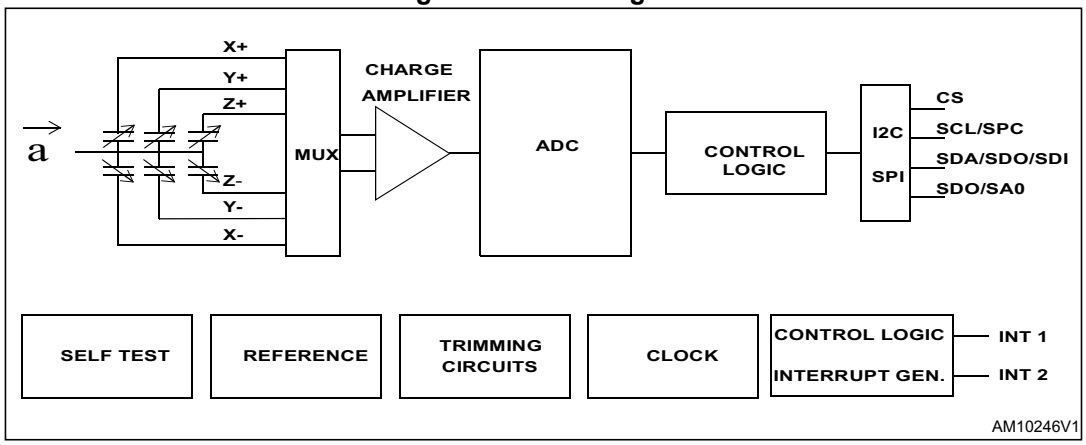
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1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Detectable accelerations and pin indicator

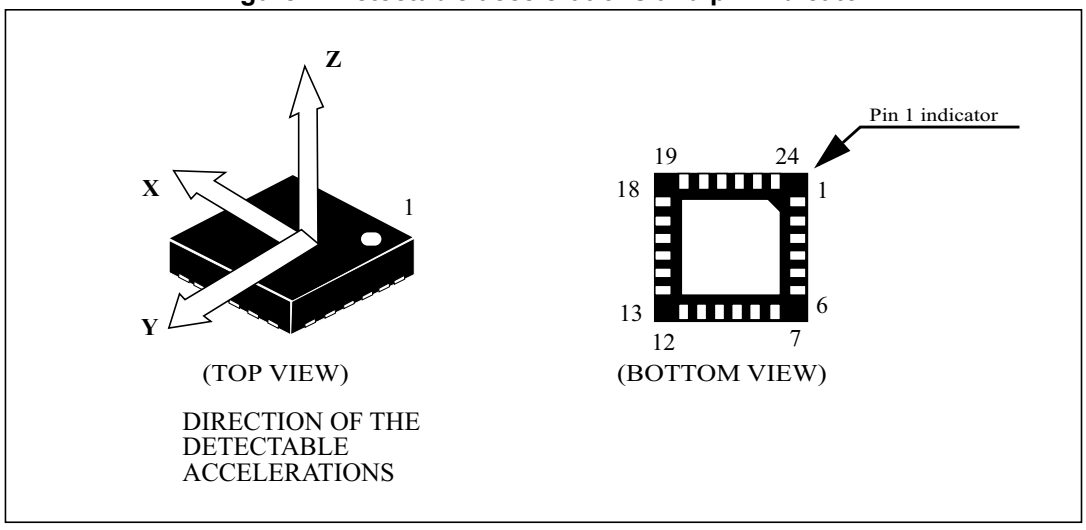


Table 2. Pin description

Pin#	Name	Function
1,2	NC	Not connected
3	INT_2	Inertial interrupt 2
4	Reserved	Connect to GND
5	VDD	Power supply
6	GND	0 V supply
7	INT_1	Inertial interrupt 1
8	GND	0 V supply
9	GND	0 V supply
10	GND	0 V supply
11	SPC SCL	SPI serial port clock (SPC) I²C serial clock (SCL) Internal active pull-up
12	CS	SPI enable I²C/SPI mode selection (0: SPI enabled; 1: I²C mode) Internal active pull-up
13	Reserved	Connect to Vdd
14	VDD_IO	Power supply for I/O pins
15	SDO SA0	SPI serial data output (SDO) I²C less significant bit of the device address (SA0) Internal active pull-up
16	SDI SDO SDA	SPI serial data input (SDI) 3-wire interface serial data output (SDO) I²C serial data (SDA) Internal active pull-up
17-24	NC	Not internally connected

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

@ Vdd=3.3 V, T=25 °C unless otherwise noted[a].

Table 3. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.(1)	Typ.(2)	Max.(1)	Unit
FS	Measurement range(3)	FS bits set to 00		±2.0		*g*
		FS bits set to 01		±4.0		
		FS bits set to 11		±8.0		
So	Sensitivity	FS bits set to 00 12-bit representation	0.9	0.98	1.1	mg/digit
		FS bits set to 01 12-bit representation	1.8	1.95	2.2	
		FS bits set to 11 12-bit representation	3.5	3.91	4.3	
TCSo	Sensitivity change vs temp.	FS bits set to 00		±0.01		%/°C
TyOff	Typical zero-*g* level offset accuracy (4),(5)	FS bits set to 00	-30	±20	+30	m*g*
TCOff	Zero-*g* level change vs. temperature	Excursion from 25 °C		±0.8		m*g*/°C
Off	Zero-*g* level offset accuracy(6)	FS bits set to 00	-300		+300	m*g*
An	Acceleration noise density	FS bits set to 00		218		µ*g*/√Hz
CrAx	Cross-axis(7)		-5		+5	%
Vst	Self-test output change(8),(9),(10)	FS bits set to 00 X-axis	-500	-800	-1100	LSb
		FS bits set to 00 Y-axis	500	800	1100	LSb
		FS bits set to 00 Z-axis	400	600	800	LSb
Wh	Product weight			60		mgram
Top	Operating temperature range		-40		+105	°C

1. Min/Max values are based on characterization results, not tested in production
2. Typical values are not guaranteed.
3. Verified by wafer level test and measurement of initial offset and sensitivity.
4. Offset can be eliminated by enabling the built-in high-pass filter.
5. Typical zero-*g* level offset as per factory calibration @ T = 25 °C.
6. Min/Max values for Off parameter are across temperature (-40 °C to 105 °C) and after MSL3 preconditioning. Based on characterization data. Not guaranteed and not tested in production.

a. The product is factory calibrated at 3.3 V. Operational power supply (Vdd) over 3.6 V is not recommended.

7. Guaranteed by design.
8. The sign of “Self-test output change” is defined by a sign bit, for all axes. Values in *Table 3* are defined with the STsign bit in the CTRL_REG4 register equal to logic “0” (positive self-test), at T = 25 °C.
9. Self-test output changes with the power supply. “Self-test output change” is defined as $OUTPUT[LSb]_{(CTRL_REG4\ ST\ bit=1)}$ - $OUTPUT[LSb]_{(CTRL_REG4\ ST\ bit=0)}$. 1LSb=4*g*/4096 at 12-bit representation, ±2 *g* full-scale.
10. Output data reaches 99% of final value after 3/ODR when enabling self-test mode, due to device filtering.

2.2 Electrical characteristics

@ Vdd = 3.3 V, T = 25 °C unless otherwise noted[b].

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ[1].	Max.	Unit
Vdd	Supply voltage		2.16	3.3	3.6	V
Vdd_IO	I/O pins supply voltage[2]		1.71		Vdd+0.1	V
Idd	Current consumption in normal mode	2.4 V to 3.6 V		250		µA
IddLP	Current consumption in low-power mode	ODR=1 Hz, BW=500 Hz, T=25 °C		10		µA
IddPdn	Current consumption in power-down mode			1		µA
VIH	Digital high-level input voltage		0.8*Vdd_IO			V
VIL	Digital low-level input voltage				0.2*Vdd_IO	V
VOH	High-level output voltage		0.9*Vdd_IO			V
VOL	Low-level output voltage				0.1*Vdd_IO	V
ODR	Output data rate in normal mode	DR bits set to 00		50		Hz
		DR bits set to 01		100		
		DR bits set to 10		400		
		DR bits set to 11		1000		
ODR_{LP}	Output data rate in low-power mode	PM bits set to 010		0.5		Hz
		PM bits set to 011		1		
		PM bits set to 100		2		
		PM bits set to 101		5		
		PM bits set to 110		10		
BW	System bandwidth			ODR/2		Hz
Ton	Turn-on time[3]	ODR = 100 Hz		1/ODR+1 ms		s
Top	Operating temperature range		-40		+105	°C

1. Typical values are not guaranteed.

b. The product is factory calibrated at 3.3 V. Operational power supply (Vdd) over 3.6 V is not recommended.

2. It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses; in this condition the measurement chain is powered off.
3. Time to obtain valid data after exiting power-down mode.

2.3 Communication interface characteristics

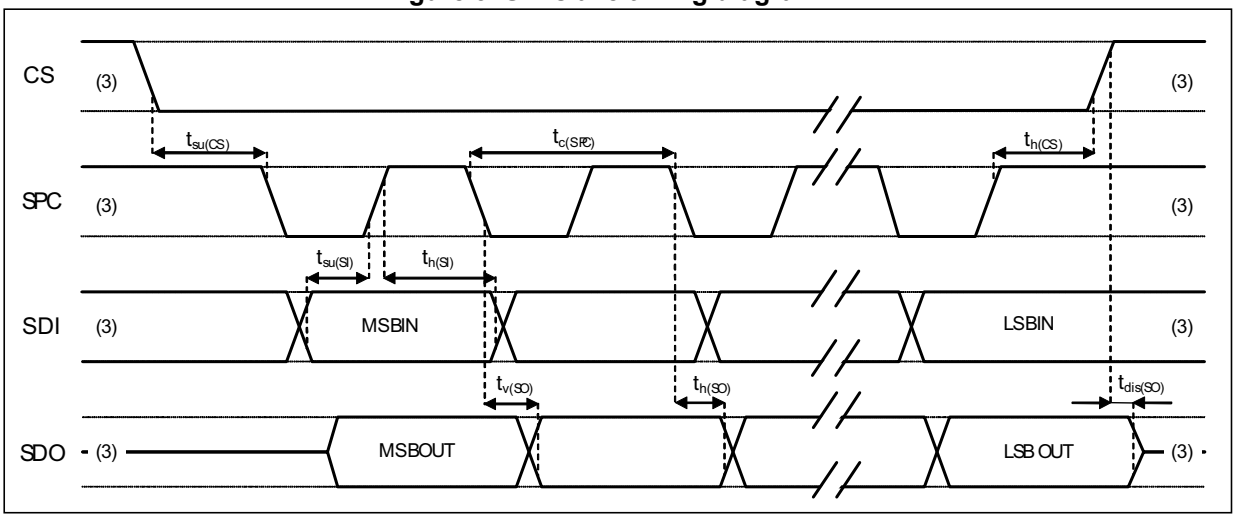
2.3.1 SPI - serial peripheral interface

Subject to general operating conditions for Vdd and Top.

Table 5. SPI slave timing values

Symbol	Parameter	Value (1)		Unit
		Min.	Max.	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	6		ns
$t_{h(CS)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

Figure 3. SPI slave timing diagram (2)



1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.
2. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.
3. When no communication is ongoing, data on CS, SPC, SDI and SDO are driven by internal pull-up resistors.

2.3.2 I²C - inter IC control interface

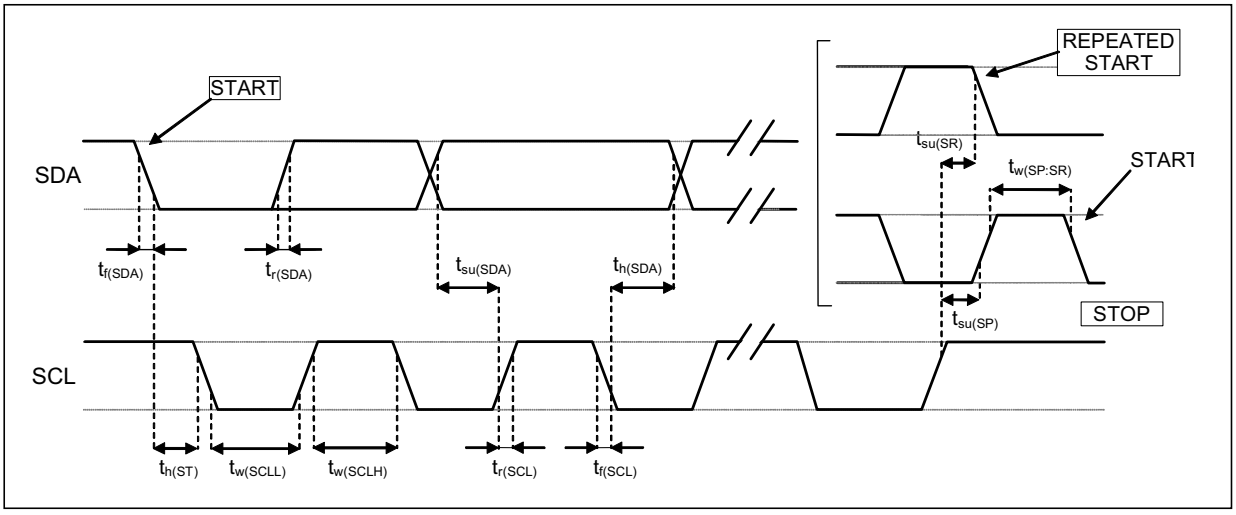
Subject to general operating conditions for Vdd and top.

Table 6. I²C slave timing values

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min.	Max.	Min.	Max.	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0.01	3.45	0.01	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.

Figure 4. I²C slave timing diagram (c)



c. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.4 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4	V
Vdd_IO	I/O pin supply voltage	-0.3 to 4	V
Vin	Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 2.5 V)(1)	3000 *g* for 0.5 ms	
		10000 *g* for 0.1 ms	
A_{UNP}	Acceleration (any axis, unpowered)(1)	3000 *g* for 0.5 ms	
		10000 *g* for 0.1 ms	
T_{OP}	Operating temperature range	-40 to +105	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	4 (HBM)	kV
		1.5 (CDM)	kV
		200 (MM)	V

1. Design guarantee; characterization done at 1500 *g*/0.5 ms, 3000 *g*/0.3 ms, 10000 *g*/0.1 ms; tests under these conditions have passed successfully.

Note: Supply voltage on any pin should never exceed 4.0 V.



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

2.5 Terminology

2.5.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined, for example, by applying a 1 *g* acceleration to it. As the sensor can measure DC accelerations, this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, a ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and also over time. The sensitivity tolerance describes the range of sensitivity of a large population of sensors.

2.5.2 Zero-*g* level

Zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady-state on a horizontal surface measures 0 *g* on the X-axis and 0 *g* on the Y-axis, whereas the Z-axis measures 1 *g*. The output is ideally in the center of the dynamic range of the sensor (the content of the OUT registers is 00h, data expressed as 2's complement number). A deviation from the ideal value in this case is called zero-*g* offset. Offset is, to some extent, a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-*g* level change vs. temperature" in *Table 3*. The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a population of sensors.

2.5.3 Self-test

Self-test allows the sensor functionality to be tested without moving it. The self-test function is off when the self-test bit (ST) of CTRL_REG4 (control register 4) is programmed to '0'. When the self-test bit of CTRL_REG4 is programmed to '1', an actuation force is applied to the sensor, simulating a definite input acceleration. In this case, the sensor outputs exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity.

When the self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test force. If the output signals change within the amplitude specified in *Table 3*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

2.5.4 Sleep-to-wakeup

The "sleep-to-wakeup" function, in conjunction with low-power mode, allows further reduction of system power consumption and development of new smart applications. The IIS328DQ may be set to a low-power operating mode, characterized by lower data rate refresh. In this way the device, even if sleeping, continues to sense acceleration and to generate interrupt requests.

When the "sleep-to-wakeup" function is activated, the IIS328DQ is able to automatically wake up as soon as the interrupt event has been detected, increasing the output data rate and bandwidth.

With this feature, the system may be efficiently switched from low-power mode to full-performance depending on user-selectable positioning and acceleration events, therefore ensuring power saving and flexibility.

3 Functionality

The IIS328DQ is a “nano”, low-power, digital output 3-axis linear accelerometer packaged in a QFPN package. The device includes a sensing element and an IC interface capable of taking information from the sensing element and providing a signal to external applications through an I²C/SPI serial interface.

3.1 Sensing element

A proprietary process is used to create a surface micromachined accelerometer. The technology makes it possible to construct suspended silicon structures which are attached to the substrate at several points called “anchors”, and are free to move in the direction of the sensed acceleration. To be compatible with traditional packaging techniques, a cap is placed on top of the sensing element to prevent blocking of moving parts during the molding phase of the plastic encapsulation.

When an acceleration is applied to the sensor, the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the capacitor.

At steady-state, the nominal value of the capacitors are a few pF, and when an acceleration is applied the maximum variation of the capacitive load is in the fF range.

3.2 IC interface

The complete measurement chain is composed of a low-noise capacitive amplifier which converts the capacitive unbalancing of the MEMS sensor into an analog voltage that is made available to the user through an analog-to-digital converter.

The acceleration data may be accessed through an I²C/SPI interface, therefore making the device particularly suitable for direct interfacing with a microcontroller.

The IIS328DQ features a data-ready signal (RDY) which indicates when a new set of measured acceleration data is available, therefore simplifying data synchronization in the digital system that uses the device.

The IIS328DQ may also be configured to generate an inertial wakeup and free-fall interrupt signal based on a programmed acceleration event along the enabled axes. Both free-fall and wakeup can be available simultaneously on two different pins.

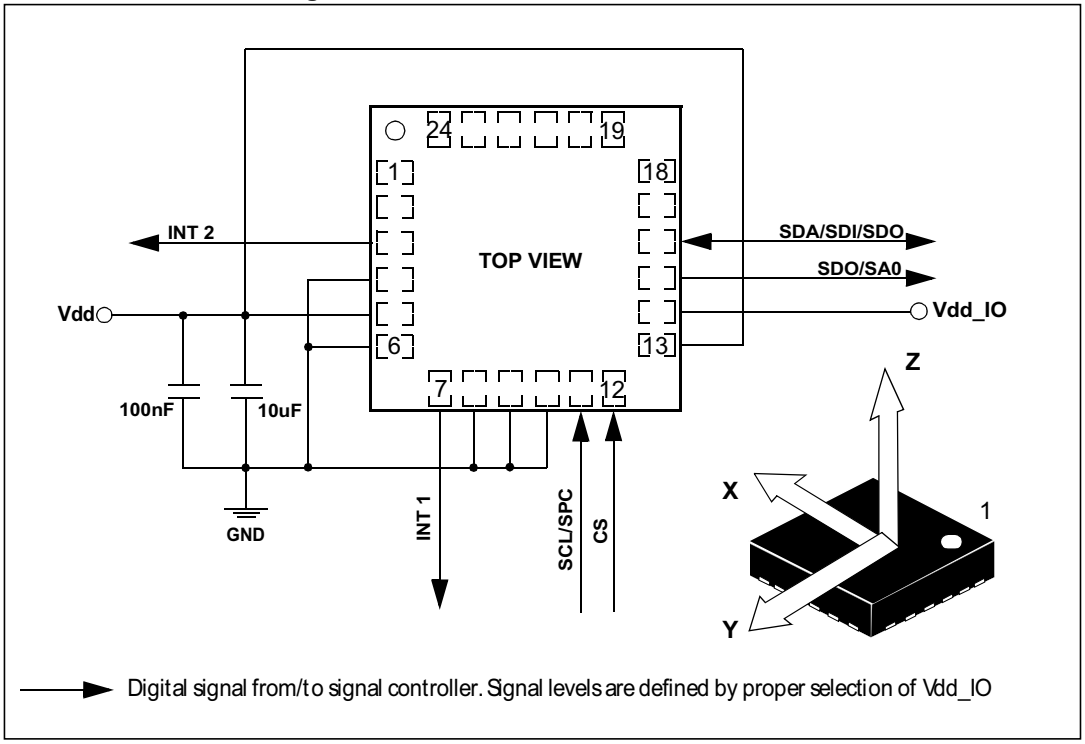
3.3 Factory calibration

The IC interface is factory calibrated for sensitivity (So) and zero-*g* level (TyOff).

The trimming values are stored inside the device in non-volatile memory. When the device is turned on, the trimming parameters are downloaded into the registers to be used during active operation. This allows the device to be used without further calibration.

4 Application hints

Figure 5. IIS328DQ electrical connections



The device core is supplied through the Vdd line while the I/O pads are supplied through the Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to pin 5 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to obtain proper behavior of the IC (refer to *Figure 5*). It is possible to remove Vdd while maintaining Vdd_IO without blocking the communication bus; in this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data is selectable and accessible through the I²C or SPI interfaces. When using the I²C, CS must be tied high.

The functions, the threshold, and the timing of the two interrupt pins (INT 1 and INT 2) can be completely programmed by the user through the I²C/SPI interface.

5 Digital interfaces

The registers embedded in the IIS328DQ may be accessed through both the I²C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped to the same pads. To select/exploit the I²C interface, the CS line must be tied high (i.e. connected to Vdd_IO).

Table 8. Serial interface pin description

Pin name	Pin description
CS	SPI enable I²C/SPI mode selection (1: I²C mode; 0: SPI enabled)
SCL SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDO	I²C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SA0 SDO	I²C less significant bit of the device address (SA0) SPI serial data output (SDO)

5.1 I²C serial interface

The IIS328DQ I²C is a bus slave. The I²C is employed to write data into registers, the content of which can also be read back.

The relevant I²C terminology is provided in *Table 9* below.

Table 9. I²C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving data to/from the interface. Both lines are connected to Vdd_IO through a pull-up resistor embedded in the IIS328DQ. When the bus is free, both lines are high.

The I²C interface is compliant with fast mode (400 kHz) I²C standards as well as with the normal mode.

5.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the IIS328DQ is 001100xb. The **SDO**/**SA0** pad can be used to modify the less significant bit of the device address. If the SA0 pad is connected to voltage supply, LSb is ‘1’ (address 0011001b), otherwise if the SA0 pad is connected to ground, the LSb value is ‘0’ (address 0011000b). This solution permits the connection and addressing of two different accelerometers to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded in the IIS328DQ behaves like a slave device, and the following protocol must be adhered to. After the start condition (ST) a slave address is sent. Once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted: the 7 LSb represent the actual register address while the MSb enables address auto-increment. If the MSb of the SUB field is ‘1’, the SUB (register address) is automatically increased to allow multiple data read/write.

The slave address is completed with a read/write bit. If the bit is ‘1’ (read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is ‘0’ (write) the master transmits to the slave with direction unchanged. *Table 10* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 10. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	001100	0	1	00110001 (31h)
Write	001100	0	0	00110000 (30h)
Read	001100	1	1	00110011 (33h)
Write	001100	1	0	00110010 (32h)

Table 11. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 12. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 13. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 14. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver cannot receive another complete byte of data until it has performed some other function, it can hold the clock line SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW-to-HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of the first register to be read.

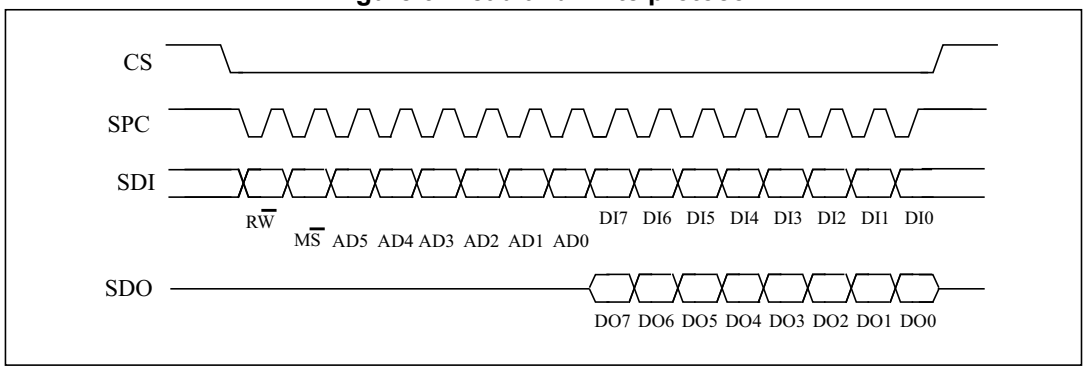
In the communication format presented, MAK is master acknowledge and NMAK is no master acknowledge.

5.2 SPI bus interface

The IIS328DQ SPI is a bus slave. The SPI allows writing to and reading from the registers of the device.

The serial interface interacts with the outside world through 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 6. Read and write protocol



CS is the serial port enable and is controlled by the SPI master. It goes low at the start of the transmission and returns high at the end. **SPC** is the serial port clock and is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are, respectively, the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in cases of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC**, after the falling edge of **CS,** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC, just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives **SDO** at the start of bit 8.

bit 1: M$\overline{S}$ bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address is auto-incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written to the device (MSb first).

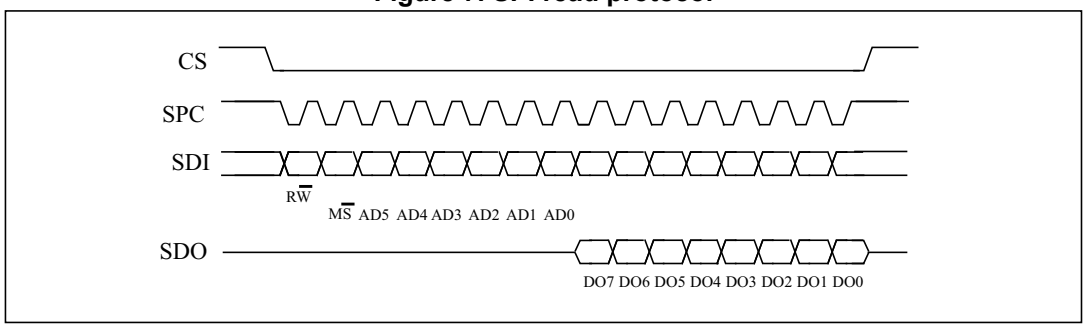
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods are added. When the M$\overline{S}$ bit is ‘0’, the address used to read/write data remains the same for every block. When the M$\overline{S}$ bit is ‘1’, the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

5.2.1 SPI read

Figure 7. SPI read protocol



The SPI read command is performed with 16 clock pulses. Multiple byte read commands are performed by adding blocks of 8 clock pulses to the previous one.

bit 0: READ bit. The value is 1.

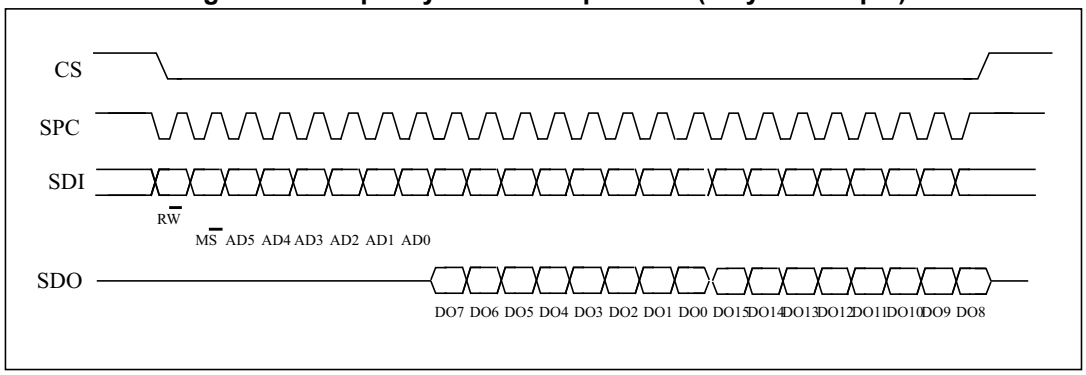
bit 1: M$\overline{S}$ bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

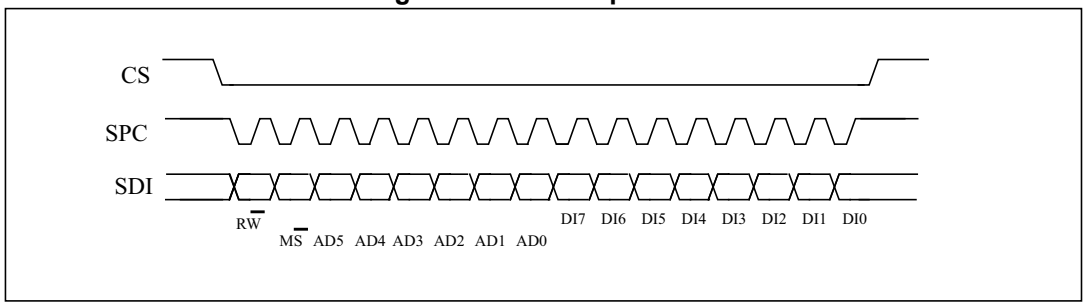
bit 16-... : data DO(...-8). Further data in multiple byte reads.

Figure 8. Multiple byte SPI read protocol (2-byte example)



5.2.2 SPI write

Figure 9. SPI write protocol



The SPI write command is performed with 16 clock pulses. Multiple byte write commands are performed by adding blocks of 8 clock pulses to the previous one.

bit 0: WRITE bit. The value is 0.

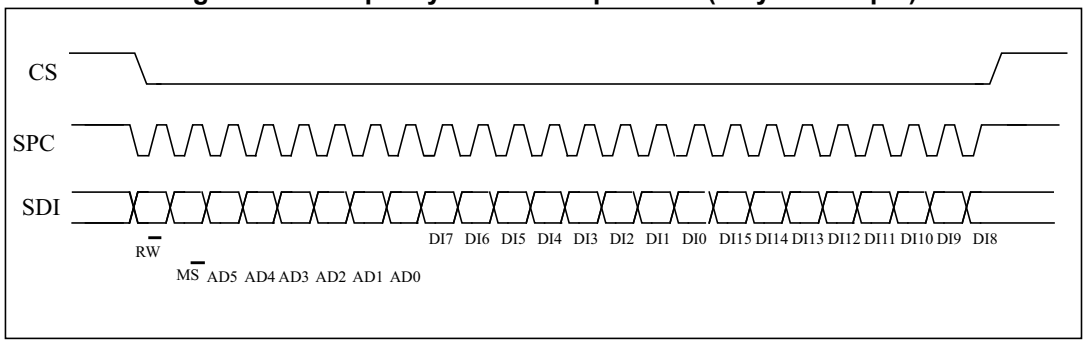
bit 1: MS bit. When 0, does not increment the address; when 1, increments the address in multiple writes.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written to the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writes.

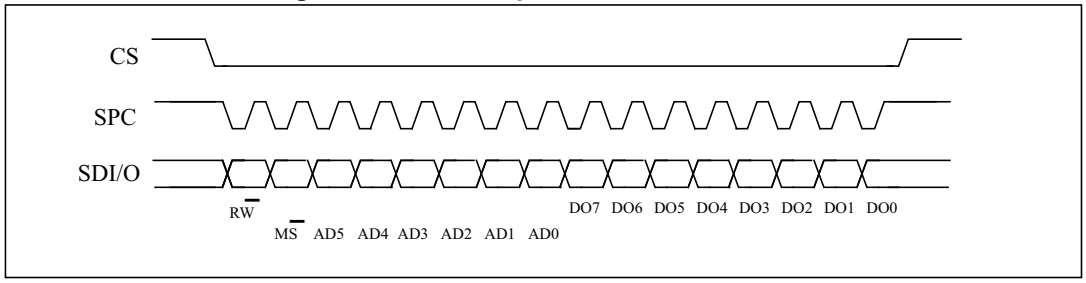
Figure 10. Multiple byte SPI write protocol (2-byte example)



5.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the SIM bit to ‘1’ (SPI serial interface mode selection) in CTRL_REG4.

Figure 11. SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: M$\overline{S}$ bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

Note: If the IIS328DQ is used in a multi-SPI slave environment (several devices sharing the same SPI bus), the accelerometer can be forced by software to remain in SPI mode. This objective can be achieved by sending at the beginning of the SPI communication the following sequence to the device:

a = read(0x17)

write(0x17, (0x80 OR a))

In this way, CTRL_REG4 is programmed to enhance the robustness of the SPI.

6 Register mapping

Table 15 below provides a list of the 8-bit registers embedded in the device, and the corresponding addresses.

Table 15. Register address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
Reserved (do not modify)		00 - 0E			Reserved
WHO_AM_I	r	0F	000 1111	00110010	Dummy register
Reserved (do not modify)		10 - 1F			Reserved
CTRL_REG1	rw	20	010 0000	00000111	
CTRL_REG2	rw	21	010 0001	00000000	
CTRL_REG3	rw	22	010 0010	00000000	
CTRL_REG4	rw	23	010 0011	00000000	
CTRL_REG5	rw	24	010 0100	00000000	
HP_FILTER_RESET	r	25	010 0101		Dummy register
REFERENCE	rw	26	010 0110	00000000	
STATUS_REG	r	27	010 0111	00000000	
OUT_X_L	r	28	010 1000	output	
OUT_X_H	r	29	010 1001	output	
OUT_Y_L	r	2A	010 1010	output	
OUT_Y_H	r	2B	010 1011	output	
OUT_Z_L	r	2C	010 1100	output	
OUT_Z_H	r	2D	010 1101	output	
Reserved (do not modify)		2E - 2F			Reserved
INT1_CFG	rw	30	011 0000	00000000	
INT1_SRC	r	31	011 0001	00000000	
INT1_THS	rw	32	011 0010	00000000	
INT1_DURATION	rw	33	011 0011	00000000	
INT2_CFG	rw	34	011 0100	00000000	
INT2_SRC	r	35	011 0101	00000000	
INT2_THS	rw	36	011 0110	00000000	
INT2_DURATION	rw	37	011 0111	00000000	
Reserved (do not modify)		38 - 3F			Reserved

Registers marked as *Reserved* must not be changed. Writing to those registers may change calibration data and therefore lead to device malfunction.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibrated values. Their content is automatically restored when the device is powered up.

7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve acceleration data. The register addresses, composed of 7 bits, are used to identify the device and to write the data through the serial interface.

7.1 WHO_AM_I (0Fh)

Table 16. WHO_AM_I register

0	0	1	1	0	0	1	0

This is the device identification register. This register contains the device identifier, which for the IIS328DQ is set to 32h.

7.2 CTRL_REG1 (20h)

Table 17. CTRL_REG1 register

PM2	PM1	PM0	DR1	DR0	Zen	Yen	Xen

Table 18. CTRL_REG1 description

PM2 - PM0	Power mode selection. Default value: 000 (000: power-down; Others: refer to *Table 19*)
DR1, DR0	Data rate selection. Default value: 00 (00: 50 Hz; Others: refer to *Table 20*)
Zen	Z-axis enable. Default value: 1 (0: Z-axis disabled; 1: Z-axis enabled)
Yen	Y-axis enable. Default value: 1 (0: Y-axis disabled; 1: Y-axis enabled)
Xen	X-axis enable. Default value: 1 (0: X-axis disabled; 1: X-axis enabled)

The **PM** bits allow selection between power-down and two active operating modes. The device is in power-down mode when the PD bits are set to “000” (default value after boot). *Table 19* shows all the possible power mode configurations and respective output data rates. Output data in the low-power modes are computed with the low-pass filter cutoff frequency defined by the DR1 and DR0 bits.

The **DR** bits, in normal-mode operation, select the data rate at which acceleration samples are produced. In low-power mode they define the output data resolution. *Table 20* shows all the possible configurations for the DR1 and DR0 bits.

Table 19. Power mode and low-power output data rate configurations

PM2	PM1	PM0	Power mode selection	Output data rate [Hz] ODR_{LP}
0	0	0	Power-down	--
0	0	1	Normal mode	ODR
0	1	0	Low-power	0.5
0	1	1	Low-power	1
1	0	0	Low-power	2
1	0	1	Low-power	5
1	1	0	Low-power	10

Table 20. Normal-mode output data rate configurations and low-pass cutoff frequencies

DR1	DR0	Output data rate [Hz] ODR	Low-pass filter cutoff frequency [Hz]
0	0	50	37
0	1	100	74
1	0	400	292
1	1	1000	780

7.3 CTRL_REG2 (21h)

Table 21. CTRL_REG2 register

BOOT	HPM1	HPM0	FDS	HPen2	HPen1	HPCF1	HPCF0

Table 22. CTRL_REG2 description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
HPM1, HPM0	High-pass filter mode selection. Default value: 00 (00: normal mode; Others: refer to *Table 23*)
FDS	Filtered data selection. Default value: 0 (0: internal filter bypassed; 1: data from internal filter sent to output register)
HPen2	High-pass filter enable for interrupt 2 source. Default value: 0 (0: filter bypassed; 1: filter enabled)
HPen1	High-pass filter enable for interrupt 1 source. Default value: 0 (0: filter bypassed; 1: filter enabled)
HPCF1, HPCF0	High-pass filter cutoff frequency configuration. Default value: 00 (00: HPc=8; 01: HPc=16; 10: HPc=32; 11: HPc=64)

The **BOOT** bit is used to refresh the content of internal registers stored in the Flash memory block. At device power-up, the content of the Flash memory block is transferred to the internal registers related to the trimming functions, to permit correct behavior of the device. If for any reason the content of the trimming register is changed, this bit can be used to restore the correct values. When the BOOT bit is set to '1' the content of the internal Flash is copied to the corresponding internal registers and is used to calibrate the device. These values are factory-trimmed and they are different for every accelerometer. They permit correct behavior of the device and normally do not need to be modified. At the end of the boot process, the BOOT bit is again set to '0'.

Table 23. High-pass filter mode configuration

HPM1	HPM0	High-pass filter mode
0	0	Normal mode (reset by reading HP_RESET_FILTER)
0	1	Reference signal for filtering
1	0	Normal mode (reset by reading HP_RESET_FILTER)

HPCF[1:0]. These bits are used to configure the high-pass filter cutoff frequency f_t which is given by:

$$f_t = \ln\left(1 - \frac{1}{HPc}\right) \cdot \frac{f_s}{2\pi}$$

The equation can be simplified to the following approximated equation:

$$f_t = \frac{f_s}{6 \cdot HPc}$$

Table 24. High-pass filter cutoff frequency configuration

HPcoeff2,1	f_t [Hz] Data rate = 50 Hz	f_t [Hz] Data rate = 100 Hz	f_t [Hz] Data rate = 400 Hz	f_t [Hz] Data rate = 1000 Hz
00	1	2	8	20
01	0.5	1	4	10
10	0.25	0.5	2	5
11	0.125	0.25	1	2.5

7.4 CTRL_REG3 [interrupt CTRL register] (22h)

Table 25. CTRL_REG3 register

IHL	PP_OD	LIR2	I2_CFG1	I2_CFG0	LIR1	I1_CFG1	I1_CFG0

Table 26. CTRL_REG3 description

IHL	Interrupt active-high/low. Default value: 0 (0: active high; 1: active low)
PP_OD	Push-pull/open-drain selection on interrupt pad. Default value 0 (0: push-pull; 1: open drain)
LIR2	Latch interrupt request on the INT2_SRC register, with the INT2_SRC register cleared by reading INT2_SRC itself. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)
I2_CFG1, I2_CFG0	Data signal on INT 2 pad control bits. Default value: 00 (see *Table 27*)
LIR1	Latch interrupt request on the INT1_SRC register, with the INT1_SRC register cleared by reading the INT1_SRC register. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)
I1_CFG1, I1_CFG0	Data signal on INT 1 pad control bits. Default value: 00 (see *Table 27*)

Table 27. Data signal on INT 1 and INT 2 pad

I1(2)_CFG1	I1(2)_CFG0	INT 1(2) Pad
0	0	Interrupt 1 (2) source
0	1	Interrupt 1 source OR interrupt 2 source
1	0	Data ready
1	1	Boot running

7.5 CTRL_REG4 (23h)

Table 28. CTRL_REG4 register

BDU	BLE	FS1	FS0	STsign	0	ST	SIM

Table 29. CTRL_REG4 description

BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated between reading MSb and LSb)
BLE	Big/little endian data selection. Default value 0 (0: data LSb @ lower address; 1: data MSb @ lower address)
FS1, FS0	Full-scale selection. Default value: 00 (00: ±2 *g*; 01: ±4 *g*; 11: ±8 *g*)
STsign	Self-test sign. Default value: 00 (0: self-test plus; 1 self-test minus)
ST	Self-test enable. Default value: 0 (0: self-test disabled; 1: self-test enabled)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)

The **BDU** bit is used to inhibit the output register update until both upper and lower register parts are read. In default mode (BDU = '0'), the lower and upper register parts are updated continuously. When the BDU is activated (BDU = 1), the content of the output registers is not updated until both MSb and LSb are read which avoids reading values related to different sample times.

7.6 CTRL_REG5 (24h)

Table 30. CTRL_REG5 register

0	0	0	0	0	0	TurnOn1	TurnOn0

Table 31. CTRL_REG5 description

TurnOn1, TurnOn0	Turn-on mode selection for sleep-to-wake function. Default value: 00

The **TurnOn** bits are used for turning on the **sleep-to-wake** function.

Table 32. Sleep-to-wake configuration

TurnOn1	TurnOn0	Sleep-to-wake status
0	0	Sleep-to-wake function is disabled
1	1	Turned on: the device is in low-power mode (ODR is defined in CTRL_REG1)

By setting TurnOn[1:0] bits to 11, the "sleep-to-wake" function is enabled. When an interrupt event occurs, the device is switched to normal mode, increasing the ODR to the value defined in CTRL_REG1. Although the device is in normal mode, the CTRL_REG1 content is not automatically changed to "normal mode" configuration.

7.7 HP_FILTER_RESET (25h)

Dummy register. Reading at this address instantaneously zeroes the content of the internal high-pass filter. If the high-pass filter is enabled, all three axes are instantaneously set to 0 *g*. This makes it possible to nullify the settling time of the high-pass filter.

7.8 REFERENCE (26h)

Table 33. REFERENCE register

Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0

Table 34. REFERENCE description

Ref7 - Ref0	Reference value for high-pass filter. Default value: 00h

This register sets the acceleration value taken as a reference for the high-pass filter output.

When the filter is turned on (at least one FDS, HPen2, or HPen1 bit is equal to ‘1’) and HPM bits are set to “01”, filter output is generated, taking this value as a reference.

7.9 STATUS_REG (27h)

Table 35. STATUS_REG register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 36. STATUS_REG description

ZYXOR	X-, Y- and Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous set before it was read)
ZOR	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)
YOR	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XOR	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)
ZYXDA	X-, Y- and Z-axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z-axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y-axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available)
XDA	X-axis new data available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available)

7.10 OUT_X_L (28h), OUT_X_H (29)

X-axis acceleration data. The value is expressed as 2’s complement.

7.11 OUT_Y_L (2Ah), OUT_Y_H (2Bh)

Y-axis acceleration data. The value is expressed as 2’s complement.

7.12 OUT_Z_L (2Ch), OUT_Z_H (2Dh)

Z-axis acceleration data. The value is expressed as 2's complement.

7.13 INT1_CFG (30h)

Table 37. INT1_CFG register

AOI	6D	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 38. INT1_CFG description

AOI	AND/OR combination of interrupt events. Default value: 0 (See *Table 39*)
6D	6-direction detection function enable. Default value: 0 (See *Table 39*)
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
ZLIE	Enable interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)

Configuration register for interrupt 1 source.

Table 39. Interrupt 1 source configurations

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6-direction movement recognition
1	0	AND combination of interrupt events
1	1	6-direction position recognition

7.14 INT1_SRC (31h)

Table 40. INT1_SRC register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 41. INT1_SRC description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Interrupt 1 source register. Read-only register.

Reading at this address clears the INT1_SRC IA bit (and the interrupt signal on the INT 1 pin) and allows the refresh of data in the INT1_SRC register if the latched option was chosen.

7.15 INT1_THS(32h)

Table 42. INT1_THS register

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 43. INT1_THS description

THS6 - THS0	Interrupt 1 threshold. Default value: 000 0000

7.16 INT1_DURATION (33h)

Table 44. INT1_DURATION register

0	D6	D5	D4	D3	D2	D1	D0

Table 45. INT2_DURATION description

D6 - D0	Duration value. Default value: 000 0000

The **D6 - D0** bits set the minimum duration of the interrupt 2 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

7.17 INT2_CFG (34h)

Table 46. INT2_CFG register

AOI	6D	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 47. INT2_CFG description

AOI	AND/OR combination of interrupt events. Default value: 0 (see *Table 48*)
6D	6-direction detection function enable. Default value: 0 (see *Table 48*)
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
ZLIE	Enable interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)

Configuration register for interrupt 2 source.

Table 48. Interrupt mode configuration

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6-direction movement recognition
1	0	AND combination of interrupt events
1	1	6-direction position recognition

7.18 INT2_SRC (35h)

Table 49. INT2_SRC register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 50. INT2_SRC description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X Low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Interrupt 2 source register. Read-only register.

Reading at this address clears the INT2_SRC IA bit (and the interrupt signal on the INT 2 pin) and allows the refresh of data in the INT2_SRC register if the latched option was chosen.

7.19 INT2_THS (36h)

Table 51. INT2_THS register

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 52. INT2_THS description

THS6 - THS0	Interrupt 1 threshold. Default value: 000 0000

7.20 INT2_DURATION (37h)

Table 53. INT2_DURATION register

0	D6	D5	D4	D3	D2	D1	D0

Table 54. INT2_DURATION description

D6 - D0	Duration value. Default value: 000 0000

The **D6 - D0** bits set the minimum duration of the interrupt 2 event to be recognized. Duration time steps and maximum values depend on the ODR chosen.

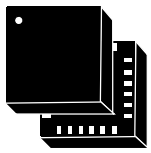
8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

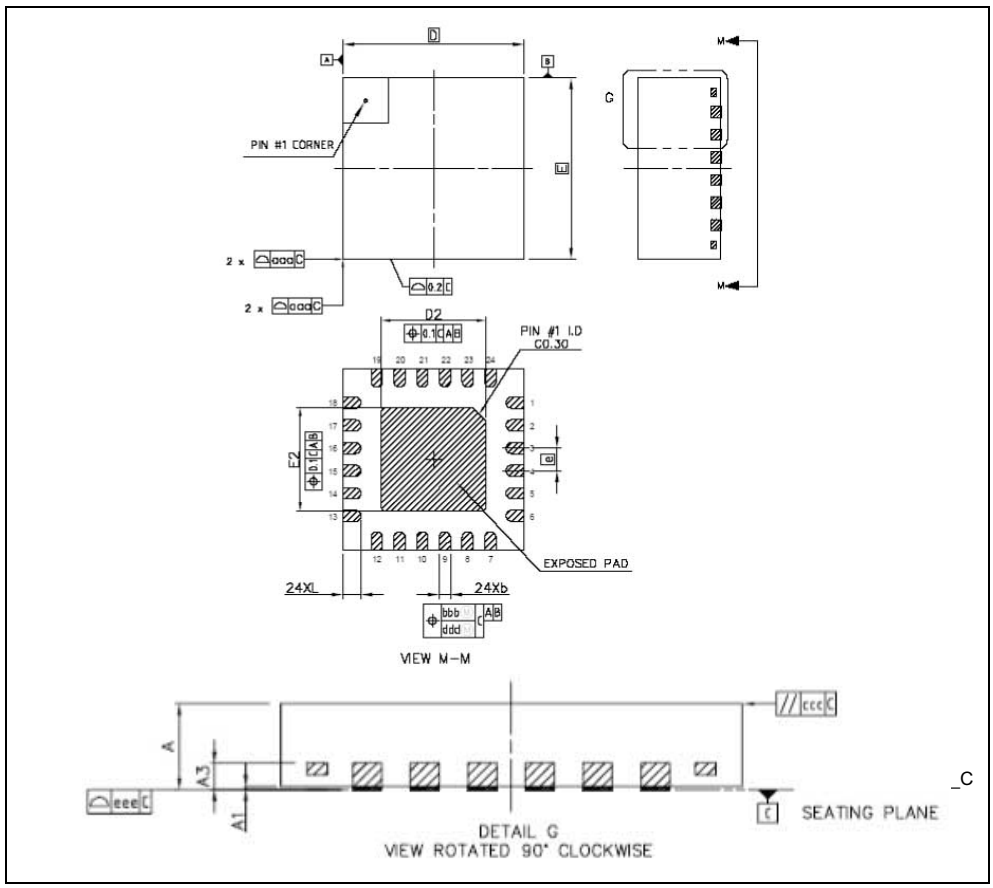
Figure 12. QFPN 4x4x1.8mm^3, 24L: mechanical data and package dimensions

Dim.	mm		
	Min.	Typ.	Max.
A	1.75	1.80	1.85
A1	0.00		0.05
A3		0.203 ref	
b	0.20	0.25	0.30
D		4.00 bsc	
D2	2.20	2.30	2.40
E		4.00 bsc	
E2	2.20	2.30	2.40
e		0.50 bsc	
L	0.35	0.40	0.45
aaa		0.10	
eee		0.08	

Outline and mechanical data



QFPN-24 (4x4x1.8 mm^3)
Quad Flat Package No lead



9 Soldering information

The QFPN-24 package is compliant with the ECOPACK®, RoHS and “Green” standard. It is qualified for soldering heat resistance according to JEDEC J-STD-020C, in MSL3 conditions.

For complete land pattern and soldering recommendations, please refer to the technical note TN0019 available on www.st.com.

9.1 General guidelines for soldering surface-mount accelerometers

The following three elements must be considered in order to adhere to common PCB design and good industrial practices when soldering MEMS sensors:

1. PCB with its own conductive layers (i.e. copper) and other organic materials used for board protection and dielectric isolation.
2. ACCELEROMETER to be mounted on the board. The accelerometer senses acceleration, but it senses also the mechanical stress coming from the board. This stress is minimized with simple PCB design rules.
3. SOLDER PASTE like SnAgCu. This solder paste can be dispensed on the board with a screen printing method through a stencil. The pattern of the solder paste on the PCB is given by the stencil mask itself.

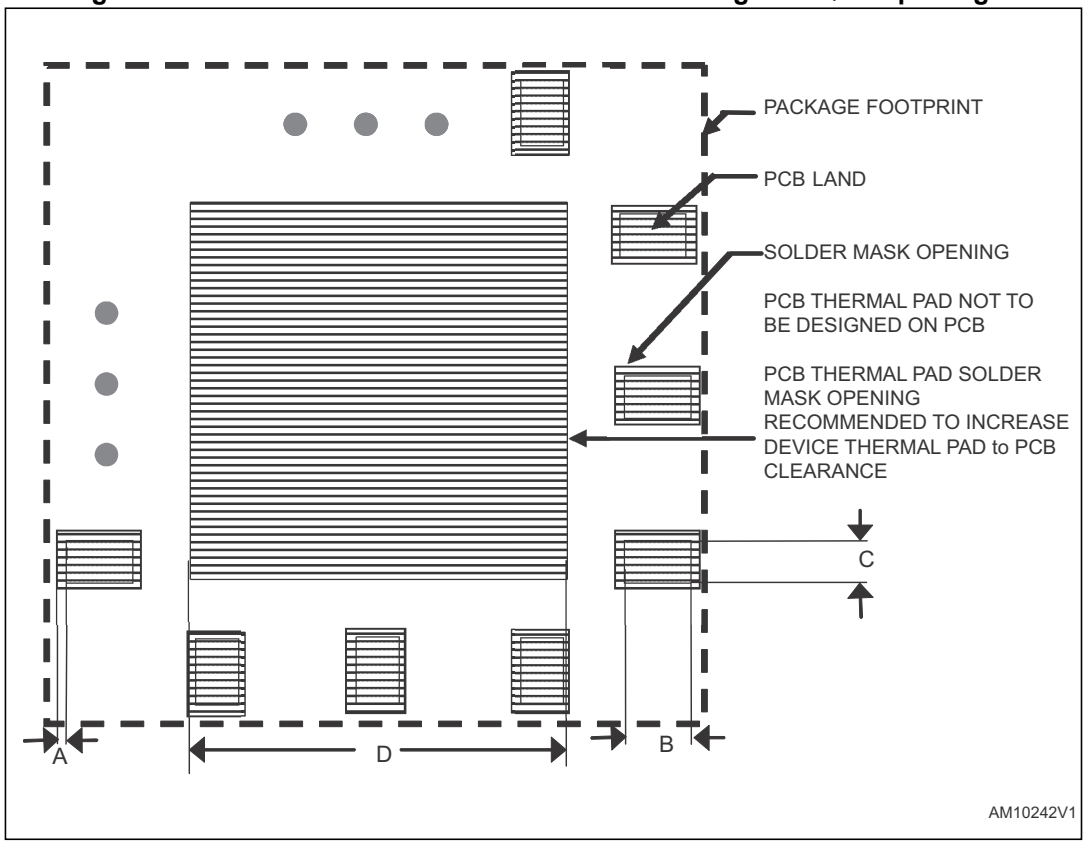
9.2 PCB design guidelines

PCB land and solder mask general recommendations are shown in *Figure 13*. Refer to *Figure 12* for specific device size, land count and pitch.

- It is recommended to open the solder mask external to the PCB land.
- It is mandatory, for correct device functionality, to ensure that some clearance is present between the accelerometer thermal pad and PCB. In order to obtain this clearance it is recommended to open the PCB thermal pad solder mask.
- The area below the sensor (on the same side of the board) must be defined as a keepout area. It is strongly recommended not to place any structure in the top metal layer underneath the sensor.
- Traces connected to pads should be as symmetrical as possible. Symmetry and balance for pad connection helps component self-alignment and leads to better control of solder paste reduction after reflow.
- For better performance over temperature it is strongly recommended not to place large insertion components like buttons or shielding boxes at distances less than 2 mm from the sensor.
- Central die pad and “Pin 1 Indicator” are physically connected to GND. Leave “Pin 1 Indicator” unconnected during soldering.

9.2.1 PCB design rules

Figure 13. Recommended land and solder mask design for QFPN packages



A = Clearance from PCB land edge to solder mask opening ≤ 0.1 mm to ensure that some solder mask remains between PCB pads

B = PCB land length = QFPN solder pad length + 0.1 mm

C = PCB land width = QFPN solder pad width + 0.1 mm

D = PCB thermal pad solder mask opening = QFPN thermal pad side + 0.2 mm

9.3 Stencil design and solder paste application

The thickness and the pattern of the solder paste are important in order to correctly mount the accelerometer on the board.

- Stainless steel stencils are recommended for solder paste application.
- A stencil thickness of 125 - 150 µm (5 - 6 mils) is recommended for screen printing
- The final thickness of the solder paste should allow proper cleaning of flux residuals and clearance between the sensor package and PCB.
- Stencil aperture should have a rectangular shape with a dimension up to 25 µm (1 mil) smaller than PCB land.
- The openings of the stencil for the signal pads should be between 50% and 80% of the PCB pad area.
- Optionally, for better solder paste release, the aperture walls should be trapezoidal and the corners rounded.
- The fine pitch of the IC leads requires accurate alignment of the stencil to the printed circuit board. The stencil and printed circuit assembly should be aligned to within 25 µm (1 mil) prior to application of the solder paste.

9.4 Process considerations

- If self-cleaning solder paste is not used, it is mandatory to properly wash the board after soldering to eliminate any possible source of leakage between adjacent pads due to flux residues.
- The PCB soldering profile depends on the number, size and placement of components on the application board. For this reason it is not possible to define a unique soldering profile for the sensor only.The user should use a time and temperature reflow profile that is derived from PCB design and manufacturing expertise.

10 Revision history

Table 55. Document revision history

Date	Revision	Changes
17-Dec-2014	1	Initial release
05-Mar-2014	2	Added Off parameter as well as min and max values for TyOff and TCOff in *Table 3: Mechanical characteristics*
21-Apr-2015	3	First public release

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