

FEATURES

- 700MHz min. shift frequency
- Extended 100E VEE range of -4.2V to -5.5V
- 8 bits wide
- Bi-directional
- Four selectable modes for full functionality
- Asynchronous Master Reset
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75K Ω input pulldown resistors
- Fully compatible with Motorola MC10E/100E141
- Pin-compatible with E241
- Available in 28-pin PLCC package

DESCRIPTION

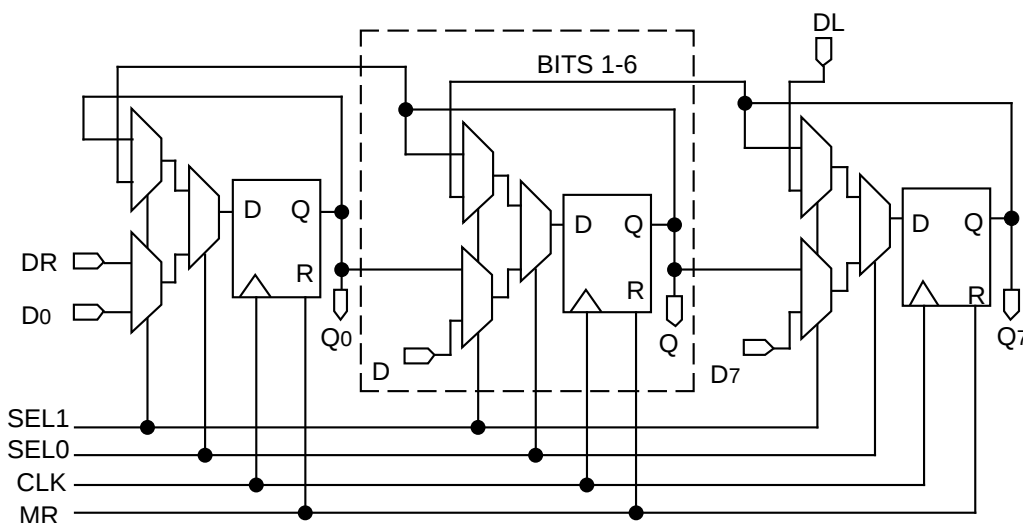
The SY10/100E141 are 8-bit, full-function shift registers designed for use in new, high-performance ECL systems. The E141 performs serial/parallel in and serial/parallel out, shifting in either direction. The eight inputs D0-D7 accept parallel input data, while DL/DR accept serial input data for left/right shifting.

The two select pins, SEL0 and SEL1 permit four modes of operation: Load, Hold, Shift Left and Shift Right, as shown in the Truth Table. Input data is clocked into the register on the rising clock edge after meeting the minimum set-up time. A logic HIGH on the Master Reset (MR) pin asynchronously resets all the registers to zero.

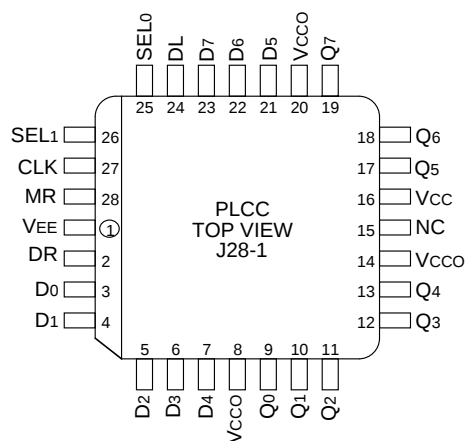
PIN NAMES

Pin	Function
D0-D7	Parallel Data Inputs
DL, DR	Serial Data Inputs
SEL0, SEL1	Mode Select Inputs
CLK	Clock
Q0-Q7	Data Outputs
MR	Master Reset
Vcco	Vcc to Output

BLOCK DIAGRAM



PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E141JC	J28-1	Commercial	SY10E141JC	Sn-Pb
SY10E141JCTR ⁽²⁾	J28-1	Commercial	SY10E141JC	Sn-Pb
SY100E141JC	J28-1	Commercial	SY100E141JC	Sn-Pb
SY100E141JCTR ⁽²⁾	J28-1	Commercial	SY100E141JC	Sn-Pb
SY10E141JY ⁽³⁾	J28-1	Industrial	SY10E141JY with Pb-Free bar-line indicator	Matte-Sn
SY10E141JYTR ^(2, 3)	J28-1	Industrial	SY10E141JY with Pb-Free bar-line indicator	Matte-Sn
SY100E141JY ⁽³⁾	J28-1	Industrial	SY100E141JY with Pb-Free bar-line indicator	Matte-Sn
SY100E141JYTR ^(2, 3)	J28-1	Industrial	SY100E141JY with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

TRUTH TABLE

Function	DL	DR	SEL0	SEL1	MR	CLK	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Load	X	X	L	L	L	Z	D0	D1	D2	D3	D4	D5	D6	D7
Shift Right	X	L	L	H	L	Z	L	Q0	Q1	Q2	Q3	Q4	Q5	Q6
	X	H	L	H	L	Z	H	L	Q0	Q1	Q2	Q3	Q4	Q5
Shift Left	L	X	H	L	L	Z	L	Q0	Q1	Q2	Q3	Q4	Q5	L
	H	X	H	L	L	Z	Q0	Q1	Q2	Q3	Q4	Q5	L	H
Hold	X	X	H	H	L	Z	Q0	Q1	Q2	Q3	Q4	Q5	L	H
	X	X	H	H	L	Z	Q0	Q1	Q2	Q3	Q4	Q5	L	H
Reset	X	X	X	X	H	X	L	L	L	L	L	L	L	L

DC ELECTRICAL CHARACTERISTICSV_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

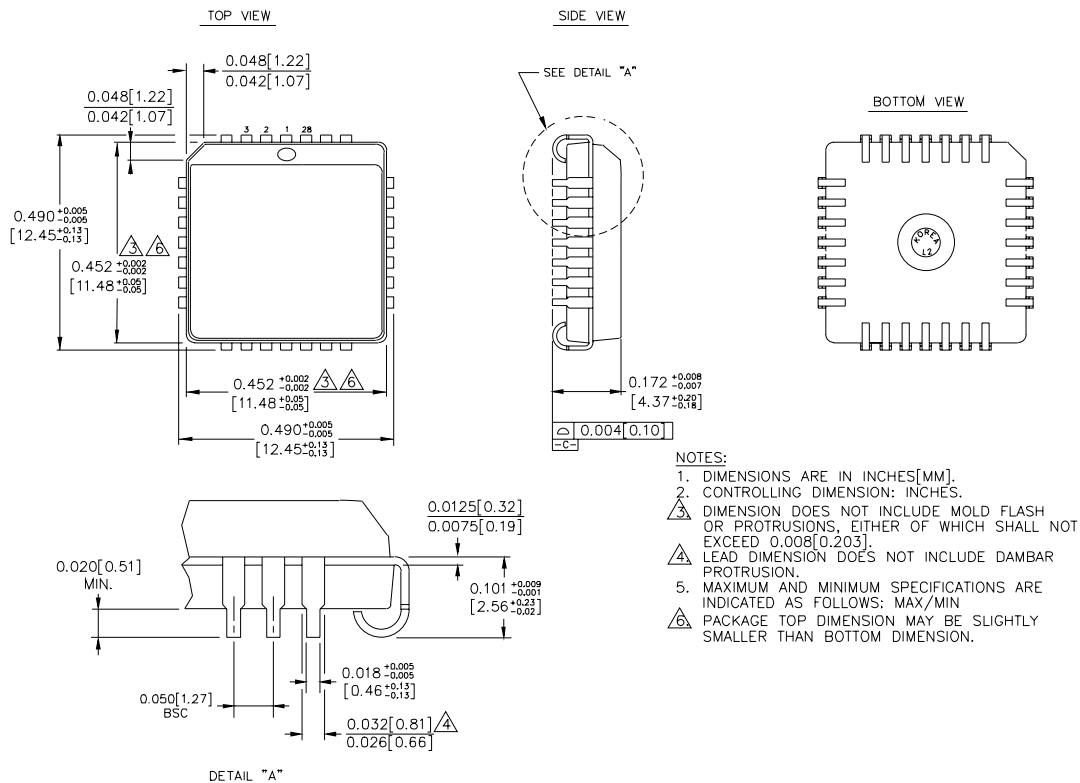
Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—
I _{EE}	Power Supply Current	—	—	—	—	—	—	—	—	—	mA	—
	10E	—	131	157	—	131	157	—	131	157		
	100E	—	131	157	—	131	157	—	151	181		

AC ELECTRICAL CHARACTERISTICSV_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f _{SHIFT}	Max. Shift Frequency	700	900	—	700	900	—	700	900	—	MHz	—
t _{PD}	Propagation Delay to Output CLK MR	625 600	750 725	975 975	625 600	750 725	975 975	625 600	750 725	975 975	ps	—
t _s	Set-up Time D SEL ₀ SEL ₁	175 350 300	25 200 150	— — —	175 350 300	25 200 150	— — —	175 350 300	25 200 150	— — —	ps	—
t _H	Hold Time D SEL ₀ SEL ₁	200 100 100	–25 –200 –150	— — —	200 100 100	–25 –200 –150	— — —	200 100 100	–25 –200 –150	— — —	ps	—
t _{RR}	Reset Recovery Time	900	700	—	900	700	—	900	700	—	ps	—
t _{PW}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t _{skew}	Within-Device Skew	—	60	—	—	60	—	—	60	—	ps	1
t _r t _f	Rise/Fall Time 20% to 80%	300	525	800	300	525	800	300	525	800	ps	—

Note:

1. Within-device skew is defined as identical transitions on similar paths through a device.

28-PIN PLCC (J28-1)

Rev. 03

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