19-2081; Rev 3; 2/07

+3.3V, 2.5Gbps Low-Power Laser Driver

General Description

The MAX3273 is a compact, low-power laser driver for applications up to 2.7Gbps. The device uses a single +3.3V supply and typically consumes 30mA. The bias and modulation current levels are programmed by external resistors. An automatic power-control (APC) loop is incorporated to maintain a constant average optical power over temperature and lifetime. The laser driver is fabricated using Maxim's in-house, second-generation SiGe process.

The MAX3273 accepts differential CML-compatible clock and data input signals. Inputs are self-biased to allow AC-coupling. An input data-retiming latch can be enabled to reject input jitter if a clock signal is available.

The driver can provide bias current up to 100mA and modulation current up to 60mA$_{P-P}$ with typical (20% to 80%) edge speeds of 59ps. A failure-monitor output is provided to indicate when the APC loop is unable to maintain average optical power. The MAX3273 is available in 4mm × 4mm, 24-pin QFN and thin QFN packages, as well as in die form.

Applications

SONET OC-48 and SDH STM-16 Transmission Systems

Add/Drop Multiplexers

Digital Cross-Connects

2.5Gbps Optical Transmitters

Pin Configurations appear at end of data sheet.

Features

- **30mA Power-Supply Current**
- **Single +3.3V Power Supply**
- **Up to 2.7Gbps (NRZ) Operation**
- **Automatic Average Power Control with Failure Monitor**
- **Programmable Modulation Current from 5mA to 60mA**
- **Programmable Bias Current from 1mA to 100mA**
- **Typical Fall Time of 59ps**
- **Selectable Data Retiming Latch**
- **Complies with ANSI, ITU, and Bellcore SDH/SONET Specifications**

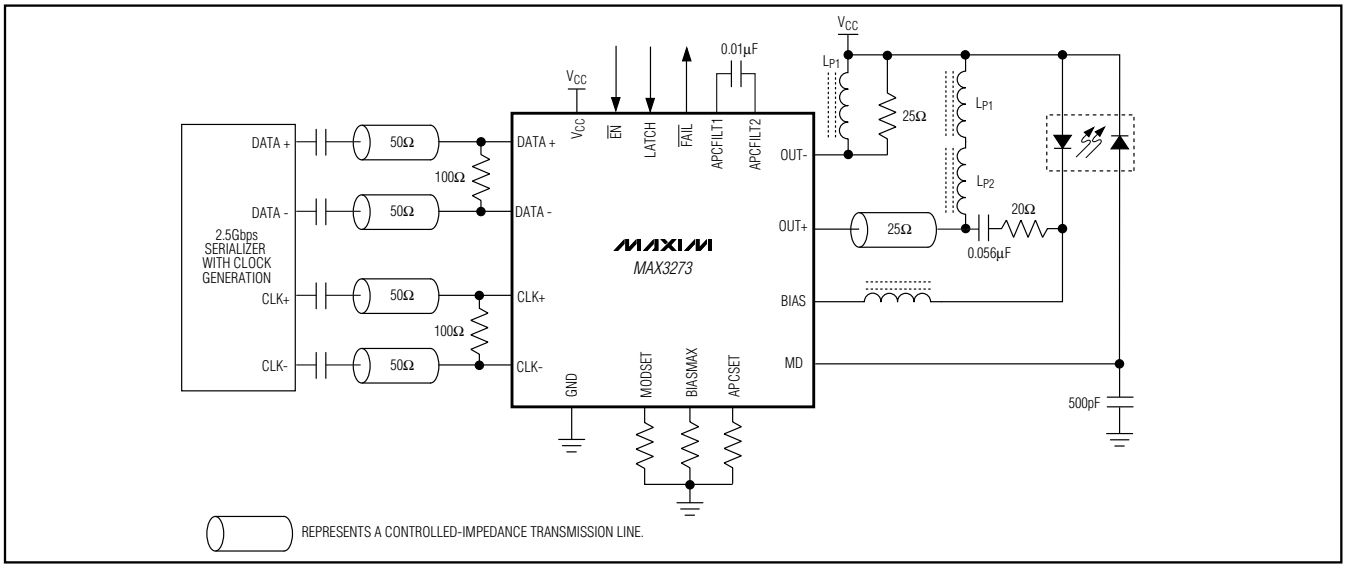
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PACKAGE CODE
MAX3273EGG	-40°C to +85°C	24 QFN (4mm × 4mm)	G2444-1
MAX3273ETG+	-40°C to +85°C	24 Thin QFN (4mm × 4mm)	T2444-2
MAX3273E/D	-40°C to +85°C	Dice*	—

**Dice are designed to operate from T_A = -40°C to +85°C, but are tested and guaranteed at T_A = +25°C only.*

+Denotes lead-free package.

Typical Application Circuit



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

+3.3V, 2.5Gbps Low-Power Laser Driver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ..... -0.5V to +6.0V
Current into BIAS, OUT+, OUT- ..... -20mA to +150mA
Current into MD ..... -5mA to +5mA
Voltage at DATA+, DATA-, CLK+, CLK-, LATCH, $\overline{EN}$, $\overline{FAIL}$ ..... -0.5V to (V_{CC} + 0.5V)
Voltage at MODSET, BIASMAX, APCSET, APCFILT1, APCFILT2 ..... -0.5V to +3.0V
Voltage at BIAS ..... +1.0V to (V_{CC} + 1.5V)
Voltage at OUT+, OUT- ..... +1.5V to (V_{CC} + 1.5V)
Current into $\overline{FAIL}$ ..... -10mA to +10mA
Continuous Power Dissipation (T_A = +85°C)
24-Pin QFN (derate 274mW/°C above +85°C) 1781mW
Storage Temperature Range ..... -55°C to +150°C
Operating Junction Temperature ..... -55°C to +150°C
Die Attach Temperature (die) ..... +400°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.14V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, I_{BIAS} = 60mA, I_{MOD} = 30mA, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	Excluding I_{BIAS} and I_{MOD}			30	45	mA
Bias-Current Range	I_{BIAS}	Voltage on BIAS pin (V_{BIAS}) = V_{CC} - 1.6V		1		100	mA
Bias Off-Current		$\overline{EN}$ = high (Note 2), $V_{BIAS} \le 2.6V$				0.2	mA
Bias-Current Stability		APC open loop (Note 3)	I_{BIAS} = 100mA		61		ppm/°C
			I_{BIAS} = 1mA		198		
Bias-Current Absolute Accuracy		APC open loop (Note 4)		-15		+15	%
Differential Input Voltage	V_{ID}	Figure 1		0.2		1.6	V_{P-P}
Common-Mode Input Voltage	V_{ICM}			V_{CC} - 1.49	V_{CC} - 1.32	V_{CC} - V_{ID}/4	V
TTL Input High Voltage	V_{IH}			2.0			V
TTL Input Low Voltage	V_{IL}					0.8	V
TTL Output High	V_{OH}	Sourcing 50µA		2.4			V
TTL Output Low	V_{OL}	Sinking 100µA				0.4	V
MD Voltage						1.6	V
Monitor Diode DC-Current Range	I_{MD}	(Note 3)		18		1000	µA
Monitor-Diode Bias Set Point Stability		I_{MD} = 1000µA		-480	83	+480	ppm/°C
		I_{MD} = 18µA		-480	159	+480	
Monitor-Diode Bias Absolute Accuracy				-15		+15	%

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.14V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, I_{BIAS} = 60mA, I_{MOD} = 30mA, T_A = +25°C, unless otherwise noted.) (Notes 5, 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Modulation-Current Range	I_{MOD}	(Note 3)	5		60	mA
Modulation Off-Current		$\overline{EN}$ = high			0.2	mA
Modulation-Current Stability		I_{MOD} = 60mA	-480	64	+480	ppm/°C
		I_{MOD} = 5mA	-480	34	+480	
Modulation-Current Absolute Accuracy		(Note 4)	-15		+15	%
Output Current Rise Time	t_R	20% to 80% (Note 7)		52	87	ps
Output Current Fall Time	t_F	20% to 80% (Note 7)		59	104	ps
Output Overshoot/Undershoot	δ	(Note 7)		15		%
Enable and Startup Delay		APC open loop		364		ns
Maximum Consecutive Identical Digits			80			bits
Pulse-Width Distortion	PWD	(Notes 7, 8)		3	45	ps
Random Jitter				1.0	1.5	ps_{RMS}
Input Latch Setup Time	T_{SU}	LATCH = high (Figure 1)		75	150	ps
Input Latch Hold Time	T_{HD}	LATCH = high (Figure 1)		0	50	ps

Note 1: Specifications at -40°C are guaranteed by design and characterization. Dice are tested at T_A= +25°C only.
Note 2: Both the bias and modulation currents are switched off if any of the current set pins is grounded.
Note 3: Guaranteed by design and characterization.
Note 4: Accuracy refers to part-to-part variation.
Note 5: AC characterization was performed by using the circuit in Figure 2.
Note 6: AC characteristics are guaranteed by design and characterization, and measured using a 2.5Gbps 2^{13} - 1 PRBS input data pattern with 80 consecutive zeros and 80 consecutive ones added.
Note 7: Measured using a 2.5Gbps repeating 0000 1111 pattern.
Note 8: PWD = (wide pulse - narrow pulse) / 2.

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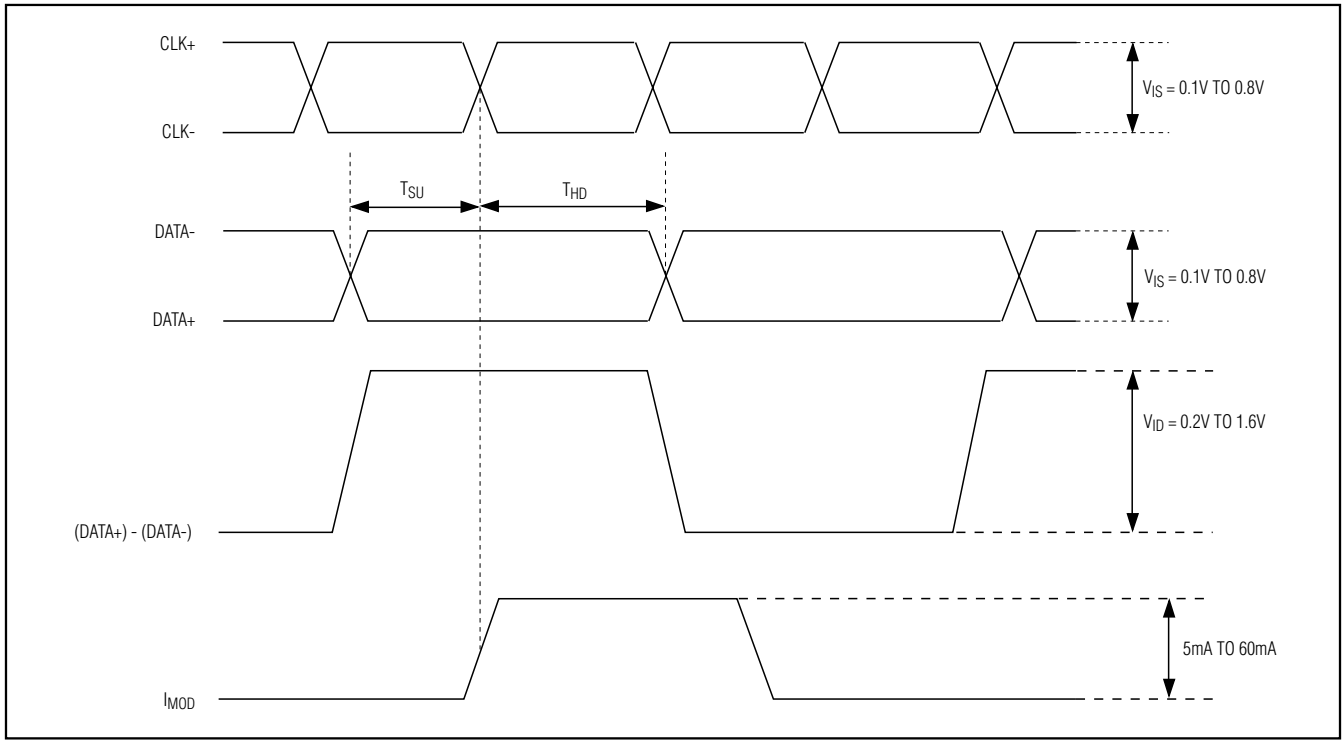


Figure 1. Required Input Signal and Setup/Hold-Time Definition

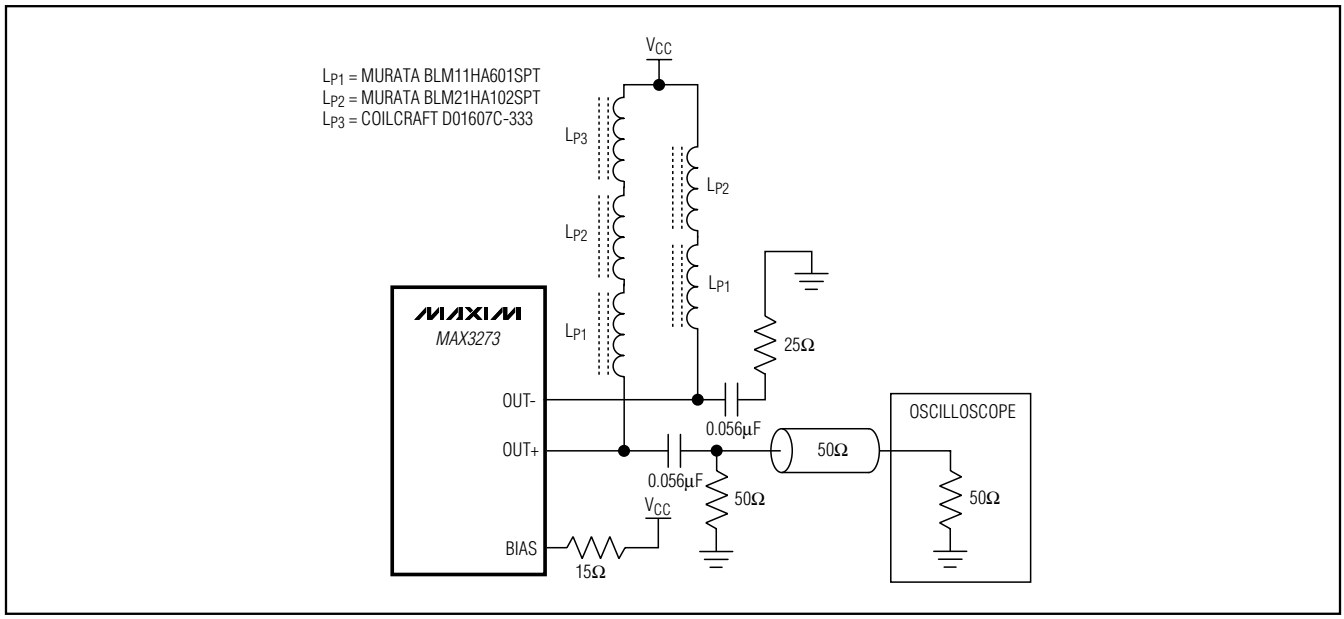
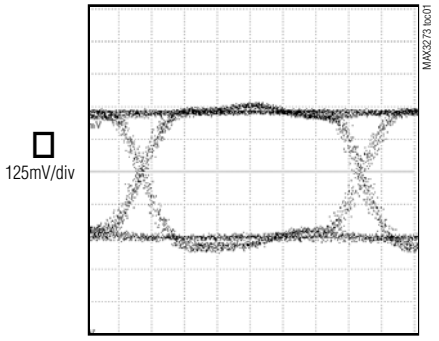


Figure 2. Output Termination for Characterization

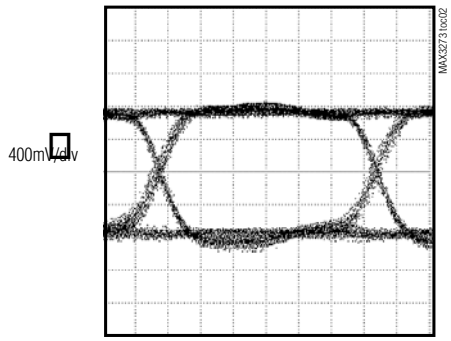
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

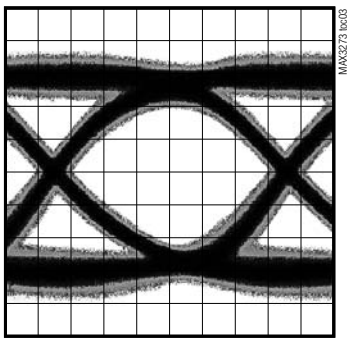
ELECTRICAL EYE DIAGRAM (I_{MOD} = 20mA, 2^{13} - 1 80CID)



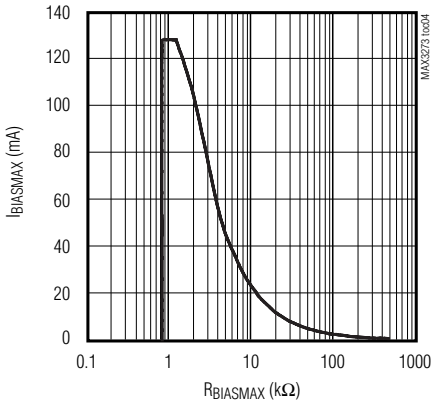
ELECTRICAL EYE DIAGRAM (I_{MOD} = 60mA, 2^{13} - 1 80CID)



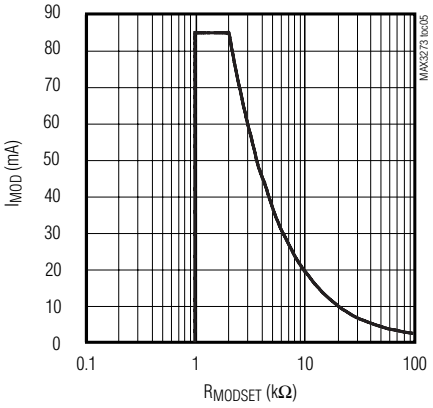
OPTICAL EYE DIAGRAM (2.488Gbps, 1300nm FP LASER, 1.87GHz FILTER)



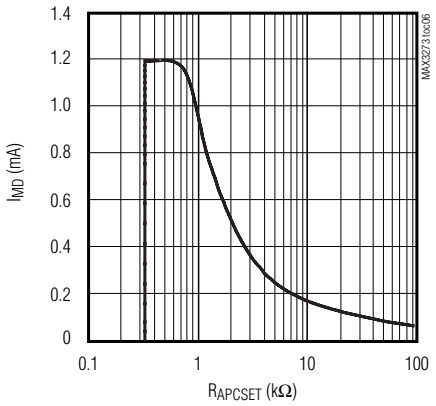
$I_{BIASMAX}$ vs. $R_{BIASMAX}$



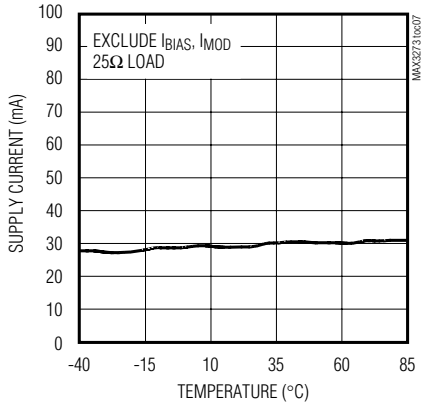
I_{MOD} vs. R_{MODSET}



I_{MD} vs. R_{APCSET}



SUPPLY CURRENT vs. TEMPERATURE

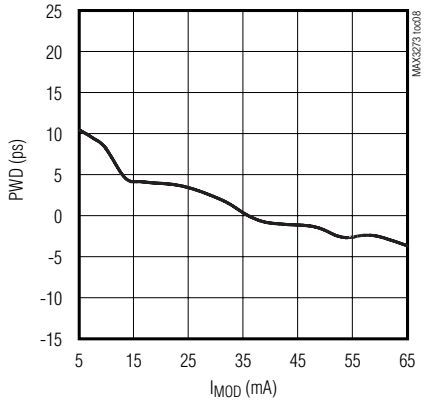


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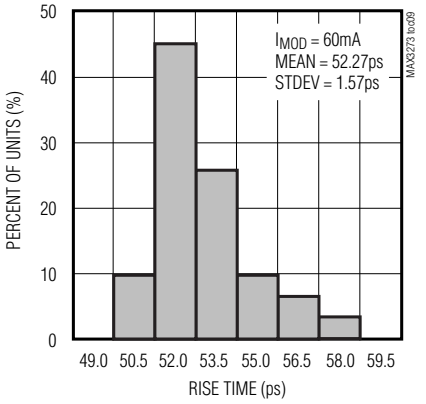
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

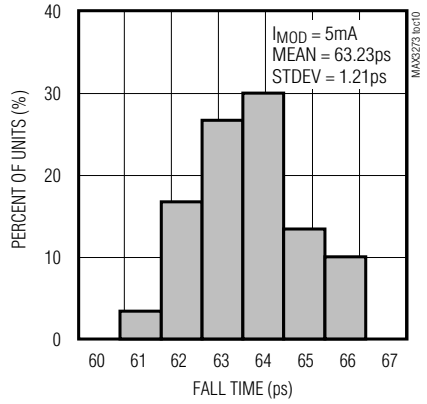
PULSE-WIDTH DISTORTION vs. I_{MOD}



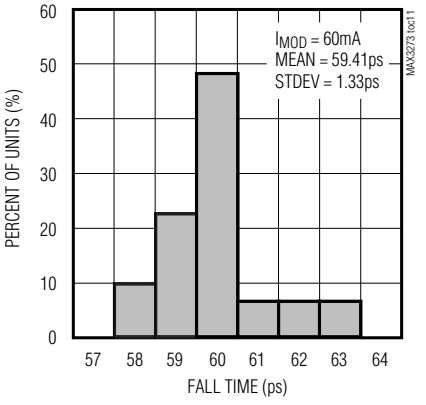
TYPICAL DISTRIBUTION OF I_{MOD} RISE TIME



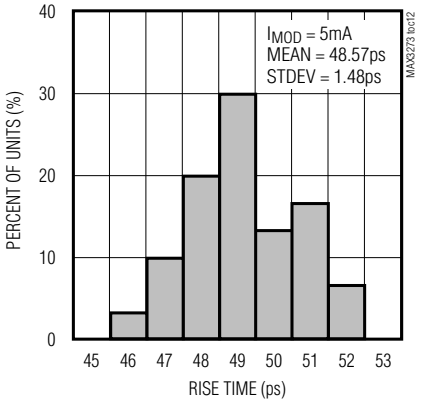
TYPICAL DISTRIBUTION OF I_{MOD} FALL TIME



TYPICAL DISTRIBUTION OF I_{MOD} FALL TIME



TYPICAL DISTRIBUTION OF I_{MOD} RISE TIME



Pin Description

PIN	NAME	FUNCTION
1, 4, 13, 15, 18	V_{CC}	Power-Supply Voltage
2	DATA+	Noninverting Data Input, with On-Chip Biasing
3	DATA-	Inverting Data Input, with On-Chip Biasing
5	CLK+	Noninverting Clock Input for Data Retiming, with On-Chip Biasing
6	CLK-	Inverting Clock Input for Data Retiming, with On-Chip Biasing
7, 9, 12	GND	Ground
8	LATCH	Data Retiming Enable Input, Active-High. Retiming disabled when floating or pulled low.
10	$\overline{EN}$	TTL/CMOS Enable Input. Low for normal operation. Float or pull high to disable laser bias and modulation currents. Internal 100kΩ pullup to V_{CC}.
11	MODSET	A resistor connected from this pin to ground sets the desired modulation current.
14	BIAS	Laser Bias Current Output. Connect to the laser through an inductor.
16	OUT+	Positive Modulation-Current Output. I_{MOD} flows into this pin when input data is high.
17	OUT-	Negative Modulation-Current Output. Current flows into this pin when input data is low. Connect to load equivalent to that on OUT+ to maintain differential output balance.
19	MD	Monitor Diode Input. Connect this pin to the anode of the monitor diode. Leave floating for open-loop operation.
20	APCFILT1	A capacitor between APCFILT1 and APCFILT2 sets the dominant pole of the APC feedback loop ($C_{APCFILT}$ = 0.01µF). Ground APCFILT1 for open-loop operation.
21	APCFILT2	See above.
22	$\overline{FAIL}$	TTL/CMOS Failure Output, Active-Low. Indicates APC failure when low.
23	APCSET	A resistor connected from this pin to ground sets the desired average optical power. Connect a 100kΩ resistor to GND for open-loop operation.
24	BIASMAX	A resistor connected from this pin to ground sets the maximum bias current. The APC function can subtract current from this maximum value, but cannot add to it. For open-loop operation, this pin sets the laser bias current.
EP	EXPOSED PAD	Ground. Solder this pad to ground.

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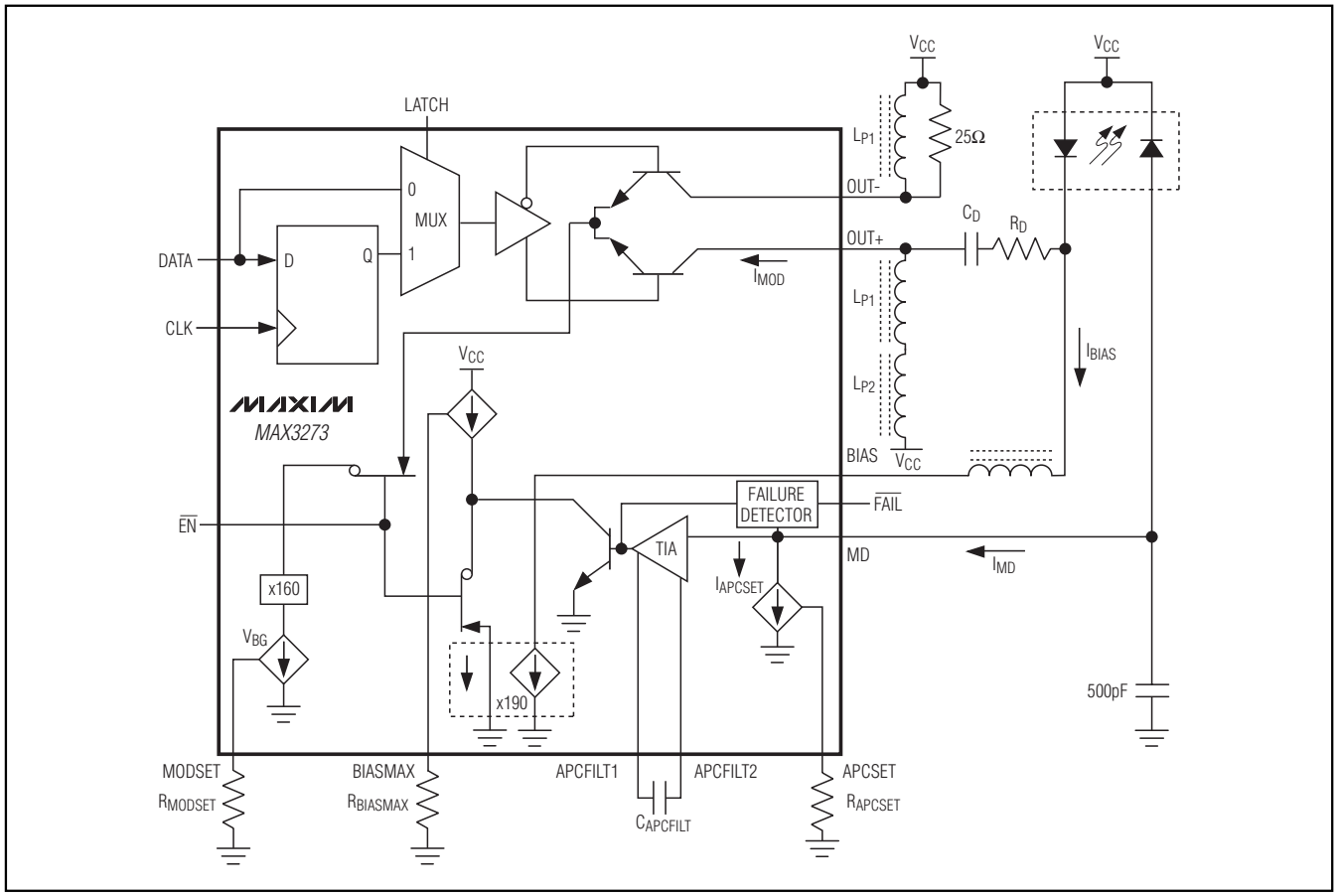


Figure 3. Functional Diagram

Detailed Description

The MAX3273 laser driver consists of two main parts: a high-speed modulation driver and a laser-biasing block with automatic power control (APC). The circuit design is optimized for both high-speed and low-voltage (+3.3V) operation. To minimize the jitter of the input signal at speeds as high as 2.7Gbps, the device accepts a differential CML clock signal for data retiming. When LATCH is high, the input data is synchronized by the clock signal. When LATCH is low, the input data is directly applied to the output stage.

The output stage is composed of a high-speed differential pair and a programmable modulation current source. Because the modulation output drives a maximum current of 60mA into the laser with an edge speed of 59ps, large transient voltage spikes can be generated (due to the parasitic inductance of the laser). These transients and the laser-forward voltage leave insufficient headroom for the proper operation of the laser driver if the modulation output is DC-coupled to the laser diode. To solve this problem, the MAX3273's modulation output is AC-coupled to the cathode of a laser diode. An external pullup inductor is necessary to DC-bias the modulation output at V_{CC}. Such a configuration isolates laser-forward voltage from the output circuitry and the supply voltage V_{CC}. A simplified functional diagram is shown in Figure 3.

The MAX3273 modulation output is optimized for driving a 25Ω load. Modulation current swings of 75mA are possible, but because of minimum power-supply and jitter requirements at 2.5Gbps, the specified maximum modulation current is limited to 60mA. To interface with the laser diode, a damping resistor (R_D) is required for impedance matching. An RC-shunt network might also be necessary to compensate for the laser-diode parasitic inductance, thereby improving the

optical output ringing and duty-cycle distortion. Refer to Maxim application note HFAN 02.0, *Interfacing Maxim Laser Drivers with Laser Diodes,* for more information.

At the data rate of 2.5Gbps, any capacitive load at the cathode of a laser diode degrades the optical output performance. Because the BIAS output is directly connected to the laser cathode, the parasitic capacitance associated with this pin is minimized by using an inductor to isolate the BIAS pin from the laser cathode.

Automatic Power Control (APC)

To maintain constant average optical power, the MAX3273 incorporates an APC loop to compensate for the changes in laser threshold current over temperature and lifetime. A back-facet photodiode mounted in the laser package is used to convert the optical power into a photocurrent. The APC loop adjusts the laser bias current so that the monitor current is matched to a reference current set by R_{APCSET}. The time constant of the APC loop is determined by an external capacitor ($C_{APCFILT}$). To minimize the pattern-dependent jitter associated with the APC loop-time constant, and to guarantee loop stability, the recommended value for $C_{APCFILT}$ is 0.01µF.

When the APC loop is functioning, the maximum allowable bias current is set by an external resistor, $R_{BIASMAX}$. An APC failure flag ($\overline{FAIL}$) is asserted low when the bias current can no longer be adjusted to achieve the desired average optical power.

APC closed-loop operation requires the user to set three currents with external resistors connected between ground and BIASMAX, MODSET, and APCSET (see Figure 3). Detailed guidelines for these resistor settings are described in the *Design Procedure* section.

Open-Loop Operation

If necessary, the MAX3273 is fully operational without APC. To disable the APC loop, ground the APCFILT1 pin. In this case, the laser current is directly set by two external resistors connected from ground to BIASMAX and MODSET. See the *Design Procedure* section for more details on open-loop operation.

Optional Data Input Latch

To minimize jitter in the input data, connect a synchronous differential clock signal to the CLK+ and CLK- inputs. When the LATCH control input is tied high, the input data is retimed on the rising edge of CLK+. If LATCH is tied low or left floating, the retiming function is disabled and the input data is directly connected to the output stage. When this latch function is not used, connect CLK+ to V_{CC} and leave CLK- unconnected.

Output Enable

The MAX3273 incorporates a TTL/CMOS input to enable the output. When $\overline{EN}$ is low, the modulation and bias outputs are enabled. When $\overline{EN}$ is high or floating, both the bias and modulation currents are off. The typical enable time is 364ns, and the typical disable time is 27ns when the bias is operated open loop.

Slow-Start

For laser safety reasons, the MAX3273 incorporates a slow-start circuit that provides a delay of 364ns for enabling a laser diode.

APC Failure Monitor

The MAX3273 provides an APC failure monitor (TTL/CMOS) to indicate an APC loop tracking failure. $\overline{FAIL}$ is asserted low when the APC loop no longer can regulate the bias current to maintain the desired monitor diode current. $\overline{FAIL}$ asserts low when the APC loop is disabled.

Short-Circuit Protection

The MAX3273 provides short-circuit protection for the modulation and bias current sources. If BIASMAX, MODSET, or APCSET is shorted to ground, the bias and modulation output turns off.

Design Procedure

When designing a laser transmitter, the optical output usually is expressed in terms of average power and extinction ratio. Table 1 gives relationships helpful in converting between the optical average power and the modulation current. These relationships are valid if the mark density and duty cycle of the optical waveform are 50%.

Programming the Modulation Current

For a given laser power (P_{AVG}), slope efficiency (η), and extinction ration (r_e), the modulation current can be calculated using Table 1. See the I_{MOD} vs. R_{MODSET} graph in the *Typical Operating Characteristics* and select the value of R_{MODSET} that corresponds to the required current at +25°C. The equation below provides a derivation of the modulation current using Table 1.

$$I_{MOD} = 2 \times \frac{P_{AVE}}{\eta} \times \frac{r_e - 1}{r_e + 1}$$

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Programming the Bias Current with APC Disabled

When using the MAX3273 in open-loop operation, the bias current is determined by the $R_{BIASMAX}$ resistor. To select this resistor, see the $I_{BIASMAX}$ vs. $R_{BIASMAX}$ graph in the *Typical Operating Characteristics* and select the value of $R_{BIASMAX}$ that corresponds to the required $I_{BIASMAX}$ at +25°C. Ground the APCFILT1 pin for open-loop operation.

Programming the Bias Current with APC Enabled

When the MAX3273's APC feature is used, program the average optical power by adjusting the APCSET resistor. To select this resistor, determine the desired monitor current to be maintained over temperature and life. See the I_{MD} vs. R_{APCSET} graph in the *Typical Operating Characteristics* and select the value of R_{APCSET} that corresponds to the required current.

When using the MAX3273 in closed-loop operation, the $R_{BIASMAX}$ resistor sets the maximum bias current available to the laser diode over temperature and life. The APC loop can subtract from this maximum value but cannot add to it. See the $I_{BIASMAX}$ vs. $R_{BIASMAX}$ graph in the *Typical Operating Characteristics* and select the value of $R_{BIASMAX}$ that corresponds to the end-of-life bias current at +85°C.

Interfacing with Laser Diodes

To minimize optical output aberrations caused by signal reflections at the electrical interface to the laser diode, a series-damping resistor (R_D) is required (see the *Typical Application Circuit*). Additionally, the MAX3273 outputs are optimized for a 25Ω load. Therefore, the series combination of R_D and R_L (where R_L represents the laser-diode resistance) should equal 25Ω. Typical values for RD are 18Ω to 23Ω. For best performance, a bypass capacitor (0.01µF typical) should be placed as close as possible to the anode of the laser diode. Depending on the exact characteristics of the laser diode and PC board layout, a resistor (R_P) of 50Ω to 100Ω in parallel with pullup inductor L_{P1} can be useful in damping overshoot and ringing in the optical output.

In some applications (depending on laser-diode parasitic inductance), an RC-shunt network between the laser cathode and ground helps minimize optical output aberrations. Starting values for most coaxial lasers are R = 75Ω in series with C = 3.3pF. These values should be experimentally adjusted until the optical output waveform is optimized.

Pattern-Dependent Jitter

When transmitting NRZ data with long strings of consecutive identical digits (CIDs), LF droop can occur and contribute to pattern-dependent jitter (PDJ). To minimize this PDJ, three external components must be properly chosen: capacitor ($C_{APCFILT}$), which dominates the APC loop time constant; pullup inductor (L_P); and AC-coupling capacitor (C_D).

To filter out noise effects and guarantee loop stability, the recommended value for $C_{APCFILT}$ is 0.01µF. This results in an APC loop bandwidth of 100kHz or a time constant of 15µs. As a result, the PDJ associated with an APC loop time constant can be ignored.

The time constant associated with the output pullup inductor ($L_P \approx L_{P2}$) and the AC-coupling capacitor (C_D) affects the PDJ. For such a second-order network, the PDJ is dominated by L_P because of the low frequency cutoff. For a data rate of 2.5Gbps, the recommended value for C_D is 0.056µF. During the maximum CID period, limit the peak voltage droop to less than 12% of the average (6% of the amplitude). The time constant can be estimated by:

$$12\% = 1 - e^{\frac{-t}{\tau_{LP}}}$$

$$\tau_{LP} = 7.8t$$

If $\tau_{LP} = L_P / 25\Omega$, and t = 100UI ≈ 40ns, then L_P = 7.8µH. To reduce the physical size of this element (L_P), use of SMD ferrite beads is recommended (Figure 2). To achieve even greater immunity to droop, use an optional third inductor (33µH, L_{P3} in Figure 2).

Input Termination Requirement

The MAX3273 data and clock inputs are CML compatible. However, it is not necessary to drive the IC with a standard CML signal. As long as the specified differential voltage swings are met, the MAX3273 operates properly.

Calculating Power Consumption

The junction temperature of the MAX3273 dice must be kept below +150°C at all times. The total power dissipation of the MAX3273 can be estimated by the following:

$$P = V_{CC} \times I_{CC} + (V_{CC} - V_f) \times I_{BIAS} + I_{MOD} \times (V_{CC} - 25 \times I_{MOD} / 2)$$

where I_{BIAS} is the maximum bias current set by $R_{BIASMAX}$, I_{MOD} is the modulation current, and V_f is the typical laser forward voltage.

$$\text{Junction temperature} = P(W) \times 37\ (°C/W)$$

Table 1. Optical Power Relations

PARAMETER	SYMBOL	RELATION
Average Power	P_{AVG}	$P_{AVG} = (P_0 + P_1) / 2$
Extinction Ratio	r_e	$r_e = P_1 / P_0$
Optical Power of a 1	P_1	$P_1 = 2P_{AVG}r_e / (r_e + 1)$
Optical Power of a 0	P_0	$P_0 = 2P_{AVG} / (r_e + 1)$
Optical Amplitude	P_{P-P}	$P_{P-P} = P_1 - P_0 = 2P_{AVG}(r_e - 1) / (r_e + 1)$
Laser Slope Efficiency	η	$\eta = P_{P-P} / I_{MOD}$
Modulation Current	I_{MOD}	$I_{MOD} = P_{P-P} / \eta$
Threshold Current	I_{TH}	P_0 at $1 \geq I_{TH}$
Bias Current	I_{BIAS}	$I_{BIAS} \geq I_{TH} + I_{MOD} / 2$
Laser-to-Monitor Transfer	ρ_{MON}	I_{MD} / P_{AVG}

Note: *Assuming a 50% average input duty cycle and mark density.*

Applications Information

An example of how to set up the MAX3273 follows.

Select Laser

A communication-grade laser should be selected for 2.5Gbps/2.7Gbps applications. Assume the laser output average power is P_{AVG} = 0, the minimum extinction ratio is r_e = 6.6 (8.2dB), the operating temperature is -40°C to +85°C, and the laser diode has the following characteristics:

- Wavelength: λ = 1310nm
- Threshold Current: I_{TH} = 22mA at +25°C
- Threshold Temperature Coefficient: β_{TH} = 1.3%/°C
- Laser-to-Monitor Transfer: ρ_{MON} = 0.2A/W
- Laser Slope Efficiency: η = 0.05mW/mA at +25°C

Determine R_{APCSET}

The desired monitor diode current is estimated by $I_{MD} = P_{AVG} \times \rho_{MON}$ = 200µA. The I_{MD} vs. R_{APCSET} graph in the *Typical Operating Characteristics* shows that R_{APCSET} should be 7.5kΩ.

Determine R_{MODSET}

To achieve a minimum extinction ratio (r_e) of 6.6 over temperature and lifetime, calculate the required extinction ratio at +25°C. Assuming r_e = 20, the peak-to-peak optical power P_{P-P} = 1.81mW, according to Table 1. The required modulation current is 1.81mW/(0.05mW/mA) = 36.2mA. The I_{MOD} vs. R_{MODSET} graph in the *Typical Operating Characteristics* shows that R_{MODSET} should be 5kΩ.

Determine $R_{BIASMAX}$

Calculate the maximum threshold current ($I_{TH(MAX)}$) at T_A = +85°C and end of life. Assuming $I_{TH(MAX)}$ = 50mA, the maximum bias current should be: $I_{BIASMAX} = I_{TH(MAX)} + (I_{MOD} / 2)$. In this example, $I_{BIASMAX}$ = 68.1mA. The $I_{BIASMAX}$ vs. $R_{BIASMAX}$ graph in the *Typical Operating Characteristics* shows that $R_{BIASMAX}$ should be 3.5kΩ.

+3.3V, 2.5Gbps Low-Power Laser Driver

Interface Models

Figures 4 and 5 show simplified input and output circuits for the MAX3273 laser driver. If dice are used, replace package parasitic elements with bondwire parasitic elements.

Wire-Bonding Die

For high-current density and reliable operation, the MAX3273 uses gold metalization. Make connections to the die with gold wire only, using ball-bonding techniques. Wedge bonding is not recommended. Die-pad size is 4 mils (100µm) square, and die thickness is 14 mils (350µm).

Layout Considerations

To minimize inductance, keep the connections between the MAX3273 output pins and laser diode as close as possible. Optimize the laser-diode performance by placing a bypass capacitor as close as possible to the laser anode. Use good high-frequency layout techniques and multilayer boards with uninterrupted ground planes to minimize EMI and crosstalk.

Laser Safety and IEC 825

Using the MAX3273 laser driver alone does not ensure that a transmitter design is compliant with IEC 825. The entire transmitter circuit and component selections must be considered. Customers must determine the level of fault tolerance required by their application, recognizing that Maxim products are not designed or authorized for use as components in systems intended for surgical implant into the body, for applications intended to support or sustain life, or for any other application where the failure of a Maxim product could create a situation where personal injury or death may occur.

Chip Information

TRANSISTOR COUNT: 1672

PROCESS: SiGe

ISOLATED SUBSTRATE

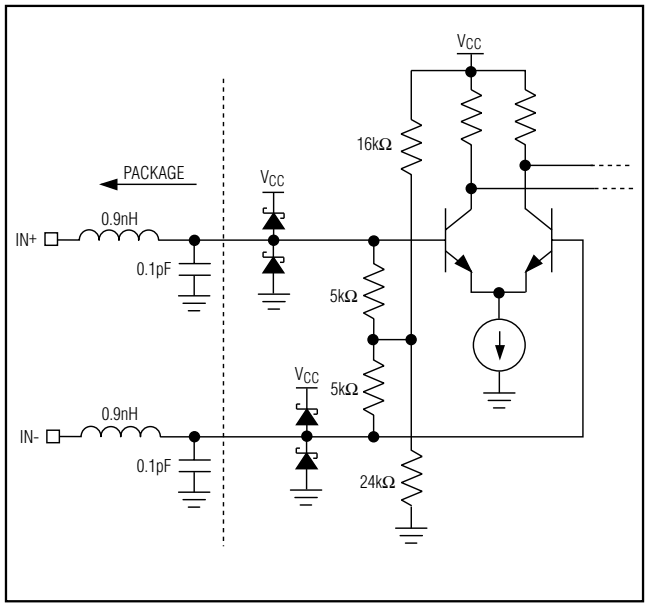


Figure 4. Simplified Input Circuit

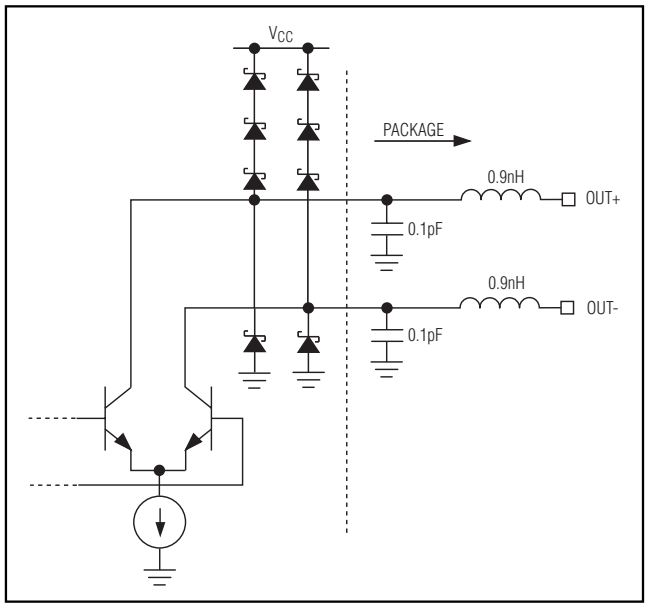
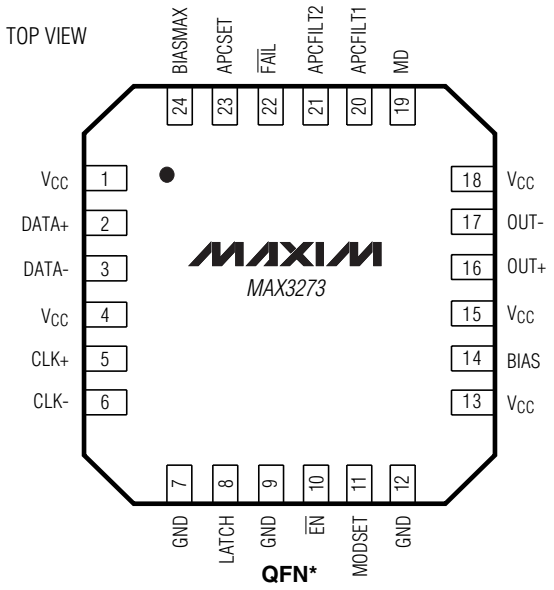


Figure 5. Simplified Output Circuit

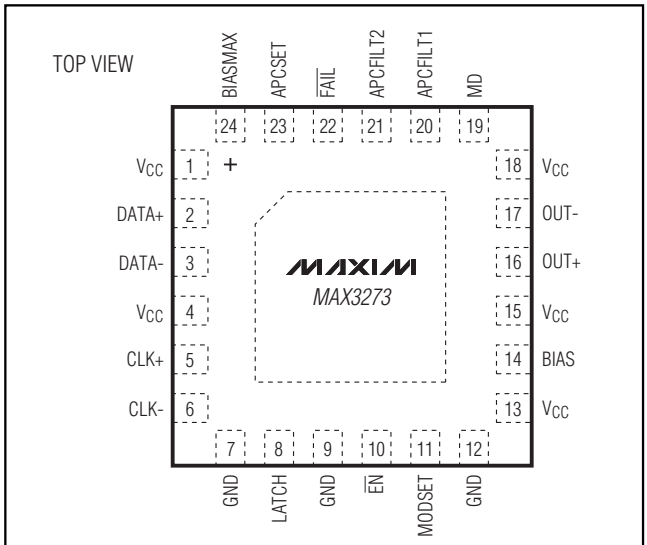
+3.3V, 2.5Gbps Low-Power Laser Driver

Pin Configurations



QFN*

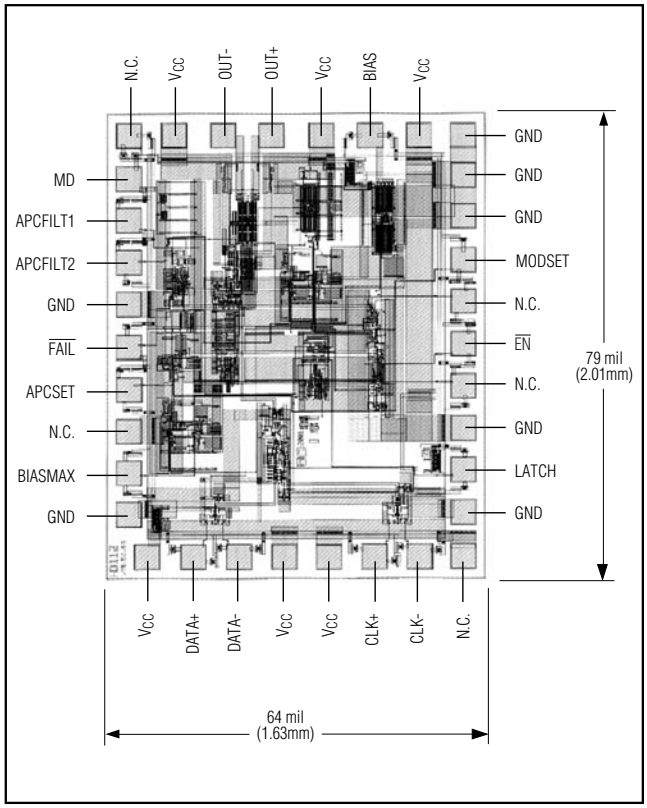
*EXPOSED PAD IS CONNECTED TO GND.



THIN QFN (4mm x 4mm)

THE EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER THERMAL AND ELECTRICAL PERFORMANCE.

Chip Topography

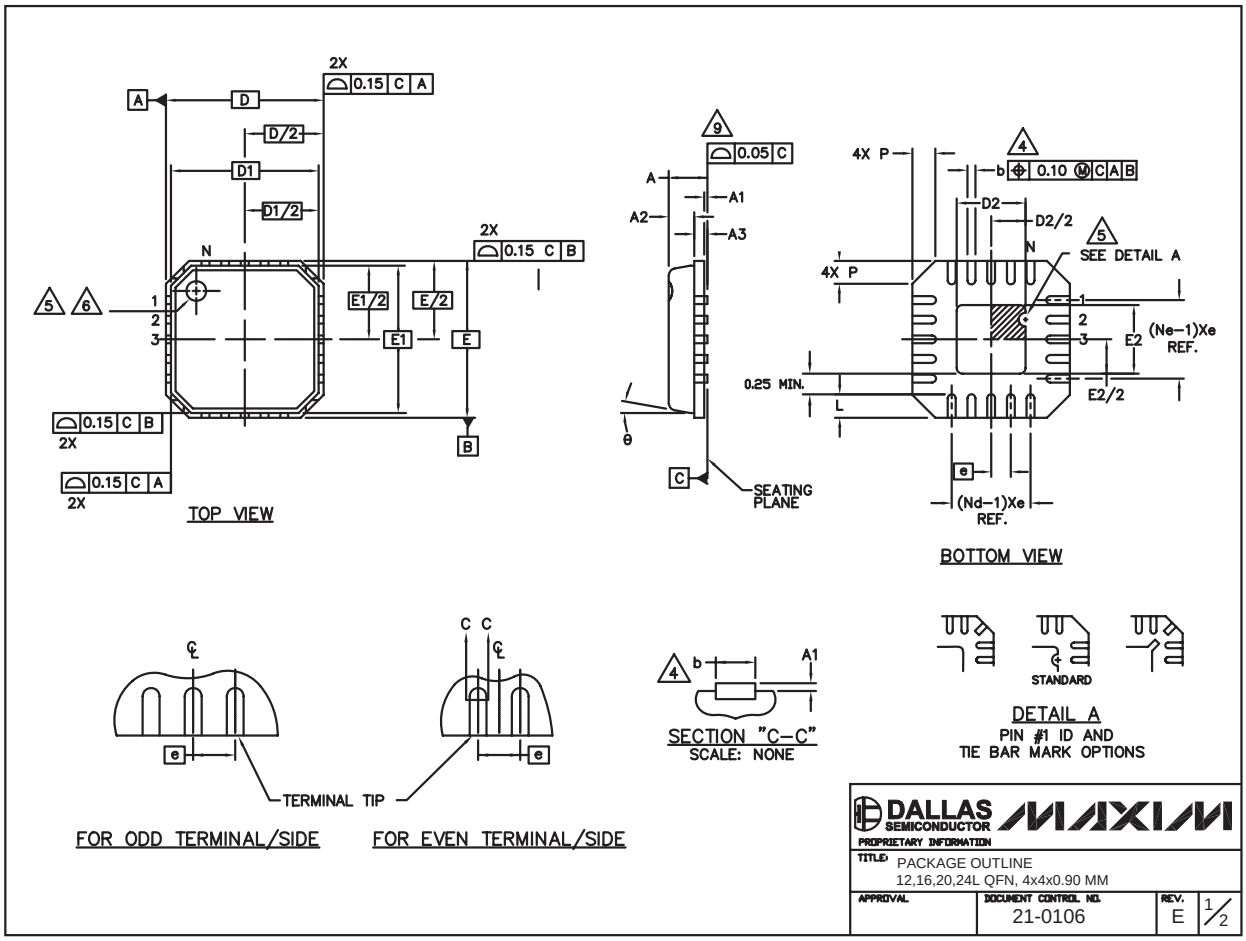


+3.3V, 2.5Gbps Low-Power Laser Driver

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

12,16,20, 24L QFN.EPS



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM).
2. DIMENSIONING & TOLERANCES CONFORM MUST TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220; EXCEPT DIMENSION "b".
11. THIS PACKAGE OUTLINE APPLIES TO PUNCHED QFN (STEPPED SIDES).

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.90	1.00	
A1	0.00	0.01	0.05	
A2	0.00	0.65	0.80	
A3		0.20 REF.		
D		4.00 BSC		
D1		3.75 BSC		
E		4.00 BSC		
E1		3.75 BSC		
θ	0°	–	12°	
P	0.24	0.42	0.60	

SYMBOL	PITCH VARIATION A			NOTE	SYMBOL	PITCH VARIATION B			NOTE	SYMBOL	PITCH VARIATION C			NOTE	SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.			MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
e	0.80 BSC				e	0.65 BSC				e	0.50 BSC				e	0.50 BSC			
N	12			3	N	16			3	N	20			3	N	24			3
Nd	3			3	Nd	4			3	Nd	5			3	Nd	6			3
Ne	3			3	Ne	4			3	Ne	5			3	Ne	6			3
L	0.50	0.60	0.75		L	0.50	0.60	0.75		L	0.50	0.60	0.75		L	0.30	0.40	0.50	
b	0.28	0.33	0.40	4	b	0.23	0.28	0.35	4	b	0.18	0.23	0.30	4	b	0.18	0.23	0.30	4

PKG. CODE	EXPOSED PAD VARIATION					
	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G1244–2	1.95	2.10	2.25	1.95	2.10	2.25
G1644–1	1.95	2.10	2.25	1.95	2.10	2.25
G2044–3	1.95	2.10	2.25	1.95	2.10	2.25
G2044–4	1.55	1.70	1.85	1.55	1.70	1.85
G2444–1	1.95	2.10	2.25	1.95	2.10	2.25

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

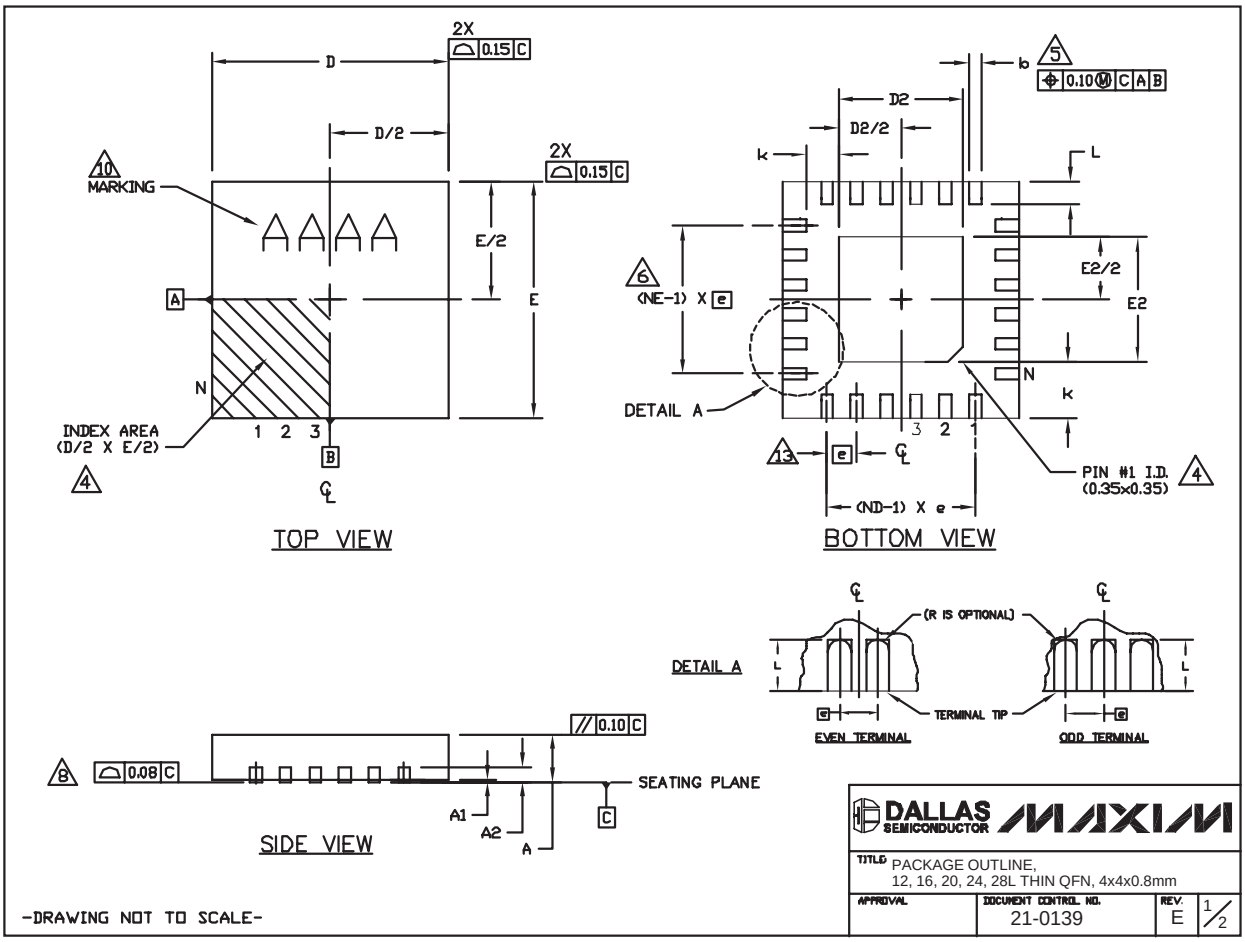
TITLE: PACKAGE OUTLINE
12,16,20,24L QFN, 4x4x0.90 MM

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0106	E	2/2

+3.3V, 2.5Gbps Low-Power Laser Driver

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS																
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4			
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25	
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	
N	12			16			20			24			28			
ND	3			4			5			6			7			
NE	3			4			5			6			7			
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE			

EXPOSED PAD VARIATIONS							
PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEEND 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	E	2/2

+3.3V, 2.5Gbps Low-Power Laser Driver

Revision History

Rev 0;	8/01:	Initial data sheet release.
Rev 1;	12/02:	Removed CP pin from Pin Description (page 7). Removed CP and GND pins from Pin Configuration (page 13). Updated package drawing with new revision (pages 14 and 15).
Rev 2;	5/03:	Updated Ordering Information and added package code (page 1). Updated package drawing with new revision (page 14).
Rev 3;	2/07:	Added thin QFN package to Ordering Information (page 1). Updated Figure 3 (added connector dot to Failure Detector) (page 8). Added missing connector dots to Figure 5 and added thin QFN pin configuration (page 13).

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