Isolated Precision Gate Driver, 4.0 A Output

Data Sheet

ADuM3123

FEATURES

- 4.0 A output short-circuit pulsed current
- Isolated working voltage
  - Secondary side to input side: 537 V
- High frequency operation: 1 MHz maximum
- 3.3 V to 5 V input logic
- 4.5 V to 18 V output drive
- Undervoltage lockout (UVLO): 2.8 V V_{DD1}
- Precise timing characteristics
  - 64 ns maximum isolator and driver propagation delay
- Complementary metal oxide semiconductor (CMOS) input logic levels
- High common-mode transient immunity: >25 kV/µs
- High junction temperature operation: 125°C
- Default low output
- Safety and regulatory approvals (pending)
  - UL recognition per UL 1577
    - 3000 V rms for 1 minute SOIC long package
  - CSA Component Acceptance Notice 5A
  - VDE certificate of conformity (pending)
    - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
    - Maximum working insulation voltage (V_{IORM}) = 560 V peak
- Narrow body, 8-lead SOIC

APPLICATIONS

- Switching power supplies
- Isolated gate bipolar transistors (IGBT)/MOSFET gate drives
- Industrial inverters

GENERAL DESCRIPTION

The ADuM3123[1] is a 4.0 A isolated, single channel driver that employs Analog Devices, Inc., *i*Coupler® technology to provide precision isolation. The ADuM3123 provides 3000 V rms isolation in the narrow-body, 8-lead SOIC package. Combining high speed CMOS and monolithic transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as the combination of pulse transformers and gate drivers.

The ADuM3123 operates with an input supply ranging from 3.0 V to 5.5 V, providing compatibility with lower voltage systems. In comparison to gate drivers employing high voltage level translation methodologies, the ADuM3123 offers the benefit of true, galvanic isolation between the input and the output. The output can continuously operate up to 380 V rms relative to the input.

As a result, the ADuM3123 provides reliable control over the switching characteristics of IGBT/MOSFET configurations over a wide range of positive and negative switching voltages.

FUNCTIONAL BLOCK DIAGRAM

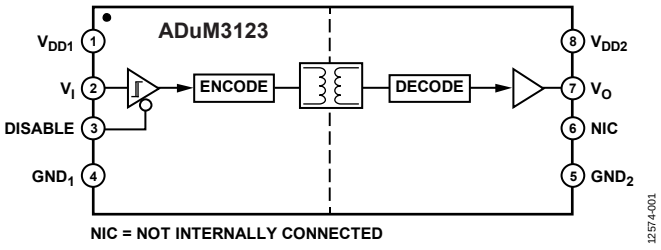

Figure 1.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,239. Other patents pending.

Rev. 0 Document Feedback

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REVISION HISTORY

7/15—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All voltages are relative to their respective ground. 4.5 V ≤ V_{DD1} ≤ 5.5 V, and 4.5 V ≤ V_{DD2} ≤ 18 V, unless stated otherwise. All minimum/maximum specifications apply over T_J = −40°C to +125°C. All typical specifications are at T_J = 25°C, V_{DD1} = 5 V, and V_{DD2} = 12 V. Switching specifications are tested with CMOS signal levels.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Supply Current, Quiescent	$I_{DDI(Q)}$		1.4	2.4	mA	
Output Supply Current, Quiescent	$I_{DDO(Q)}$		2.3	3.7	mA	
Supply Current at 1 MHz						
V_{DD1} Supply Current	I_{DD1}		1.6	2.5	mA	Up to 1 MHz, no load
V_{DD2} Supply Current	I_{DD2}		5.6	8.0	mA	Up to 1 MHz, no load
Input Currents	I_I	−1	+0.01	+1	µA	0 V ≤ V_I ≤ V_{DD1}
Input Threshold						
Logic High	V_{IH}	0.7 × V_{DD1}			V	
Logic Low	V_{IL}			0.3 × V_{DD1}	V	
Output Voltages						
Logic High	V_{OH}	V_{DD2} − 0.1	V_{DD2}		V	V_O = −20 mA, V_I = V_{IH}
Logic Low	V_{OL}		0.0	0.15	V	V_O = +20 mA, V_I = V_{IL}
Undervoltage Lockout, V_{DD1} Supply						
Positive Going Threshold	V_{DD1UV+}		2.8		V	
Negative Going Threshold	V_{DD1UV-}		2.6		V	
Hysteresis	V_{DD1UVH}		0.2		V	
Undervoltage Lockout, V_{DD2} Supply						
Positive Going Threshold	V_{DD2UV+}		4.1	4.4	V	A Grade
			6.9	7.4	V	B Grade
			10.5	11.1	V	C Grade
Negative Going Threshold	V_{DD2UV-}	3.2	3.6		V	A Grade
		5.7	6.2		V	B Grade
		9.0	9.6		V	C Grade
Hysteresis	V_{DD2UVH}		0.5		V	A Grade
			0.7		V	B Grade
			0.9		V	C Grade
Output Short-Circuit Pulsed Current[1]	$I_{O(SC)}$	2.0	4.0		A	V_{DD2} = 12 V
Output Source Resistance	R_{ON_P}	0.25	0.95	1.5	Ω	V_{DD2} = 12 V, I_{V_O} = −250 mA
Output Sink Resistance	R_{ON_N}	0.55	0.6	1.35	Ω	V_{DD2} = 12 V, I_{V_O} = 250 mA
THERMAL SHUTDOWN TEMPERATURES						
Junction Temperature Shutdown						
Rising Edge	T_{JR}		150		°C	
Falling Edge	T_{JF}		140		°C	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						See Figure 17
Pulse Width[2]	PW	50			ns	C_L = 2 nF, V_{DD2} = 12 V
Maximum Data Rate[3]		1			MHz	C_L = 2 nF, V_{DD2} = 12 V
Propagation Delay[4]	t_{DHL}, t_{DLH}	19	40	62	ns	C_L = 2 nF, V_{DD2} = 12 V
ADuM3123 A Grade		25	46	68	ns	C_L = 2 nF, V_{DD2} = 4.5 V
Propagation Delay Skew[5]	t_{PSK}			12	ns	C_L = 2 nF, V_{DD2} = 12 V
Output Rise Time/Fall Time (10% to 90%)	t_R/t_F	1	12	24	ns	C_L = 2 nF, V_{DD2} = 12 V
Supply Current						
Dynamic Input	$I_{DDI(D)}$		0.05		mA/Mbps	V_{DD2} = 12 V
Dynamic Output	$I_{DDO(D)}$		1.65		mA/Mbps	V_{DD2} = 12 V
Refresh Rate	f_r		1.2		Mbps	V_{DD2} = 12 V

[1] Short-circuit duration less than 1 µs. Average power must conform to the limits shown in the Absolute Maximum Ratings section.
[2] The minimum pulse width is the shortest pulse width at which the specified timing parameter is guaranteed.
[3] The maximum data rate is the fastest data rate at which the specified timing parameter is guaranteed.
[4] t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL}, to the output falling 90% threshold of the V_O signal. t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH}, to the output rising 10% level of the V_O signal. See Figure 17 for waveforms of propagation delay parameters.
[5] t_{PSK} is the magnitude of the worst case difference in t_{DLH} and/or t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See Figure 17 for waveforms of propagation delay parameters.

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All voltages are relative to their respective ground. 3.0 V ≤ V_{DD1} ≤ 3.6 V, and 4.5 V ≤ V_{DD2} ≤ 18 V, unless stated otherwise. All minimum/maximum specifications apply over T_J = −40°C to +125°C. All typical specifications are at T_J = 25°C, V_{DD1} = 3.3 V, and V_{DD2} = 12 V. Switching specifications are tested with CMOS signal levels.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Supply Current, Quiescent	$I_{DDI(Q)}$		0.87	1.4	mA	
Output Supply Current, Quiescent	$I_{DD2(Q)}$		2.3	3.7	mA	
Supply Current at 1 MHz						
V_{DD1} Supply Current	I_{DD1}		1.1	1.5	mA	Up to 1 MHz, no load
V_{DD2} Supply Current	I_{DD2}		5.6	8.0	mA	Up to 1 MHz, no load
Input Currents	I_I	−10	+0.01	+10	μA	0 V ≤ V_I ≤ V_{DD1}
Input Threshold						
Logic High	V_{IH}	0.7 × V_{DD1}			V	
Logic Low	V_{IL}			0.3 × V_{DD1}	V	
Output Voltages						
Logic High	V_{OH}	V_{DD2} − 0.1	V_{DD2}		V	V_O = −20 mA, V_I = V_{IH}
Logic Low	V_{OL}		0.0	0.15	V	V_O = +20 mA, V_I = V_{IL}
Undervoltage Lockout, V_{DD1} Supply						
Positive Going Threshold	V_{DD1UV+}		2.8		V	
Negative Going Threshold	V_{DD1UV-}		2.6		V	
Hysteresis	V_{DD1UVH}		0.2		V	
Undervoltage Lockout, V_{DD2} Supply						
Positive Going Threshold	V_{DD2UV+}		4.1	4.4	V	A Grade
			6.9	7.4	V	B Grade
			10.5	11.1	V	C Grade
Negative Going Threshold	V_{DD2UV-}	3.2	3.6		V	A Grade
		5.7	6.2		V	B Grade
		9.0	9.6		V	C Grade
Hysteresis	V_{DD2UVH}		0.5		V	A Grade
			0.7		V	B Grade
			0.9		V	C Grade
Output Short-Circuit Pulsed Current[1]	$I_{O(SC)}$	2.0	4.0		A	V_{DD2} = 12 V
Output Source Resistance	R_{ON_P}	0.25	0.95	1.5	Ω	V_{DD2} = 12 V, I_{V_O} = −250 mA
Output Sink Resistance	R_{ON_N}	0.55	0.6	1.35	Ω	V_{DD2} = 12 V, I_{V_O} = 250 mA
THERMAL SHUTDOWN TEMPERATURES						
Junction Temperature Shutdown						
Rising Edge	T_{JR}		150		°C	
Falling Edge	T_{JF}		140		°C	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						See Figure 17
Pulse Width[2]	PW	50			ns	C_L = 2 nF, V_{DD2} = 12 V
Maximum Data Rate[3]		1			MHz	C_L = 2 nF, V_{DD2} = 12 V
Propagation Delay[4]	t_{DHL}, t_{DLH}	25	44	64	ns	C_L = 2 nF, V_{DD2} = 12 V
ADuM3123 A Grade		28	49	71	ns	C_L = 2 nF, V_{DD2} = 4.5 V
Propagation Delay Skew[5]	t_{PSK}			12	ns	C_L = 2 nF, V_{DD2} = 12 V
Output Rise/Fall Time (10% to 90%)	t_R/t_F	1	12	24	ns	C_L = 2 nF, V_{DD2} = 12 V
Dynamic Input Supply Current	$I_{DDI(D)}$		0.05		mA/Mbps	V_{DD2} = 12 V
Dynamic Output Supply Current	$I_{DDO(D)}$		1.65		mA/Mbps	V_{DD2} = 12 V
Refresh Rate	f_r		1.1		Mbps	V_{DD2} = 12 V

[1] Short-circuit duration less than 1 µs. Average power must conform to the limits shown in the Absolute Maximum Ratings section.
[2] The minimum pulse width is the shortest pulse width at which the specified timing parameter is guaranteed.
[3] The maximum data rate is the fastest data rate at which the specified timing parameter is guaranteed.
[4] t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL}, to the output falling 90% threshold of the V_O signal. t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH}, to the output rising 10% level of the V_O signal. See Figure 17 for waveforms of propagation delay parameters.
[5] t_{PSK} is the magnitude of the worst case difference in t_{DLH} and/or t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See Figure 17 for waveforms of propagation delay parameters.

PACKAGE CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)	R_{I-O}		10^{12}		Ω	
Capacitance (Input to Output)	C_{I-O}		2.0		pF	f = 1 MHz
Input Capacitance	C_I		4.0		pF	
IC Thermal Resistance, Junction to Ambient	θ_{JA}		95		°C/W	

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3000	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	3.9 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	3.9 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

REGULATORY INFORMATION

The ADuM3123 is pending approval by the organizations listed in Table 5.

Table 5.

UL	CSA	VDE
Recognized under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
Single Protection 3000 V rms Isolation Voltage	Basic insulation per CSA 60950-1-07 and IEC 60950-1, 380 V rms (537 V peak) maximum working voltage	Reinforced insulation, 560 V peak
File pending	File pending	File pending

[1] In accordance with UL 1577, each ADuM3123 is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (current leakage detection limit = 5 µA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM3123 is proof tested by applying an insulation test voltage ≥ 1050 V peak for 1 second (partial discharge detection limit = 5 pC). An asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 approval.

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

This isolator is suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking on the package denotes DIN V VDE V 0884-10 approval for a 560 V peak working voltage.

Table 6.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input-to-Output Test Voltage, Method b1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, t_m = 1 sec, partial discharge < 5 pC	$V_{pd(m)}$	1050	V peak
Input-to-Output Test Voltage, Method a	$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC	$V_{pd(m)}$		
After Environmental Tests Subgroup 1			896	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC		672	V peak
Highest Allowable Overvoltage		V_{IOTM}	4242	V peak
Surge Isolation Voltage	V_{PEAK} = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	6000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Maximum Junction Temperature		T_S	150	°C
Safety Total Dissipated Power		P_S	1.31	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

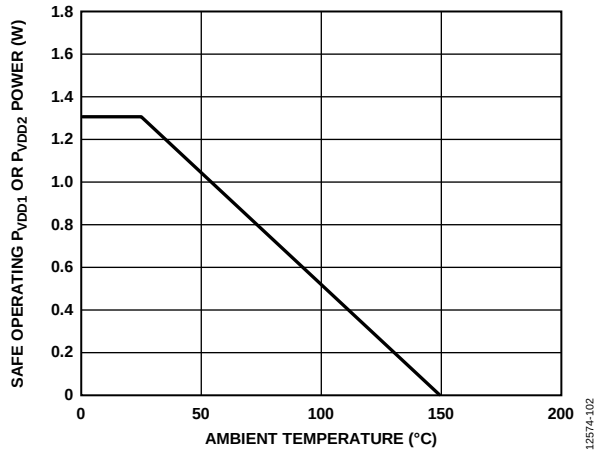

Figure 2. ADuM3123 Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature, per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 7.

Parameter	Symbol	Value
Operating Junction Temperature	T_J	−40°C to +125°C
Supply Voltages[1]		
	V_{DD1}	3.0 V to 5.5 V
	V_{DD2}	4.5 V to 18 V
Maximum Input Signal Rise/Fall Times	t_{VIA}, t_{VIB}	1 ms
Common-Mode Transient Static[2]		−50 kV/µs to +50 V/µs
Dynamic Common-Mode Transient Immunity[3]		−25 kV/µs to +25 kV/µs

[1] All voltages are relative to their respective ground. See the Applications Information section for information on immunity to external magnetic fields.
[2] Static common-mode transient immunity is defined as the largest dv/dt between GND_1 and GND_2 with inputs held either high or low such that the output voltage remains either above $0.8 \times V_{DD2}$ for V_I = high, or 0.8 V for V_I = low. Operation with transients above recommended levels can cause momentary data upsets.
[3] Dynamic common-mode transient immunity is defined as the largest dv/dt between GND_1 and GND_2 with switching edge coincident with the transient test pulse. Operation with transients above recommended levels can cause momentary data upsets.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 8.

Parameter	Symbol	Rating
Storage Temperature Range	T_{ST}	−55°C to +150°C
Operating Junction Temperature Range	T_J	−40°C to +150°C
Supply Voltages[1]	V_{DD1}, V_{DD2}	−0.3 V to +6.0 V −0.3 V to +20 V
Input Voltage[1, 2]	V_{IN}	−0.3 V to V_{DDI} + 0.3 V
Output Voltage[1, 2]	V_{OUT}	−0.3 V to V_{DDO} + 0.3 V
Average Output Current per Pin	I_{OUT}	−35 mA to +35 mA
Common-Mode Transients[3]	C_{MH}, C_{ML}	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective ground.
[2] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively.
[3] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Ratings can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 9. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage			50-year minimum lifetime
Bipolar Waveform	565	V peak	
Unipolar Waveform	1131	V peak	
DC Voltage	1131	V peak	50-year minimum lifetime

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 10. Truth Table (Positive Logic)[1]

DISABLE	V_I Input	V_{DD1} State	V_{DD2} State	V_O Output	Comments
L	L	Powered	Powered	L	Outputs return to the input state within 1 µs of DISABLE set to low
L	H	Powered	Powered	H	Outputs return to the input state within 1 µs of DISABLE set to low
H	X	Powered	Powered	L	Outputs take on default low state within 3 µs of DISABLE set to high
L	L	Unpowered	Powered	L	Output returns to the input state within 1 µs of V_{DD1} power restoration
X	X	Powered	Unpowered	Indeterminate	Outputs return to the input state within 50 µs of V_{DD2} power restoration

[1] X is don't care, L is low, and H is high.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

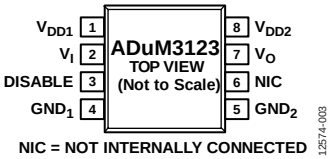

Figure 3. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_I	Gate Drive Input.
3	DISABLE	Disable. Connect to Logic Low to Enable.
4	GND_1	Ground 1. Ground reference for Isolator Side 1.
5	GND_2	Ground 2. Ground reference for Isolator Side 2.
6	NIC	Not Internally Connected.
7	V_O	Gate Drive Output.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

TYPICAL PERFORMANCE CHARACTERISTICS

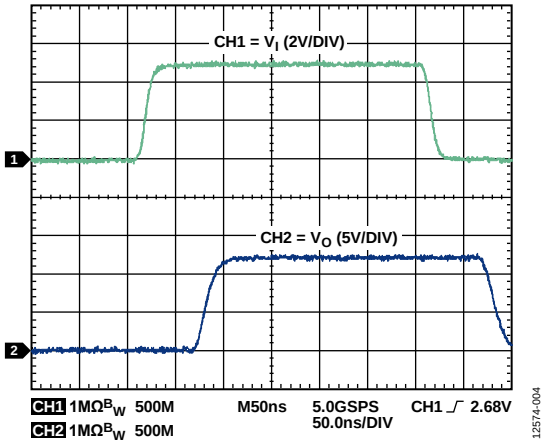

Figure 4. Input to Output Waveform for 2 nF Load, 3.6 Ω Series Gate Resistor with 12 V Output Supply

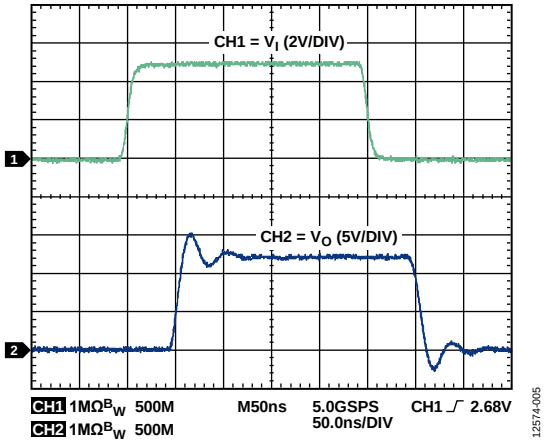

Figure 5. Input to Output Waveform for 2 nF Load, 0 Ω Series Gate Resistor with 12 V Output Supply

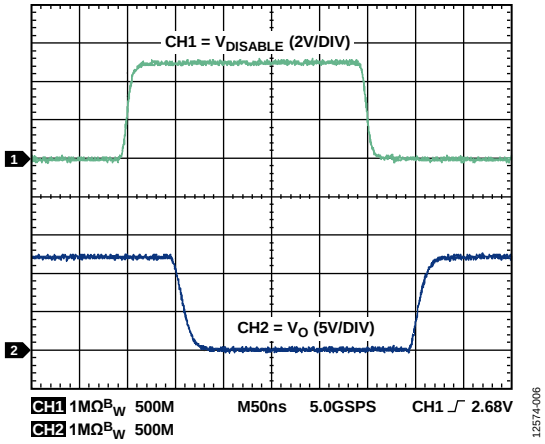

Figure 6. DISABLE to Output Waveform for 2 nF Load, 3.6 Ω Resistor with 12 V Output Supply, $V_I = V_{DD1}$

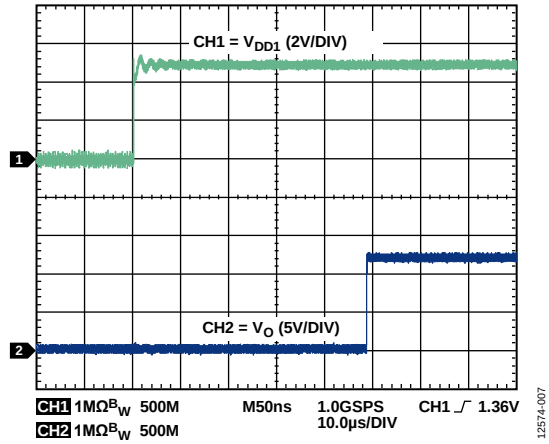

Figure 7. Typical V_{DD1} Delay to Output Waveform, $V_I = V_{DD1}$

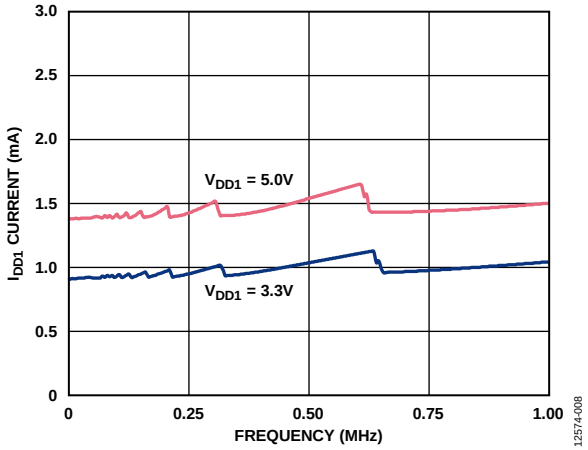

Figure 8. Typical I_{DD1} Current vs. Frequency

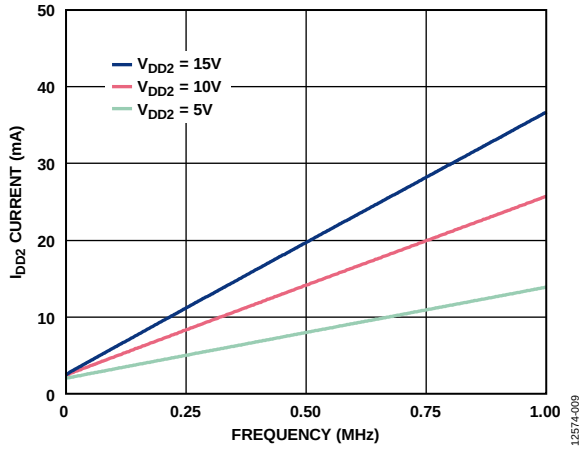

Figure 9. Typical I_{DD2} Current vs. Frequency with 2 nF Load

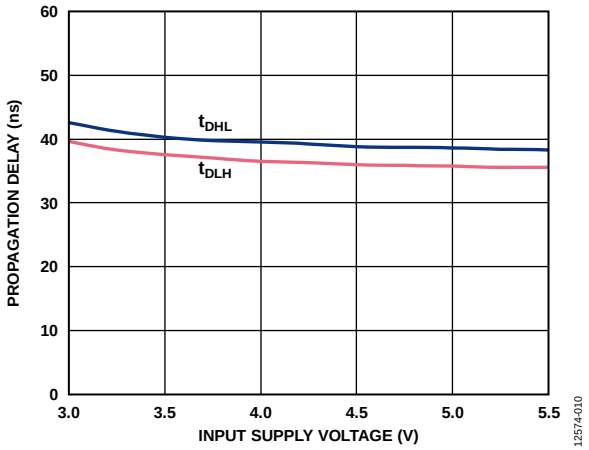

Figure 10. Typical Propagation Delay vs. Input Supply Voltage, V_{DD2} = 12 V

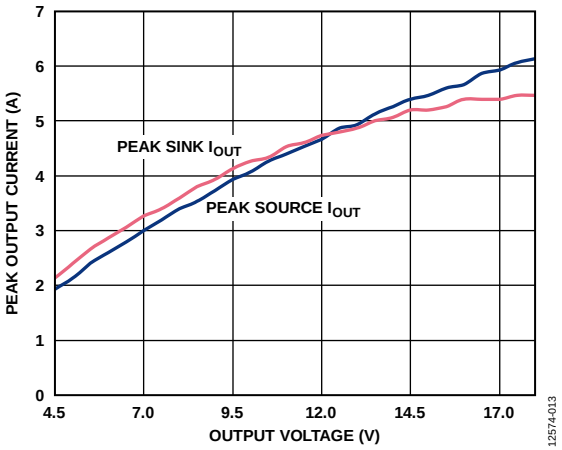

Figure 13. Typical Peak Output Current vs. Output Voltage, 1.2 Ω Series Resistance

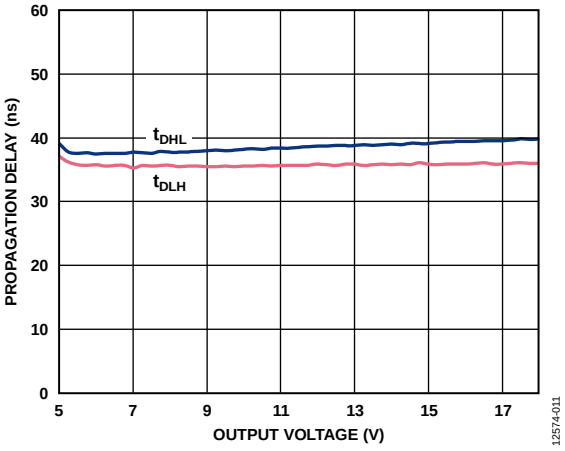

Figure 11. Typical Propagation Delay vs. Output Voltage, V_{DD1} = 5 V

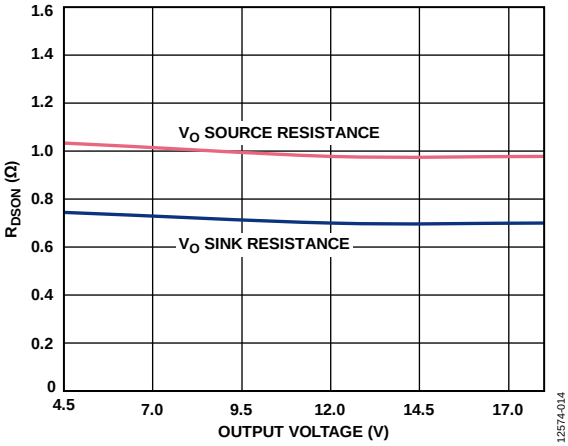

Figure 14. Typical Output Resistance (R_{DSON}) vs. Output Voltage

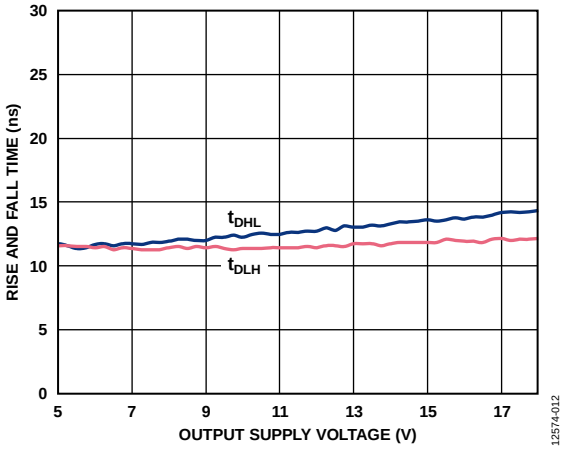

Figure 12. Typical Rise and Fall Time vs. Output Supply Voltage

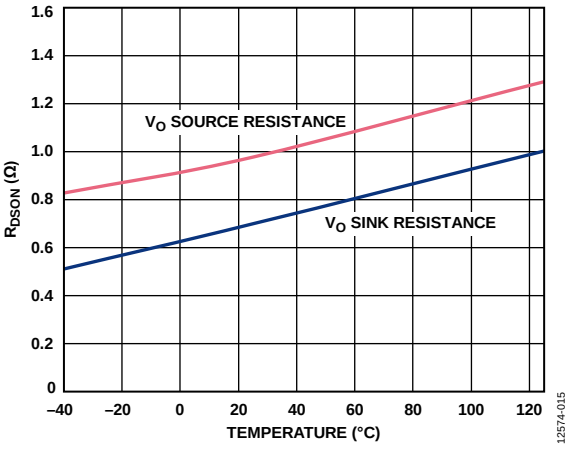

Figure 15. Typical Output Resistance (R_{DSON}) vs. Temperature, V_{DD2} = 12 V

APPLICATIONS INFORMATION

PRINTED CIRCUIT BOARD (PCB) LAYOUT

The ADuM3123 digital isolator requires no external interface circuitry for the logic interface. Power supply bypassing is required at the input and output supply pins, as shown in Figure 16. Use a small ceramic capacitor with a value between 0.01 µF and 0.1 µF to provide a good high frequency bypass.

In addition, on the output power supply pins (V_{DD1} and V_{DD2}), it is recommended to add a 10 µF capacitor in parallel to provide the charge required to drive the gate capacitance at the ADuM3123 outputs. When using lower value capacitors for decoupling, ensure that voltage drop during switching transients are acceptable. The required decoupling is a function of the gate capacitance being driven vs. the acceptable voltage drop. On the output supply pin, avoid bypass capacitor use of vias or employ multiple vias to reduce the inductance in the bypassing. The total lead length between both ends of the smaller capacitor and the input or output power supply pin must not exceed 20 mm. Place bypass capacitors as near to the device as possible for the best performance.

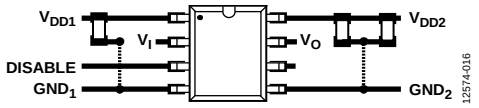

Figure 16. Recommended PCB Layout

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high output. The ADuM3123 specifies t_{DLH} (see Figure 17) as the time between the rising input high logic threshold, V_{IH}, to the output rising 10% threshold of the V_O signal. Likewise, the falling propagation delay, t_{DHL}, is defined as the time between the input falling logic low threshold, V_{IL}, and the output falling 90% threshold of the V_O signal. The rise and fall times are dependent on the loading conditions and are not included in the propagation delay, as is the industry standard for gate drivers.

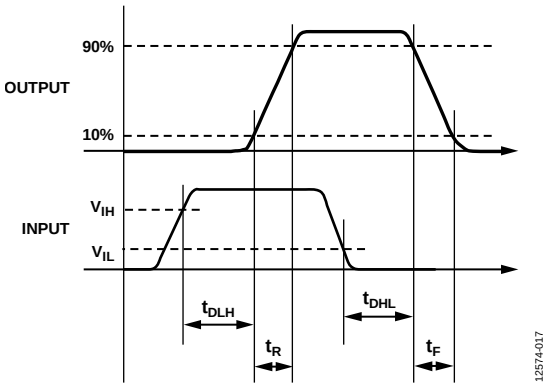

Figure 17. Propagation Delay Parameters

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM3123 components operating under the same conditions.

THERMAL LIMITATIONS AND SWITCH LOAD CHARACTERISTICS

For isolated gate drivers, the necessary separation between the input and output circuits prevents the use of a single thermal pad beneath the device, and heat is, therefore, dissipated mainly through the package pins.

The effective load capacitance being driven, switching frequency, operating voltage, and external series resistance primarily drives the power dissipation within the device. To calculate the power dissipation within each channel, use the following equation:

$$P_{DISS} = C_{EFF} \times (V_{DD2})^2 \times f_{SW} \times \frac{R_{DSON}}{R_{DSON} + R_{GATE}}$$

where:
C_{EFF} is the effective capacitance of the load.
V_{DD2} is the secondary side voltage.
f_{SW} is the switching frequency.
R_{DSON} is the internal resistance of the ADuM3123 (R_{ON_P}, R_{ON_N}).
R_{GATE} is the external gate resistor.

To find temperature rise above ambient temperature, multiply the total power dissipation by θ_{JA}, which is then added to the ambient temperature to find the approximate internal junction temperature of the ADuM3123.

Each of the ADuM3123 isolator outputs has a thermal shutdown protection function. This function sets an output to a logic low level when the rising junction temperature typically reaches 150°C and turns back on after the junction temperature has fallen from the shutdown value by about 10°C.

OUTPUT LOAD CHARACTERISTICS

The ADuM3123 output signals depend on the characteristics of the output load, which is typically an N-channel MOSFET. The driver output response to an N-channel MOSFET load can be modeled with a switch output resistance (R_{SW}), an inductance due to the PCB trace (L_{TRACE}), a series gate resistor (R_{GATE}), and a gate to source capacitance (C_{GS}), as shown in Figure 18.

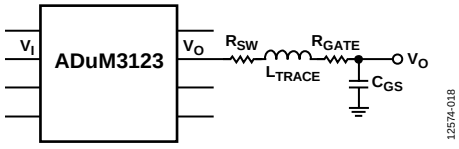

Figure 18. RLC Model of the Gate of an N-Channel MOSFET

R_{SW} is the switch resistance of the internal ADuM3123 driver output (0.95 Ω typical for source and 0.6 Ω typical for sink). R_{GATE} is the intrinsic gate resistance of the MOSFET and any external series resistance. A MOSFET that requires a 4.0 A gate driver has a typical intrinsic gate resistance of about 1 Ω and a gate to source capacitance (C_{GS}) of between 2 nF and 10 nF. L_{TRACE} is the inductance of the PCB trace, typically a value of 5 nH or less for a well designed layout with a very short and wide connection from the ADuM3123 output to the gate of the MOSFET.

The following equation defines the Q factor of the RLC circuit, which indicates how the ADuM3123 output responds to a step change. For a well damped output, Q is less than one. Adding a series gate resistance dampens the output response.

$$Q = \frac{1}{(R_{SW} + R_{GATE})} \times \sqrt{\frac{L_{TRACE}}{C_{GS}}}$$

To reduce output ringing, add a series gate resistance to dampen the response. For applications using a load of 1 nF or less, add a series gate resistor of about 5 Ω. It is recommended that the Q factor be below 1, which results in a damped system, with a value of 0.7 as the recommended target.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions of more than 1 µs (typical) at the input, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output.

If the decoder receives no internal pulses for more than about 3 µs (typical), the input side is assumed to be unpowered or nonfunctional, in which case, the isolator output is forced to a default low state by the watchdog timer circuit. In addition, the outputs are in a low default state while the power is coming up before the UVLO threshold is crossed.

The limitation on the ADuM3123 magnetic field immunity is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the ADuM3123 is examined because it represents the most susceptible mode of operation. The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2, \; n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the nth turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM3123 and an imposed requirement that the induced voltage is at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 19.

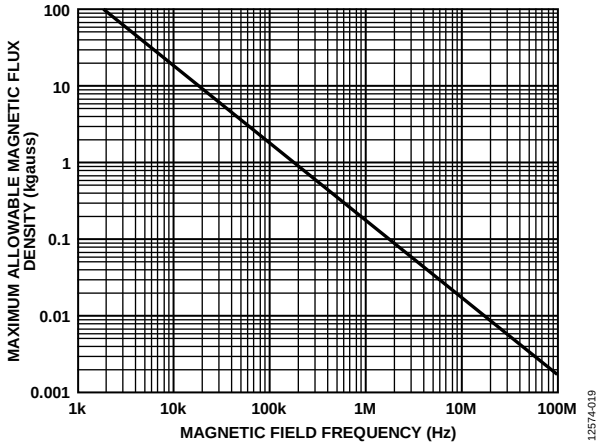

Figure 19. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This induced voltage level is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and had the worst-case polarity), the received pulse is reduced from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM3123 transformers. Figure 20 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM3123 is immune and only affected by extremely large currents operated at a high frequency and near to the component. For the 1 MHz example, place a 0.5 kA current 5 mm away from the ADuM3123 to affect the operation of the component.

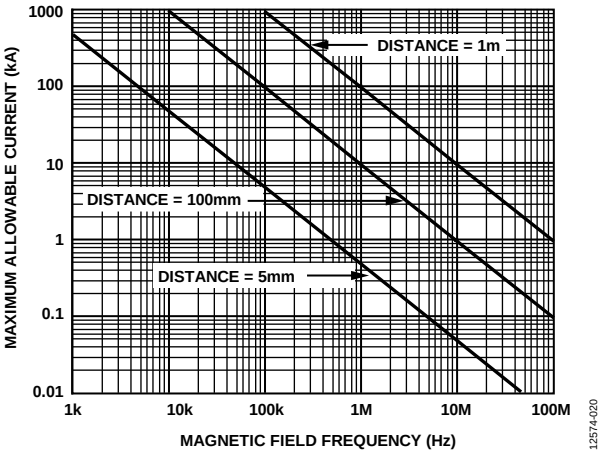

Figure 20. Maximum Allowable Current for Various Current to ADuM3123 Spacings

POWER CONSUMPTION

The supply current at a given channel of the ADuM3123 isolator is a function of the supply voltage, channel data rate, and channel output load.

For the input side, the supply current is given by

$$I_{DDI} = I_{DDI(Q)} \qquad f \leq 0.5f_r$$

$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)} \qquad f > 0.5f_r$$

For the output side, the supply current is given by

$$I_{DDO} = I_{DDO(Q)} \qquad f \leq 0.5f_r$$

$$I_{DDO} = (I_{DDO(D)} + (0.5) \times C_L V_{DD2}) \times (2f - f_r) + I_{DDO(Q)} \qquad f > 0.5f_r$$

where:
$I_{DDI(D)}$, $I_{DDO(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).
C_L is the output load capacitance (pF).
V_{DD2} is the output supply voltage (V).
f is the input logic signal frequency (MHz, half of the input data rate, NRZ signaling).
f_r is the input stage refresh rate (Mbps).
$I_{DDI(Q)}$, $I_{DDO(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total I_{DD1} and I_{DD2} supply current, the supply currents for each input and output channel corresponding to I_{DD1} and I_{DD2} are calculated and totaled.

Figure 8 provides the total input I_{DD1} supply current as a function of frequency for the input channel. Figure 9 provides the total I_{DD2} supply current as a function of frequency for the output loaded with 2 nF capacitance.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM3123.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values shown in Table 9 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM3123 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 21, Figure 22, and Figure 23 illustrate these different isolation voltage waveforms.

A bipolar ac voltage environment is the worst case for the *i*Coupler products and is the 50-year operating lifetime that Analog Devices recommends for maximum working voltage. In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. The lower stress of the unipolar or dc voltage allows operation at higher working voltages while still achieving a 50-year service life. Treat any cross-insulation voltage waveform that does not conform to Figure 22 or Figure 23 as a bipolar ac waveform, and limit its peak voltage to the 50-year lifetime voltage value listed in Table 9.

Note that the voltage presented in Figure 22 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

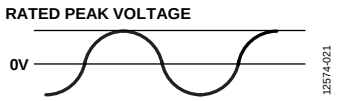

Figure 21. Bipolar AC Waveform

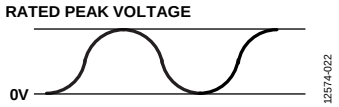

Figure 22. Unipolar AC Waveform

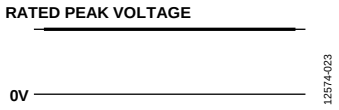

Figure 23. DC Waveform

OUTLINE DIMENSIONS

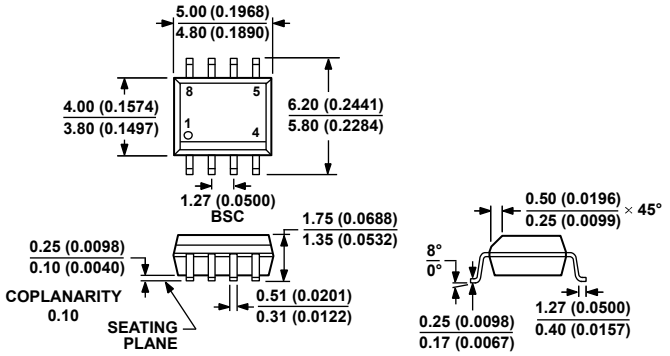

Figure 24. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	No. of Channels	Output Peak Current (A)	Minimum Output Voltage (V)	Temperature Range	Package Description	Package Option
ADuM3123ARZ	1	4	4.4	−40°C to +125°C	8-Lead SOIC_N	R-8
ADuM3123ARZ-RL7	1	4	4.4	−40°C to +125°C	8-Lead SOIC_N, 7″ Tape and Reel	R-8
ADuM3123BRZ	1	4	7.4	−40°C to +125°C	8-Lead SOIC_N	R-8
ADuM3123BRZ-RL7	1	4	7.4	−40°C to +125°C	8-Lead SOIC_N, 7″ Tape and Reel	R-8
ADuM3123CRZ	1	4	11.1	−40°C to +125°C	8-Lead SOIC_N	R-8
ADuM3123CRZ-RL7	1	4	11.1	−40°C to +125°C	8-Lead SOIC_N, 7″ Tape and Reel	R-8
EVAL-ADUM3123EBZ					Evaluation Board	

[1] Z = RoHS Compliant Part.