

Features

- Supports requirements of ITU-T G.8262 for Synchronous Ethernet Equipment Slave Clocks (EEC option 1 and 2)
- Supports requirements of Telcordia GR-1244 Stratum 3 and GR-253, ITU-T G.813, and G.781 SETS
- Supports ITU-T G.823, G.824 and G.8261 for 2048 kbit/s and 1544 kbit/s interfaces
- Programmable synthesizers generate any clock-rate from 1 Hz to 750 MHz
- Two precision synthesizers generate clocks with jitter below 0.8 ps RMS for 10 G PHYs
- Programmable digital PLL synchronize to any clock rate from 1 Hz to 750 MHz
- Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
- Digital PLL filter jitter from 0.1 mHz, 1 mHz, 10 mHz, 0.1 Hz, 1.7 Hz, 3.6 Hz, 7 Hz, 14 Hz,

Ordering Information

ZL30153GGG	100 Pin LBGA	Trays
ZL30153GGG2	100 Pin LBGA*	Trays

*Pb Free Tin/Silver/Copper
-40°C to +85°C

28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz or 896 Hz

- Automatic hitless reference switching and digital holdover on reference fail
- Four reference inputs configurable as single ended or differential
- Eight LVPECL outputs and four LVCMOS outputs
- Operates from a single crystal resonator or clock oscillator
- Configurable via SPI/I2C interface

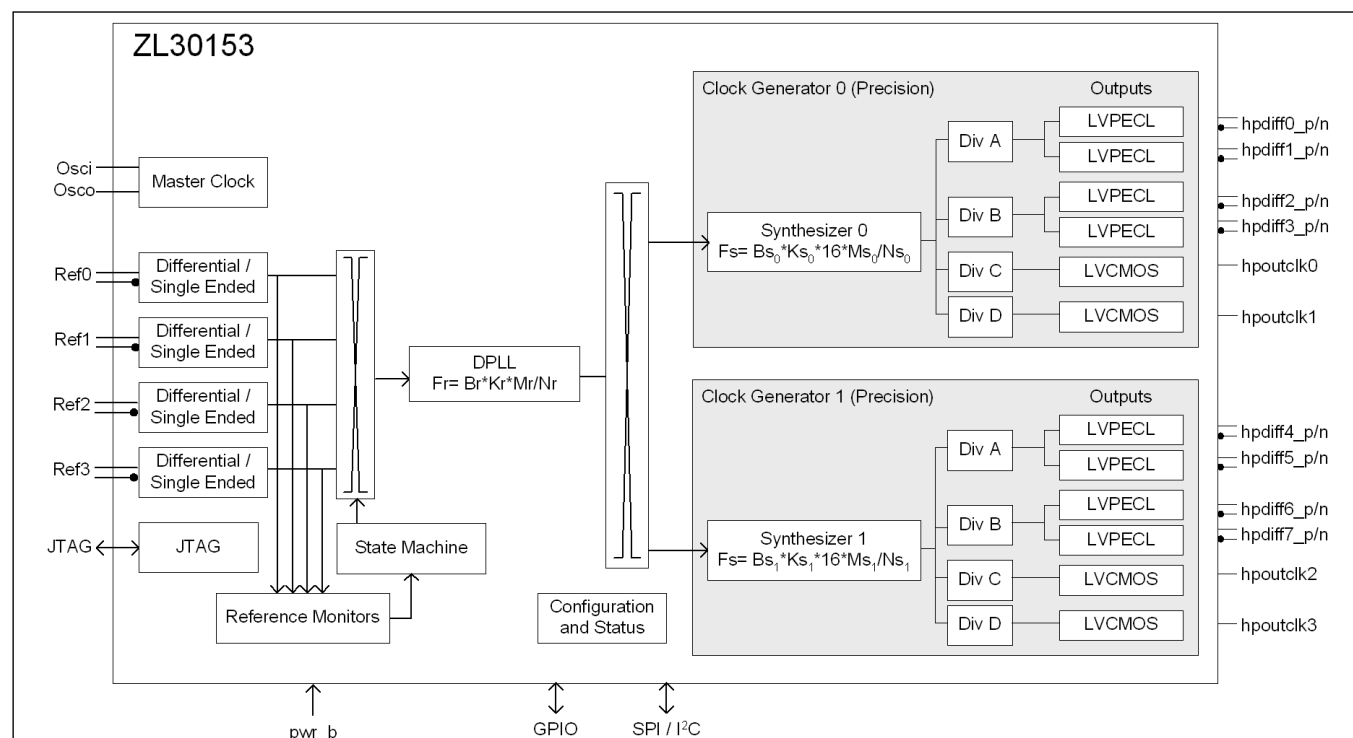
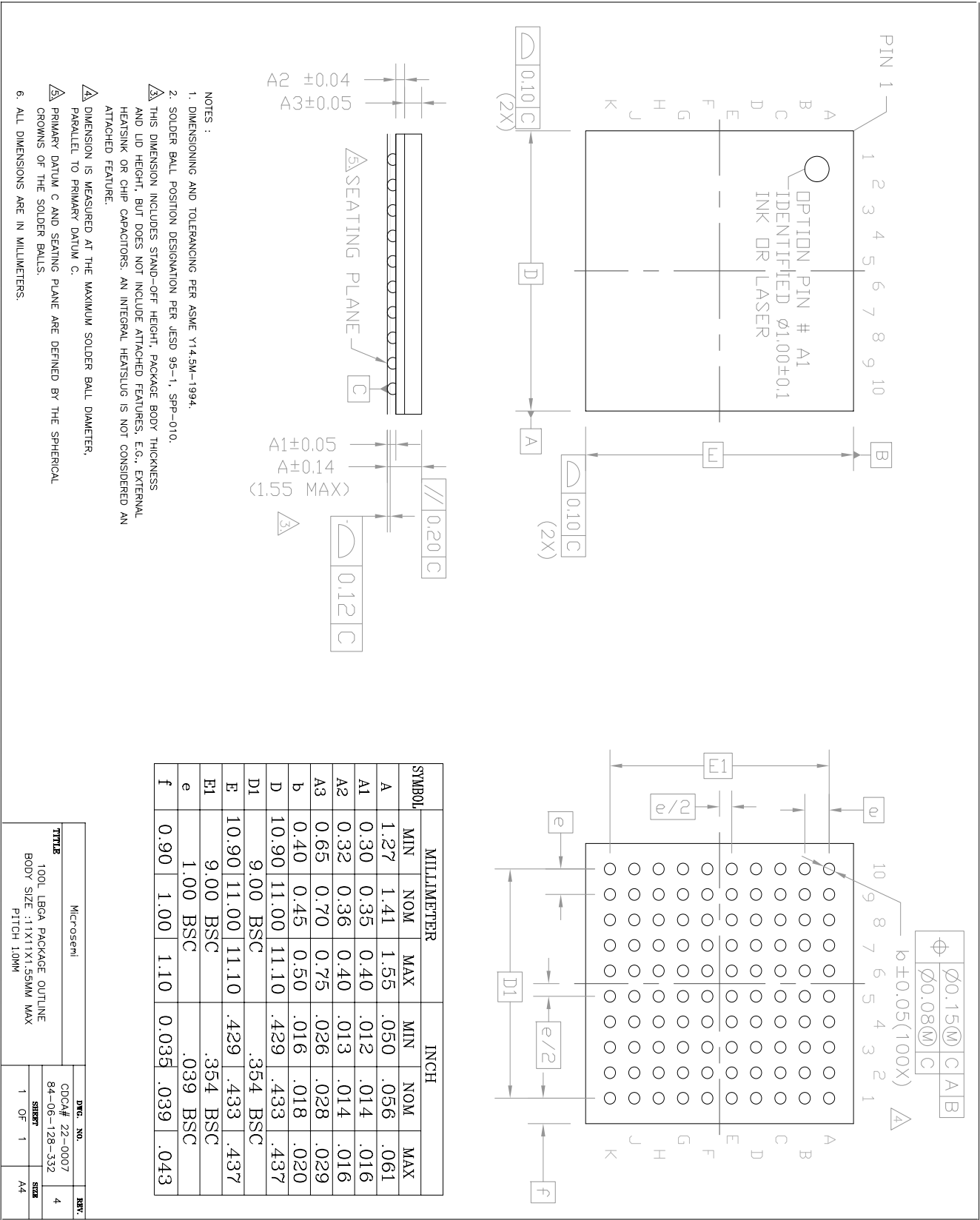


Figure 1 - Functional Block Diagram

Applications

- 10 Gigabit line cards
- Synchronous Ethernet, 10GBASE-R and 10GBASE-W
- OTN multiplexers and transponders
- SONET/SDH, Fibre Channel, XAUI

Mechanical Drawing





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