LM49350 Boomer® Audio Power Amplifier Series High Performance Audio Codec Sub-System with a Ground-Referenced Stereo Headphone Amplifier & an Ultra Low EMI Class D Loudspeaker Amplifier with Dual I²S/PCM Digital Audio Interfaces

Check for Samples: LM49350, LM49350RLEVAL

FEATURES

- High Performance 96dB SNR Stereo DAC
- High Performance 94dB SNR Stereo ADC
- Up to 192kHz Stereo Audio Playback
- Up to 48kHz Stereo Recording
- Dual Bidirectional I²S or PCM Compatible Audio Interfaces
- Read/Write I²C Compatible Control Interface
- Flexible Digital Mixer with Sample Rate Conversion
- Dual Sigma-Delta PLLs for Operation from any Clock at Any Sample rate
- Digital 3D Stereo Enhancement
- Dual 5 Band Parametric Equalizers
- Cascadable DSP Effects that Allow 10 Band Parametric Equalization
- ALC/Compressor/Limiter on Both DAC and ADC Paths
- Ultra Low EMI, Class D Loudspeaker Amplifier with Spread Spectrum Control
- Ground Referenced Output Cap-Less Headphone Amplifier Operation
- Earpiece Speaker Amplifier with Reduced Power Consumption Mode for Mono Differential Line out Applications
- Stereo Auxiliary Inputs or Mono Differential Input
- Differential Stereo Microphone Inputs with Single-Ended Option
- Automatic Level Control for Digital Audio Inputs, Stereo Microphone Inputs, and Stereo Auxiliary Inputs
- Flexible Audio Routing from Input to Output
- 16 Step Volume Control for Microphones with 2dB Steps
- 32 Step Volume Control for Auxiliary Inputs in 1.5dB Steps
- Micro-Power Shutdown Mode
- Available in the 3.5 x 3.5 mm 36 Bump DSBGA Package

APPLICATIONS

- Smart Phones
- Mobile Phones and VOIP Phones
- Portable GPS Navigator and Portable Gaming Devices
- Portable DVD/CD/AAC/MP3/MP4 Players
- Digital Cameras/Camcorders

KEY SPECIFICATIONS

- P_{HP} at A_V_{DD} = 3.3V, Stereo 32Ω, 1% THD 69mW/ch (typ)
- P_{LS} at LS_V_{DD} = 5V, 8Ω, 1% THD 1.2W (typ)
- P_{LS} at LS_V_{DD} = 4.2V, 8Ω, 1% THD 825mW (typ)
- P_{LS} at LS_V_{DD} = 3.3V, 8Ω, 1% THD 495mW (typ)
- P_{EP} at A_V_{DD} = 3.3V, 32Ω BTL, 1% THD 58mW (typ)
- Supply Voltage Range
  - D_V_{DD} = 1.7V to 2.0V
  - LS_V_{DD} and A_V_{DD} = 2.7V to 5.5V
  - I/O_V_{DD} = 1.6V to 4.5V
- SNR (Stereo DAC at 48kHz) 96dB (typ)
- SNR (Stereo ADC at 48kHz) 94dB (typ)
- PSRR at 217 Hz, A_V_{DD} = 3.3V, (HP from AUX) 97dB (typ)

DESCRIPTION

The LM49350 is a high performance audio subsystem that supports both analog and digital audio functions. The LM49350 includes a high quality stereo DAC, a high quality stereo ADC, a stereo headphone amplifier that supports ground referenced output cap-less operation, a dual mode earpiece speaker amplifier, and a low EMI Class D loudspeaker amplifier. It is designed for demanding applications in mobile phones and other portable devices.

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DESCRIPTION CONTINUED

The LM49350 features dual bi-directional I^2S or PCM audio interfaces for full range audio and an I^2C compatible interface for control. The stereo DAC path features an SNR of 96dB with 24-bit 48 kHz input. The headphone amplifier delivers $69mW_{RMS}$ (typ) to a 32Ω single-ended stereo load with less than 1% distortion (THD+N) when A_V_{DD} = 3.3V. The earpiece speaker amplifier delivers $58mW_{RMS}$ (typ) to a 32Ω bridged-tied load with less than 1% distortion (THD+N) when A_V_{DD} = 3.3V. The loudspeaker amplifier delivers up to 495mW into an 8Ω load with less than 1% distortion when LS_V_{DD} = 3.3V and up to 1.2W when LS_V_{DD} = 5.0V.

The LM49350 employs advanced techniques to reduce power consumption, to reduce controller overhead, to speed development time, and to eliminate click and pop. Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. It is therefore ideally suited for mobile phone and other low voltage applications where minimal power consumption, PCB area and cost are primary requirements.

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LM49350 Overview

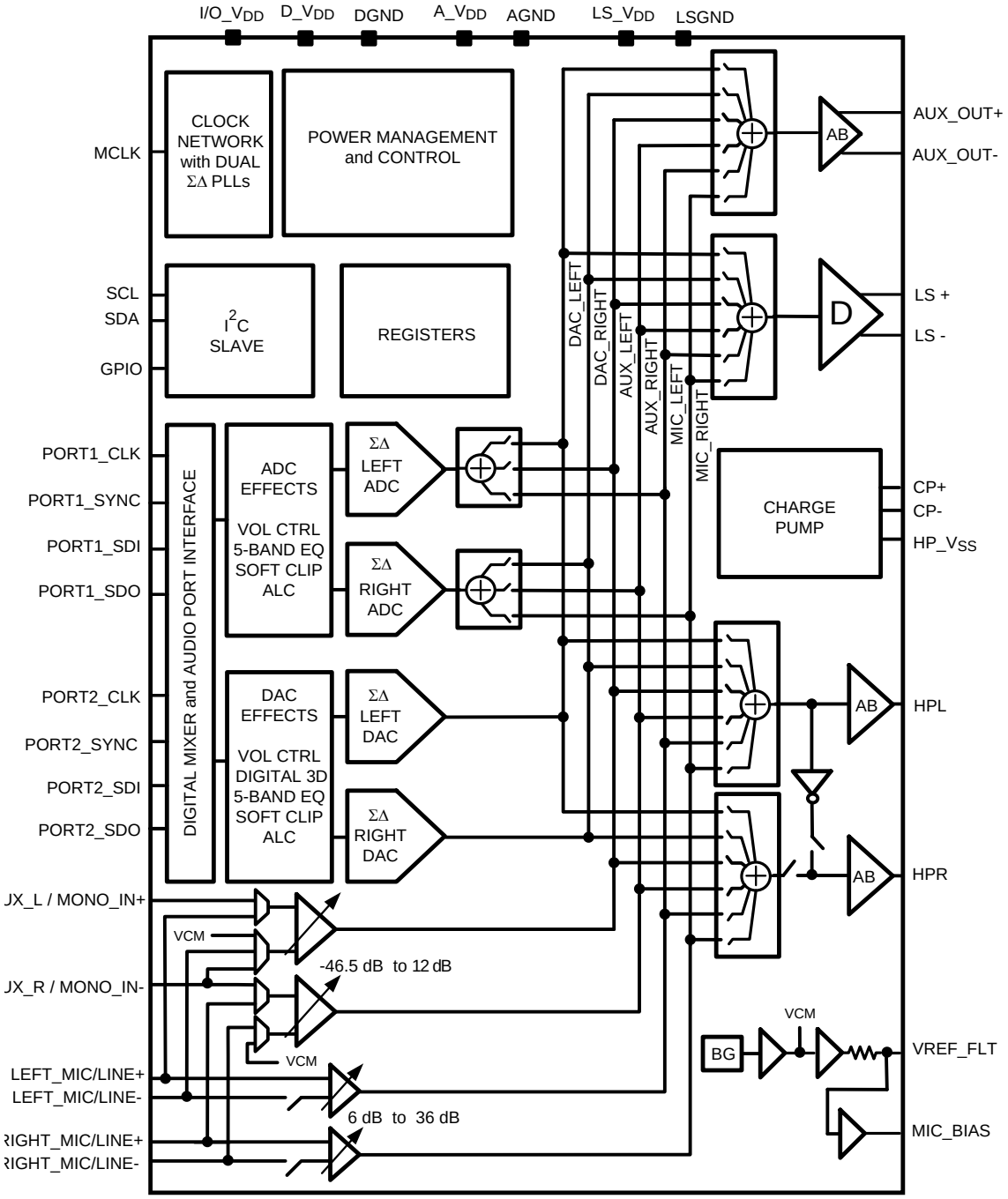


Figure 1. LM49350 Block Diagram

Typical Application

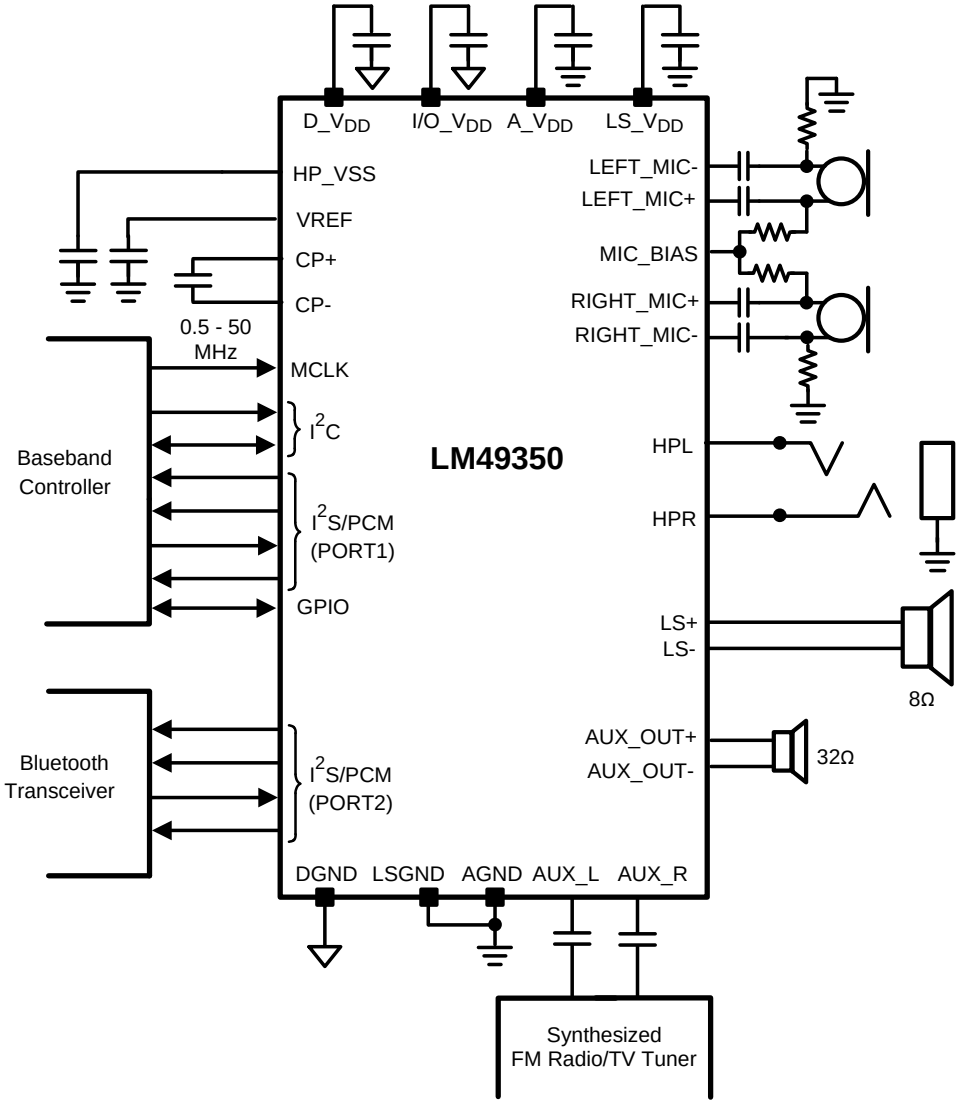


Figure 2. Example Application in Multimedia Phone with a Dedicated Earpiece and Mono Loudspeaker

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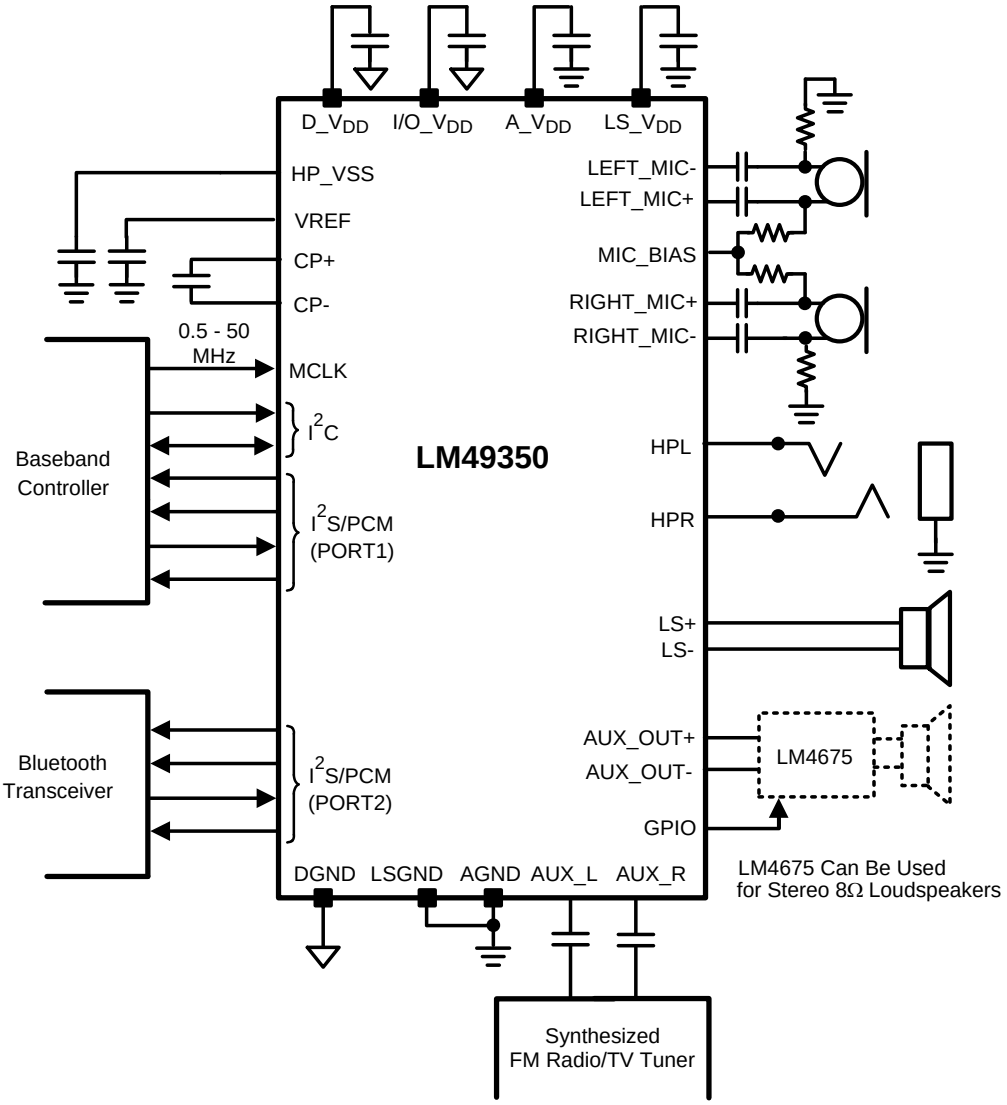


Figure 3. Example Application in Multimedia Phone Using Stereo Loudspeaker

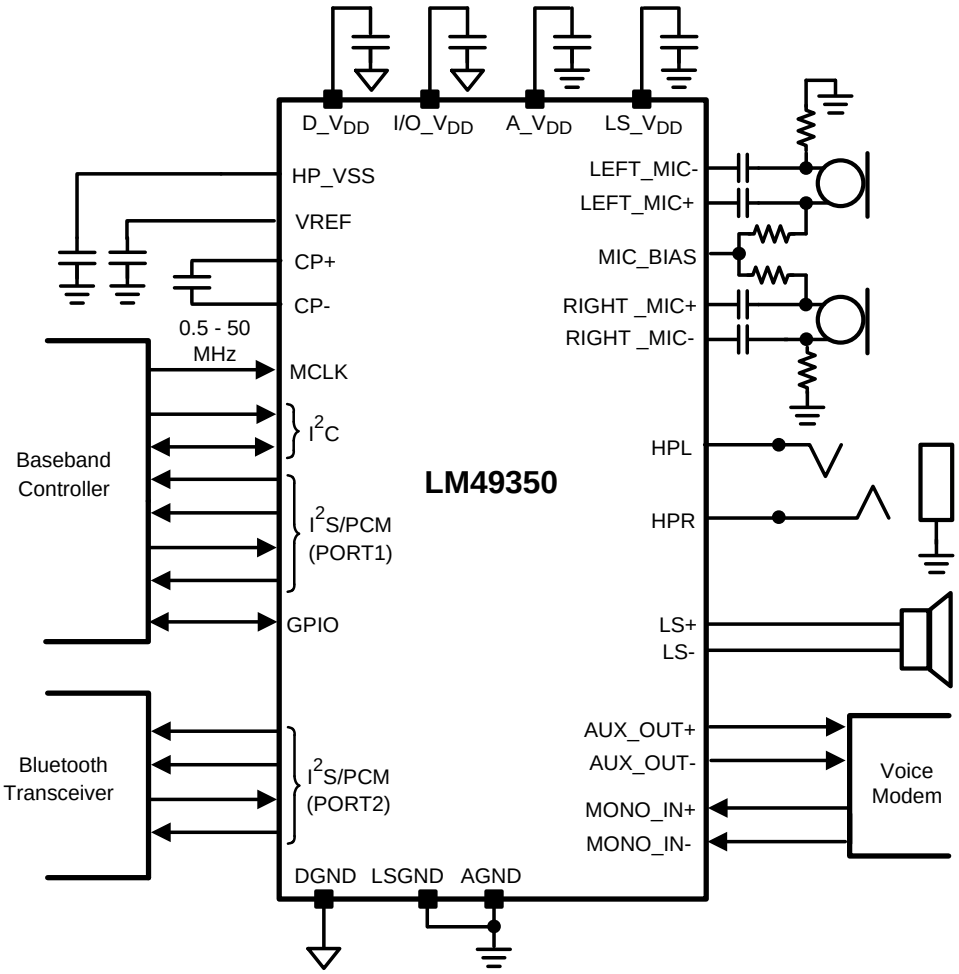


Figure 4. Example Application in a Multimedia Phone Using a Dedicated RF Module for Voice Modern Functions

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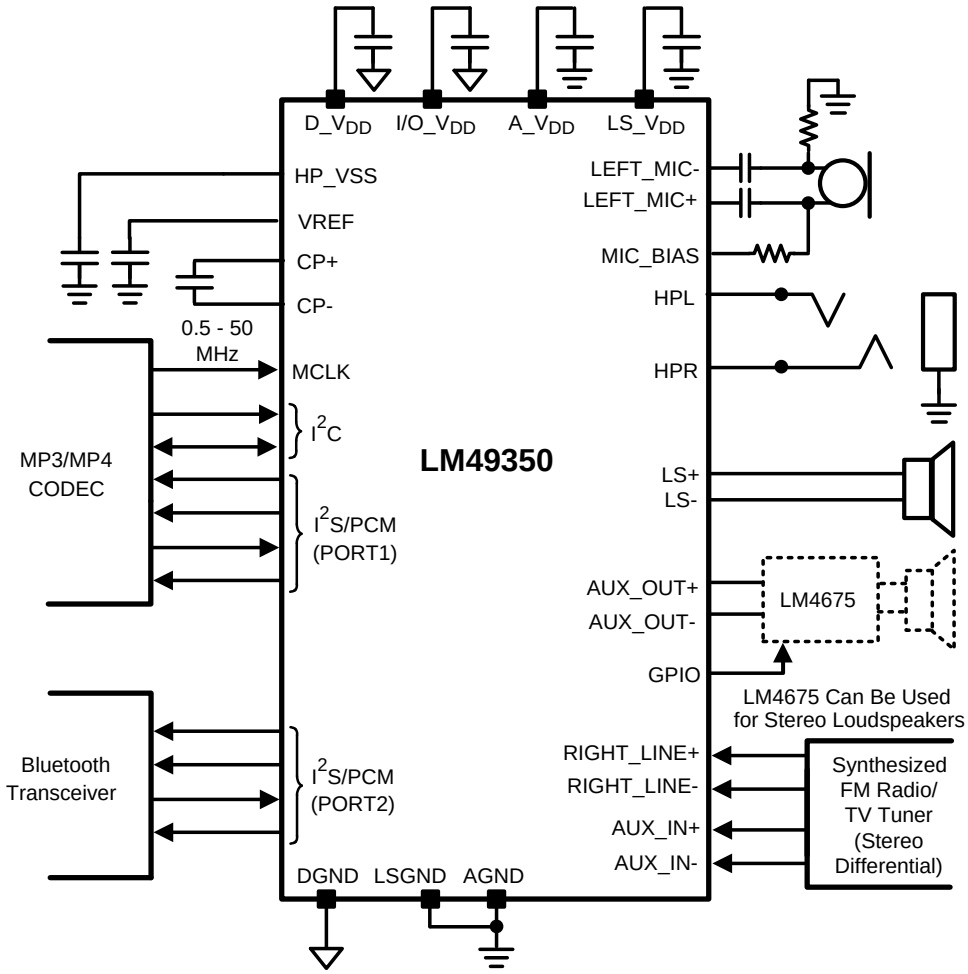


Figure 5. Example Application in a Portable Media Player with a Differential Stereo Line Input

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Connection Diagram

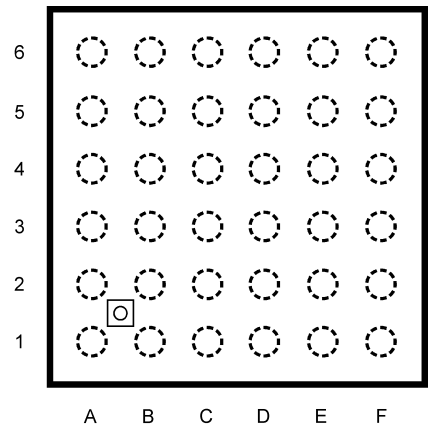


Figure 6. 36 Bump DSBGA
Top View (Bump Side Down)
See Package Number YPG0036TTA

PIN DESCRIPTIONS

Pin	Pin Name	Type	Direction	Description
A1	HPR	Analog	Output	Headphone right output
A2	A_V_{DD}	Supply	Input	Headphone and mixer power supply input
A3	AGND	Supply	Input	Headphone and mixer ground
A4	VREF_FLT	Analog	Input/Output	Filter point for the microphone power supply and internal references
A5	GPIO	Digital	Input/Output	General purpose input or output
A6	SDA	Digital	Input/Output	I^2C interface data line
B1	HPL	Analog	Output	Headphone left output
B2	AUX_R	Analog	Input	Right analog input
B3	AUX_L	Analog	Input	Left analog input
B4	PORT2_SYNC	Digital	Input/Output	Audio Port 2 SYNC Signal (can be master or slave)
B5	PORT2_SDI	Digital	Input	Audio Port 2 serial data input
B6	SCL	Digital	Input	I^2C interface clock line
C1	HP_V_{SS}	Analog	Output	Negative power supply pin for the headphone amplifier
C2	AUX_OUT+	Analog	Output	Auxiliary positive output
C3	AUX_OUT-	Analog	Output	Auxiliary negative output
C4	PORT2_SDO	Digital	Output	Audio port 2 serial data out
C5	PORT2_CLK	Digital	Input/Output	Audio port 2 clock signal (can be master or slave)
C6	MCLK	Digital	Input	Input clock from 0.5MHz to 50 MHz
D1	CP-	Analog	Input/Output	Charge pump flying capacitor negative input
D2	CP+	Analog	Input/Output	Charge pump flying capacitor positive input
D3	MIC_BIAS	Analog	Output	Microphone ultra clean supply (2.2V)
D4	PORT1_SYNC	Digital	Input/Output	Audio Port 1 sync signal (can be master or slave)
D5	PORT1_SDO	Digital	Output	Audio Port 1 serial data output
D6	DGND	Supply	Input	Digital ground
E1	LSGND	Supply	Input	Loudspeaker ground
E2	LS_V_{DD}	Supply	Input	Loudspeaker power supply input
E3	RIGHT_MIC-	Analog	Input	Right microphone negative input
E4	LEFT_MIC-	Analog	Output	Left microphone negative input
E5	PORT1_SDI	Digital	Input	Audio Port 1 serial data input

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PIN DESCRIPTIONS (continued)

Pin	Pin Name	Type	Direction	Description
E6	D_V_{DD}	Supply	Input	Digital power supply input
F1	LS +	Analog	Output	Loudspeaker positive output
F2	LS -	Analog	Output	Loudspeaker negative output
F3	RIGHT_MIC +	Analog	Input	Right microphone positive input
F4	LEFT_MIC +	Analog	Input	Left microphone positive input
F5	PORT1_CLK	Digital	Input/Output	Audio Port 1 clock signal (can be master or slave)
F6	I/O_V_{DD}	Supply	Input	Digital interface power supply input

PIN TYPE DEFINITIONS

Analog Input — A pin that is used by the analog and is never driven by the device. Supplies are part of this classification.

Analog Output — A pin that is driven by the device and should not be driven by external sources.

Analog Input/Output — A pin that is typically used for filtering a DC signal within the device. Passive components can be connected to these pins.

Digital Input — A pin that is used by the digital but is never driven by the device.

Digital Output — A pin that is driven by the device and should not be driven by another device to avoid contention.

Digital Input/Output — A pin that is either open drain (SDA) or a bidirectional CMOS in/out. In the latter case the direction is selected by a control register within the LM49350.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

Analog Supply Voltage (A_V_{DD} and LS_V_{DD})		6.0V
Digital Supply Voltage D_V_{DD}		2.2V
I/O Supply Voltage I/O_V_{DD}		5.5V
Storage Temperature		−65°C to +150°C
Power Dissipation(4)		Internally Limited
ESD Ratings	Human Body Model(5)	2000V
	Machine Model(6)	200V
Junction Temperature		150°C
Thermal Resistance θ_{JA} – YPG36 (soldered down to PCB with 2in^2 1oz. copper plane)		60°C/W
Soldering Information		See Applications Note AN-1112 (SNVA009).

(1) *"Absolute Maximum Ratings"* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

(2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.

(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.

(5) Human body model, applicable std. JESD22-A114C.

(6) Machine model, applicable std. JESD22-A115-A.

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OPERATING RATINGS

Temperature Range		−40°C to +85°C
Supply Voltage	A_V_{DD} and LS_V_{DD} (1)	2.7V to 5.5V
	D_V_{DD}	1.7V to 2.0V
	I/O_V_{DD}	1.6V to 4.5V

(1) LS_V_{DD} need to be the highest voltage than A_V_{DD}, D_V_{DD}, and I/O_V_{DD}. For proper power supply sequence, LS_V_{DD} need to be applied first.

ELECTRICAL CHARACTERISTICS: $A_V_{DD} = LS_V_{DD} = 3.3V$; $D_V_{DD} = I/O_V_{DD} = 1.8V$ (1) (2)

The following specifications apply for $R_{L(LS)} = 8\Omega$, $R_{L(HP)} = 32\Omega$, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM49350		Units (Limits)
			Typical (3)	Limit (4)	
DC CHARACTERISTICS (Digital current combines D_V_{DD} and I/O_V_{DD}. Analog current combines A_V_{DD} and LS_V_{DD})					
DI_{SD}	Digital Shutdown Current	Shutdown Mode, f_{MCLK} = 13MHz, PLL Off	2	15	µA (max)
DI_{ST}	Digital Standby Current	f_{MCLK} = 12.288MHz, PMC On only	0.25	1	mA (max)
DI_{DD}	Digital Active Current (MP3 Mode)	f_{MCLK} = 11.2896MHz, f_S = 44.1kHz, Stereo DAC On, OSR_{DAC} = 128, PLL Off, HP On	0.9	2	mA (max)
	Digital Active Current (FM Mode)	f_{MCLK} = 13MHz Analog Audio modes	0.2	0.5	mA (max)
	Digital Active Current (FM Record Mode)	f_{MCLK} = 12.288MHz, f_S = 48kHz, Stereo ADC On, OSR_{ADC} = 128, PLL Off, Stereo Analog Inputs On	1.5	2	mA (max)
	Digital Active Current (CODEC Mode)-	f_{MCLK} = 11.2896MHz, f_S = 44.1kHz, Mono ADC On, Stereo DAC On, OSR = 128, PLL Off, MIC On	2.7	3.8	mA (max)
AI_{SD}	Analog Shutdown Current	Shutdown Mode	0.3	5	µA (max)
AI_{ST}	Analog Standby Quiescent Current	Reference Voltages On only	0.85	1.5	mA (max)
AI_{DD}	Analog Supply Current (MP3 Mode)	f_{MCLK} = 11.2896MHz, f_S = 44.1kHz, Stereo DAC On, OSR_{DAC} = 128, PLL Off, HP On	7.8	10	mA (max)
	Analog Supply Current (FM Mode)	Stereo Analog Inputs On, HP On	5.3	7	mA (max)
	Analog Supply Current (FM Record Mode)	f_{MCLK} = 12.288MHz, f_S = 48kHz, Stereo ADC On, OSR_{ADC} = 128, PLL Off, Stereo Analog Inputs On	9.8	12	mA (max)
	Analog Supply Current (CODEC Mode)	f_{MCLK} = 11.2896MHz, f_S = 44.1kHz, Mono ADC On, Stereo DAC On, OSR = 128, PLL Off, MIC On	13	15	mA (max)
$PLLI_{DD}$	PLL Total Active Current	f_{MCLK} = 13MHz, f_{PLLOUT} = 12MHz, PLL On only	2.9	5.5	mA (max)
HPI_{DD}	Headphone Quiescent Current	Stereo HP On only	3.5		mA
LSI_{DD}	Loudspeaker Quiescent Current	LS On only	2.9		mA
$MICI_{DD}$	Microphone Quiescent Current	mono MIC + MIC Bias On	0.5		mA
$ADCI_{DD}$	ADC Total Active Current	f_S = 48kHz, Stereo	9		mA
$DACI_{DD}$	DAC Total Active Current	f_S = 48kHz, Stereo	5.5		mA

(1) *"Absolute Maximum Ratings"* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

(2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.

(3) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.

(4) Datasheet min/max specification limits are specified by test or statistical analysis.

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ELECTRICAL CHARACTERISTICS: A_V_{DD} = LS_V_{DD} = 3.3V; D_V_{DD} = I/O_V_{DD} = 1.8V[1][2] (continued)

The following specifications apply for $R_{L(LS)}$ = 8Ω, $R_{L(HP)}$ = 32Ω, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM49350		Units (Limits)
			Typical[3]	Limit[4]	
$AUXINI_{DD}$	Auxiliary Input Amplifier Quiescent Current	Stereo Auxiliary Inputs enabled	0.7		mA
$AUXOUTI_{DD}$	Auxiliary Output Amplifier Quiescent Current	AUX_LINE_OUT enabled	0.5		mA
		Earpiece mode enabled	1.0		mA
LOUDSPEAKER AMPLIFIER					
LS_{EFF}	Loudspeaker Efficiency	P_O = 400mW, R_L = 8Ω	83		%
THD+N	Total Harmonic Distortion + Noise	P_O = 400mW, f = 1kHz, R_L = 8Ω, Mono Input Signal	0.07		%
P_O	Output Power	R_L = 8Ω, f = 1kHz, THD+N = 1%, Mono Input Signal			
		LS_V_{DD} = 3.3V LS_V_{DD} = 4.2V LS_V_{DD} = 5V	495 825 1.2	400	mW (min) mW W
		R_L = 4Ω, f = 1kHz, THD+N = 1%, Mono Input Signal			
		LS_V_{DD} = 3.3V LS_V_{DD} = 4.2V LS_V_{DD} = 5V	800 1.4 2		mW W W
PSRR	Power Supply Rejection Ration	V_{RIPPLE} = 200mV_{P-P} f_{RIPPLE} = 217Hz Mono Input Terminated V_{REF} = 1.0µF	73	55	dB (min)
SNR	Signal-to-Noise Ratio	Reference = V_{OUT} (1% THD+N) Gain = 0dB, A-weighted Mono Input Terminated	95	85	dB (min)
e_{OS}	Output Noise	Gain = 0dB, A-weighted, Mono Input Terminated	35		µV
V_{OS}	Offset Voltage	Gain = 0dB, form Mono Input	10	50	mV (max)
T_{WU}	Turn-On Time	PMC Clock = 300kHz	28		ms
HEADPHONE AMPLIFIERS					
THD+N	Total Harmonic Distortion + Noise	P_O = 7.5mW, f = 1kHz, R_L = 32Ω Stereo Analog Input Signal	0.025	0.1	% (max)
P_O	Headphone Output Power	R_L = 32Ω, f = 1kHz, THD+N = 1%, Stereo Analog Input Signal	69	60	mW (min)
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{P-P}, f_{RIPPLE} = 217Hz Stereo Analog Inputs Terminated, V_{REF} = 1.0µF, Mono Differential Input Mode	97	75	dB (min)
SNR	Signal-to-Noise Ratio	Reference = V_{OUT} (1% THD+N) Gain = 0dB, A-weighted Stereo Inputs Terminated	106	98	dB (min)
		Reference = V_{OUT} (0dBFS) Gain = 0dB, A-weighted, I^2S Input = Digital Zero	96	90	dB (min)
e_{OS}	Output Noise	Gain = 0dB, A-weighted, Stereo Inputs Terminated	8		µV
		Gain = 0dB, A-weighted, I^2S Input = Digital Zero	16		µV
X_{TALK}	Crosstalk	P_O = 60mW, f = 1kHz, R_L = 32Ω Stereo Analog Input Signal	71		dB
ΔA_{CH-CH}	Channel-to-Channel Gain Matching		0.03		dB

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ELECTRICAL CHARACTERISTICS: A_V_{DD} = LS_V_{DD} = 3.3V; D_V_{DD} = I/O_V_{DD} = 1.8V[1][2] (continued)

The following specifications apply for $R_{L(LS)}$ = 8Ω, $R_{L(HP)}$ = 32Ω, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM49350		Units (Limits)
			Typical[3]	Limit[4]	
V_{OS}	Output Offset Voltage	AUX Gain = 0dB From Differential Mono Input	0.5	6	mV (max)
		DAC Gain = 0dB, From DAC Input f_{MCLK} = 12.288MHz, PLL off	1	6	mV (max)
T_{WU}	Turn-On Time	PMC Clock = 300kHz	28		ms
AUXILIARY OUTPUTS					
THD+N	Total Harmonic Distortion + Noise	AUX_LINE_OUT R_L = 5kΩ, V_{OUT} = $1V_{RMS}$	0.004		%
		Earpiece mode, f = 1kHz R_L = 32Ω BTL, P_{OUT} = 20mW	0.08		%
P_{OUT}	Output Power	Earpiece mode, f = 1kHz R_L = 32Ω BTL, THD+N = 1%	58	45	mW (min)
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = $200mV_{P-P}$, f_{RIPPLE} = 217Hz Mono Input terminated, C_{REF} = 1µF AUX_LINE_OUT	100		dB
		V_{RIPPLE} = $200mV_{P-P}$, f_{RIPPLE} = 217Hz Mono Input terminated, C_{REF} = 1µF Earpiece mode	94	62	dB (min)
SNR	Signal-to-Noise Ratio	Gain = 0dB, V_{REF} = V_{OUT} (1%THD+N) A-weighted, Mono Input Terminated	100		dB
$\in_{OUT}$	Output Noise	Gain = 0dB, V_{REF} = V_{OUT} (1%THD+N) A-weighted, Mono Input Terminated	13		µV
V_{OS}	Output Offset Voltage	Gain = 0dB, From Mono Input AUX_LINE_OUT	7		mV
		Gain = 0dB, From Mono Input Earpiece mode	3	15	mV (max)
T_{WU}	Turn-On Time	PMC Clock = 300kHz	28		ms
STEREO ADC					
$THD+N_{ADC}$	ADC Total Harmonic Distortion + Noise	Differential Line Input V_{IN} = $200mV_{RMS}$, f = 1kHz Gain = 0dB	0.03		%
PB_{ADC}	ADC Passband	HPF On, f_S = 48kHz Lower -3dB Point	300		Hz
		HPF On, Upper -3dB Point	$0.41*f_S$		kHz
R_{ADC}	ADC Ripple	ADC Compensated	0.1		dB
SNR_{ADC}	ADC Signal-to-Noise Ratio	Reference = V_{OUT} (0dBFS) Gain = 6dB, A-weighted From MIC, f_S = 8kHz	90		dB
		Reference = V_{OUT} (0dBFS) Gain = 0dB, A-weighted From Stereo Input, f_S = 48kHz	94		dB
ADC_{LEVEL}	ADC Full Scale Input Level		1		V_{RMS}
STEREO DAC					
$THD+N_{DAC}$	DAC Total Harmonic Distortion + Noise	I^2S Input V_{IN} = $500mFFS_{RMS}$, f = 1kHz Gain = 0dB	0.05		%
DAC_{LEVEL}	DAC Full Scale Output Level		1		V_{RMS}
R_{DAC}	DAC Ripple		0.1		dB
PB_{DAC}	DAC Passband	Upper –3dB Point	$0.45*f_S$		kHz
SNR_{DAC}	DAC Signal-to-Noise Ratio	f_S = 48kHz, A-weighted	96		dB

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ELECTRICAL CHARACTERISTICS: A_V_{DD} = LS_V_{DD} = 3.3V; D_V_{DD} = I/O_V_{DD} = 1.8V[1][2] (continued)

The following specifications apply for $R_{L(LS)}$ = 8Ω, $R_{L(HP)}$ = 32Ω, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM49350		Units (Limits)
			Typical[3]	Limit[4]	
MIC BIAS					
V_{BIAS}	Microphone Bias Voltage	MIC input selected	2.2		V
VOLUME CONTROL					
VCR_{AUX}	Stereo Input Volume Control Range	Minimum Gain	–46.5		dB
		Maximum Gain	12		dB
VCR_{DAC}	DAC Volume Control Range	Minimum Gain	–76.5		dB
		Maximum Gain	18		dB
VCR_{ADC}	ADC Volume Control Range	Minimum Gain	–76.5		dB
		Maximum Gain	18		dB
VCR_{MIC}	MIC Volume Control Range	Minimum Gain	6		dB
		Maximum Gain	36		dB
SS_{AUX}	AUX Volume Control Stepsize		1.5		dB
SS_{DAC}	DAC Volume Control Stepsize		1.5		dB
SS_{ADC}	DAC Volume Control Stepsize		1.5		dB
SS_{MIC}	MIC Volume Control Stepsize		2		dB
SV_{AUX}	AUX Volume Setting Variation			±1	dB (max)
SV_{MIC}	MIC Volume Setting Variation			±1	dB (max)
ANALOG INPUTS					
$AUXR_R_{IN}$	Right Auxiliary Input Impedance	AUXR Gain = 12dB	17.5		kΩ
		AUXR Gain = 0dB	38		kΩ
		AUXR Gain = –46.5dB	64		kΩ
$AUXL_R_{IN}$	Right Auxiliary Input Impedance	AUXL Gain = 12dB	17.5		kΩ
		AUXL Gain = 0dB	38		kΩ
		AUXL Gain = –46.5dB	64		kΩ
$MICR_R_{IN}$	Right Microphone Input Impedance	All MIC gain settings	50		kΩ
$MICL_R_{IN}$	Left Microphone Input Impedance	All MIC gain settings	50		kΩ

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TIMING CHARACTERISTICS: DV_{DD} = I/OV_{DD} = 1.8V(1)(2)

The following specifications apply for $R_{L(SP)}$ = 8Ω, $R_{L(HP)}$ = 32Ω, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM49350		Units (Limits)
			Typical(3)	Limit(4)	
PLL					
f_{IN}	PLL Input Frequency Range	Minimum MCLK Frequency		0.5	MHz (min)
		Maximum MCLK Frequency		50	MHz (max)
DIGITAL AUDIO INTERFACE TIMING					
t_{BCLKR}	BCK rise time			3	ns (max)
t_{BCLKCF}	BCK fall time			3	ns (max)
t_{BCLKDS}	BCK duty cycle		50		%
t_{DL}	WS Propagation Delay from BCK falling edge			10	ns (max)
t_{DST}	DATA Setup Time to BCK Rising Edge			10	ns (min)
t_{DHT}	DATA Hold Time from BCK Rising Edge			10	ns (min)
CONTROL INTERFACE TIMING					
	SCL Frequency			400	kHz (max)
1	Hold Time (repeated START Condition)			0.6	µs (min)
2	Clock Low Time			1.3	µs (min)
3	Clock High Time			600	ns (min)
4	Setup Time for a Repeated START Condition			600	ns (min)
5	Data Hold Time	Output		300 900	ns (min) ns (max)
		Input		0 900	ns (min) ns (max)
6	Data Setup Time			100	ns (min)
7	Rise Time of SDA and SCL			$20+0.1C_B$ 300	ns (min) ns (max)
8	Fall Time SDA and SCL			$15+0.1C_B$ 300	ns (min) ns (max)
9	Setup Time for STOP Condition			600	ns (min)
10	Bus Free Time Between a STOP and START Condition			1.3	µs (min)
C_B	Bus Capacitance			10 200	pF (min) pF(max)

(1) *"Absolute Maximum Ratings"* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

(2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.

(3) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.

(4) Datasheet min/max specification limits are specified by test or statistical analysis.

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TIMING CHARACTERISTICS: DV_{DD} = I/OV_{DD} = 1.8V(1)(2)

The following specifications apply for $R_{L(SP)}$ = 8Ω, $R_{L(HP)}$ = 32Ω, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM49350		Units (Limit)
			Typical(3)	Limit(4)	
PLL					
f_{IN}	PLL Input Frequency Range	Minimum MCLK Frequency		0.5	MHz (min)
		Maximum MCLK Frequency		50	MHz (max)
I^2S MASTER TIMING					
$I2S_CLK_{PER}$	I2S_CLK Period	I^2S Master	81.38		ns
tCLK_L	I2S_CLK Low Time	I^2S Master	37		ns
tCLK_H	I2S_CLK High Time	I^2S Master	37		ns
t_{WS_DLY}	WS Propagation Delay from I2S_CLK falling edge	I^2S Master	21		ns
t_{SDO_DLY}	SDO Propagation Delay from I2S_CLK falling edge	I^2S Master	21		ns
t_{DST}	SDI Setup Time to I2S_CLK Rising Edge	I^2S Master	20		ns
t_{DHT}	SDI Hold Time to I2S_CLK Rising Edge	I^2S Master	20		ns
I^2S SLAVE TIMING					
$I2S_CLK_{PER}$	I2S_CLK Period	I^2S Slave		81.38	ns (min)
tCLK_L	I2S_CLK Low Time	I^2S Slave		37	ns (min)
tCLK_H	I2S_CLK High Time	I^2S Slave		37	ns (min)
t_{SDO_DLY}	SDO Propagation Delay from I2S_CLK falling edge	I^2S Slave	21		ns
t_{DST}	SDI Setup Time to I2S_CLK Rising Edge	I^2S Slave		20	ns (min)
t_{DHT}	SDI Hold Time to I2S_CLK Rising Edge	I^2S Slave		20	ns (min)
t_{WS_ST}	WS Setup Time to I2S_CLK Rising Edge	I^2S Slave		20	ns (min)
t_{WS_HT}	WS Hold Time to I2S_CLK Rising Edge	I^2S Slave		20	ns (min)

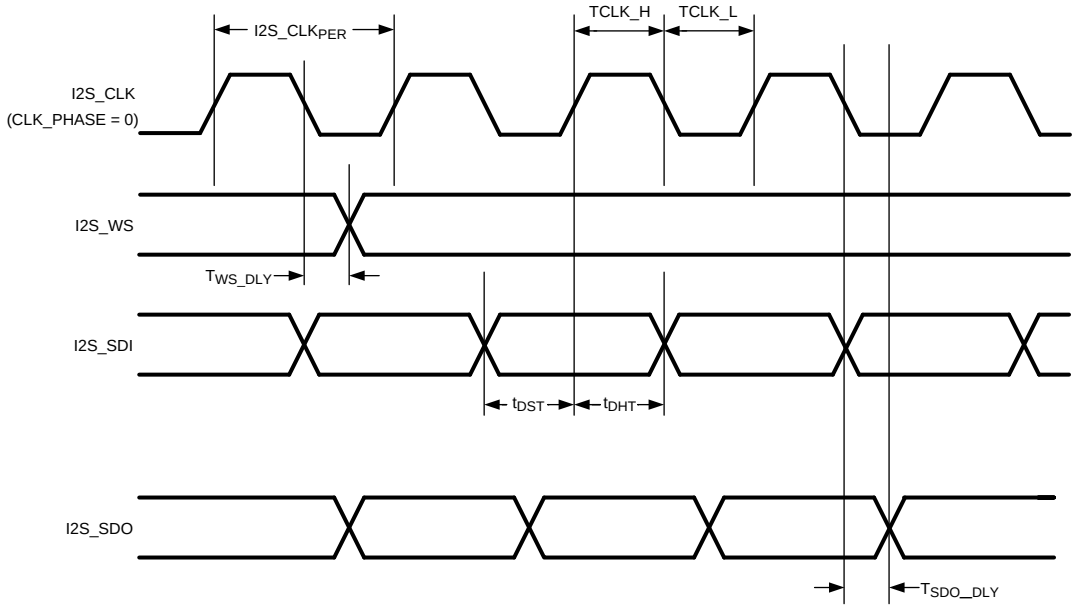
(1) *"Absolute Maximum Ratings"* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

(2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.

(3) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.

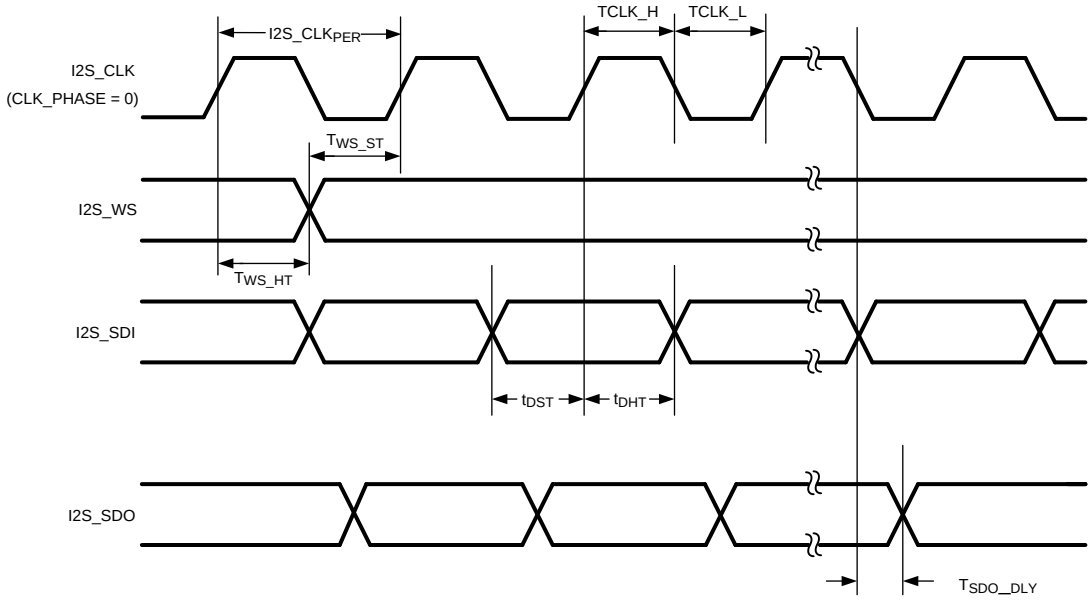
(4) Datasheet min/max specification limits are specified by test or statistical analysis.

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w = write (SDA = “0”)
r = read (SDA = “1”)
ack = acknowledge (SDA pulled down by slave)
rs = repeated start

Figure 7. Timing for I²S Master



w = write (SDA = “0”)
r = read (SDA = “1”)
ack = acknowledge (SDA pulled down by slave)
rs = repeated start

Figure 8. Timing for I²S Slave

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TYPICAL PERFORMANCE CHARACTERISTICS

DAC Frequency Response
f_S = 48kHz, OSR = 128

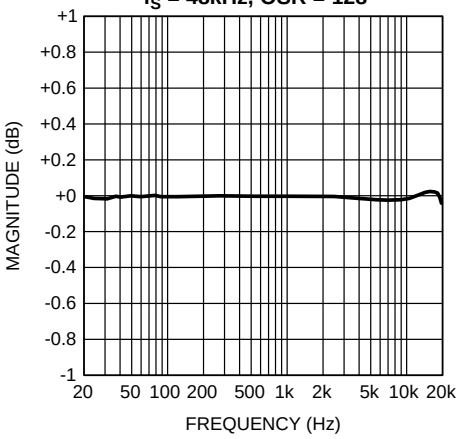


Figure 9.

DAC Frequency Response
f_S = 8kHz, OSR = 128

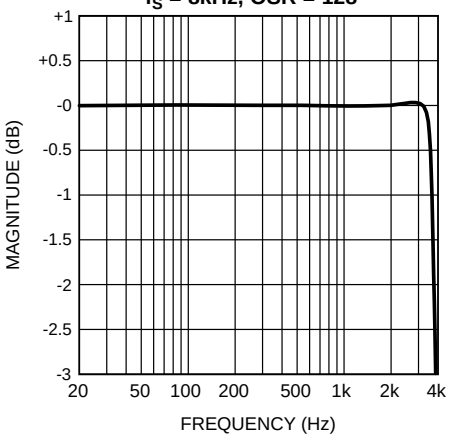


Figure 10.

Stereo Audio ADC Frequency Response
f_S = 48kHz, OSR = 128, C_{IN} = 1µF, MIC gain = 6dB

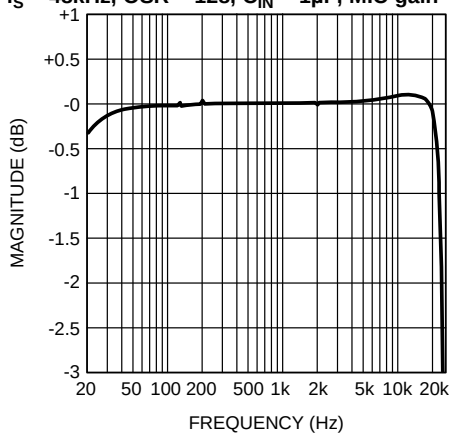


Figure 11.

Stereo Audio ADC Frequency Response
f_S = 8kHz, OSR = 128, C_{IN} = 1µF, MIC gain = 6dB

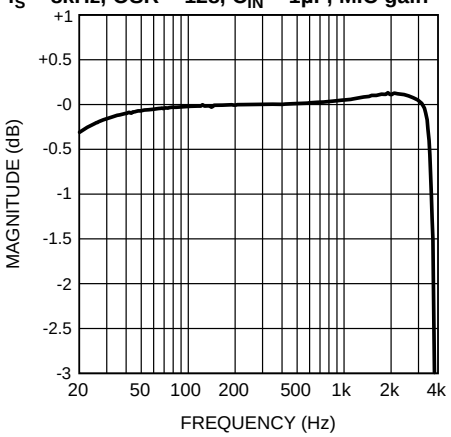


Figure 12.

Stereo Audio ADC HPF Frequency Response
f_S = 48kHz, OSR = 128, C_{IN} = 1µF, MIC gain = 6dB
(Top-No HPF, Upper-HPF_Mode = '101',
Lower-HPF_Mode = '110)'
Bottom-HPF_Mode = '111'

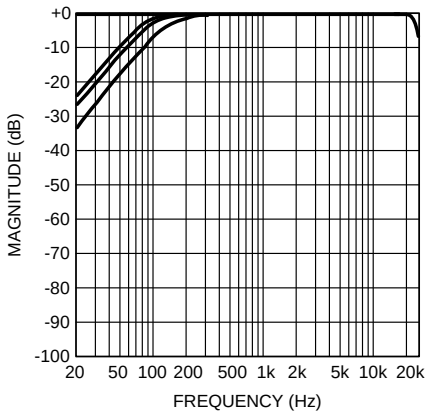


Figure 13.

Mono Voice ADC Frequency Response
f_S = 48kHz, OSR = 128, C_{IN} = 1µF, MIC gain = 6dB

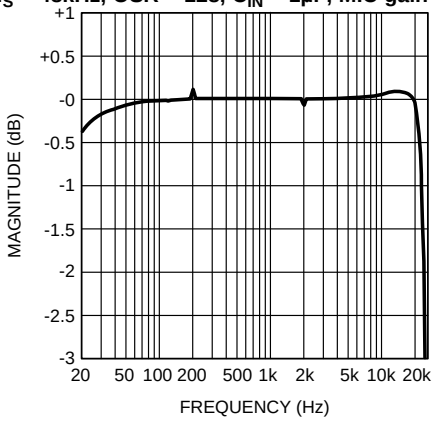


Figure 14.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Mono Voice ADC Frequency Response
f_S = 8kHz, OSR = 128, C_{IN} = 1µF, MIC gain = 6dB

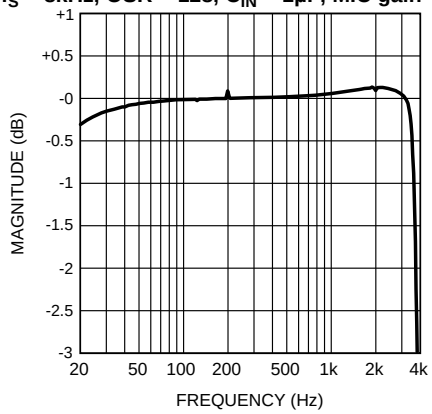


Figure 15.

Mono Voice ADC HPF Frequency Response
f_S = 48kHz, OSR = 128, C_{IN} = 1µF, MIC gain = 6dB
(Top-No HPF)
(From Left to Right:
HPF_Mode = '000', '001', '010', '011', '100')

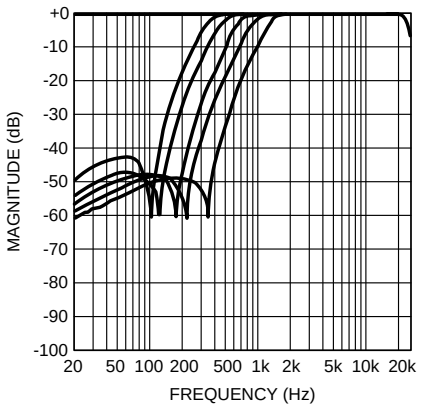


Figure 16.

Mono Voice ADC HPF Frequency Response
f_S = 8kHz, OSR = 128, C_{IN} = 1µF, MIC gain = 6dB
(Top-No HPF)
(From Left to Right:
HPF_Mode = '000', '001', '010', '011', '100')

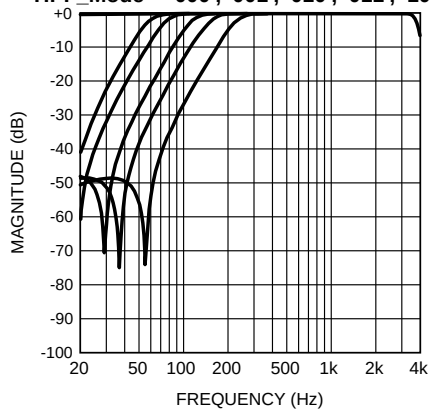


Figure 17.

ADC Output THD+N vs Frequency
Differential Line Input, Aux Gain = 0dB
V_{IN} = 200mV_{RMS}, f_S = 48kHz

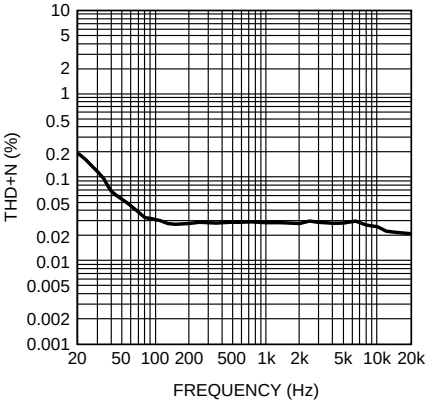


Figure 18.

ADC Output THD+N vs Frequency
Differential MIC Input, MIC Gain = 6dB
V_{IN} = 100mV_{RMS}, f_S = 48kHz

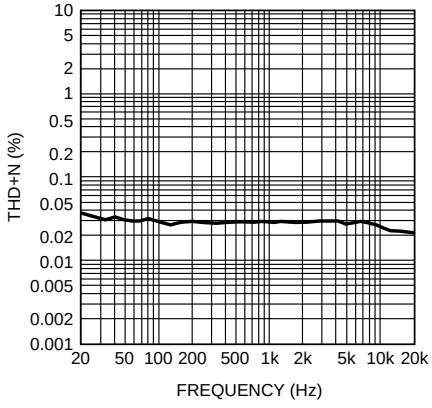


Figure 19.

ADC Output THD+N vs V_{IN}
Differential Line Input, Aux Gain = 0dB
V_{IN} = 1kHz, f_S = 48kHz

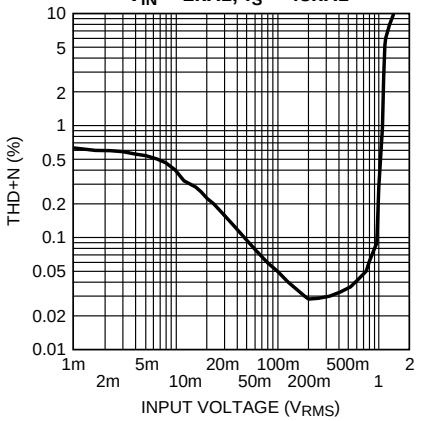


Figure 20.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

ADC Output THD+N vs V_{IN}
Differential MIC Input, MIC Gain = 6dB
V_{IN} = 1kHz, f_S = 48kHz

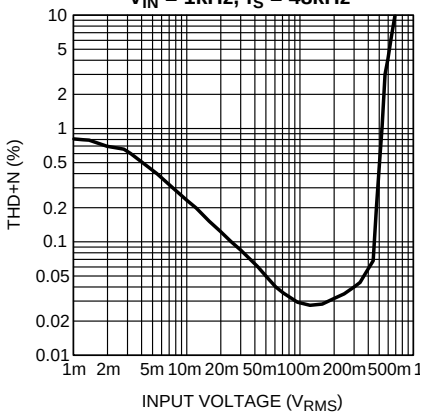


Figure 21.

Loudspeaker THD+N vs Frequency
Differential Aux Input, Aux Gain = 0dB
V_{DD} = 3.3V, P_{OUT} = 400mW, R_L = 8Ω

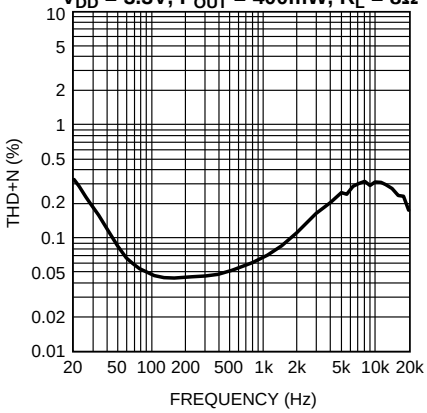


Figure 22.

Loudspeaker THD+N vs Frequency
Differential Aux Input, Aux Gain = 0dB
V_{DD} = 5V, P_{OUT} = 400mW, R_L = 8Ω

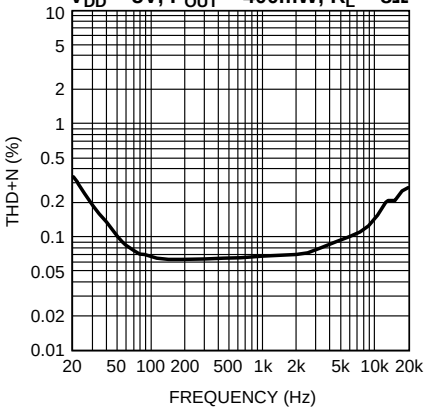


Figure 23.

Loudspeaker THD+N vs Frequency
Differential Aux Input, Aux Gain = 0dB
LS_V_{DD} = 3.3V, P_{OUT} = 500mW, R_L = 4Ω

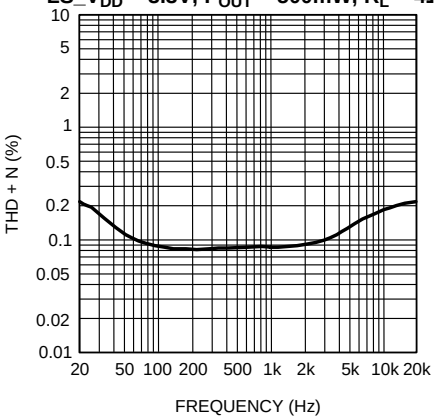


Figure 24.

Loudspeaker THD+N vs Output Power
Differential Aux Input, Aux Gain = 0dB
V_{DD} = 3.3V, V_{IN} = 1kHz, R_L = 8Ω

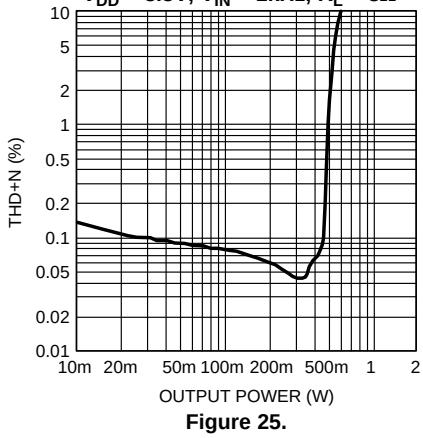


Figure 25.

Loudspeaker THD+N vs Output Power
Differential Aux Input, Aux Gain = 0dB
V_{DD} = 4.2V, V_{IN} = 1kHz, R_L = 8Ω

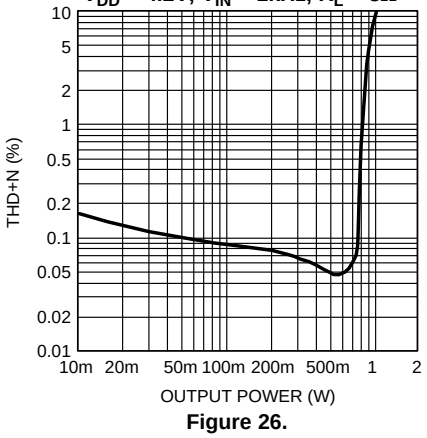


Figure 26.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Loudspeaker THD+N vs Output Power
Differential Aux Input, Aux Gain = 0dB
V_{DD} = 5V, V_{IN} = 1kHz, R_L = 8Ω

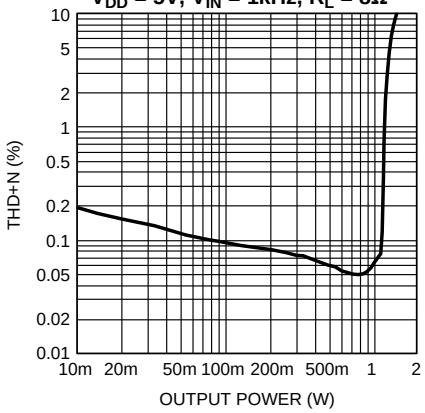


Figure 27.

Loudspeaker THD+N vs Output Power
Differential Aux Input, Aux Gain = 0dB
LS_V_{DD} = 3.3V, R_L = 4Ω, f = 1kHz

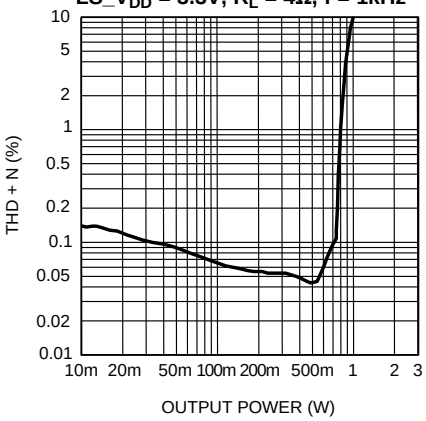


Figure 28.

Loudspeaker THD+N vs Output Power
Differential Aux Input, Aux Gain = 0dB
LS_V_{DD} = 4.2V, R_L = 4Ω, f = 1kHz

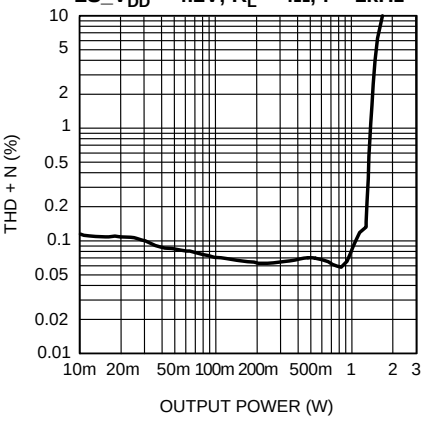


Figure 29.

Loudspeaker THD+N vs Output Power
Differential Aux Input, Aux Gain = 0dB
LS_V_{DD} = 5V, R_L = 4Ω, f = 1kHz

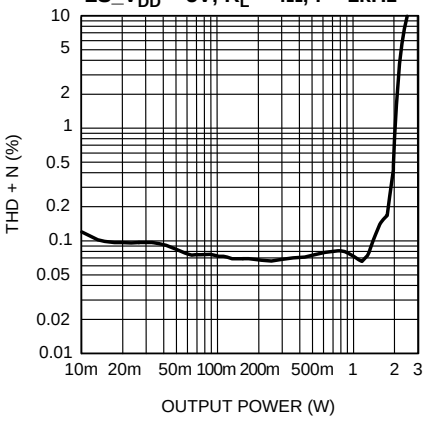


Figure 30.

Loudspeaker PSRR vs Frequency
LS_V_{DD} = 3.3V, Aux Gain = 0dB
Differential Aux Input to Ground
V_{RIPPLE} = 200mV_{PP}

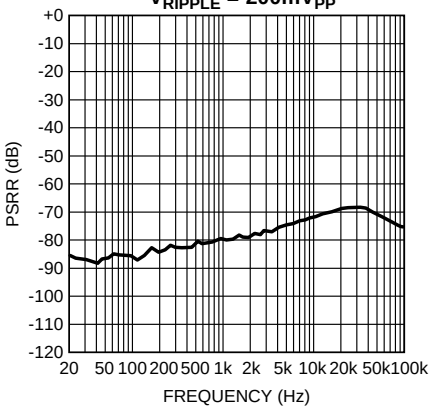


Figure 31.

Loudspeaker PSRR vs Frequency
LS_V_{DD} = 4.2V, Aux Gain = 0dB
Differential Aux Input to Ground
V_{RIPPLE} = 200mV_{PP}

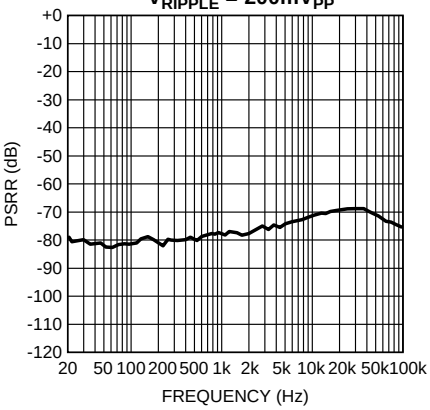


Figure 32.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Loudspeaker PSRR vs Frequency
LS_V_{DD} = 5V, Aux Gain = 0dB
Differential Aux Input to Ground
V_{RIPPLE} = 200mV_{PP}

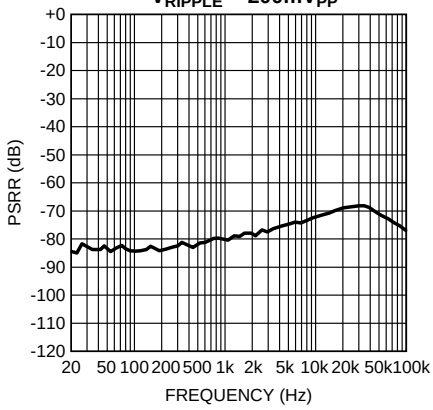


Figure 33.

Headphone THD+N vs Frequency
Stereo Aux Input, Aux Gain = 0dB
V_{DD} = 3.3V, P_{OUT} = 7.5mW, R_L = 32Ω

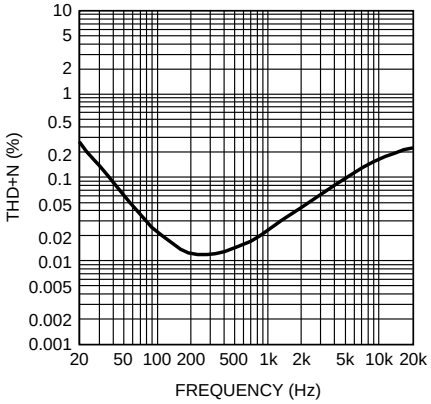


Figure 34.

Headphone THD+N vs Frequency
Stereo Aux Input, Aux Gain = 0dB
V_{DD} = 5V, P_{OUT} = 7.5mW, R_L = 32Ω

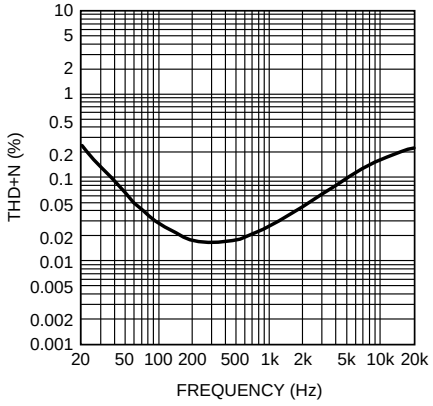


Figure 35.

Headphone THD+N vs Frequency
Differential Aux Input, Aux Gain = 0dB
A_V_{DD} = 3.3V, P_{OUT} = 7.5mW, R_L = 16Ω

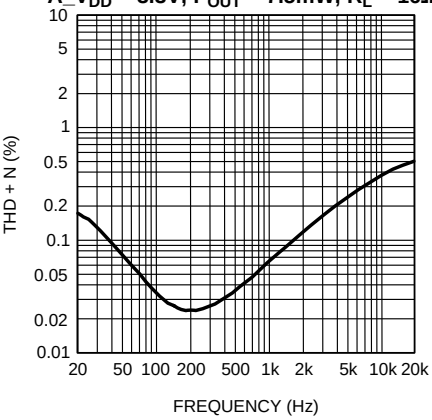


Figure 36.

Headphone THD+N vs Output Power
Stereo Aux Input, Aux Gain = 0dB
V_{DD} = 3.3V, V_{IN} = 1kHz, R_L = 32Ω

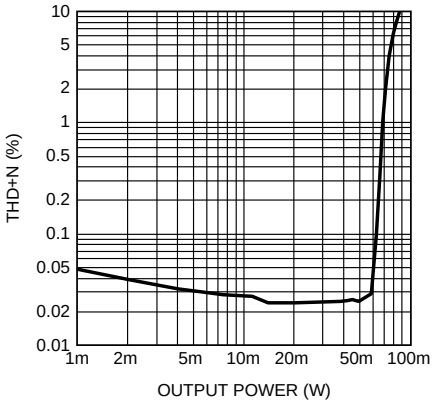


Figure 37.

Headphone THD+N vs Output Power
Stereo Aux Input, Aux Gain = 0dB
V_{DD} = 5V, V_{IN} = 1kHz, R_L = 32Ω

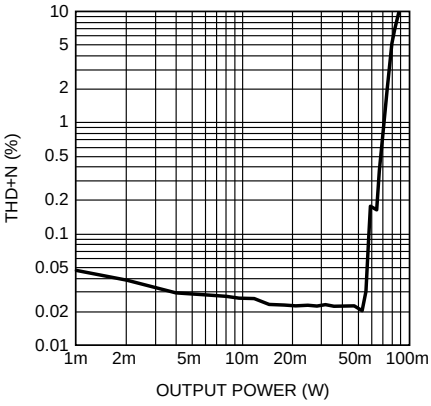


Figure 38.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Headphone THD+N vs Output Power
A_V_{DD} = 3.3V, Stereo Aux Input, Aux Gain = 0dB
R_L = 16Ω, f = 1kHz

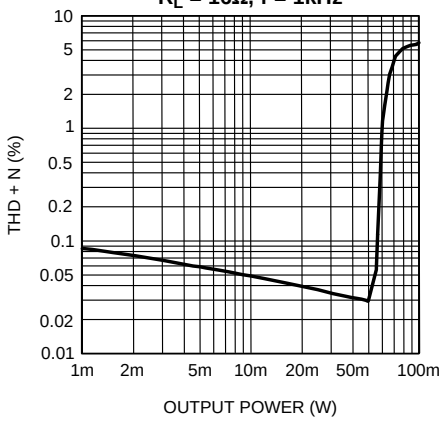


Figure 39.

Headphone PSRR vs Frequency
Differential Aux Input to Ground, Aux Gain = 0dB
V_{RIPPLE} = 200mV_{PP}

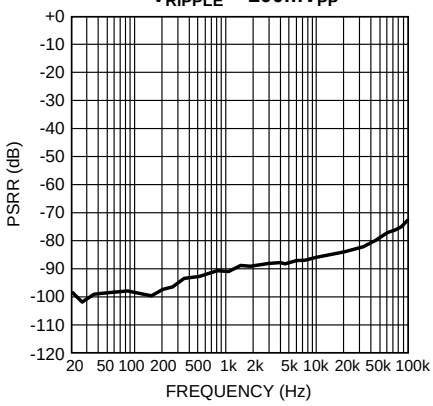


Figure 40.

Headphone Crosstalk vs Frequency
Stereo Aux Inputs, Aux Gain = 0dB, R_L = 32Ω

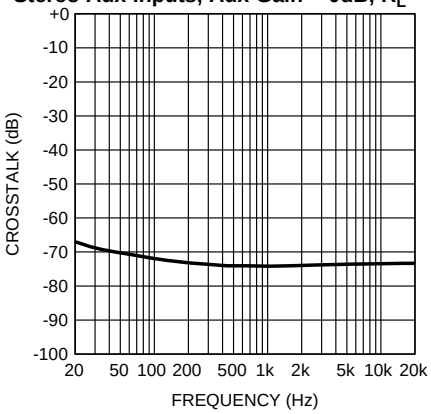


Figure 41.

Earpiece THD+N vs Frequency
Differential Aux Input, Aux Gain = 0dB
A_V_{DD} = 3.3V, P_{OUT} = 20mW, R_L = 32Ω

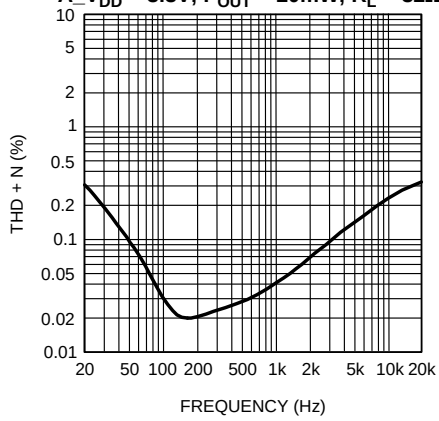


Figure 42.

Earpiece THD+N vs Output Power
Differential Aux Input, Aux Gain = 0dB
A_V_{DD}45 = 3.3V, R_L = 32Ω, f = 1kHz

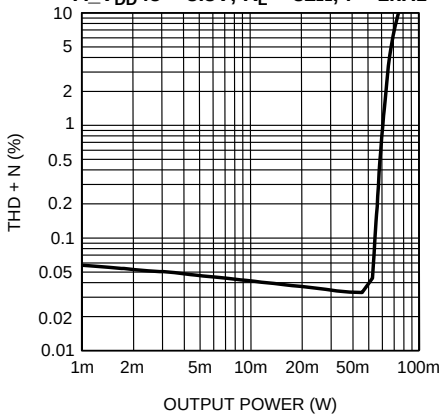


Figure 43.

Earpiece PSRR vs Frequency
Differential Aux Input to Ground, Aux Gain = 0dB
V_{RIPPLE} = 200mV_{PP}

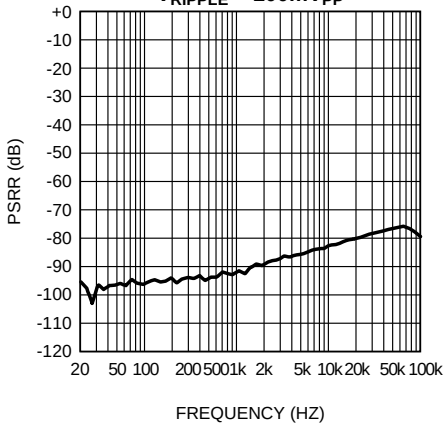


Figure 44.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

AUXOUT THD+N vs Frequency
Differential Aux Input, Aux Gain = 0dB
V_{DD} = 5V, V_{OUT} = 1V_{RMS}, R_L = 5kΩ

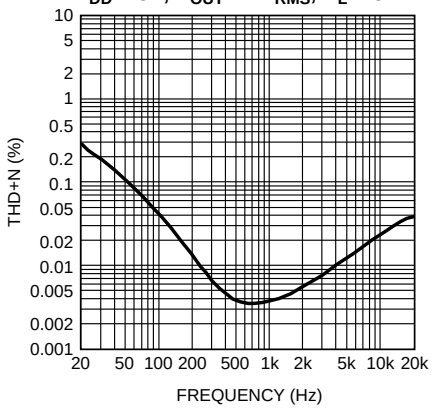


Figure 45.

AUXOUT THD+N vs Output Voltage
Differential Aux Input, Aux Gain = 0dB
V_{IN} = 1kHz, R_L = 5kΩ

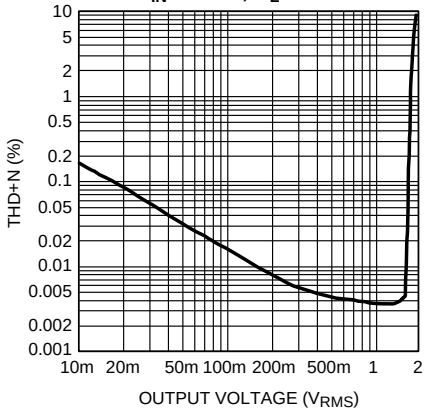
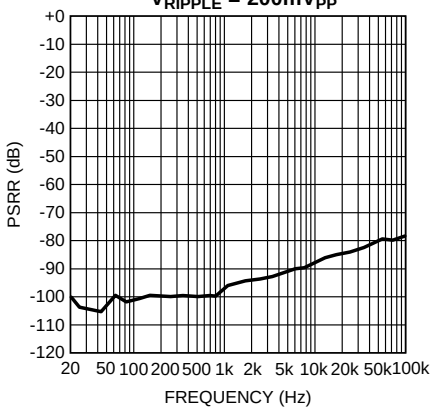


Figure 46.

Figure 47.

AUXOUT PSRR vs Frequency
Differential Aux Input to Ground, Aux Gain = 0dB
V_{RIPPLE} = 200mV_{PP}



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SYSTEM CONTROL

Method 1. I²C Compatible Interface

I²C SIGNALS

In I²C mode the LM49350 pin SCL is used for the I²C clock SCL and the pin SDA is used for the I²C data signal SDA. Both these signals need a pull-up resistor according to I²C specification. The I²C slave address for LM49350 is **0011010_2**.

I²C DATA VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when SCL is LOW.

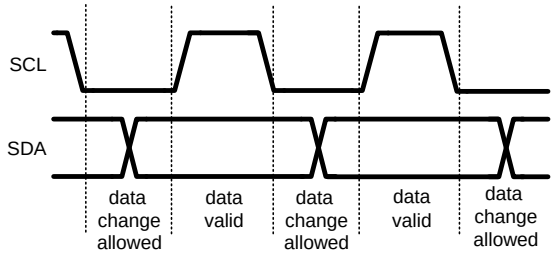


Figure 48. I²C Signals: Data Validity

I²C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

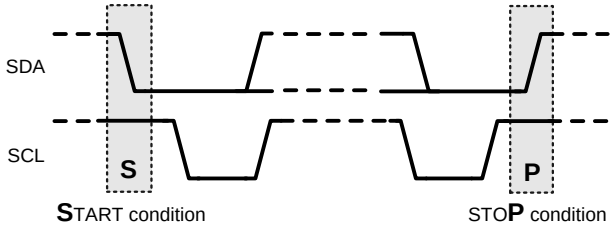


Figure 49. I²C Start and Stop Conditions

TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eight bit which is a data direction bit (R/W). The LM49350 address is **0011010_2**. For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

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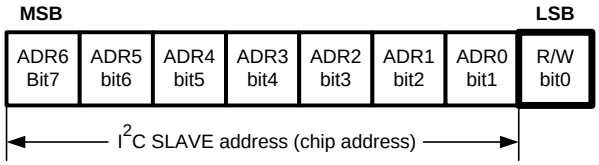
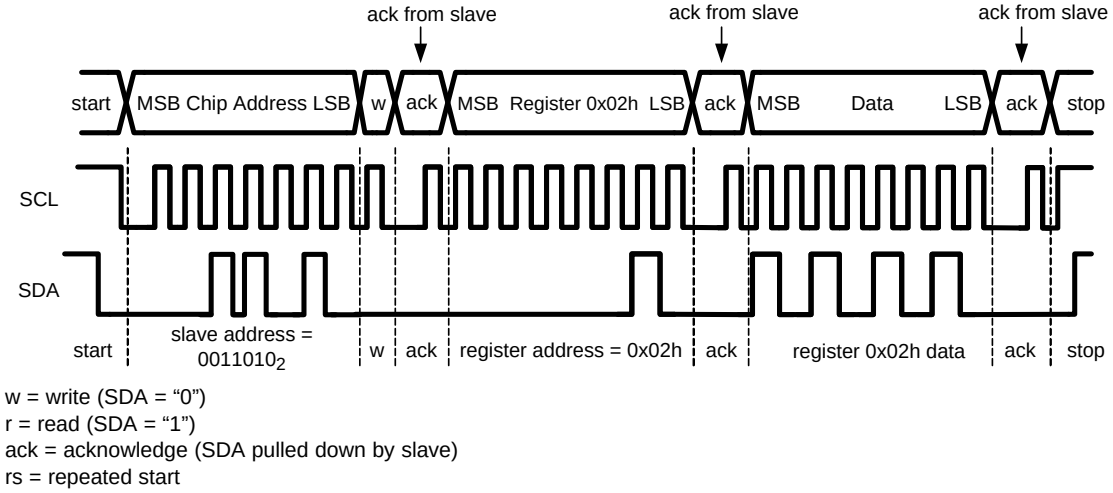


Figure 50. I²C Chip Address

Register changes take effect at the SCL rising edge during the last ACK from slave.



w = write (SDA = “0”)
r = read (SDA = “1”)
ack = acknowledge (SDA pulled down by slave)
rs = repeated start

Figure 51. Example I²C Write Cycle

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Figure 52 waveform.

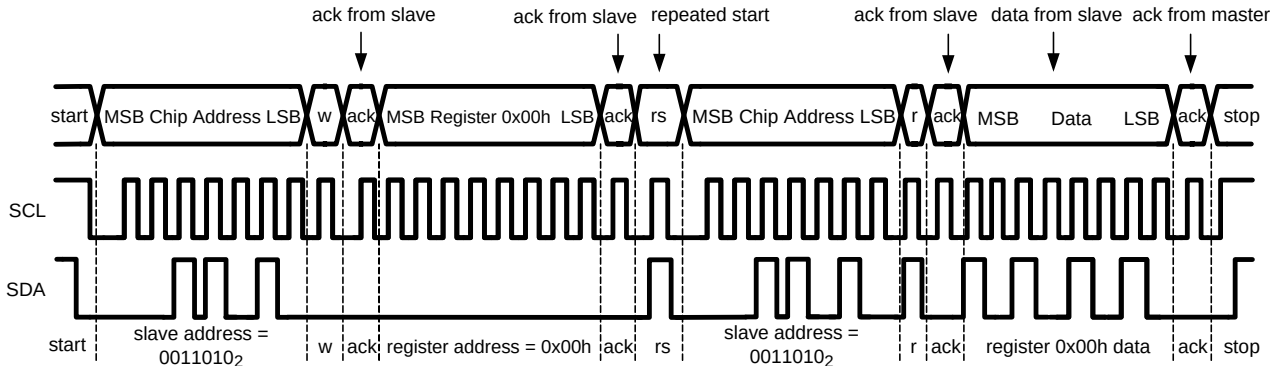


Figure 52. Example I²C Read Cycle

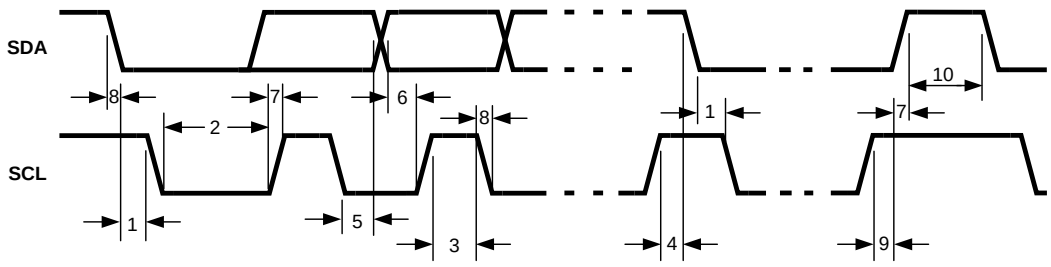


Figure 53. I²C Timing Diagram

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I²C TIMING PARAMETERS(1)

Symbol	Parameter	Limit		Units
		Min	Max	
1	Hold Time (repeated) START Condition	0.6		µs
2	Clock Low Time	1.3		µs
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns
5	Data Hold Time (Output direction, delay generated by LM49350)	300	900	ns
5	Data Hold Time (Input direction, delay generated by the Master)	0	900	ns
6	Data Setup Time	100		ns
7	Rise Time of SDA and SCL	$20+0.1C_b$	300	ns
8	Fall Time of SDA and SCL	$15+0.1C_b$	300	ns
9	Set-up Time for STOP condition	600		ns
10	Bus Free Time between a STOP and a START Condition	1.3		µs
C_B	Capacitive Load for Each Bus Line	10	200	pF

(1) **NOTE:** Data specified by design

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Device Register Map

Table 1. Device Register Map(1)

Address	Register	7	6	5	4	3	2	1	0
BASIC SETUP									
0x00h	PMC	CHIP	PORT2	PORT1	MCLK	OSC	PLL2	PLL1	CHIP
	SETUP	ACTIVE	CLK OVR	CLK OVR	OVR	ENB	ENB	ENB	ENABLE
0x01h	PMC CLOCKS							PMC_CLK_SEL	
0x02h	PMC CLK_DIV	PMC_CLK_DIV(R)							
PLLs									
0x03h						PLL2_CLK_SEL		PLL1_CLK_SEL	
0x04h	PLL1 M		PLL1 M						
0x05h	PLL1 N	PLL1 N							
0x06h	PLL1 N_MOD		PLL2 P2[8]	PLL1 P1[8]	PLL1 N_MOD				
0x07h	PLL1 P1	PLL1 P1 [7:0]							
0x08h	PLL1 P2	PLL1 P2[7:0]							
0x09h	PLL2 M		PLL2 M						
0x0Ah	PLL2 N	PLL2 N							
0x0Bh	PLL2 N_MOD			PLL2 P[8]	PLL2 N_MOD				
0x0Ch	PLL2 P	PLL2 P[7:0]							
ANALOG MIXER									
0x10h	CLASSD			AUXL_LS	AUXR_LS	MICL_LS	MICR_LS	DACL_LS	DACR_LS
0x11h	HEAD PHONESL			AUXL_HPL	AUXR_HPL	MICL_HPL	MICR_HPL	DACL_HPL	DACR_HPL
0x12h	HEAD PHONESR			AUXL_HPR	AUXR_ HPR	MICL_HPR	MICR_HPR	DACL_ HPR	DACR_ HPR
0x13h	AUX_OUT			AUXL_AX	AUXR_AX	MICL_AX	MICR_AX	DACL_AX	DACR_AX
0x14h	OUTPUT OPTIONS				CP_ FORCE	AUX-6dB	LS-6dB	HP-6dB	EPMODE
0x15h	ADC			AUXL_ ADCR	AUXR_ ADCL	MICL_ ADCR	MICR_ ADCL	DACL_ ADCR	DACR_ ADCL
0x16h	MICL_LVL			MUTE	SE/DIFF	MIC_L_LEVEL			
0x17h	MICR_LVL			MUTE	SE/DIFF	MIC_R_LEVEL			
0x18h	AUXL_LVL		FROM LINEL	AUX_L_LEVEL					
0x19h	AUXR_LVL	DIFF_MODE	FROM LINER	AUX_R_LEVEL					
ADC									
0x20h	ADC BASIC	DSPONLY	ADC_CLK_SEL			MUTE_R	MUTE_L	ADC_OSR	MONO
0x21h	ADC CLOCK	ADC_CLK_DIV (T)							
0x22h	ADC_DSP								ADC_TRIM
DAC									
0x30h	DAC_BASIC	DSPONLY	DAC_CLK_SEL			MUTE_R	MUTE_L	DAC_OSR	
0x31h	DAC_CLOCK	DAC_CLK_DIV (S)							
0x32h	DAC_DSP								DAC_TRIM

(1) Unless otherwise specified, the default values of the I^2C registers is 0x00h.

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Table 1. Device Register Map[1] (continued)

Address	Register	7	6	5	4	3	2	1	0
DIGITAL MIXER									
0x40h	IPLVL1	PORT2_RX_R_LVL		PORT2_RX_L_LVL		PORT1_RX_R_LVL		PORT1_RX_L_LVL	
0x41h	IPLVL2	INTERP_L_LVL		INTERP_R_LVL		ADC_R_LVL		ADC_L_LVL	
0x42h	OPPORT1			MONO	SWAP	R_SEL		L_SEL	
0x43h	OPPORT2			MONO	SWAP	R_SEL		L_SEL	
0x44h	OPDAC		SWAP	ADCR	PORT2R	PORT1R	ADCL	PORT2L	PORT1L
0x45h	OPDECI			MXRCLK_SEL		R_SEL		L_SEL	
AUDIO PORT 1									
0x50h	BASIC	STEREO_SYNC_MODE	STEREO_SYNC_PHASE	CLK_PH	SYNC_MS	CLK_MS	TX_ENB	RX_ENB	STEREO
0x51h	CLK_GEN1		CLK_SEL	HALF_CYCLE_DIVDER					
0x52h	CLK_GEN2					SYNTH_DENOM	SYNTH_NOM		
0x53h	SYNC_GEN			SYNC_WIDTH(MONO MODE)			SYNC_RATE		
0x54h	DATA_WIDTH	TX_EXTRA_BITS		TX_WIDTH			RX_WIDTH		
0x55h	RX_MODE	A/ULAW	COMPAND	MSB_POSITION					RX_MODE
0x56h	TX_MODE	A/ULAW	COMPAND	MSB_POSITION					TX_MODE
AUDIO PORT 2									
0x60h	BASIC	STEREO_SYNC_MODE	STEREO_SYNC_PHASE	CLK_PH	SYNC_MS	CLK_MS	TX_ENB	RX_ENB	STEREO
0x61h	CLK_GEN1		CLK_SEL	HALF_CYCLE_DIVDER					
0x62h	CLK_GEN2					SYNTH_DENOM	SYNTH_NOM		
0x63h	SYNC_GEN			SYNC_WIDTH(MONO MODE)			SYNC_RATE		
0x64h	DATA_WIDTH	TX_EXTRA_BITS		TX_WIDTH			RX_WIDTH		
0x65h	RX_MODE	A/ULAW	COMPAND	MSB_POSITION					RX_MODE
0x66h	TX_MODE	A/ULAW	COMPAND	MSB_POSITION					TX_MODE
EFFECTS ENGINE									
0x70h	ADC FX				ADC	ADC	ADC	ADC	ADC
					SCLP ENB	EQ ENB	PK ENB	ALC ENB	HPF_ENB
0x71h	DAC FX				DAC	DAC	DAC	DAC	DAC
					SCLP ENB	3D ENB	EQ ENB	PK ENB	ALC ENB
ADC EFFECTS									
0x80h	HPF						HPF MODE		
0x81h	ADC		SOURCE	SOURCE	STEREO	LIMITER	SAMPLE_RATE		
	ALC 1		OVR	SEL	LINK				
0x82h	ADC				NG_ENB	NOISE_FLOOR			
	ALC 2								
0x83h	ADC				ALC_TARGET_LEVEL				
	ALC 3								
0x84h	ADC				ATTACK_RATE				
	ALC 4								
0x85h	ADC	PK_DECAY_RATE			DECAY_RATE/RELEASE_RATE				
	ALC 5								

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Table 1. Device Register Map[1] (continued)

Address	Register	7	6	5	4	3	2	1	0
0x86h	ADC ALC 6				HOLDTIME				
0x87h	ADC ALC 7			MAX_LEVEL					
0x88h	ADC ALC 8			MIN_LEVEL					
0x89h	ADC L LEVEL			ADC_L_LEVEL					
0x8Ah	ADC R LEVEL			ADC_R_LEVEL					
0x8Bh	EQ BAND 1		LEVEL					FREQ	
0x8Ch	EQ BAND 2	Q	LEVEL					FREQ	
0x8Dh	EQ BAND 3	Q	LEVEL					FREQ	
0x8Eh	EQ BAND 4	Q	LEVEL					FREQ	
0x8Fh	EQ BAND 5		LEVEL					FREQ	
0x90h	SOFTCLIP 1				SOFT KNEE	THRESHOLD			
0x91h	SOFTCLIP 2				RATIO				
0x92h	SOFTCLIP 3				LEVEL				
ADC EFFECT MONITORS									
0x98h	LVLMONL	ADC LEFT LEVEL MONITOR							
0x99h	LVLMONR	ADC RIGHT LEVEL MONITOR							
0x9Ah	FXCLIP	SCLP_R CLIP	SCLP_L CLIP	EQ_R CLIP	EQ_L CLIP	GAIN_R CLIP	GAIN_L CLIP	ADC_R CLIP	ADC_L CLIP
0x9Bh	ALCMONL	SCLP_R DISTORT	SCLP_L DISTORT	ADC LEFT ALC MONITOR					
0x9Ch	ALCMONR	SCLP_L DISTORT	SCLP_R DISTORT	ADC RIGHT ALC MONITOR					
DAC EFFECTS									
0xA0h	DAC ALC 1				STEREO LINK	LIMITER	SAMPLE_RATE		
0xA1h	DAC ALC 2				NG_ENB	NOISE_FLOOR			
0xA2h	DAC ALC 3				AGC_TARGET_LEVEL				
0xA3h	DAC ALC 4				ATTACK_RATE				
0xA4h	DAC ALC 5	PK_DECAY_RATE			DECAY_RATE/RELEASE_RATE				
0xA5h	DAC ALC 6				HOLDTIME				
0xA6h	DAC ALC 7			MAX_LEVEL					
0xA7h	DAC ALC 8			MIN_LEVEL					

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Table 1. Device Register Map[1] (continued)

Address	Register	7	6	5	4	3	2	1	0
0xA8h	DAC L LEVEL	DAC_L_LEVEL							
0xA9h	DAC R LEVEL	DAC_R_LEVEL							
0xAAh	DAC_3D	ATTEN	FILTER_TYPE				EFFECT_LEVEL		EFFECT_ MODE
0xABh	EQ BAND 1		LEVEL					FREQ	
0xACh	EQ BAND 2	Q	LEVEL					FREQ	
0xADh	EQ BAND 3	Q	LEVEL					FREQ	
0xAEh	EQ BAND 4	Q	LEVEL					FREQ	
0xAFh	EQ BAND 5		LEVEL					FREQ	
0xB0h	SOFTCLIP 1				SOFT KNEE	THRESHOLD			
0xB1h	SOFTCLIP 2				RATIO				
0xB2h	SOFTCLIP 3				LEVEL				
DAC EFFECT MONITORS									
0xB8h	LVLMONL	DAC LEFT LEVEL MONITOR							
0xB9h	LVLMONR	DAC RIGHT LEVEL MONITOR							
0xBAh	FXCLIP	SCLP_R CLIP	SCLP_L CLIP	EQ_R CLIP	EQ_L CLIP	3D_R CLIP	3D_L CLIP	GAIN_R CLIP	GAIN_L CLIP
0xBBh	ALCMONL	SCLP_R DISTORT	SCLP_L DISTORT	DAC LEFT ALC MONITOR					
0xBCh	ALCMONR	SCLP_L DISTORT	SCLP_R DISTORT	DAC RIGHT ALC MONITOR					
GPIO									
0xE0h	GPIO	TEMP	SHORT	GPIO_RX	GPIO_TX	GPIO_MODE			
SPREAD SPECTRUM									
0xF1h	SS						SS_ DISABLE	RSVD	RSVD
ADC COMPENSATION FILTER									
0xF8h	ADC_C0_ LSB	ADC_C0_LSB							
0xF9h	ADC_C0_ MSB	ADC_C0_MSB							
0xFAh	ADC_C1_ LSB	ADC_C1_LSB							
0xFBh	ADC_C1_ MSB	ADC_C1_MSB							
0xFCh	ADC_C2_ LSB	ADC_C2_LSB							
0xFDh	ADC_C2_M SB	ADC_C2_MSB							
0xFEh	AUX_LINE_ OUT			AUX_LINE_ OUT	RSVD				

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Basic PMC Setup Register

This register is used to control the LM49350's Basic Power Management Setup:

Table 2. PMC_SETUP (0x00h)

Bits	Field	Description	
0	CHIP_ENABLE	When this bit is set the power management will enable the MCLK I/O or internal oscillator(1). It will then use this clock to sequence the enabling of the analog references and bias points. When this bit is cleared the PMC will bring the analog down gently and disable the MCLK or oscillator.	
		CHIP _ENABLE	Chip Status
		0	Turn Chip Off
		1	Turn Chip On
1	PLL1_ENB	This enables the primary PLL	
		PLL1_ENABLE	PLL1 Status
		0	PLL1 Off
		1	PLL1 On
2	PLL2_ENB	This enables the secondary PLL	
		PLL2_ENABLE	PLL2 Status
		0	PLL2 Off
		1	PLL2 On
3	OSC_ENB	This enables the internal 300kHz Oscillator. For analog only chip modes, the oscillator can be used instead of an external system clock to drive the chip's power management (PMC).	
		OSC_ENABLE	Oscillator Status
		0	Oscillator Off
		1	Oscillator On
4	MCLK_OVR	This forces the MCLK input to enable, regardless of requirement. If set, the audio ports and digital mixer can be activated even if the chip is in shutdown mode. This assumes that MCLK is selected as the clock source and that there is an active clock signal driving the MCLK pin. Setting this bit reduces power consumption, by allowing audio ports and digital mixer to operate while the analog sections of the chip is powered down.	
		MCLK_OVR	Comment
		0	I/O control is automatic
		1	MCLK input forced on.
5	PORT1_CLK_OVR	This forces the clock input of Audio Port 1 input to enable, regardless of other port settings.	
		PORT1_CLK_OVR	Comment
		0	I/O control is automatic
		1	PORT_CLK input forced on
6	PORT2_CLK_OVR	This forces the clock input of Audio Port 2 input to enable, regardless of other port settings.	
		PORT2_CLK_OVR	Comment
		0	I/O control is automatic
		1	PORT_CLK input forced on
7	CHIP_ACTIVE	This bit is used to read back the enable status of the chip.	

(1) If the PMC is set to operate from one of the audio ports then it will wait for the port to be enabled or the relevant over ride bit to be set, forcing the port clock input to enable.

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PMC Clocks Register

This register is used to control the LM49350's Basic Power Management Setup:

Table 3. PMC_SETUP (0x01h)

Bits	Field	Description	
1:0	PMC_CLK_SEL	This selects the source of the PMC input clock.	
		PMC_CLK_SEL	PMC Input Clock Source
		00	MCLK (Default divide is 40)
		01	Internal 300kHz Oscillator
		10	DAC SOURCE CLOCK
		11	ADC SOURCE CLOCK

PMC Clock Divide Register

This register is used to control the LM49350's Power Management Circuits Clocks:

Table 4. PMC_SETUP (0x02h) (Default data value is 0x50h)

Bits	Field	Description	
7:0	PMC_CLK_DIV	This programs the half cycle divider that precedes the PMC. The PMC should run from a 300kHz clock. The default of this divider is 0x50h (divide by 40) to get a ≈300kHz PMC clock from a 12MHz or 12.288MHz MCLK. Program this divider with the division you want, multiplied by 2, and subtract 1.	
		PMC_CLK_DIV	Divide by
		00000000	1
		00000001	1
		00000010	1.5
		00000011	2
		00000100	2.5
		00000101	3
		—	—
		11111101	126
		11111110	127.5
		11111111	128

LM49350 Clock Network

Refer to Figure 54

The audio DAC and ADC operate at a clock frequency of 2*OSR*f_S where OSR is the oversampling ratio and f_S is the sampling frequency of the DAC or ADC. The DAC can operate at four different OSR settings (128, 125, 64, 32). The ADC can operate at three different OSR settings (128, 125, 64). For example, if the stereo DAC or ADC is set at OSR = 128, a 12.288MHz clock is required for 48kHz data. If a 12.288MHz clock is not available, then one of the LM49350's dual PLLs can be used to generate the desired clock frequency. Otherwise, if a 12.288MHz is available, then the PLL can be bypassed to reduce power consumption. The DAC clock divider (S divider) or ADC clock divider (T divider) can also be used to generate the correct clock. If an 18.432 MHz clock is available, the S or T divider could be set to 1.5 in order to generate a 12.288MHz clock from 18.432MHz without using a PLL.

The DAC path clock (DAC_SOURCE_CLK) and ADC path clock (ADC_SOURCE_CLK) can be driven directly by the MCLK input, the PORT1_CLK input, the PORT2_CLK input, PLL1's output, or PLL2's output.

For instances where a PLL must be used, the PLL input clock can come from three sources. The clock input to PLL1 or PLL2 can come from the MCLK input, the PORT1_CLK input, or the PORT2_CLK input.

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The LM49350's Power Management Circuit (PMC) requires a clock that is independent from the DAC or ADC. It is recommended to provide a ≈300kHz clock at Point C. The PMC clock divider (R divider) is available to generate the correct clock to the PMC block. The PMC clock path can be driven directly by the MCLK input, the internal 300kHz oscillator, the DAC_SOURCE_CLK, or the ADC_SOURCE_CLK.

Table 5. DAC Clock Requirements

DAC Sample Rate (kHz)	Clock Required at A (OSR = 128)	Clock Required at A (OSR= 125)	Clock Required at A (OSR = 64)	Clock Required at A (OSR = 32)
8	2.048 MHz	2 MHz	1.024 MHz	0.512 MHz
11.025	2.8224 MHz	2.75625 MHz	1.4112 MHz	0.7056 MHz
12	3.072 MHz	3 MHz	1.536 MHz	0.768 MHz
16	4.096 MHz	4 MHz	2.048 MHz	1.024 MHz
22.05	5.6448 MHz	5.5125 MHz	2.8224 MHz	1.4112 MHz
24	6.144 MHz	6 MHz	3.072 MHz	1.536 MHz
32	8.192 MHz	8 MHz	4.096 MHz	2.048MHz
44.1	11.2896 MHz	11.025 MHz	5.6448 MHz	2.8224 MHz
48	12.288 MHz	12 MHz	6.144 MHz	3.072 MHz
96	24.576 MHz	24 MHz	12.288 MHz	6.144 MHz
192	—	—	24.576 MHz	12.288 MHz

Table 6. ADC Clock Requirements

ADC Sample Rate (kHz)	Clock Required at B (OSR = 128)	Clock Required at B (OSR= 125)	Clock Required at B (OSR = 64)
8	2.048 MHz	2 MHz	1.024 MHz
11.025	2.8224 MHz	2.75625 MHz	1.4112 MHz
12	3.072 MHz	3 MHz	1.536 MHz
16	4.096 MHz	4 MHz	2.048 MHz
22.05	5.6448 MHz	5.5125 MHz	2.8224 MHz
24	6.144 MHz	6 MHz	3.072 MHz
32	8.192 MHz	8 MHz	4.096 MHz
44.1	11.2896 MHz	11.025 MHz	5.6448 MHz
48	12.288 MHz	12 MHz	6.144 MHz

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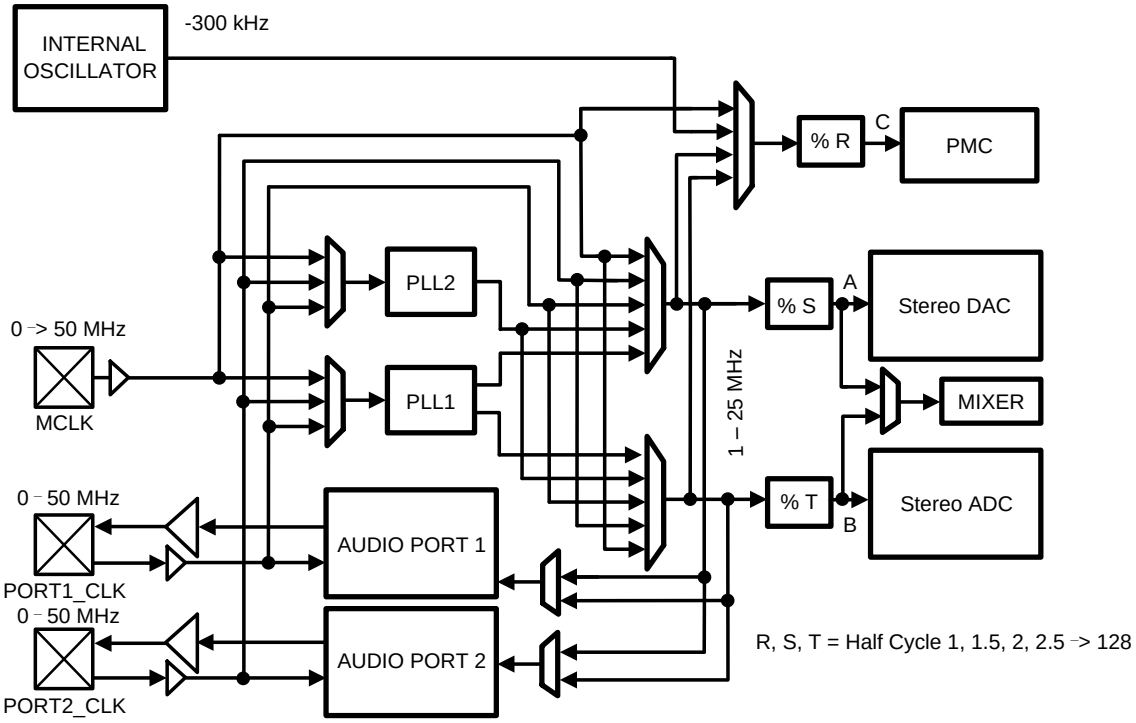


Figure 54. Internal Clock Network

PLL Setup Registers

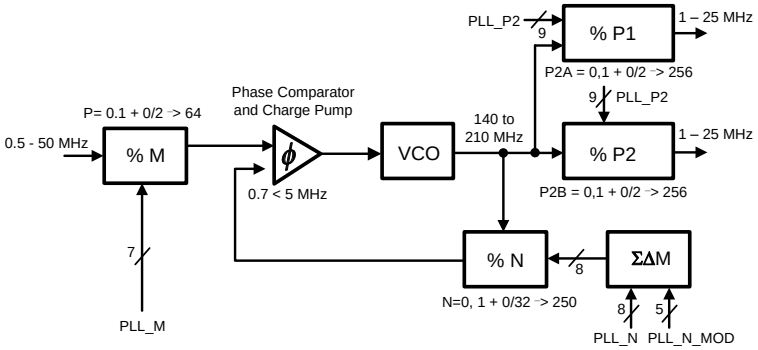


Figure 55. PLL1 Loop

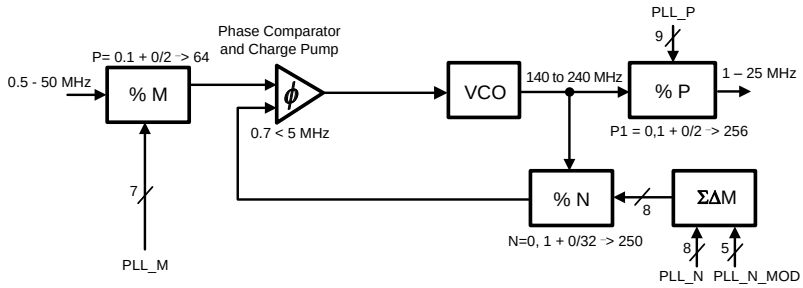


Figure 56. PLL2 Loop

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The LM49350 contains two PLLs for flexible operation of its dual audio ports. PLL1 has a P1 and P2 output divider thereby allowing PLL1 to generate two distinct clock outputs. The equations for PLL1's generated output clocks are as follows:

$$f_{OUT1} = (f_{IN} \cdot N_1 / M_1 \cdot P_1) \quad (1)$$

$$f_{OUT2} = (f_{IN} \cdot N_1 / M_1 \cdot P_2) \quad (2)$$

where:

$$N_1 = PLL1_N + PLL1_N_MOD \quad (3)$$

$$M_1 = (PLL1_M + 1) / 2 \quad (4)$$

$$P_1 = (PLL1_P1 + 1) / 2 \quad (5)$$

$$P_2 = (PLL1_P2 + 1) / 2 \quad (6)$$

The equations for PLL2's generated output clock are as follows:

$$f_{OUT3} = (f_{IN}.N_2 / M_2.P) \quad (7)$$

where:

$$N_2 = PLL2_N + PLL2_N_MOD \quad (8)$$

$$M_2 = (PLL2_M + 1) / 2 \quad (9)$$

$$P = (PLL2_P + 1) / 2 \quad (10)$$

The VCO frequency and comparison frequencies are as follows:

$$f_{VCO} = f_{OUT}.P \quad (11)$$

$$f_{COMP} = f_{IN}/M \quad (12)$$

Keep f_{VCO} between 140MHz to 240MHz and keep f_{COMP} between 700kHz to 5MHz.

Table 7. PLL Settings for Common System Clock Frequencies

f_{IN} (MHz)	M	N	N_MOD	P	f_{OUT} (MHz)	Error (Hz)
12	2.5	32	0	12.5	12288000	0
13	15.5	175	26	12	12287970	–30
14.4	12.5	128	0	12	12288000	0
16.2	13.5	128	0	12.5	12288000	0
16.8	3.5	32	0	12.5	12288000	0
19.2	12.5	96	0	12	12288000	0
19.68	20.5	160	0	12.5	12288000	0
19.8	16.5	128	0	12.5	12288000	0
27	22.5	128	0	12.5	12288000	0
12	12.5	147	0	12.5	11289600	0
12.288	10	147	0	16	11289600	0
13	9	144	19	18.5	11289603	+3
13.5	15.5	213	28	16.5	11289589	–11
14.4	12.5	147	0	15	11289600	0
16.2	22.5	196	0	12.5	11289600	0
16.8	12.5	126	0	15	11289600	0
19.2	20	147	0	12.5	11289600	0
19.68	20.5	147	0	12.5	11289600	0
19.8	27.5	196	0	12.5	11289600	0
27	37.5	196	0	12.5	12289600	0
11.2896	10.5	195	0	17.5	12000000	0
12.288	8	125	0	16	12000000	0
13	6.5	102	0	17	12000000	0
13.5	4.5	68	0	17	12000000	0
14.4	6	85	0	17	12000000	0
16.2	13.5	170	0	17	12000000	0

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Table 7. PLL Settings for Common System Clock Frequencies (continued)

f_{IN} (MHz)	M	N	N_MOD	P	f_{OUT} (MHz)	Error (Hz)
16.8	7	85	0	17	12000000	0
19.2	8	85	0	17	12000000	0
19.68	20.5	200	0	16	12000000	0
19.8	16.5	170	0	17	12000000	0
11.2896	8	125	0	16	11025000	0
12	10	147	0	16	11025000	0
12.288	8	114	27	16	11025000	0
13	6.5	96	15	17.5	11025000	0
13.5	10	147	0	18	11025000	0
14.4	4	49	0	16	11025000	0
16.2	4	49	0	18	11025000	0
16.8	16	189	0	18	11025000	0
19.2	16	147	0	16	11025000	0
19.68	16	189	0	18	11025000	0
19.8	16	147	0	16.5	11025000	0

Table 8. PLL_CLOCK_SOURCE (0x03h)

Bits	Field	Description	
1:0	PLL1_CLK_SEL	This selects the source of the input clock to PLL1	
		PLL1_CLK_SEL	PLL1 Input Clock Source
		00	MCLK
		01	PORT1_CLK
		10	PORT2_CLK
		11	RESERVED

Table 9. PLL1_M (0x04h)

Bits	Field	Description	
6:0	PLL1_M	This programs the PLL1 M divider to divide from 1 to 64.	
		PLL1_M	PLL1 Input Divider Vaue
		000000	1
		000001	1
		000010	1.5
		000011	2
		000100	2.5
		000101	3
		—	—
		1111101	63
		1111110	63.5
		1111111	64

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Table 10. PLL1_N (0x05h)

Bits	Field	Description	
7:0	PLL1_N	This programs the PLL1 N divider to divide from 1 to 250.	
		PLL1_N	Feedback Divider Value
		00000000 to 00001010	10
		00001011	11
		00001100	12
		00001101	13
		00001110	14
		00001111	15
		—	—
		11111000	248
		11111001	249
		11111010 to 11111111	250

Table 11. PLL1_N_MOD (0x06h)

Bits	Field	Description	
4:0	PLL1_N_MOD	This programs the sigma-delta modulator in PLL1	
		PLL1_N_MOD	Fractional Part of N
		00000	0
		00001	1/32
		00010	2/32
		00011	3/32
		00100	4/32
		00101	5/32
		—	—
		11101	20/32
		11110	30/32
		11111	31/32
5	PLL1_P1[8]	This sets the MSB of the 1st P Divider on PLL1 which is part of a standard half-cycle divider control.	
6	PLL1_P2[8]	This sets the MSB of the 2nd P Divider on PLL1 which is part of a standard half-cycle divider control.	

Table 12. PLL1_P1 (0x07h)

Bits	Field	Description	
7:0	PLL1_P1[7:0]	This programs the 8 LSBs of the PLL1's P1 Divider. These LSBs combine with PLL1_P1[8] which allows the P1 divider to divide by up to 256	
		PLL1_P1	P1 Divider Value
		000000000	1
		000000001	1
		000000010	1.5
		000000011	2
		000000100	2.5
		000000101	3
		—	—
		111111101	255
		111111110	255.5
		111111111	256

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Table 13. PLL1_P2 (0x08h)

Bits	Field	Description	
7:0	PLL1_P2[7:0]	This programs 8 LSBs of PLL1's P2 Divider. These LSBs combine with PLL1_P2[8] which allows the P2 divider to divide by up to 256	
		PLL1_P2	P2 Divider Value
		000000000	1
		000000001	1
		000000010	1.5
		000000011	2
		000000100	2.5
		000000101	3
		—	—
		111111101	255
		111111110	255.5
		111111111	256

Table 14. PLL2_M (0x09h)

Bits	Field	Description	
6:0	PLL2_M	This programs the PLL2 M divider to divide from 1 to 64.	
		PLL2_M	PLL2 Input Divider Value
		0000000	1
		0000001	1
		0000010	1.5
		0000011	2
		0000100	2.5
		0000101	3
		—	—
		1111101	63
		0000010	63.5
		1111111	64

Table 15. PLL2_N (0x0Ah)

Bits	Field	Description	
7:0	PLL2_N	This programs PLL2's N divider to divide from 10 to 250.	
		PLL2_N	Comment
		00000000 to 00001010	10
		00001011	11
		00001100	12
		00001101	13
		00001110	14
		00001111	15
		—	—
		11111000	248
		11111001	249
		11111010 to 11111111	250

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Table 16. PLL2_N_MOD (0x0Bh)

Bits	Field	Description	
4:0	PLL2_N_MOD	This programs the sigma-delta modulator in PLL2	
		PLL2_N_MOD	Fractional Part of N
		00000	0
		00001	1/32
		00010	2/32
		00011	3/32
		00100	4/32
		00101	5/32
		—	—
		11101	29/32
		11110	30/32
		11111	31/32
5	PLL2_P[8]	This is the MSB of the P Divider on PLL2.	

Table 17. PLL2_P (0x0Ch)

Bits	Field	Description	
7:0	PLL2_P[7:0]	This programs the 8 LSBs of PLL2's P Divider. These LSBs combine with PLL2_P[8] which allows the P divider to divide by up to 256	
		PLL2_P	P Divides by
		000000000	1
		000000001	1
		000000010	1.5
		000000011	2
		000000100	2.5
		000000101	3
		—	—
		111111101	255
		111111110	255.5
		111111111	256

Analog Mixer Control Registers

This register is used to control the LM49350's Analog Mixer:

Table 18. CLASS_D_OUTPUT (0x10h)

Bits	Field	Description
0	DACR_LS	The right DAC output is added to the loudspeaker output.
1	DACL_LS	The left DAC output is added to the loudspeaker output.
2	MICR_LS	The right MIC input is added to the loudspeaker output. Setting this bit enables MIC BIAS.
3	MICL_LS	The left MIC input is added to the loudspeaker output. Setting this bit enables MIC BIAS.
4	AUXR_LS	The right AUX input is added to the loudspeaker output.
5	AUXL_LS	The left AUX input is added to the loudspeaker output.

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CLASS D LOUDSPEAKER AMPLIFIER

The LM49350 features a filterless modulation scheme. The differential outputs of the device switch at 300kHz from V_{DD} to GND. When there is no input signal applied, the two outputs (LS+ and LS-) switch with a 50% duty cycle, with both outputs in phase. Because the outputs of the LM49350 are differential, the two signals cancel each other. This results in no net voltage across the speaker, thus there is no load current during an idle state, conserving power.

With an input signal applied, the duty cycle (pulse width) of the LM49350 outputs changes. For increasing output voltages, the duty cycle of LS+ increases, while the duty cycle of LS- decreases. For decreasing output voltages, the converse occurs, the duty cycle of LS- increases while the duty cycle of LS+ decreases. The difference between the two pulse widths yields the differential output voltage.

SPREAD SPECTRUM MODULATION

The LM49350 features a fitlerless spread spectrum modulation scheme that eliminates the need for output filters, ferrite beads or chokes. The switching frequency varies by ±30% about a 300kHz center frequency, reducing the wideband spectral content, improving EMI emissions radiated by the speaker and associated cables and traces. Where a fixed frequency class D exhibits large amounts of spectral energy at multiples of the switching frequency, the spread spectrum architecture of the LM49350 spreads that energy over a larger bandwidth. The cycle-to-cycle variation of the switching period does not affect the audio reproduction or efficiency.

CLASS D POWER DISSIPATION AND EFFICIENCY

In general terms, efficiency is considered to be the ratio of useful work output divided by the total energy required to produce it with the difference being the power dissipated, typically, in the IC. The key here is “useful” work. For audio systems, the energy delivered in the audible bands is considered useful including the distortion products of the input signal. Sub-sonic (DC) and super-sonic components (>22kHz) are not useful. The difference between the power flowing from the power supply and the audio band power being transduced is dissipated in the LM49350 and in the transducer load. The amount of power dissipation in the LM49350's class D amplifier is very low. This is because the ON resistance of the switches used to form the output waveforms is typically less than 0.25Ω. This leaves only the transducer load as a potential "sink" for the small excess of input power over audio band output power. The LM49350 dissipates only a fraction of the excess power requiring no additional PCB area or copper plane to act as a heat sink.

EMI/RFI Filtering

If system level PCB layout constraints require the LM49350’s Class D output bumps to be placed far away from the speaker or the Class D output traces to be routed near EMI/RFI sensitive components, an external EMI/RFI filter should be used. A series ferrite bead placed close to the Class D output bumps along with a shunt capacitor to ground placed close to the ferrite bead will reduce the EMI/RFI emissions of the Class D amplifier’s switching outputs. The ferrite bead must be rated with a current rating high enough to properly drive the loudspeaker. The ferrite bead that is rated for 1A or greater is recommended. The DC resistance of the ferrite bead is another important specification that must be taken into consideration. A low DC resistance will minimize any power losses dissipated by the EMI/RFI filter thereby preserving the power efficiency advantages of the Class D amplifier. Selecting a ferrite bead with high DC resistance will decrease output power delivered to speaker and reduce the Class D amplifier’s efficiency. The shunt capacitor needs to have low ESR. A 10pF ceramic capacitor with a X7R dielectric is recommended as a starting point. Care needs to be taken to ensure that the value of the shunt capacitor does not exceed 47pF when using a low resistance ferrite bead in order to prevent permanent damage to the low side FETs of the Class D output stage.

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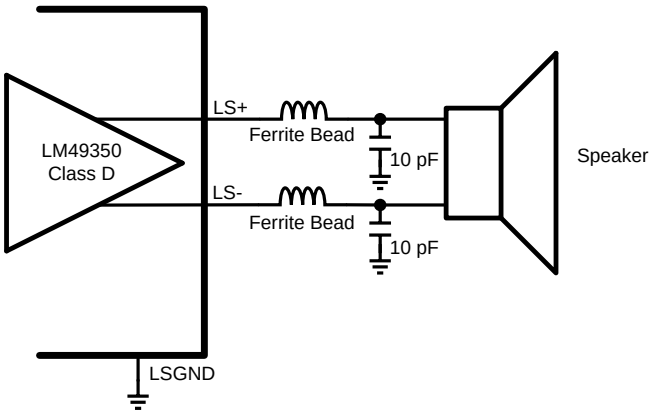


Figure 57. EMI/RFI Filter for the Class D Amplifier

Table 19. LEFT HEADPHONE_OUTPUT (0x11h)

Bits	Field	Description
0	DACR_HPL	The right DAC output is added to the left headphone output.
1	DACL_HPL	The left DAC output is added to the left headphone output.
2	MICR_HPL	The right MIC input is added to the left headphone output. Setting this bit enables MIC BIAS.
3	MICL_HPL	The left MIC input is added to the left headphone output. Setting this bit enables MIC BIAS.
4	AUXR_HPL	The right AUX input is added to the left headphone output.
5	AUXL_HPL	The left AUX input is added to the left headphone output.

Table 20. RIGHT HEADPHONE_OUTPUT (0x12h)

Bits	Field	Description
0	DACR_HPR	The right DAC output is added to the right headphone output.
1	DACL_HPR	The left DAC output is added to the right headphone output.
2	MICR_HPR	The right MIC input is added to the right headphone output. Setting this bit enables the MIC BIAS output.
3	MICL_HPR	The left MIC input is added to the right headphone output. Setting this bit enables the MIC BIAS output.
4	AUXR_HPR	The right AUX input is added to the right headphone output.
5	AUXL_HPR	The left AUX input is added to the right headphone output.

HEADPHONE AMPLIFIER FUNCTION

The LM49350 headphone amplifier features TI's ground referenced architecture that eliminates the large DC-blocking capacitors required at the outputs of traditional headphone amplifiers. A low-noise inverting charge pump creates a negative supply (HP_V_{SS}) from the positive supply voltage (LS_V_{DD}). The headphone amplifiers operate from these bipolar supplies, with the amplifier outputs biased about GND, instead of a nominal DC voltage (typically $V_{DD}/2$), like traditional amplifiers. Because there is no DC component to the headphone output signals, the large DC-blocking capacitors (typically 220µF) are not necessary, conserving board space and system cost, while improving frequency response.

CHARGE PUMP CAPACITOR SELECTION

Use low ESR ceramic capacitors (less than 100mΩ) for optimum performance.

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CHARGE PUMP FLYING CAPACITOR (C6)

The flying capacitor (C6) affects the load regulation and output impedance of the charge pump. A C6 value that is too low results in a loss of current drive, leading to a loss of amplifier headroom. A higher valued C6 improves load regulation and lowers charge pump output impedance to an extent. Above 2.2µF, the $R_{DS(ON)}$ of the charge pump switches and the ESR of C6 and C5 dominate the output impedance. A lower value capacitor can be used in systems with low maximum output power requirements. Please refer to the demonstration board schematic shown in Schematic Diagram.

CHARGE PUMP FLYING CAPACITOR (C5)

The value and ESR of the hold capacitor (C5) directly affects the ripple on CPV_{SS}. Increasing the value of C5 reduces output ripple. Decreasing the ESR of C5 reduces both output ripple and charge pump output impedance. A lower value capacitor can be used in systems with low maximum output power requirements. Please refer to the demonstration board schematic shown in Schematic Diagram.

Table 21. AUX_OUTPUT (0x13h)

Bits	Field	Description
0	DACR_AUX	The right DAC output is added to the AUX output.
1	DACL_AUX	The left DAC output is added to the AUX output.
2	MICR_AUX	The right MIC input is added to the AUX output. Setting this bit enables the MIC BIAS output.
3	MICL_AUX	The left MIC input is added to the AUX output. Setting this bit enables the MIC BIAS output.
4	AUXR_AUX	The right AUX input is added to the AUX output.
5	AUXL_AUX	The left AUX input is added to the AUX output.

AUXILIARY OUTPUT AMPLIFIER

The LM49350's auxiliary output (AUXOUT) amplifier provides differential drive capability to loads that are connected across its outputs. This results in output signals at the AUX_OUT+ and AUX_OUT- pins that are 180 degrees out of phase with respect to each other. This effectively doubles the maximum possible output swing for a specific supply voltage when compared to single-ended output configurations. The differential output configuration also allows the load to be isolated from ground since both the AUX_OUT+ and AUX_OUT- pins are biased at the same DC potential. This eliminates the need for any large and expensive DC blocking capacitors at the AUXOUT amplifier outputs. The load can then be directly connected to the positive and negative outputs of the AUXOUT amplifier which then isolates it from any ground noise, thereby improving signal to noise ratio (SNR) and power supply rejection ratio (PSRR).

The AUXOUT amplifier has two modes of operation. The primary mode of operation is high current drive mode (Earpiece Mode) where the AUXOUT amplifier can be used to differentially drive a mono earpiece speaker. The secondary mode of operation is low current drive mode where the AUXOUT amplifier operates in a power saving mode (AUX_LINE_OUT Mode) to provide a differential output that is used as a mono differential line level input to a standalone mono differential input class D amplifier (LM4675) for stereo loudspeaker applications.

Table 22. OUTPUT_OPTIONS (0x14h)

Bits	Field	Description
0	EPMODE	If set the HPR output is driven with the negative input of the HPL output stage.
1	HP_NEG_6dB	If set, both HPL and HPR are attenuated by 6dB. This is useful when adding stereo signals that need more headroom due to being highly correlated.
2	LS_NEG_6dB	If set the class D output is attenuated by 6dB. This is useful when adding stereo signals that need more headroom due to being highly correlated.
3	AUX_NEG_6dB	If set the AUX output is attenuated by 6dB. This is useful when adding stereo signals that need more headroom due to being highly correlated.
4	CP_FORCE	If set, a -LS_VDD rail will be created on HP_VSS, even if the HP output stage is not required.

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Table 23. ADC_INPUT (0x15h)

Bits	Field	Description
0	DACR_ADCR	The right DAC output is added to the ADC right input.
1	DACL_ADCL	The left DAC output is added to the ADC left input.
2	MICR_ADCR	The right MIC input is added to the ADC right input. Setting this bit enables MIC BIAS.
3	MICL_ADCL	The left MIC input is added to the ADC left input. Setting this bit enables MIC BIAS.
4	AUXR_ADCR	The right AUX input is added to the ADC right input.
5	AUXL_ADCL	The left AUX input is added to the ADC left input.

Table 24. MIC_L_INPUT (0x16h)

Bits	Field	Description	
3:0	MIC_L_LEVEL	This sets the gain of the left microphone preamp.	
		MIC_L_LEVEL	Gain
		0000	6dB
		0001	8dB
		0010	10dB
		0011	12dB
		0100	14dB
		0101	16dB
		0110	18dB
		0111	20dB
		1000	22dB
		1001	24dB
		1010	26dB
		1011	28dB
		1100	30dB
		1101	32dB
		1110	34dB
		1111	36dB
4	SE_DIFF	If set, the MIC_L negative input is ignored.	
5	MUTE	If set, the left microphone preamp is muted.	

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Table 25. MIC_R_INPUT (0x17h)

Bits	Field	Description	
3:0	MIC_R_LEVEL	This sets the gain of the right microphone preamp.	
		MIC_R_LEVEL	Gain
		0000	6dB
		0001	8dB
		0010	10dB
		0011	12dB
		0100	14dB
		0101	16dB
		0110	18dB
		0111	20dB
		1000	22dB
		1001	24dB
		1010	26dB
		1011	28dB
		1100	30dB
		1101	32dB
		1110	34dB
		1111	36dB
4	SE_DIFF	If set, the MIC_R negative input is ignored.	
5	MUTE	If set, the right microphone preamp is muted.	

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Table 26. AUX_L_INPUT (0x18h)

Bits	Field	Description			
5:0	AUX_L_LEVEL	This programs the left AUX input level. All gain changes are performed at zero crossings.			
		AUX_L_LEVEL	Level	AUX_L_LEVEL	Level
		000000	–46.5dB	100000	1.5dB
		000001	–45dB	100001	3dB
		000010	–43.5dB	100010	4.5dB
		000011	–42dB	100011	6dB
		000100	–40.5dB	100100	7.5dB
		000101	–39dB	100101	9dB
		000110	–37.5dB	100110	10.5dB
		000111	–36dB	100111	12dB
		001000	–34.5dB	101000	12dB
		001001	–33dB	101001	12dB
		001010	–31.5dB	101010	12dB
		001011	–30dB	101011	12dB
		001100	–28.5dB	101100	12dB
		001101	–27dB	101101	12dB
		001110	–25.5dB	101110	12dB
		001111	–24dB	101111	12dB
		010000	–22.5dB	110000	12dB
		010001	–21dB	110001	12dB
		010010	–19.5dB	110010	12dB
		010011	–18dB	110011	12dB
		010100	–16.5dB	110100	12dB
		010101	–15dB	110101	12dB
		010110	–13.5dB	110110	12dB
		010111	–12dB	110111	12dB
		011000	–10.5dB	111000	12dB
		011000	–9dB	111001	12dB
		011001	–7.5dB	111010	12dB
		011010	–6dB	111011	12dB
		011100	–4.5dB	111100	12dB
		011101	–3dB	111101	12dB
		011110	–1.5dB	111110	12dB
		011111	0dB	111111	12dB
6	FROM_LINE_L	If set, the LEFT_MIC/LINE differential input is routed to the AUX_L input amplifier for line level volume control. This bit overrides the DIFF_MODE (bit 7 of 0x19h) setting.			

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Table 27. AUX_R_INPUT (0x19h)

Bits	Field	Description			
5:0	AUX_R_LEVEL	This programs the right AUX input level. All gain changes are performed at zero crossings.			
		AUX_R_LEVEL	Level	AUX_R_LEVEL	Level
		000000	–46.5dB	100000	1.5dB
		000001	–45dB	100001	3dB
		000010	–43.5dB	100010	4.5dB
		000011	–42dB	100011	6dB
		000100	–40.5dB	100100	7.5dB
		000101	–39dB	100101	9dB
		000110	–37.5dB	100110	10.5dB
		000111	–36dB	100111	12dB
		001000	–34.5dB	101000	12dB
		001001	–33dB	101001	12dB
		001010	–31.5dB	101010	12dB
		001011	–30dB	101011	12dB
		001100	–28.5dB	101100	12dB
		001101	–27dB	101101	12dB
		001110	–25.5dB	101110	12dB
		001111	–24dB	101111	12dB
		010000	–22.5dB	110000	12dB
		010001	–21dB	110001	12dB
		010010	–19.5dB	110010	12dB
		010011	–18dB	110011	12dB
		010100	–16.5dB	110100	12dB
		010101	–15dB	110101	12dB
		010110	–13.5dB	110110	12dB
		010111	–12dB	110111	12dB
		011000	–10.5dB	111000	12dB
		011000	–9dB	111001	12dB
		011001	–7.5dB	111010	12dB
		011010	–6dB	111011	12dB
		011100	–4.5dB	111100	12dB
		011101	–3dB	111101	12dB
		011110	–1.5dB	111110	12dB
		011111	0dB	111111	12dB
6	FROM_LINE_R	If set, the RIGHT_MIC/LINE differential input is routed to the AUX_R input amplifier for line level volume control. This bit overrides the DIFF_MODE (bit 7) setting.			
7	DIFF_MODE	If set, the stereo single-ended inputs AUX_L and AUX_R convert to a mono differential input pair MONO_IN+ and MONO_IN-. (MONO_IN+) - (MONO_IN-) is routed to the AUX_L input amplifier. (MONO_IN-) - (MONO_IN+) is routed to the AUX_R input amplifier. (unless overriden by the respective FROM_LINE bits).			

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ADC Control Registers

This register is used to control the LM49350's ADC:

Table 28. ADC Basic (0x20h)

Bits	Field	Description		
0	MONO	This sets mono or stereo operation of the ADC.		
		MONO	ADC Operation	
		0	Stereo Audio	
		1	Mono Voice (Right ADC channel disabled, Left ADC channel active)	
1	OSR	This sets the oversampling ratio of the ADC.		
		OSR	Stereo Audio ADC Oversampling Ratio	Mono Voice ADC Oversampling Ratio
		0	128	125
		1	64	128
2	MUTE_L	If set, a digital mute is applied to the Left (or mono) ADC output.		
3	MUTE_R	If set, a digital mute is applied to the Right ADC output.		
6.4	ADC_CLK_SEL	This selects the source of the ADC clock domain, ADC_SOURCE_CLK.		
		ADC_CLK_SEL	Source	
		000	MCLK	
		001	PORT1_RX_CLK	
		010	PORT2_RX_CLK	
		011	PLL1_OUTPUT2	
		100	PLL2_OUTPUT	
7	ADC_DSP_ONLY	If set the ADC's analog circuitry is disabled to reduce power consumption, however, ADC DSP functionality is maintained. This can be used to perform asyncronous resampling between audio rates of a common family. Setting this bit is also useful whenever applying Automatic Level Control (ALC) to an analog only audio path.		

Table 29. ADC_CLK_DIV (0x21h)

Bits	Field	Description	
7:0	ADC_CLK_DIV	This programs the half cycle divider that preceeds the ADC. The input of this divider should be around 12MHz. The default of this divider is 0x00. Program this divider with the division you want, multiplied by 2, and subtract 1.	
		ADC_CLK_DIV	Divides by
		00000000	1
		00000001	1
		00000010	1.5
		00000011	2
		—	—
		11111101	127
		11111110	127.5
		11111111	128

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Table 30. ADC TRIM (0x22h)

Bits	Field	Description
7:0	ADC_TRIM	If set, the ADC is compensated with recommended compensation filter coefficients. The recommended ADC compensation filter coefficients are programmed as follows:
		Register 0xF8h set to 0x00h
		Register 0xF9h set to 0x01h
		Register 0xFAh set to 0x96h
		Register 0xFBh set to 0xFBh
		Register 0xFCh set to 0x30h
		Register 0xFDh set to 0x62h

DAC Control Registers

This register is used to control the LM49350's DAC:

Table 31. DAC Basic (0x30h)

Bits	Field	Description	
1:0	MODE	This programs the over sampling ratio of the stereo DAC.	
		MODE	DAC Oversampling Ratio
		00	125
		01	128
		10	64
		11	32
2	MUTE_L	This digitally mutes the Left DAC output.	
3	MUTE_R	This digitally mutes the Right DAC output.	
6:4	DAC_CLK_SEL	This selects the source of the DAC clock domain, DAC_SOURCE_CLK.	
		DAC_CLK_SEL	Source
		000	MCLK
		001	PORT1_RX_CLK
		010	PORT2_RX_CLK
		011	PLL1_OUTPUT1
		100	PLL2_OUTPUT
7	DSP_ONLY	If set, the DAC's analog circuitry is disabled to reduce power consumption, however DAC DSP functionality is maintained. This can be used to perform asyncronous resampling between audio rates of a common family.	

Table 32. DAC_CLK_DIV (0x31h)

Bits	Field	Description	
7:0	DAC_CLK_DIV	This programs the half cycle divider that precedes the DAC. The input of this divider should be around 12MHz. The default of this divider is 0x00. Program this divider with the division you want, multiplied by 2, and subtract 1.	
		DAC_CLK_DIV	Divides by
		00000000	1
		00000001	1
		00000010	1.5
		00000011	2
		—	—
		11111101	127
		11111110	127.5
		11111111	128

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Digital Mixer Control Registers

DIGITAL MIXER

The LM49350's digital mixer allows for flexible routing of digital audio signals between both audio ports, DAC, and ADC. This mixer handles which digital data path (Port1 RX data, Port2 RX data, or ADC output) is routed to the DAC input. The digital mixer also selects the appropriate digital data path [Port1 RX data, Port2 RX data, ADC output, or DAC DSP (Interpolator)] output that is used for data transmission on Audio Port 1 and 2. Audio inputs to the digital mixer can be attenuated down to -18dB to avoid clipping conditions. The digital mixer also allows direct routing from the DAC interpolator output to the ADC decimator input which allows the DAC and ADC DSP blocks to be cascaded without having to enable the analog of the DAC and ADC inorder to save power.

Another key feature of the digital mixer is sample rate conversion (SRC) between audio ports. This allows simultaneous operation of the dual audio ports even if each port is operating at a different sample rate. The LM49350 can be used as an audio port bridge with SRC capability. The digital mixer allows either straight pass through between audio ports or, if desired, DSP effects can be added to the digital audio signal during audio port bridge operation. The digital mixer automatically handles stereo I^2S to mono PCM conversion between audio ports and vice versa.

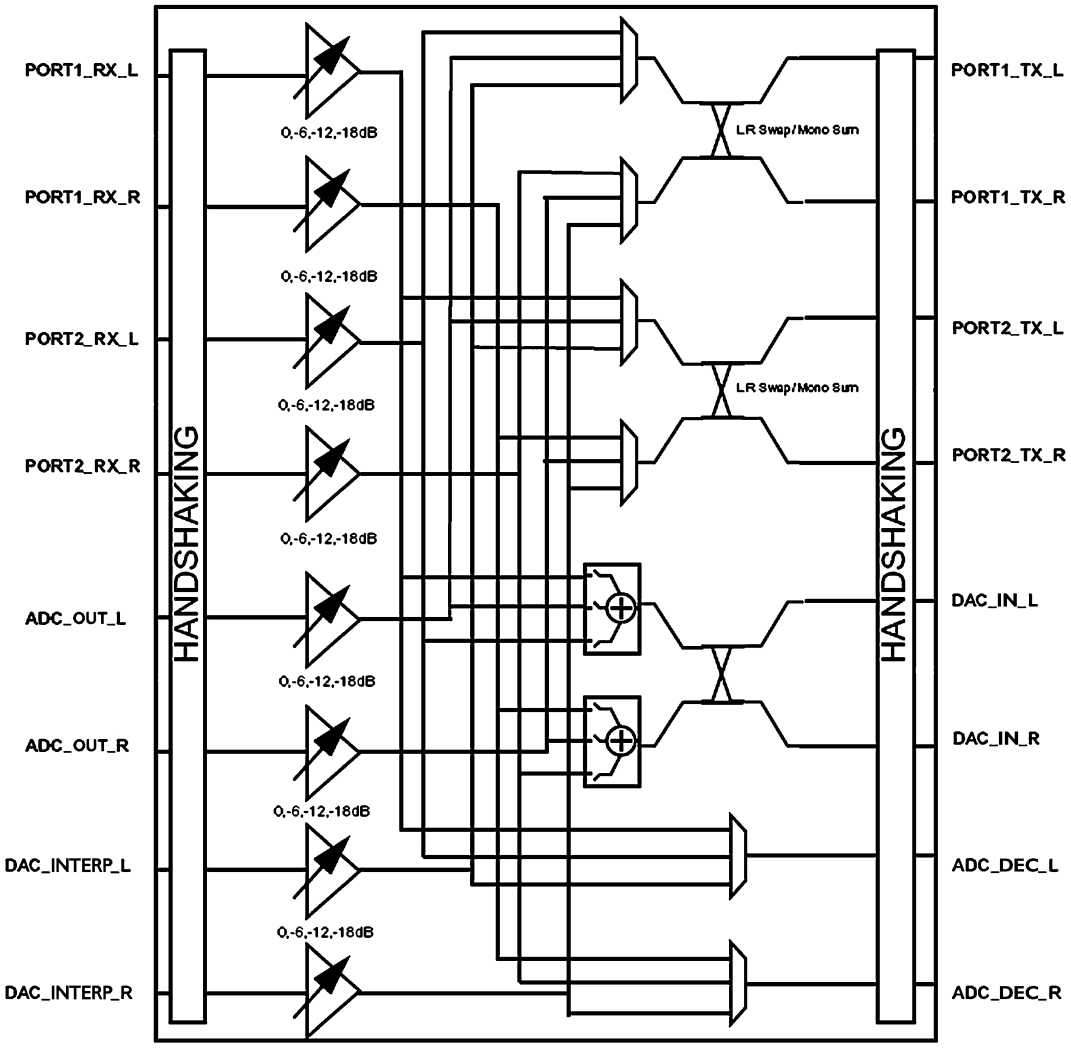


Figure 58. Digital Mixer

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The LM49350 includes two separate and independent DSP blocks, one for the DAC and the other for the ADC. The digital mixer also allows both DSP blocks to be cascaded together in either order so that the DSP effects from both blocks can be combined into the same signal path. For example, the 5 band parametric EQ of each DSP block can be combined together to form a 10 band parametric EQ for added flexibility.

This register is used to control the LM49350's digital mixer:

Table 33. Input Levels 1 (0x40h)

Bits	Field	Description	
1:0	PORT1_RX_L_LVL	This programs the input level of the data arriving from the left receive channel of Audio Port 1.	
		PORT1_RX_L_LVL	Level
		00	0dB
		01	–6dB
		10	–12dB
		11	–18dB
3:2	PORT1_RX_R_LVL	This programs the input level of the data arriving from the right receive channel of Audio Port 1.	
		PORT1_RX_R_LVL	Level
		00	0dB
		01	–6dB
		10	–12dB
		11	–18dB
5:4	PORT2_RX_L_LVL	This programs the input level of the data arriving from the left receive channel of Audio Port 2.	
		PORT2_RX_L_LVL	Level
		00	0dB
		01	–6dB
		10	–12dB
		11	–18dB
7:6	PORT2_RX_R_LVL	This programs the input level of the data arriving from the right receive channel of Audio Port 2.	
		PORT2_RX_R_LVL	Level
		00	0dB
		01	–6dB
		10	–12dB
		11	–18dB

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Table 34. Input Levels 2 (0x41h)

Bits	Field	Description	
1:0	ADC_L_LVL	This programs the input level of the data arriving from the left ADC channel.	
		ADC_L_LVL	Level
		00	0dB
		01	–6dB
		10	–12dB
		11	–18dB
3:2	ADC_R_LVL	This programs the input level of the data arriving from the right ADC channel.	
		ADC_R_LVL	Level
		00	0dB
		01	–6dB
		10	–12dB
		11	–18dB
5:4	INTERP_L_LVL	This programs the input level of the data arriving from the left DAC's interpolator output.	
		INTERP_L_LVL	Level
		00	0dB
		01	–6dB
		10	–12dB
		11	–18dB
7:6	INTERP_R_LVL	This programs the input level of the data arriving from the right DAC's interpolator output.	
		INTERP_R_LVL	Level
		00	0dB
		01	–6dB
		10	–12dB
		11	–18dB

Table 35. Audio Port 1 Input (0x42h)

Bits	Field	Description	
1:0	L_SEL	This selects which input is fed to the Left TX Channel of Audio Port 1.	
		L_SEL	Selected Input
		00	None
		01	ADC_L
		10	PORT2_RX_L
		11	DAC_INTERP_L
3:2	R_SEL	This selects which input is fed to the Right TX Channel of Audio Port 1.	
		R_SEL	Selected Input
		00	None
		01	ADC_R
		10	PORT2_RX_R
		11	DAC_INTERP_R
4	SWAP	If set, this swaps the Left and Right outputs to Audio Port 1. The swap bit can be used to control which microphone is being used for audio port transmit. For example, if LEFT_MIC is used as a primary handset microphone and RIGHT_MIC is used a headset microphone, the SWAP bit allows the audio port to select one of the microphones at a time for audio port transmit via the ADC.	
5	MONO	If set, the right channel is ignored and the left channel becomes (left+right)/2.	

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Table 36. Audio Port 2 Input (0x43h)

Bits	Field	Description	
1:0	L_SEL	This selects which input is fed to Audio Port 2's Left TX Channel.	
		L_SEL	Selected Input
		00	None
		01	ADC_L
		10	PORT1_RX_L
		11	DAC_INTERP_L
3:2	R_SEL	This selects which input is fed to Audio Port 2's Right TX Channel.	
		R_SEL	Selected Input
		00	None
		01	ADC_R
		10	PORT1_RX_R
		11	DAC_INTERP_R
4	SWAP	If set, this swaps the Left and Right outputs to Audio Port 2. The swap bit can be used to control which microphone is being used for audio port transmit. For example, if LEFT_MIC is used as a primary handset microphone and RIGHT_MIC is used a headset microphone, the SWAP bit allows the audio port to select one of the microphones at a time for audio port transmit via the ADC.	
5	MONO	If set, the right channel is ignored and the left channel becomes (left+right)/2.	

Table 37. DAC Input Select (0x44h)

Bits	Field	Description
0	PORT1_L	This adds Audio Port 1's left RX channel to the DAC's left input.
1	PORT2_L	This adds Audio Port 2's left RX channel to the DAC's left input.
2	ADC_L	This adds the ADC's left output to the DAC's left input
3	PORT1_R	This adds Audio Port 1's right RX channel to the DAC's right input.
4	PORT2_R	This adds Audio Port 2's right RX channel to the DAC's right input.
5	ADC_R	This adds the ADC's right output to the DAC's right input.
6	SWAP	If set, this swaps the Left and Right inputs to the DAC.

Table 38. Decimator Input Select (0x45h)

Bits	Field	Description	
1:0	L_SEL	This selects which input is fed to the left ADC's decimator input.	
		L_SEL	Selected Input
		00	None
		01	PORT1_RX_L
		10	PORT2_RX_L
		11	DAC_INTERP_L
3:2	R_SEL	This selects which input is fed to the right ADC's decimator input.	
		R_SEL	Selected Input
		00	None
		01	PORT1_RX_R
		10	PORT2_RX_R
		11	DAC_INTERP_R

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Table 38. Decimator Input Select (0x45h) (continued)

Bits	Field	Description	
5:4	MXR_CLK_SEL	This selects sets the source of the Digital Mixer Clock. The 'Auto' setting will automatically select the source with the highest clock frequency. Whenever the DAC interpolator (DAC_OSR_L or DAC_OSR_R) is selected then MXR_CLK_SEL should be set to '10'.	
		MXR_CLK_SEL	Selected Input
		00	Auto
		01	MCLK
		10	DAC
		11	ADC

Audio Port Control Registers

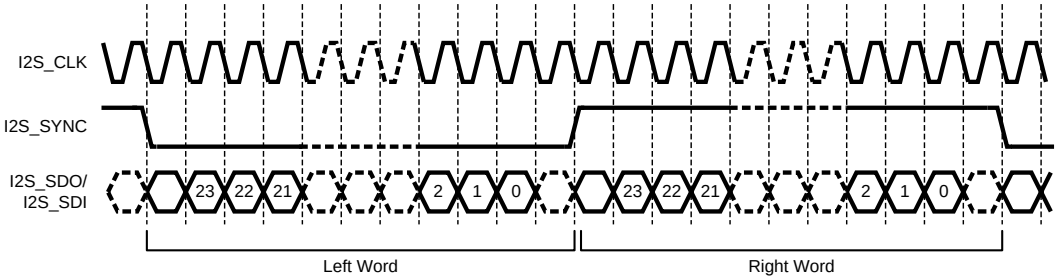


Figure 59. I²S Serial Data Format (24 bit example)

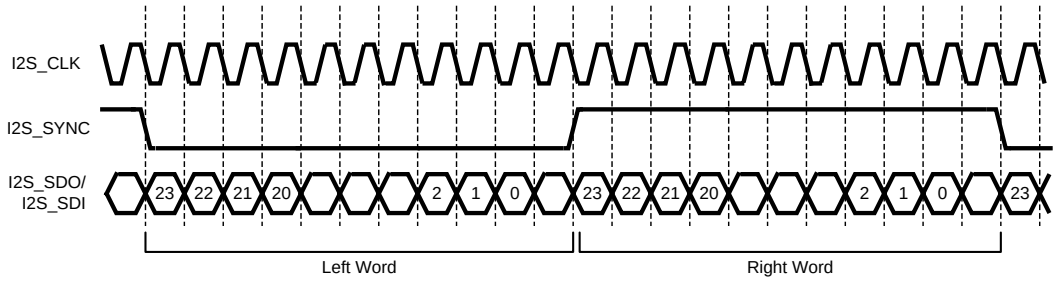


Figure 60. Left Justified Data Format (24 bit example)

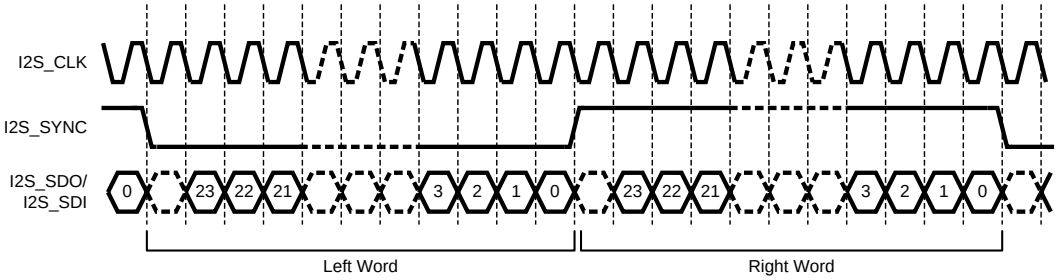


Figure 61. Right Justified Data Format (24 bit example)

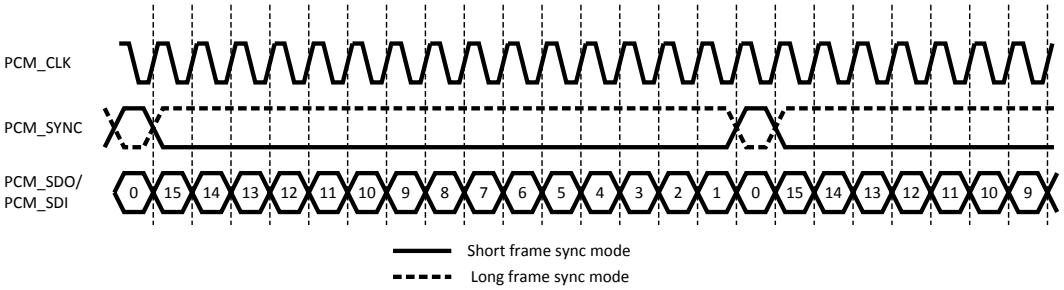


Figure 62. PCM Serial Data Format (16 bit example)

The following registers are used to control the LM49350's audio ports. Audio Port 1 and Audio Port 2 are identical. Port 1 is programmed through the (0x5Xh) registers. Port 2 is programmed through the (0x6Xh) registers.

Table 39. BASIC_SETUP (0x50h/0x60h)

Bits	Field	Description	
0	STEREO	If set, the audio port will receive and transmit stereo data.	
1	RX_ENABLE	If set the input is enabled (enables the SDI port and input shift register and any clock generation required).	
2	TX_ENABLE	If set the output is enabled (enables the SDO port and output shift register and any clock generation required).	
3	CLOCK_MS	If set the audio port will transmit the clock when either the RX or TX is enabled.	
4	SYNC_MS	If set the audio port will transmit the sync signal when either the RX or TX is enabled.	
5	CLOCK_PHASE	This sets how data is clocked by the Audio Port.	
		CLOCK_PHASE	Audio Data Mode
		0	I^2S (TX on falling edge, RX on rising edge)
		1	PCM (TX on rising edge, RX on falling edge)
6	STEREO_SYNC_PHASE	If set, this reverses the left and right channel data of the Audio Port.	
		STEREO_SYNC_PHASE	Audio Port Data Orientation
		0	Left channel data goes to left channel output. Right channel data goes to right channel output.
		1	Right channel data goes to left channel output. Left channel data goes to right channel output.
7	SYNC_INVERT	If this bit is set the SYNC is inverted before the receiver and transmitter.	
		SYNC_INVERT	Sync Orientation
		0	SYNC Low = Left, SYNC High = Right
		1	SYNC Low = Right, SYNC High = Left

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Table 40. CLK_GEN_1 (0x51h/0x61h)

Bits	Field	Description	
5:0	HALF_CYCLE_CLK_DIV	This programs the half-cycle divider that generates the master clocks in the audio port. The input of this divider should be around 12MHz. The default of this divider is 0x00, i.e. bypassed. Program this divider with the division you want, multiplied by 2, and subtract 1.	
		HALF_CYCLE_CLK_DIV	Divides By
		000000	BYPASS
		000001	1
		000010	1.5
		000011	2
		—	—
		111101	31
		111110	31.5
		11111	32
6	CLOCK_SEL	This selects the clock source of the master mode Audio Port Clock generator's half-cycle divider. 0 = DAC_SOURCE_CLK 1 = ADC_SOURCE_CLK	

Table 41. CLK_GEN_1 (0x52h/62h)

Bits	Field	Description	
2:0	SYNTH_NUM	Along with SYNTH_DENOM, this sets the clock divider that generates the Port 1 or Port 2 clock in master mode.	
		SYNTH_NUM	Numerator
		000	SYNTH_DENOM (1/1)
		001	100/SYNTH_DENOM
		010	96/SYNTH_DENOM
		011	80/SYNTH_DENOM
		100	72/SYNTH_DENOM
		101	64/SYNTH_DENOM
		110	48/SYNTH_DENOM
		111	0/SYNTH_DENOM
3	SYNTH_DENOM	Along with SYNTH_NUM, this sets the clock divider that generates the Port 1 or Port 2 clock in master mode.	
		SYNTH_DENOM	Denominator
		0	128
		1	125

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Table 42. CLK_GEN_1 (0x53h/63h)

Bits	Field	Description	
2:0	SYNC_RATE	This sets the number of clock cycles before the sync pattern repeats. This depends if the audio port data is mono or stereo. **In MONO mode:**	
		SYNC_RATE	Number of Clock Cycles
		000	8
		001	12
		010	16
		011	18
		100	20
		101	24
		110	25
		111	32
		In STEREO mode:	
		SYNC_RATE	Number of Clock Cycles
		000	16
		001	24
		010	32
		011	36
		100	40
		101	48
		110	50
		111	64
5:3	SYNC_WIDTH	In MONO mode, this programs the width (in number of bits) of the SYNC signal.	
		SYNC_WIDTH	Width of SYNC (in bits)
		000	1
		001	2
		010	4
		011	7
		100	8
		101	11
		110	15
		111	16

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Table 43. DATA_WIDTHS (0x54h/64h)

Bits	Field	Description	
2:0	RX_WIDTH	This programs the expected bits per word of the serial data input SDI.	
		RX_WIDTH	Bits
		000	24
		001	20
		010	18
		011	16
		100	14
		101	13
		110	12
		111	8
5:3	TX_WIDTH	This programs the bits per word of the serial data output SDO.	
		TX_WIDTH	Description
		000	24
		001	20
		010	18
		011	16
		100	14
		101	13
		110	12
		111	8
7:6	TX_EXTRA_BITS	This programs the TX data output padding.	
		TX_EXTRA_BITS	Description
		00	0
		01	1
		10	High-Z
		11	High-Z

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Table 44. RX_MODE (0x55h/65h)

Bits	Field	Description	
0	RX_MODE	This sets the RX data input justification with respect to the SYNC signal.	
		RX_MODE	Description
		0	MSB Justified
		1	LSB Justified
5:1	MSB_POSITION	This specifies the bit location of the MSB from the start of the frame (MSB Justified) or from the end of the frame (LSB Justified).	
		MSB_POSITION	Description
		00000	0(Left Justified/PCM Long)
		00001	1(I^2S/PCM Short)
		00010	2
		00011	3
		00100	4
		00101	5
		00110	6
		00111	7
		01000	8
		01001	9
		01010	10
		01011	11
		01100	12
		01101	13
		01110	14
		01111	15
		10000	16
		10001	17
		10010	18
		10011	19
		10100	20
		10101	21
		10110	22
		10111	23
		11000	24
		11001	25
		11010	26
		11011	27
		11100	28
		11101	29
		11110	30
		11111	31
6	COMPAND	If set, audio data will be companded.	
7	µLaw/A-Law	This sets the audio companding mode.	
		µLaw/A-Law	Compand Mode
		0	µLaw
		1	A-Law

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Table 45. TX_MODE (0x56h/x66h)

Bits	Field	Description	
0	TX_MODE	This sets the TX data output justification with respect to the SYNC signal.	
		TX_MODE	Description
		0	MSB Justified
		1	LSB Justified
5:1	MSB_POSITION	This specifies the bit location of the MSB from the start of the frame (MSB Justified) or from the end of the frame (LSB Justified).	
		MSB_POSITION	Description
		00000	0(Left Justified/PCM Long)
		00001	1(I^2S/PCM Short)
		00010	2
		00011	3
		00100	4
		00101	5
		00110	6
		00111	7
		01000	8
		01001	9
		01010	10
		01011	11
		01100	12
		01101	13
		01110	14
		01111	15
		10000	16
		10001	17
		10010	18
		10011	19
		10100	20
		10101	21
		10110	22
		10111	23
		11000	24
		11001	25
		11010	26
		11011	27
		11100	28
		11101	29
		11110	30
		11111	31
6	COMPAND	If set, audio data will be companded.	
7	µLaw/A-Law	This sets the audio companding mode.	
		µLaw/A-Law	Compand Mode
		0	µLaw
		1	A-Law

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Digital Effects Engine

DIGITAL SIGNAL PROCESSOR (DSP)

The LM49350 is designed to handle the entire audio signal conditioning and processing within the audio system, thereby freeing up the workload of any other applications processor contained within the system. The LM49350 features two independent DSPs, one for the DAC and the other for the ADC. Each DSP is fully featured and performs as a professional quality digital audio effects engine. The data paths on each DSP engine are 24 bits wide for ultimate flexibility. Both DSP engines feature digital volume control, automatic level control (ALC), digital soft clip compression, and a 5-band parametric EQ. The ADC DSP engine adds a dedicated high-pass filter to reduce wind noise or pop noise during uplink. The DAC DSP engine adds a digital 3D algorithm that allows for stereo widening of the original audio signal. The effects chain of each DSP engine is shown by the diagrams below.

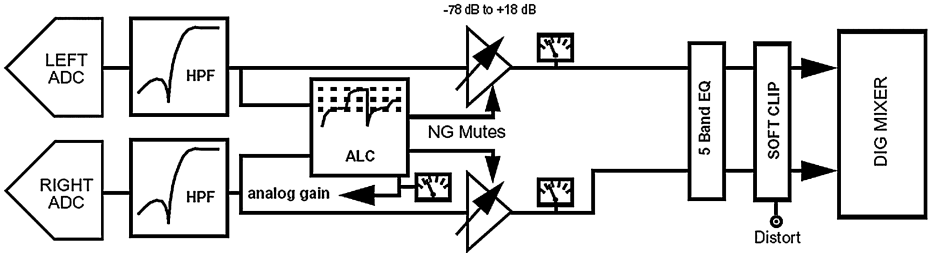


Figure 63. ADC DSP Effects Chain

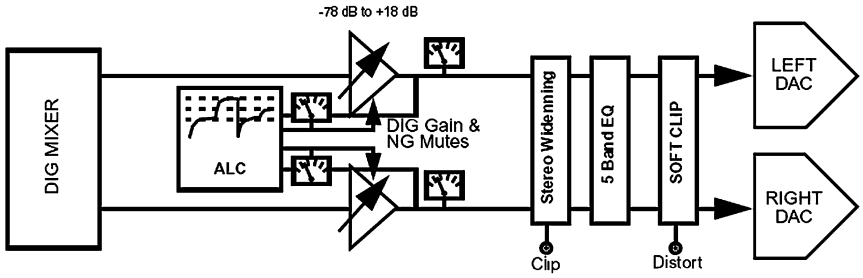


Figure 64. DAC DSP Effects Chain

The ADC and DAC DSP engines can be cascaded together in any order via the digital mixer to combine different audio effects to the same signal path. For example, a signal can be processed with high-pass filtering from the ADC effects engine with 3D stereo widening from the DAC effects engine. The 5-band parametric EQs from each DSP engine can be combined to form a single 10-band parametric EQ or a single 5-band parametric EQ with ±30dB (instead of ±15dB) gain control for each band.

Table 46. ADC EFFECTS (0x70h)

Bits	Field	Description
0	ADC_HPF_ENB	This enables the ADC's High Pass Filter.
1	ADC_ALC_ENB	This enables the ADC's Auto Level Control.
2	ADC_PK_ENB	This enables the ADC's Peak Detector.
3	ADC_EQ_ENB	This enables the ADC's 5-band Parametric EQ.
4	ADC_SCLP_ENB	This enables the ADC's Soft Clip Feature.

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Table 47. DAC EFFECTS (0x71h)

Bits	Field	Description
0	DAC_ALC_ENB	This enables the DAC's Auto Level Control.
1	DAC_PK_ENB	This enables the DAC's Peak Detector.
2	DAC_EQ_ENB	This enables the DAC's 5-band Parametric EQ.
3	DAC_3D_ENB	This enables the DAC's Stereo Widening Circuit.
4	ADC_SCLP_ENB	This enables the DAC's Soft Clip Feature.

Table 48. HPF MODE (0x80h)

Bits	Field	Description		
2:0	HPF_MODE	This configures the ADC's High Pass Filter. To calculate the –3dB cutoff frequency, multiply the coefficient by the sample rate (Hz): $f_C = X_N.f_{S(Hz)}$		
		HPF_MODE	Coefficient	Filter Characteristics
				f_C = 220Hz for:
		000	X_0 = 0.0275	8kHz Voice
		001	X_1 = 0.01833	12kHz Voice
		010	X_2 = 0.01375	16kHz Voice
		011	X_3 = 0.009166	24kHz Voice
		100	X_4 = 0.006875	32kHz Voice
				f_C = 100Hz for:
		101	X_5 = 0.003125	32kHz Audio
		110	X_6 = 0.0020833	48kHz Audio
				f_C =150Hz for:
		111	X_7 = 0.0015625	96kHz Audio

ALC OVERVIEW

The Automatic Level Control (ALC) system can be used to regulate the audio output level to a user defined target level. The ALC feature is especially useful whenever the level of the audio input is unknown, unpredictable, or has a large dynamic range. The main purpose of the ALC is to optimize the dynamic range of the audio input to audio output path.

There are two separate and independent ALC circuits in the LM49350. One of the ALC circuits is located within the DAC DSP effects block. The other ALC circuit is integrated into the ADC DSP effects block. The DAC ALC controls the DAC digital gain. The ADC ALC controls the auxiliary input amplifier gain or microphone preamplifier gain. The dual ALCs can be used to regulate the level of the analog (Stereo Auxiliary, mono differential, Stereo MIC/LINE) and digital (Port1 Data In, Port2 Data In) audio inputs. The ALC regulated output can be routed to any of the LM49350's amplifier outputs for playback. The ALC regulated output can also be routed to Audio Port1 or Audio Port2 for digital data transmission via I^2S or PCM.

Only audio inputs that are considered signals (rather than noise) are sent to the ALC's peak detector block. The peak detector compares the level of the audio input versus the ALC target level (TARGET_LEVEL). Signals lower than the target level will be amplified and signals higher than the target level will be attenuated. Any audio input that is lower than the level specified by the noise floor level (NOISE_FLOOR) will be considered as noise and will be gated from the ALC's peak detector in order to avoid noise pumping. So it is important to set NOISE_FLOOR to correlate with the signal to noise ratio of the corresponding audio path. In some instances (ie. Conference calls), it may be desirable to mute audio input signals that consist solely of background noise from the audio output. This is accomplished by enabling the ALC's noise gate (NG_ENB). When the noise gate is enabled, signals lower than the noise floor level will be muted from the audio output.

If the audio input signal is below the target level, the ALC will increase the gain of the corresponding volume control until the signal reaches the target level. The rate at which the ALC performs gain increases is known as decay rate (DECAY RATE). But before each ALC gain increase the ALC must wait a predetermined amount of time (HOLD TIME). If the audio input signal is above the target level, the ALC will decrease the gain of the corresponding volume control until the signal reaches the target level. The rate at which the ALC performs attenuation is known as attack rate (ATTACK RATE). The ALC's peak detector tracks increases in audio input

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signal amplitude instantaneously, but tracks decreases in audio input signal amplitude at programmable rate (PEAK DECAY TIME). ATTACK RATE, DECAY RATE, HOLD TIME, and PEAK DECAY TIME are fully adjustable which allows flexible operation of the ALC circuit. The ALC's timers are based on the sample rate of the DAC or ADC, so the closest corresponding sample rate must be programmed into the ALC SAMPLE RATE setting (for DAC ALC) or the ALC MODE setting (for ADC ALC).

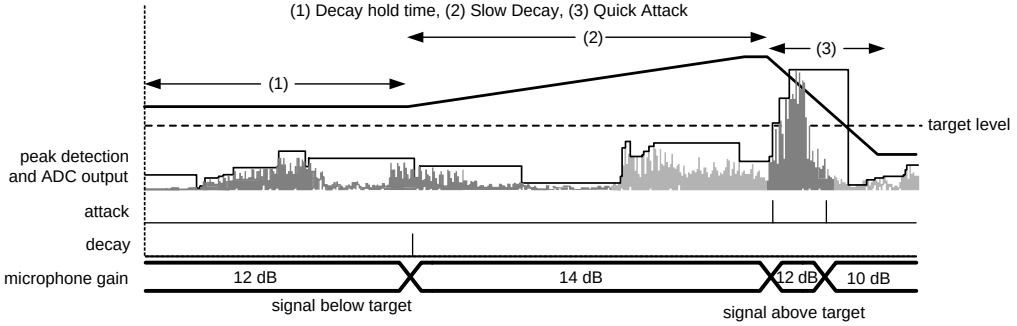


Figure 65. ALC Example

Table 49. ADC_ALC_1 (0x81h)

Bits	Field	Description	
2:0	SAMPLE_RATE	This programs the timers on the ALC with the closest sample rate of the ADC.	
		SAMPLE_RATE	ADC Fs
		000	8kHz
		001	12kHz
		010	16kHz
		011	24kHz
		100	32kHz
		101	48kHz
		110	96kHz
		111	192kHz
3	LIMITER	If set, the circuit will never apply gain to the signal, no matter how small, but it will attenuate the signal as soon as it reaches target and release it at the decay rate, once signal level reduces below target. The I^2C gain setting (at the time the LIMITER is enabled) is the maximum gain that the ALC will apply. Care should be taken when choosing the optimum I^2C gain setting whenever enabling the Limiter.	
4	STEREO LINK	If set, the ALC circuit uses the stereo average of the input signals to control the gain of the stereo output. This maintains stereo imaging. If this bit is cleared, then both channels operate as dual mono.	
5	SOURCE_SEL	If SOURCE_OVR is set then this manually overrides the selection of the input amplifier that is used to alter the gain for ALC operation. 0 = Both ALCs control AUX gain 1 = Both ALCs control MIC gain	
6	SOURCE_OVR	If set, the output of the ALC is not set automatically but is controlled by the SOURCE_SEL bit. If cleared each ALC controls the input gain of the amplifier (AUX or MIC) that is set to that ADC channel (or MIC if both are selected).	

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Table 50. ADC_ALC_2 (0x82h)

Bits	Field	Description	
3:0	NOISE_FLOOR	This sets the anticipated noise floor. Signals lower than the noise floor specified will be gated from the ALC to avoid noise pumping.	
		NOISE_FLOOR	Noise Floor (dB)
		0000	–39
		0001	–42
		0010	–45
		0011	–48
		0100	–51
		0101	–54
		0110	–57
		0111	–60
		1000	–63
		1001	–66
		1010	–69
		1011	–72
		1100	–75
		1101	–78
		1110	–81
		1111	–84
4	NG_ENB	This enables the Noise Gate.	

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Table 51. ADC_ALC_3 (0x83h)

Bits	Field	Description	
4:0	TARGET_LEVEL	This sets the desired target output level. Signals lower than this will be amplified and signals larger than this will be attenuated.	
		TARGET_LEVEL	Target Level (dB)
		00000	–1.5
		00001	–3
		00010	–4.5
		00011	–6
		00100	–7.5
		00101	–9
		00110	–10.5
		00111	–12
		01000	–13.5
		01001	–15
		01010	–16.5
		01011	–18
		01100	–19.5
		01101	–21
		01110	–22.5
		01111	–24
		10000	–25.5
		10001	–27
		10010	–28.5
		10011	–30
		10100	–31.5
		10101	–33
		10110	–34.5
		10111	–36
		11000	–37.5
		11001	–39
		11010	–40.5
		11011	–42
		11100	–43.5
		11101	–45
		11110	–46.5
		11111	–48

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Table 52. ADC_ALC_4 (0x84h)

Bits	Field	Description	
4:0	ATTACK_RATE	This sets the rate at which the ALC will reduce gain if it detects the input signal is large.	
		ATTACK_RATE	Time between gain steps (µs)
		00000	21
		00001	42
		00010	83
		00011	167
		00100	250
		00101	333
		00110	417
		00111	542
		01000	729
		01001	958
		01010	1250
		01011	1604
		01100	1896
		01101	2208
		01110	2792
		01111	3708
		10000	4792
		10001	5688
		10010	6563
		10011	8396
		10100	11000
		10101	14167
		10110	17083
		10111	20000
		11000	25000
		11001	32000
		11010	45000
		11011	60000
		11100	75000
		11101	87500
		11110	100000
		11111	114583

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Table 53. ADC_ALC_5 (0x85h)

Bits	Field	Description	
4:0	DECAY_RATE	This sets the rate at which the ALC will increase gain if it detects the input signal is too small.	
		DECAY_RATE	Time between gain steps (µs)
		00000	104
		00001	125
		00010	167
		00011	250
		00100	292
		00101	396
		00110	500
		00111	708
		01000	896
		01001	1250
		01010	1396
		01011	2000
		01100	2708
		01101	3500
		01110	4750
		01111	6250
		10000	8000
		10001	11000
		10010	14000
		10011	18500
		10100	25000
		10101	32000
		10110	42000
		10111	55000
		11000	72500
		11001	100000
		11010	125000
		11011	160000
		11100	225000
		11101	300000
		11110	375000
		11111	500000 (0.5s)
7:5	PK_DECAY_RATE	PK_DECAY_RATE	Max Time to track decay
		000	1.3ms
		001	2.6ms
		010	5.3ms
		011	10.6ms
		100	21.3ms
		101	42.6.3ms
		110	85.5ms
		111	2.73 secs

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Table 54. ADC_ALC_6 (0x86h)

Bits	Field	Description	
4:0	HOLD_TIME	This sets how long the ALC circuit waits before increasing the gain.	
		HOLD_TIME	Time (ms)
		00000	1
		00001	1.25
		00010	1.6
		00011	2
		00100	2.5
		00101	3.2
		00110	4
		00111	5
		01000	6.25
		01001	8
		01010	10
		01011	12.5
		01100	16
		01101	20
		01110	25
		01111	32
		10000	40
		10001	50
		10010	64
		10011	80
		10100	100
		10101	125
		10110	160
		10111	200
		11000	250
		11001	320
		11010	400
		11011	500
		11100	640
		11101	800
		11110	1000
		11111	1250

Table 55. ADC_ALC_7 (0x87h)

Bits	Field	Description
5:0	MAX_LEVEL	This sets the maximum allowed gain of the volume control to the output amplifier. If the volume control is less than 6 bits the relevant LSBs are used as the limit and the MSBs are ignored.

Table 56. ADC_ALC_8 (0x88h)

Bits	Field	Description
5:0	MIN_LEVEL	This sets the minimum allowed gain of the volume control to the output amplifier. If the volume control is less than 6 bits the relevant LSBs are used as the limit and the MSBs are ignored.

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Table 57. ADC_L_LEVEL (0x89h) (Default data value is 0x33h)

Bits	Field	Description			
5:0	ADC_L_LEVEL	This sets the post ADC digital gain of the left channel.			
		ADC_L_LEVEL	Level	ADC_L_LEVEL	Level
		000000	-76.5dB	100000	-28.5dB
		000001	-75dB	100001	-27dB
		000010	-73.5dB	100010	-25.5dB
		000011	-72dB	100011	-24dB
		000100	-70.5dB	100100	-22.5dB
		000101	-69dB	100101	-21dB
		000110	-67.5dB	100110	-20.5dB
		000111	-66dB	100111	-18dB
		001000	-64.5dB	101000	-16.5dB
		001001	-63dB	101001	-15dB
		001010	-61.5dB	101010	-13.5dB
		001011	-60dB	101011	-12dB
		001100	-58.5dB	101100	-10.5dB
		001101	-57dB	101101	-9dB
		001110	-55.5dB	101110	-7.5dB
		001111	-54dB	101111	-6dB
		010000	-52.5dB	110000	-4.5dB
		010001	-51dB	110001	-3dB
		010010	-49.5dB	110010	-1.5dB
		010011	-48dB	110011	0dB
		010100	-46.5dB	110100	1.5dB
		010101	-45dB	110101	3dB
		010110	-43.5dB	110110	4.5dB
		010111	-42dB	110111	6dB
		011000	-40.5dB	111000	7.5dB
		011001	-39dB	111001	9dB
		011010	-37.5dB	111010	10.5dB
		011011	-36dB	111011	12dB
		011100	-34.5dB	111100	13.5dB
		011101	-33dB	111101	15dB
		011110	-31.5dB	111110	16.5dB
		011111	-30dB	111111	18dB

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Table 58. ADC_R_LEVEL (0x8Ah) (Default data value is 0x33h)

Bits	Field	Description			
5:0	ADC_R_LEVEL	This sets the post ADC digital gain of the right channel.			
		ADC_R_LEVEL	Level	ADC_R_LEVEL	Level
		000000	-76.5dB	100000	-28.5dB
		000001	-75dB	100001	-27dB
		000010	-73.5dB	100010	-25.5dB
		000011	-72dB	100011	-24dB
		000100	-70.5dB	100100	-22.5dB
		000101	-69dB	100101	-21dB
		000110	-67.5dB	100110	-20.5dB
		000111	-66dB	100111	-18dB
		001000	-64.5dB	101000	-16.5dB
		001001	-63dB	101001	-15dB
		001010	-61.5dB	101010	-13.5dB
		001011	-60dB	101011	-12dB
		001100	-58.5dB	101100	-10.5dB
		001101	-57dB	101101	-9dB
		001110	-55.5dB	101110	-7.5dB
		001111	-54dB	101111	-6dB
		010000	-52.5dB	110000	-4.5dB
		010001	-51dB	110001	-3dB
		010010	-49.5dB	110010	-1.5dB
		010011	-48dB	110011	0dB
		010100	-46.5dB	110100	1.5dB
		010101	-45dB	110101	3dB
		010110	-43.5dB	110110	4.5dB
		010111	-42dB	110111	6dB
		011000	-40.5dB	111000	7.5dB
		011001	-39dB	111001	9dB
		011010	-37.5dB	111010	10.5dB
		011011	-36dB	111011	12dB
		011100	-34.5dB	111100	13.5dB
		011101	-33dB	111101	15dB
		011110	-31.5dB	111110	16.5dB
		011111	-30dB	111111	18dB

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Table 59. EQ_BAND_1 (0x8Bh)

Bits	Field	Description	
1:0	FREQ	This sets the Sub-bass shelving filter's cut-off frequency. The cut-off frequencies shown are based on a 48kHz sample rate. Using lower sample rates will scale down the cut-off frequencies proportionately.	
		FREQ	Frequency (Hz)
		00	60
		01	80
		10	100
		11	120
6:2	LEVEL	This sets the gain at f_c.	
		LEVEL	Effect
		00000	Off (0dB)
		00001	-15dB
		00010	-14dB
		00011	-13dB
		00100	-12dB
		00101	-11dB
		00110	-10dB
		00111	-9dB
		01000	-8dB
		01001	-7dB
		01010	-6dB
		01011	-5dB
		01100	-4dB
		01101	-3dB
		01110	-2dB
		01111	-1dB
		10000	0dB
		10001	1dB
		10010	2dB
		10011	3dB
		10100	4dB
		10101	5dB
		10110	6dB
		10111	7dB
		11000	8dB
		11001	9dB
		11010	10dB
		11011	11dB
		11100	12dB
		11101	13dB
		11110	14dB
		11111	15dB

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Table 60. EQ_BAND_2 (0x8Ch)

Bits	Field	Description	
1:0	FREQ	This sets the Bass peak filter's center frequency. The cut-off frequencies shown are based on a 48kHz sample rate. Using lower sample rates will scale down the cut-off frequencies proportionately.	
		FREQ	Frequency (Hz)
		00	150
		01	200
		10	250
		11	300
6:2	LEVEL	This sets the gain at fc.	
		LEVEL	Effect
		00000	Off (0dB)
		00001	-15dB
		00010	-14dB
		00011	-13dB
		00100	-12dB
		00101	-11dB
		00110	-10dB
		00111	-9dB
		01000	-8dB
		01001	-7dB
		01010	-6dB
		01011	-5dB
		01100	-4dB
		01101	-3dB
		01110	-2dB
		01111	-1dB
		10000	0dB
		10001	1dB
		10010	2dB
		10011	3dB
		10100	4dB
		10101	5dB
		10110	6dB
		10111	7dB
		11000	8dB
		11001	9dB
		11010	10dB
		11011	11dB
		11100	12dB
		11101	13dB
		11110	14dB
		11111	15dB
7	Q	Programs the width of the peak filter.	
		Q	Bandwidth
		0	2/3 Octave
		1	4/3 Octave

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Table 61. EQ_BAND_3 (0x8Dh)

Bits	Field	Description	
1:0	FREQ	This sets the Mid peak filter's center frequency. The cut-off frequencies shown are based on a 48kHz sample rate. Using lower sample rates will scale down the cut-off frequencies proportionately.	
		FREQ	Frequency (Hz)
		00	600
		01	800
		10	1k
		11	1.2k
6:2	LEVEL	This sets the gain at f_C.	
		LEVEL	Effect
		00000	Off (0dB)
		00001	-15dB
		00010	-14dB
		00011	-13dB
		00100	-12dB
		00101	-11dB
		00110	-10dB
		00111	-9dB
		01000	-8dB
		01001	-7dB
		01010	-6dB
		01011	-5dB
		01100	-4dB
		01101	-3dB
		01110	-2dB
		01111	-1dB
		10000	0dB
		10001	1dB
		10010	2dB
		10011	3dB
		10100	4dB
		10101	5dB
		10110	6dB
		10111	7dB
		11000	8dB
		11001	9dB
		11010	10dB
		11011	11dB
		11100	12dB
		11101	13dB
		11110	14dB
		11111	15dB
7	Q	This programs the width of the peak filter.	
		Q	Bandwidth
		0	2/3 Octave
		1	4/3 Octave

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Table 62. EQ_BAND_4 (0x8Eh)

Bits	Field	Description	
1:0	FREQ	This sets the Treble peak filter's center frequency. The cut-off frequencies shown are based on a 48kHz sample rate. Using lower sample rates will scale down the cut-off frequencies proportionately.	
		FREQ	Frequency (Hz)
		00	2k
		01	2.7k
		10	3.4k
		11	4.1k
6:2	LEVEL	This sets the gain at f_C.	
		LEVEL	Effect
		00000	Off (0dB)
		00001	-15dB
		00010	-14dB
		00011	-13dB
		00100	-12dB
		00101	-11dB
		00110	-10dB
		00111	-9dB
		01000	-8dB
		01001	-7dB
		01010	-6dB
		01011	-5dB
		01100	-4dB
		01101	-3dB
		01110	-2dB
		01111	-1dB
		10000	0dB
		10001	1dB
		10010	2dB
		10011	3dB
		10100	4dB
		10101	5dB
		10110	6dB
		10111	7dB
		11000	8dB
		11001	9dB
		11010	10dB
		11011	11dB
		11100	12dB
		11101	13dB
		11110	14dB
		11111	15dB
7	Q	This programs the width of the peak filter.	
		Q	Bandwidth
		0	2/3 Octave
		1	4/3 Octave

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Table 63. EQ_BAND_5 (0x8Fh)

Bits	Field	Description	
1:0	FREQ	This sets the presence shelving filter's cut-off frequency. The cut-off frequencies shown are based on a 48kHz sample rate. Using lower sample rates will scale down the cut-off frequencies proportionately.	
		FREQ	Frequency (Hz)
		00	7k
		01	9k
		10	11k
		11	20k
6:2	LEVEL	This sets the gain at f_C.	
		LEVEL	Effect
		00000	Off (0dB)
		00001	-15dB
		00010	-14dB
		00011	-13dB
		00100	-12dB
		00101	-11dB
		00110	-10dB
		00111	-9dB
		01000	-8dB
		01001	-7dB
		01010	-6dB
		01011	-5dB
		01100	-4dB
		01101	-3dB
		01110	-2dB
		01111	-1dB
		10000	0dB
		10001	1dB
		10010	2dB
		10011	3dB
		10100	4dB
		10101	5dB
		10110	6dB
		10111	7dB
		11000	8dB
		11001	9dB
		11010	10dB
		11011	11dB
		11100	12dB
		11101	13dB
		11110	14dB
		11111	15dB

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Table 64. SOFTCLIP1 (0x90h)

Bits	Field	Description	
3:0	THRESHOLD	This sets the threshold level of the audio compressor. Audio signals above the threshold will be compressed.	
		THRESHOLD	Threshold Level (dB)
		0000	-36dB
		0001	-30dB
		0010	-24dB
		0011	-20dB
		0100	-18dB
		0101	-17dB
		0110	-16dB
		0111	-15dB
		1000	-14dB
		1001	-12dB
		1010	-10dB
		1011	-8dB
		1100	-6dB
		1101	-4dB
		1110	-2.5dB
		1111	-1dB
4	SOFT_KNEE	If set, the audio compressor will automatically apply higher compression ratios to audio signals higher than the threshold level. As the audio signal approaches levels higher than the threshold, SOFT_KNEE will increase the compression RATIO. The highest compression that the SOFT_KNEE algorithm will apply is the compression that is set by RATIO.	

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Table 65. SOFTCLIP2 (0x91h)

Bits	Field	Description	
4:0	RATIO	This sets the ratio at which the audio is compressed to when it passes beyond the threshold. In SOFT_KNEE mode this is the final level of compression.	
		RATIO	Ratio
		00000	1:1 (Bypass)
		00001	1:1.2
		00010	1:1.4
		00011	1:1.7
		00100	1:2.0
		00101	1:2.4
		00110	1:2.8
		00111	1:3.4
		01000	1:4.0
		01001	1:4.7
		01010	1:5.7
		01011	1:6.7
		01100	1:8.0
		01101	1:9.5
		01110	1:11.3
		01111	1:13.5
		10000	1:16.0
		10001	1:19.0
		10010	1:22.8
		10011	1:27.0
		10100	1:32.0
		10101	1:37.9
		10110	1:45.5
		10111	1:53.9
		11000	1:64.0
		11001	1:75.0
		11010	1:91.0
		11011	1:108
		11100	1:128
		11101	1:152
		11110	1:182
		11111	1:215

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Table 66. SOFTCLIP3 (0x92h)

Bits	Field	Description	
4:0	LEVEL	This sets the post compressor gain level.	
		LEVEL	Level (dB)
		00000	-22.5dB
		00001	-21dB
		00010	-19.5dB
		00011	-18dB
		00100	-16.5dB
		00101	-15dB
		00110	-13.5dB
		00111	-12dB
		01000	-10.5dB
		01001	-9dB
		01010	-7.5dB
		01011	-6dB
		01100	-4.5dB
		01101	-3dB
		01110	-1.5dB
		01111	0dB
		10000	1.5dB
		10001	3dB
		10010	4.5dB
		10011	6dB
		10100	7.5dB
		10101	9dB
		10110	10.5dB
		10111	12dB
		11000	13.5dB
		11001	15dB
		11010	16.5dB
		11011	18dB
		11100	19.5dB
		11101	21dB
		11110	22.5dB
		11111	24dB

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DAC Effects Registers

Table 67. DAC_ALC_1 (0xA0h)

Bits	Field	Description	
2:0	SAMPLE_ RATE	This programs the timers on the ALC with the closest DAC sample rate.	
		SAMPLE_ RATE	DAC Fs
		000	8kHz
		001	12kHz
		010	16kHz
		011	24kHz
		100	32kHz
		101	48kHz
		110	96kHz
		111	192kHz
3	LIMITER	If set, the circuit will never apply gain to the signal, no matter how small, but it will attenuate the signal as soon as it reaches target and release it at the decay rate, once signal level reduces below target. The I^2C gain setting (at the time the LIMITER is enabled) is the maximum gain that the ALC will apply. Care should be taken when choosing the optimum I^2C gain setting whenever enabling the Limiter.	
4	STEREO LINK	If set, the ALC circuit uses the stereo average of the input signals to control the gain of the stereo output. This maintains stereo imaging. If this bit is cleared, then both channels operate as dual mono.	

Table 68. DAC_ALC_2 (0xA1h)

Bits	Field	Description	
3:0	NOISE_FLOOR	This sets the anticipated noise floor. Signals lower than the specified noise floor will be gated from the ALC to avoid noise pumping.	
		NOISE_FLOOR	Noise Floor (dB)
		0000	-39
		0001	-42
		0010	-45
		0011	-48
		0100	-51
		0101	-54
		0110	-57
		0111	-60
		1000	-63
		1001	-66
		1010	-69
		1011	-72
		1100	-75
		1101	-78
		1110	-81
		1111	-84
4	NG_ENB	This enables the Noise Gate	

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Table 69. DAC_ALC_3 (0xA2h)

Bits	Field	Description	
4:0	TARGET_LEVEL	This sets the desired output level. Signals lower than this will be amplified and signals larger than this will be attenuated.	
		TARGET_LEVEL	Target Level (dB)
		00000	-1.5
		00001	-3
		00010	-4.5
		00011	-6
		00100	-7.5
		00101	-9
		00110	-10.5
		00111	-12
		01000	-13.5
		01001	-15
		01010	-16.5
		01011	-18
		01100	-19.5
		01101	-21
		01110	-22.5
		01111	-24
		10000	-25.5
		10001	-27
		10010	-28.5
		10011	-30
		10100	-31.5
		10101	-33
		10110	-34.5
		10111	-36
		11000	-37.5
		11001	-39
		11010	-40.5
		11011	-42
		11100	-43.5
		11101	-45
		11110	-46.5
		11111	-48

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Table 70. DAC_ALC_4 (0xA3h)

Bits	Field	Description	
4:0	ATTACK_RATE	This sets the rate at which the ALC will reduce gain if it detects the input signal is too large.	
		ATTACK_RATE	Time between gain steps(us)
		00000	21
		00001	42
		00010	83
		00011	167
		00100	250
		00101	333
		00110	417
		00111	542
		01000	729
		01001	958
		01010	1250
		01011	1604
		01100	1896
		01101	2208
		01110	2792
		01111	3708
		10000	4792
		10001	5688
		10010	6563
		10011	8396
		10100	11000
		10101	14167
		10110	17083
		10111	20000
		11000	25000
		11001	32000
		11010	45000
		11011	60000
		11100	75000
		11101	87500
		11110	100000
		11111	114583

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Table 71. DAC_ALC_5 (0xA4h)

Bits	Field	Description	
4:0	DECAY_RATE	This sets the rate at which the ALC will increase gain if it detects the input signal is too small.	
		DECAY_RATE	Time between gain steps (us)
		00000	104
		00001	125
		00010	167
		00011	250
		00100	292
		00101	396
		00110	500
		00111	708
		01000	896
		01001	1250
		01010	1396
		01011	2000
		01100	2708
		01101	3500
		01110	4750
		01111	6250
		10000	8000
		10001	11000
		10010	14000
		10011	18500
		10100	25000
		10101	32000
		10110	42000
		10111	55000
		11000	72500
		11001	100000
		11010	125000
		11011	160000
		11100	225000
		11101	300000
		11110	375000
		11111	500000 (0.5s)
7:5	PK_DECAY_RATE	This sets how precise the ALC will track amplitude reductions of the audio input. The shorter the length of time for PK_DECAY_RATE, the more responsive the ALC will be when applying gain increases whenever the audio falls below target level.	
		PK_DECAY_RATE	Time
		000	1.3ms
		001	2.6ms
		010	5.3ms
		011	10.6ms
		100	21.3ms
		101	42.6ms
		110	85.5ms
		111	2.73secs

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Table 72. DAC_ALC_6 (0xA5h)

Bits	Field	Description	
4:0	HOLD_TIME	This sets how long the ALC circuit waits before increasing the gain.	
		HOLDTIME	Time (ms)
		00000	1
		00001	1.25
		00010	1.6
		00011	2
		00100	2.5
		00101	3.2
		00110	4
		00111	5
		01000	6.25
		01001	8
		01010	10
		01011	12.5
		01100	16
		01101	20
		01110	25
		01111	32
		10000	40
		10001	50
		10010	64
		10011	80
		10100	100
		10101	125
		10110	160
		10111	200
		11000	250
		11001	320
		11010	400
		11011	500
		11100	640
		11101	800
		11110	1000
		11111	1250

Table 73. DAC_ALC_7 (0xA6h)

Bits	Field	Description
5:0	MAX_LEVEL	This sets the maximum allowed gain to the digital level control when the ALC is used.

Table 74. DAC_ALC_8 (0xA7h)

Bits	Field	Description
5:0	MIN_LEVEL	This sets the minimum allowed gain to the digital level control when the ALC is used.

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Table 75. DAC_L_LEVEL (0xA8h) (Default data value is 0x33h)

Bits	Field	Description			
5:0	DAC_L_LEVEL	This sets the pre DAC digital gain.			
		DAC_L_LEVEL	Level	DAC_L_LEVEL	Level
		000000	-76.5dB	100000	-28.5dB
		000001	-75dB	100001	-27dB
		000010	-73.5dB	100010	-25.5dB
		000011	-72dB	100011	-24dB
		000100	-70.5dB	100100	-22.5dB
		000101	-69dB	100101	-21dB
		000110	-67.5dB	100110	-20.5dB
		000111	-66dB	100111	-18dB
		001000	-64.5dB	101000	-16.5dB
		001001	-63dB	101001	-15dB
		001010	-61.5dB	101010	-13.5dB
		001011	-60dB	101011	-12dB
		001100	-58.5dB	101100	-10.5dB
		001101	-57dB	101101	-9dB
		001110	-55.5dB	101110	-7.5dB
		001111	-54dB	101111	-6dB
		010000	-52.5dB	110000	-4.5dB
		010001	-51dB	110001	-3dB
		010010	-49.5dB	110010	-1.5dB
		010011	-48dB	110011	0dB
		010100	-46.5dB	110100	1.5dB
		010101	-45dB	110101	3dB
		010110	-43.5dB	110110	4.5dB
		010111	-42dB	110111	6dB
		011000	-40.5dB	111000	7.5dB
		011001	-39dB	111001	9dB
		011010	-37.5dB	111010	10.5dB
		011011	-36dB	111011	12dB
		011100	-34.5dB	111100	13.5dB
		011101	-33dB	111101	15dB
		011110	-31.5dB	111110	16.5dB
		011111	-30dB	111111	18dB

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Table 76. DAC_R_LEVEL (0xA9h) (Default data value is 0x33h)

Bits	Field	Description			
5:0	DAC_R_LEVEL	This sets the pre DAC digital gain.			
		DAC_R_LEVEL	Level	DAC_R_LEVEL	Level
		000000	-76.5dB	100000	-28.5dB
		000001	-75dB	100001	-27dB
		000010	-73.5dB	100010	-25.5dB
		000011	-72dB	100011	-24dB
		000100	-70.5dB	100100	-22.5dB
		000101	-69dB	100101	-21dB
		000110	-67.5dB	100110	-20.5dB
		000111	-66dB	100111	-18dB
		001000	-64.5dB	101000	-16.5dB
		001001	-63dB	101001	-15dB
		001010	-61.5dB	101010	-13.5dB
		001011	-60dB	101011	-12dB
		001100	-58.5dB	101100	-10.5dB
		001101	-57dB	101101	-9dB
		001110	-55.5dB	101110	-7.5dB
		001111	-54dB	101111	-6dB
		010000	-52.5dB	110000	-4.5dB
		010001	-51dB	110001	-3dB
		010010	-49.5dB	110010	-1.5dB
		010011	-48dB	110011	0dB
		010100	-46.5dB	110100	1.5dB
		010101	-45dB	110101	3dB
		010110	-43.5dB	110110	4.5dB
		010111	-42dB	110111	6dB
		011000	-40.5dB	111000	7.5dB
		011001	-39dB	111001	9dB
		011010	-37.5dB	111010	10.5dB
		011011	-36dB	111011	12dB
		011100	-34.5dB	111100	13.5dB
		011101	-33dB	111101	15dB
		011110	-31.5dB	111110	16.5dB
		011111	-30dB	111111	18dB

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Table 77. DAC_3D (0xAAh)

Bits	Field	Description	
0	EFFECT_MODE	This sets the digital 3D stereo enhancement mode.	
		EFFECT_MODE	Type
		0	Loudspeaker
		1	Headphone
2:1	EFFECT_LEVEL	This sets the applied level of 3D effect.	
		EFFECT_LEVEL	Level
		00	25%
		01	37.50%
		10	50%
		11	75%
6:3	FILTER_TYPE	This sets the 3D effect filter response.	
		FILTER_TYPE	Response
		0000	200Hz HPF
		0001	300Hz HPF
		0010	600Hz HPF
		0011	900Hz HPF
		0100	200Hz-500Hz BPF
		0101	200Hz-1kHz BPF
		0110	200Hz-1.6kHz BPF
		0111	200Hz-2.5kHz BPF
		1000	300Hz-1kHz BPF
		1001	300Hz-1.6kHz BPF
		1010	300Hz-2.5kHz BPF
		1011	600Hz-1kHz BPF
		1100	600Hz-1.6kHz BPF
		1101	600Hz-2.5kHz BPF
		1110	900Hz-1.6kHz BPF
		1111	900Hz-2.5kHz BPF
7	ATTENUATE	If set, the inputs are reduced by 6dB before 3D effects are applied in order to avoid clipping.	

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Table 78. EQ_BAND_1 (0xABh)

Bits	Field	Description	
1:0	FREQ	This sets the Sub-bass shelving filter's cut-off frequency. The cut-off frequencies shown are based on a 48kHz sample rate. Using lower sample rates will scale down the cut-off frequencies proportionately.	
		FREQ	Frequency (Hz)
		00	60
		01	80
		10	100
		11	120
6:2	LEVEL	This sets the gain at f_C.	
		LEVEL	Effect
		00000	Off (0dB)
		00001	-15dB
		00010	-14dB
		00011	-13dB
		00100	-12dB
		00101	-11dB
		00110	-10dB
		00111	-9dB
		01000	-8dB
		01001	-7dB
		01010	-6dB
		01011	-5dB
		01100	-4dB
		01101	-3dB
		01110	-2dB
		01111	-1dB
		10000	0dB
		10001	1dB
		10010	2dB
		10011	3dB
		10100	4dB
		10101	5dB
		10110	6dB
		10111	7dB
		11000	8dB
		11001	9dB
		11010	10dB
		11011	11dB
		11100	12dB
		11101	13dB
		11110	14dB
		11111	15dB

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Table 79. EQ_BAND_2 (0xACh)

Bits	Field	Description	
1:0	FREQ	This sets the Bass peak filter's center frequency. The cut-off frequencies shown are based on a 48kHz sample rate. Using lower sample rates will scale down the cut-off frequencies proportionately.	
		FREQ	Frequency (Hz)
		00	150
		01	200
		10	250
		11	300
6:2	LEVEL	This sets the gain at f_C.	
		LEVEL	Effect
		00000	Off (0dB)
		00001	-15dB
		00010	-14dB
		00011	-13dB
		00100	-12dB
		00101	-11dB
		00110	-10dB
		00111	-9dB
		01000	-8dB
		01001	-7dB
		01010	-6dB
		01011	-5dB
		01100	-4dB
		01101	-3dB
		01110	-2dB
		01111	-1dB
		10000	0dB
		10001	1dB
		10010	2dB
		10011	3dB
		10100	4dB
		10101	5dB
		10110	6dB
		10111	7dB
		11000	8dB
		11001	9dB
		11010	10dB
		11011	11dB
		11100	12dB
		11101	13dB
		11110	14dB
		11111	15dB
7	Q	This programs the width of the peak filter.	
		Q	Bandwidth
		0	2/3 Octave
		1	4/3 Octave

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Table 80. EQ_BAND_3 (0xADh)

Bits	Field	Description	
1:0	FREQ	This sets the Mid peak filter's center frequency. The cut-off frequencies shown are based on a 48kHz sample rate. Using lower sample rates will scale down the cut-off frequencies proportionately.	
		FREQ	Frequency (Hz)
		00	600
		01	800
		10	1k
		11	1.2k
6:2	LEVEL	This sets the gain at f_C.	
		LEVEL	Effect
		00000	Off (0dB)
		00001	-15dB
		00010	-14dB
		00011	-13dB
		00100	-12dB
		00101	-11dB
		00110	-10dB
		00111	-9dB
		01000	-8dB
		01001	-7dB
		01010	-6dB
		01011	-5dB
		01100	-4dB
		01101	-3dB
		01110	-2dB
		01111	-1dB
		10000	0dB
		10001	1dB
		10010	2dB
		10011	3dB
		10100	4dB
		10101	5dB
		10110	6dB
		10111	7dB
		11000	8dB
		11001	9dB
		11010	10dB
		11011	11dB
		11100	12dB
		11101	13dB
		11110	14dB
		11111	15dB
7	Q	This programs the width of the peak filter.	
		Q	Bandwidth
		0	2/3 Octave
		1	4/3 Octave

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Table 81. EQ_BAND_4 (0xAEh)

Bits	Field	Description	
1:0	FREQ	This sets the Treble peak filter's center frequency. The cut-off frequencies shown are based on a 48kHz sample rate. Using lower sample rates will scale down the cut-off frequencies proportionately.	
		FREQ	Frequency (Hz)
		00	2k
		01	2.7k
		10	3.4k
		11	4.1k
6:2	LEVEL	This sets the gain at f_C.	
		LEVEL	Effect
		00000	Off (0dB)
		00001	-15dB
		00010	-14dB
		00011	-13dB
		00100	-12dB
		00101	-11dB
		00110	-10dB
		00111	-9dB
		01000	-8dB
		01001	-7dB
		01010	-6dB
		01011	-5dB
		01100	-4dB
		01101	-3dB
		01110	-2dB
		01111	-1dB
		10000	0dB
		10001	1dB
		10010	2dB
		10011	3dB
		10100	4dB
		10101	5dB
		10110	6dB
		10111	7dB
		11000	8dB
		11001	9dB
		11010	10dB
		11011	11dB
		11100	12dB
		11101	13dB
		11110	14dB
		11111	15dB
7	Q	This programs the width of the peak filter.	
		Q	Bandwidth
		0	2/3 Octave
		1	4/3 Octave

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Table 82. EQ_BAND_5 (0xAFh)

Bits	Field	Description	
1:0	FREQ	This sets the presence shelving filter's cut-off frequency. The cut-off frequencies shown are based on a 48kHz sample rate. Using lower sample rates will scale down the cut-off frequencies proportionately.	
		FREQ	Frequency (Hz)
		00	7k
		01	9k
		10	11k
		11	20k
6:2	LEVEL	This sets the gain at f_C.	
		LEVEL	Effect
		00000	Off (0dB)
		00001	-15dB
		00010	-14dB
		00011	-13dB
		00100	-12dB
		00101	-11dB
		00110	-10dB
		00111	-9dB
		01000	-8dB
		01001	-7dB
		01010	-6dB
		01011	-5dB
		01100	-4dB
		01101	-3dB
		01110	-2dB
		01111	-1dB
		10000	0dB
		10001	1dB
		10010	2dB
		10011	3dB
		10100	4dB
		10101	5dB
		10110	6dB
		10111	7dB
		11000	8dB
		11001	9dB
		11010	10dB
		11011	11dB
		11100	12dB
		11101	13dB
		11110	14dB
		11111	15dB

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Table 83. SOFTCLIP1 (0xB0h)

Bits	Field	Description	
3:0	TRESHOLD	This sets the threshold level of the audio compressor. Audio signals above the threshold will be compressed.	
		THRESHOLD	Threshold Level (dB)
		0000	-36dB
		0001	-30dB
		0010	-24dB
		0011	-20dB
		0100	-18dB
		0101	-17dB
		0110	-16dB
		0111	-15dB
		1000	-14dB
		1001	-12dB
		1010	-10dB
		1011	-8dB
		1100	-6dB
		1101	-4dB
		1110	-2.5dB
		1111	-1dB
4	SOFT_KNEE	If set, the audio compressor will automatically apply higher compression ratios to audio signals higher than the threshold level. As the audio signal approaches levels higher than the threshold, SOFT_KNEE will increase the compression RATIO. The highest compression that the SOFT_KNEE algorithm will apply is the compression that is set by RATIO.	

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Table 84. SOFTCLIP2 (0xB1h)

Bits	Field	Description	
4:0	RATIO	This sets the ratio at which the audio is compressed to when it passes beyond the threshold. In soft clip mode this is the final level of compression.	
		RATIO	Ratio
		00000	1:1 (Bypass)
		00001	1:1.2
		00010	1:1.4
		00011	1:1.7
		00100	1:2.0
		00101	1:2.4
		00110	1:2.8
		00111	1:3.4
		01000	1:4.0
		01001	1:4.7
		01010	1:5.7
		01011	1:6.7
		01100	1:8.0
		01101	1:9.5
		01110	1:11.3
		01111	1:13.5
		10000	1:16.0
		10001	1:19.0
		10010	1:22.8
		10011	1:27.0
		10100	1:32.0
		10101	1:37.9
		10110	1:45.5
		10111	1:53.9
		11000	1:64
		11001	1:75.9
		11010	1:91.0
		11011	1:108
		11100	1:128
		11101	1:152
		11110	1:182
		11111	1:215

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Table 85. SOFTCLIP3 (0xB2h)

Table 40:			
Bits	Field	Description	
4:0	LEVEL	This sets the post compressor gain level.	
		LEVEL	Level (dB)
		00000	-22.5dB
		00001	-21dB
		00010	-19.5dB
		00011	-18dB
		00100	-16.5dB
		00101	-15dB
		00110	-13.5dB
		00111	-12dB
		01000	-10.5dB
		01001	-9dB
		01010	-7.5dB
		01011	-6dB
		01100	-4.5dB
		01101	-3dB
		01110	-1.5dB
		01111	0dB
		10000	1.5dB
		10001	3dB
		10010	4.5dB
		10011	6dB
		10100	7.5dB
		10101	9dB
		10110	10.5dB
		10111	12dB
		11000	13.5dB
		11001	15dB
		11010	16.5dB
		11011	18dB
		11100	19.5dB
		11101	21dB
		11110	22.5dB
		11111	24dB

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GPIO Registers

Table 86. GPIO (0xE0h)

Bits	Field	Description	
3:0	GPIO_MODE	This sets the mode of the GPIO pin.	
		GPIO_MODE	GPIO Function
		0000	OFF (input disabled)
		0001	GPIO_RX
		0010	GPIO_TX
		0011	HP_ENB (out)
		0100	$\overline{\text{HP_ENB}}$ (out)
		0101	LS_ENB (out)
		0110	$\overline{\text{LS_ENB}}$ (out)
		0111	SHORT_CCT or THERMAL (out)
		1000	SHORT_CCT or THERMAL or CLIP (out)
		1001	CLIP (out)
		1010	ADC_NG_ACTIVE (out)
		1011	$\overline{\text{ADC_NG_ACTIVE}}$ (out)
		1100	MIC_MUTE (in)
		1101	$\overline{\text{MIC_MUTE}}$ (in)
		1110	CHIP_ENB (in)
		1111	$\overline{\text{CHIP_ENB}}$ (in)
4	GPIO_TX	If set, the GPIO pin will transmit a logic high whenever GPIO_MODE is set to '0010'.	
5	GPIO_RX	This bit reports what logic level is present on the GPIO pin.	
6	SHORT_CCT	If set, the GPIO records that a short circuit event has occurred on the class D outputs.	
7	THERMAL_EVENT	If set records that a temperature event has occurred on the die. Clear on Write (1).	

Table 87. DEBUG1 (0xF0h)

Bits	Field	Description	
1:0	DAC_DITHER _LVL	This sets the amount of DAC dither. Lower levels of the dither may improve the noise floor of the DAC.	
		DAC_DITHER _LVL	Level
		00	Very Small
		01	Small
		10	Medium (Default)
		11	Large
3:2	DAC_DITHER _MODE	This sets the DAC dither mode.	
		DAC_DITHER _MODE	Mode
		00	AUTOMATIC
		01	ON
		10	OFF
4	Not Used		
5	SOFT_RESET	If set, the LM49350 enters RESET mode. To bring the LM49350 back out of RESET mode, then set this bit back to zero.	
7:6	RSVD	Reserved	

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Table 88. Spread Spectrum (0xF1h)

Bits	Field	Description
1:0	RSVD	Reserved
2	SS_DISABLE	If this bit is set, Spread Spectrum mode will be disabled from the Class D amplifier.

Table 89. ADC Compensation Filter C0 LSBs (0xF8h)

Bits	Field	Description
7:0	ADC_CO_LSB	Bits 7:0 of C0[15:0]

Table 90. ADC Compensation Filter C0 MSBs (0xF9h)

Bits	Field	Description
7:0	ADC_CO_MSB	Bits 15:0 of C0[15:0]

Table 91. ADC Compensation Filter C1 LSBs (0xFAh)

Bits	Field	Description
7:0	ADC_C1_LSB	Bits 7:0 of C1[15:0]

Table 92. ADC Compensation Filter C1 MSBs (0xFBh)

Bits	Field	Description
7:0	ADC_C1_MSB	Bits 15:0 of C1[15:0]

Table 93. ADC Compensation Filter C2 LSBs (0xFCh)

Bits	Field	Description
7:0	ADC_C2_LSB	Bits 7:0 of C2[15:0]

Table 94. ADC Compensation Filter C2 MSBs (0xFDh)

Bits	Field	Description
7:0	ADC_C2_MSB	Bits 15:0 of C2[15:0]

Table 95. AUX_LINEOUT (0xFE)

Bits	Field	Description
4:0	RSVD	Reserved
5	AUX_LINE_OUT	If set, the earpiece amplifier operates in a low current drive mode for line out applications in order to reduce power consumption.

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Schematic Diagram

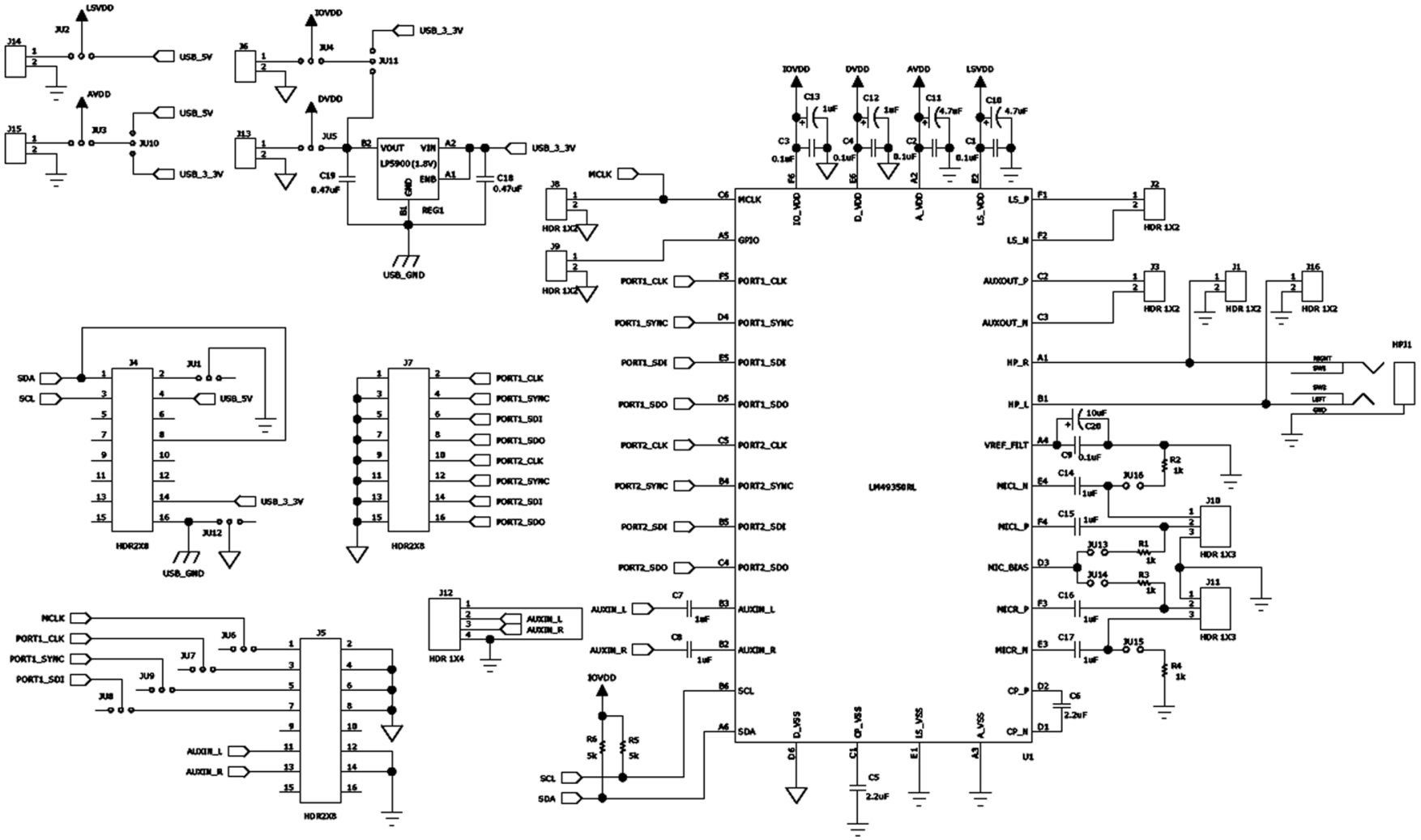


Figure 66. Demo Board Schematic

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Demonstration Board Layout

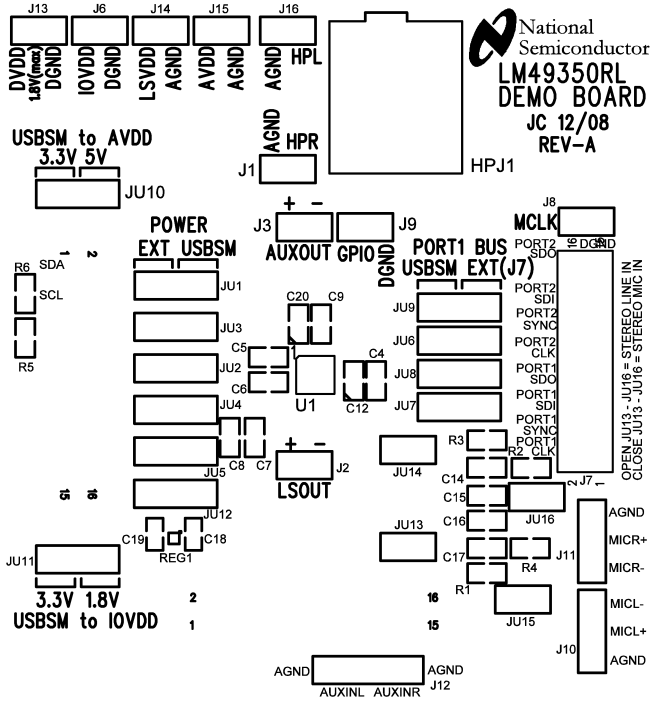


Figure 67. Top Silkscreen Layer

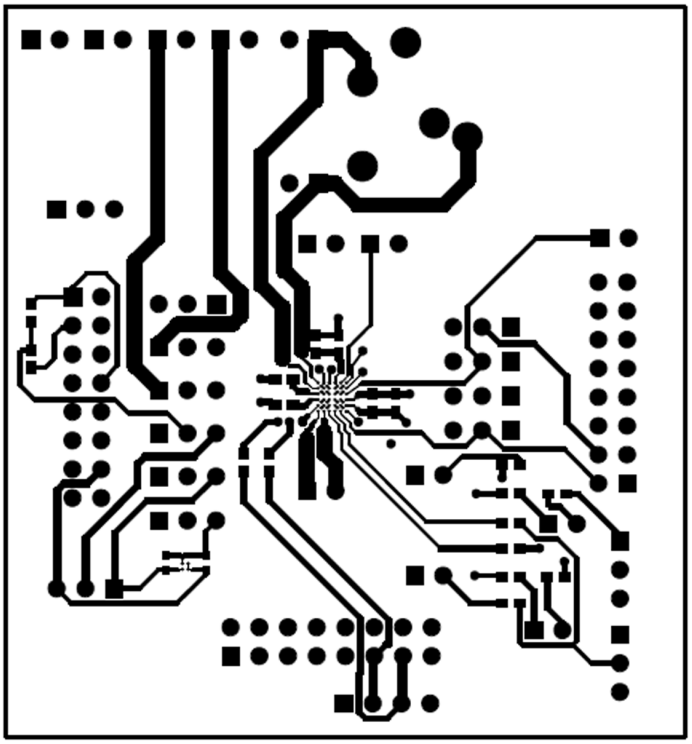


Figure 68. Top Layer

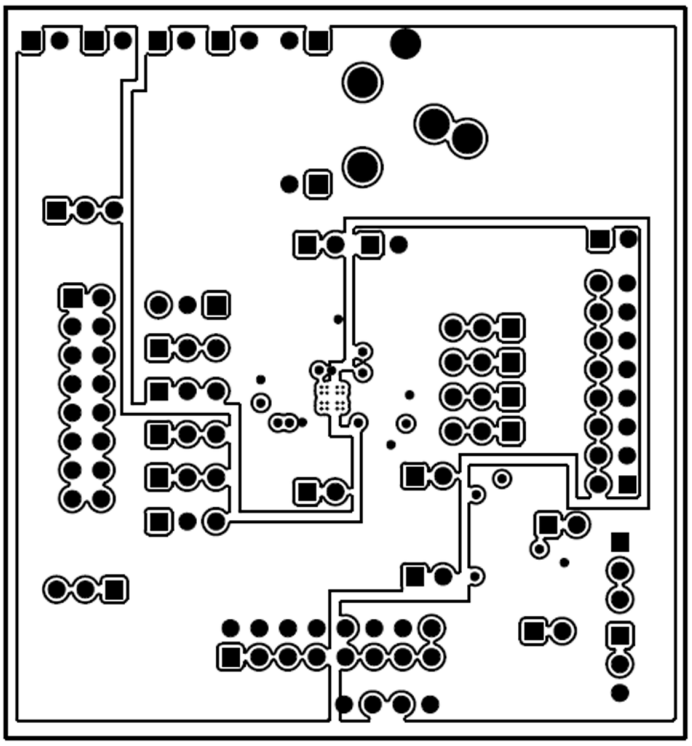


Figure 69. Inner Layer 1

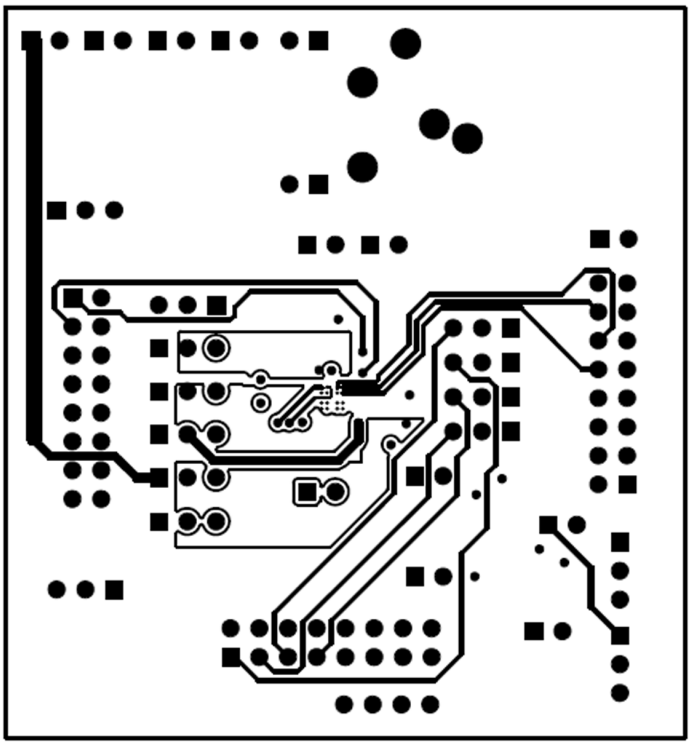


Figure 70. Inner Layer 2

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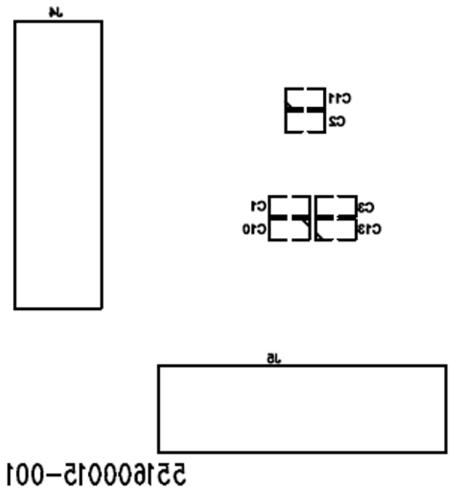


Figure 71. Bottom Silkscreen Layer

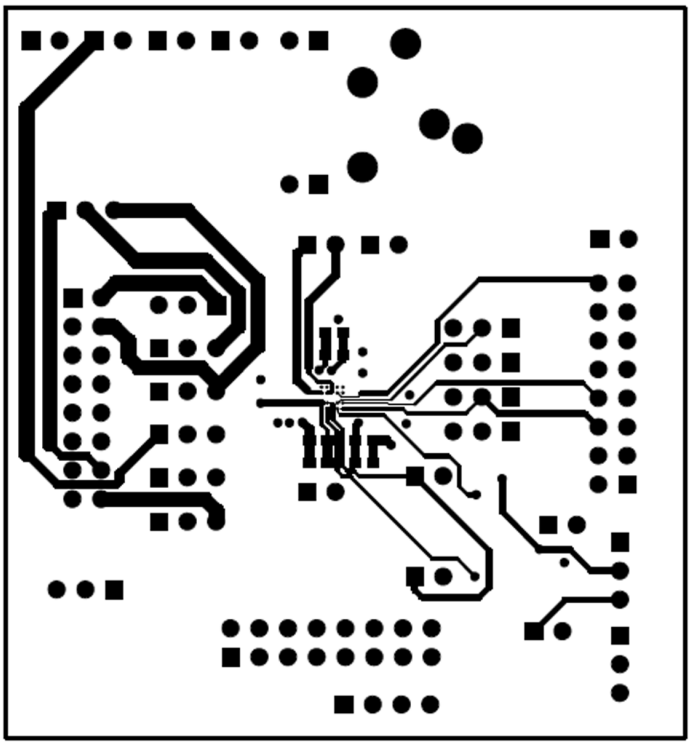


Figure 72. Bottom Layer

APPLICATION NOTE FOR LM49350

POWER CONNECTIONS

Recommended target application circuit must provide same voltage level for A_V_{DD} and LSV_{DD} to get performance on Electrical Specifications on LM49350 datasheet.

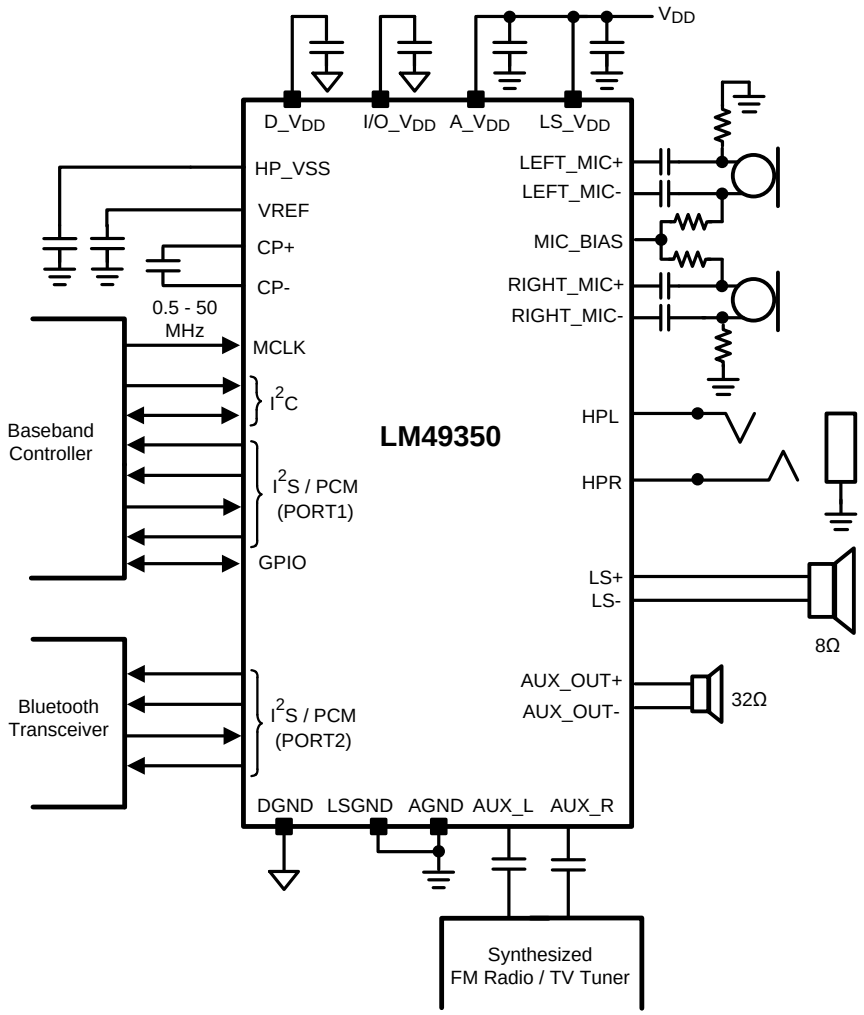


Figure 73. Recommended Power Connection

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MICROPHONE BIAS CONFIGURATIONS

Schematic Considerations for MEMs Microphones

The internal microphone bias of the LM49350 is provided through a two stage amplifier. Adding a capacitor larger than 100pF directly to this pin can cause instability. In many cases, when using MEMs microphones, a larger bypass capacitor is required on the MIC_BIAS pin. To avoid oscillations and to keep the device stable, it is recommended to add a resistor (R_B) greater than 10Ω in series with the capacitor (C_B). Another option is to bias the MEMs microphone from the 1.8V supply used for D_V_{DD}/IO_V_{DD}.

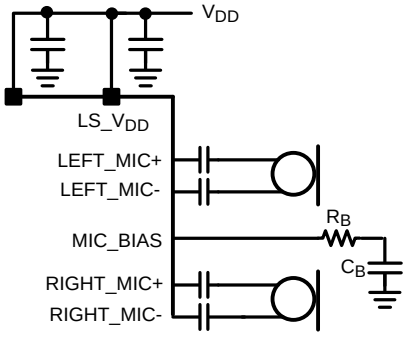


Figure 74. Schematic for MEMs Microphones

Schematic Considerations for ECM Microphones

When using ECM microphones, refer to the configurations shown in Figure 73 or Figure 74 to bias the microphones. In many cases, an RC filter is required to provide a more stable microphone bias (see Figure 74). In this case, a 10Ω resistor (R_B) in series with C_B is recommended.

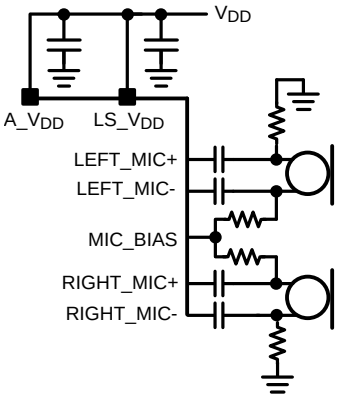


Figure 75. Schematic Option for ECM Microphones

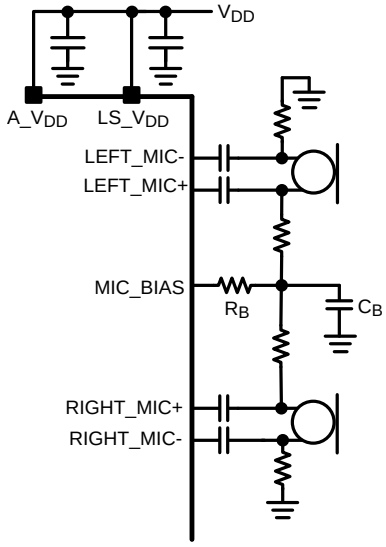


Figure 76. Schematic Option for ECM Microphones

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PCB LAYOUT CONSIDERATIONS

Microphone Inputs

When routing the differential microphone inputs the electrical length of the two traces should be well matched. The differential input pair can be routed in parallel on the same plane or the traces can overlap on two adjacent planes. It is important to surround these traces with a ground plane or trace to isolate the microphone inputs from the noise coupling from the class D amplifier.

Class D Loudspeaker

To minimize trace resistance and therefore maintain the highest possible output power, the power (LS_V_{DD}) and class D output (LS-, LS+) traces should be as wide as possible. It is also essential to keep these same traces as short and well shielded as possible to decrease the amount of EMI radiation.

Capacitors

All supply bypass capacitors (for A_V_{DD}, D_V_{DD}. I/O V_{DD}, and LS_V_{DD}), and charge pump capacitors should be as close to the device as possible. Careful consideration should be taken with the ground connection of the analog supply (A_V_{DD}) bypass cap, for proper performance it should be referenced to a low noise ground plane. The charge pump capacitors and traces connecting the capacitor to the device should be kept away from the input and output traces to avoid noise coupling issues.

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REVISION HISTORY

Rev	Date	Description
1.0	09/03/08	Initial released.
1.01	09/04/08	Text edits.
1.02	09/22/08	Text edits.
1.03	10/24/08	Text edits.
1.04	12/15/08	Text edits and replaced the top silkscreen layer.
1.05	05/27/09	Added the EMI/RFI section and the corresponding graphic.
1.06	05/29/09	Text edits.
1.07	04/09/10	Text edits.
1.08	04/15/10	Text edits.
1.09	09/17/10	Added the Application section required for Leadcore (chipset partner).
1.10	03/23/11	Input minor text edits.
1.11	04/05/11	Added sections 29.2 and 29.3 including their corresponding graphics, then generated a CONFIDENTIAL version for LEADCORE.
1.12	04/12/11	Edited Figure 32 and input text edits.
1.13	04/13/11	Input text edits.
1.14	08/24/11	Added table: RX_MODE (0x55h/65h).
1.15	03/16/12	Added the one more Timing Char table (DV_{DD} = I/OV_{DD} = 1.8V with the 2 diagrams (Timing I^2S Master and Timing for I^2S Slave).
1.16	06/29/12	Edited Figures 2, 3, 4, and 5 (Typical Application circuit diagrams).

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM49350RL/NOPB	LIFEBUY	DSBGA	YPG	36	250	Green (RoHS & no Sb/Br)	SNAG	Level-1-260C-UNLIM	-40 to 85	GJ8	
LM49350RLX/NOPB	LIFEBUY	DSBGA	YPG	36	1000	Green (RoHS & no Sb/Br)	SNAG	Level-1-260C-UNLIM	-40 to 85	GJ8	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

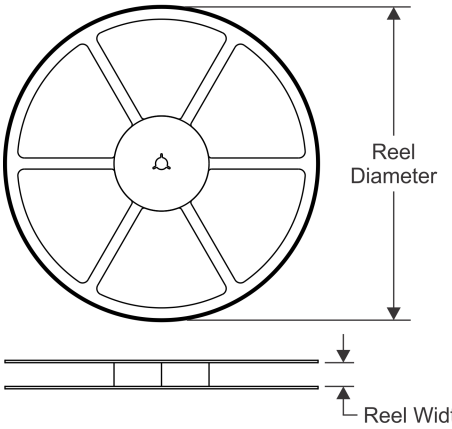
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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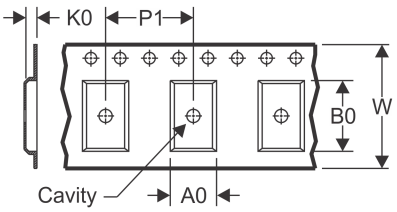
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

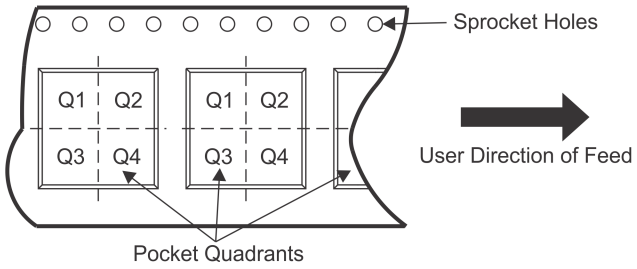


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

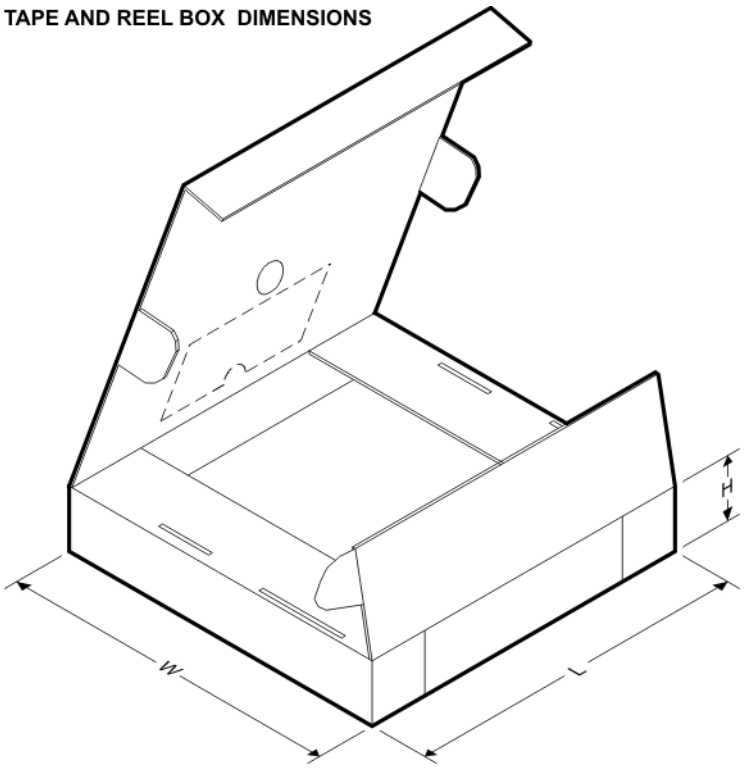
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM49350RL/NOPB	DSBGA	YPG	36	250	178.0	12.4	3.63	3.63	0.76	8.0	12.0	Q1
LM49350RLX/NOPB	DSBGA	YPG	36	1000	178.0	12.4	3.63	3.63	0.76	8.0	12.0	Q1

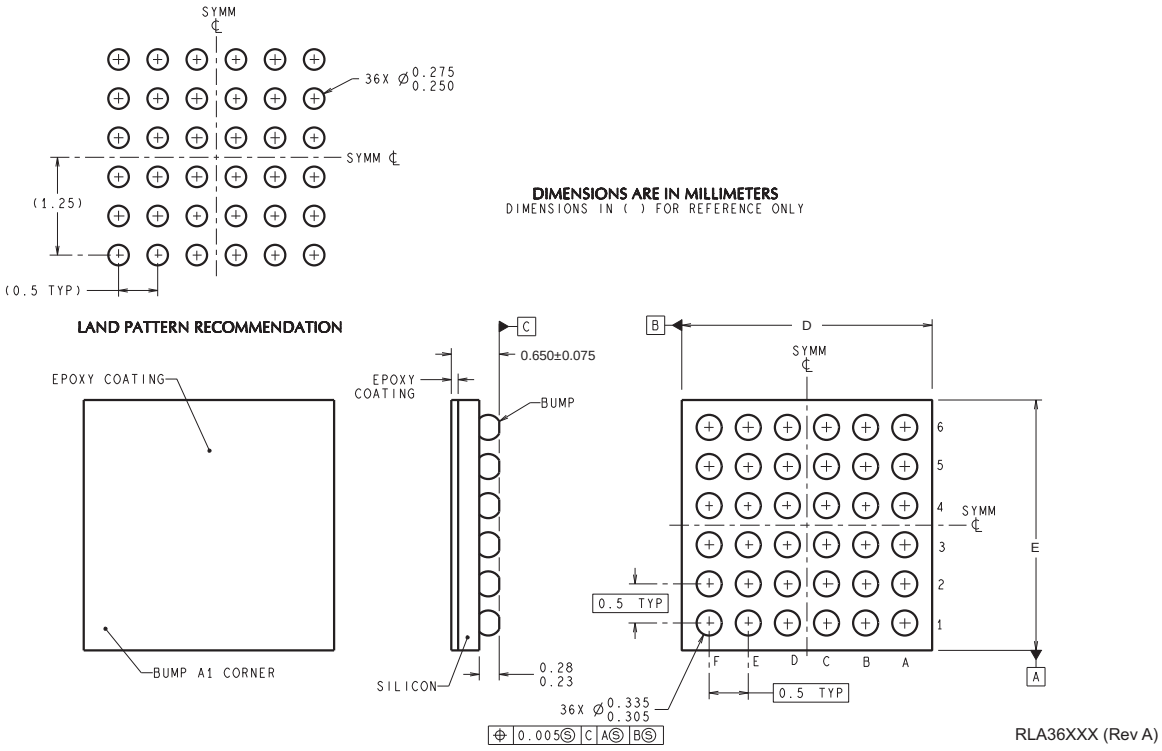
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM49350RL/NOPB	DSBGA	YPG	36	250	210.0	185.0	35.0
LM49350RLX/NOPB	DSBGA	YPG	36	1000	210.0	185.0	35.0

YPG0036



D: Max = 3.49 mm, Min = 3.43 mm

E: Max = 3.49 mm, Min = 3.43 mm

4214895/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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