

# AN-1886 LM3686 Evaluation Board

### 1 Introduction

This evaluation board is designed to enable independent evaluation of the LM3686 electrical performance. Each board is pre-assembled and tested in the factory.

The evaluation kit is available in the following voltages LM3686TL-181228EVB (DCDC = 1.8, LILO = 1.2, LDO = 2.8). This user's guide contains information about the evaluation board. For further information on device electrical characteristics and component selection, please refer to LM3686 Step-Down DC-DC Converter with Integrated Post Linear Regulators System and Low-Noise Linear Regulator (SNVS520).

## 2 General Description

The LM3686 is a step-down DC-DC converter with two integrated low dropout linear regulators optimized for powering ultra-low voltage circuits from a single Li-Ion cell or 3 cell NiMH/NiCd batteries. It provides three outputs with combined load current up to 900 mA over an input voltage range from 2.7V to 5.5V.

The device offers superior features and performance for many applications. Automatic intelligent switching between PWM low-noise and PFM low-current mode offers improved system control. During full-power operation, a fixed-frequency 3 MHz (typ.), PWM mode drives loads from  $\sim$ 70 mA to 600 mA max. Hysteretic PFM mode extends the battery life through reduction of the quiescent current to 28  $\mu$ A (typ.) at light load and system standby. Internal synchronous rectification provides high efficiency.

It also features internal protection against short-circuit and over-temperature conditions.

For the Evaluation Board, the typical post regulation application is realized: the output voltage of the DC-DC converter is used as supply for the linear regulator ( $V_{OUT\_DCDC} = V_{IN\_LILO}$ ). Thereby, a higher efficiency and lower power dissipation of the system can be achieved compared to using the battery voltage  $V_{BATT}$  as supply for the linear regulator ( $V_{IN\_LILO}$ ).

### **3 General Operation Recommendations**

Three enable pins allow the separate operation of either the DC-DC, post-regulation linear regulator or the linear regulator alone. If the DC-DC is not enabled during startup of the post-regulation linear regulator, a parallel small-pass transistor supplies the linear regulator from  $V_{BATT}$  with maximal 50 mA. In the combined operation where both Enables are raised or lowered together, the small pass transistor is deactivated, and the big-pass transistor provides 350 mA output current. In shutdown mode (Enable pins pulled low), the device turns off and reduces battery consumption to 2.5  $\mu$ A (typ.).

A load of up to 600 mA maximum may be connected from the  $V_{OUT\_DCDC}$  pin to GND if no additional load is applied at the output of the linear regulator. For  $V_{OUT\_LILO}$ , the maximum load is 350 mA, while the LDO supplies a maximum of 300 mA. As in the typical post regulation application the load of the linear regulator is supplied by the DC-DC converter, the combined maximum load conditions are:

300 mA at  $V_{\text{OUT LILO}}$  plus 300 mA at  $V_{\text{OUT DCDC}}$ .

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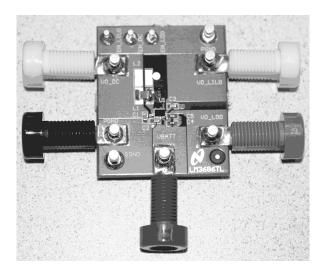


Figure 1. LM3686 Board Layout

# 4 Typical Application Circuit

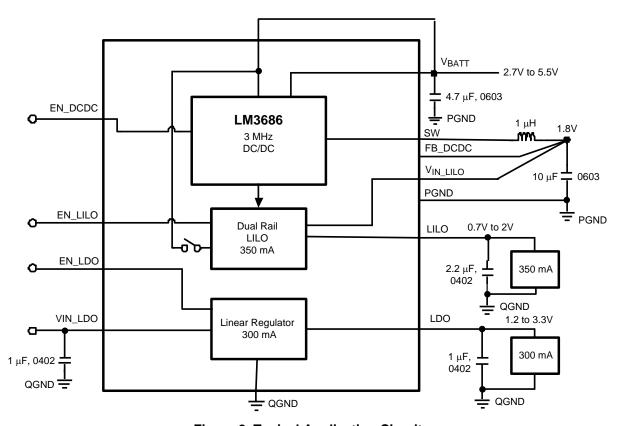
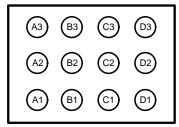


Figure 2. Typical Application Circuit



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# 5 Connection Diagram



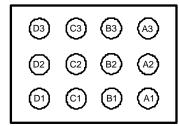


Figure 3. Connection Diagram 12-Bump Thin DSBGA Package, Large Bump, 0.5 mm Pitch Left: Top View, Right: Bottom View

# 6 Pin Descriptions

**Table 1. Pin Descriptions** 

| Pin Number | Symbol                | Name and Function   |  |  |
|------------|-----------------------|---|--|--|
| A1         | PGND                  | Power Ground pin  |  |  |
| A2         | SW                    | Switching node connection to the internal PFET switch and NFET synchronous rectifier.   |  |  |
| A3         | FB_DCDC               | Feedback analog input for the DC-DC converter. Connect to the output filter capacitor.  |  |  |
| B1         | V <sub>BATT</sub>     | Power supply input for switcher. Connect to the input filter capacitor.   |  |  |
| B2         | EN_LILO               | Enable input for the linear regulator. The linear regulator is in shutdown mode if voltage at t pin is < 0.4V and is enabled if > 1.0V. Do not leave this pin floating. |  |  |
| B3         | EN_DCDC               | Enable input for the DC-DC converter. The DC-DC converter is in shutdown mode if voltage this pin is < 0.4V and is enabled if > 1.1V. Do not leave this pin floating.   |  |  |
| C1         | $V_{IN\_LDO}$         | Input power to LDO. ( Must tie to V <sub>BATT</sub> at all times )  |  |  |
| C2         | EN_LDO                | Enable input for the linear regulator. The linear regulator is in shutdown mode if voltage at t pin is < 0.4V and is enabled if > 1.1V. Do not leave this pin floating. |  |  |
| C3         | QGND                  | Quiet GND pin for LDO and reference circuit.  |  |  |
| D1         | $V_{OUT\_LDO}$        | Voltage output of the linear regulator.   |  |  |
| D2         | V <sub>OUT_LILO</sub> | Voltage output of the low input linear regulator  |  |  |
| D3         | V <sub>IN_LILO</sub>  | Input power to LILO (V <sub>IN_LILO</sub> connects to output of DCDC or standalone).  |  |  |

**Table 2. Enable Combinations** 

| EN_DCDC | EN_LILO | EN_LDO | Function  |  |
|---------|---------|--------|---|--|
| 0       | 0       | 0      | No Outputs  |  |
| 0       | 0       | 1      | Linear Regulator enabled only (EN_LDO), supply from $V_{IN\_LDO}$ , $I_{OUT\_MAX} = 300$ mA   |  |
| 0       | 1       | 0      | Linear Regulator enabled only LILO supplies from $V_{IN\_LDO}$ , $I_{OUT\_MAX} = 50$ mA, $V_{IN\_LDO} > = V_{OUT\_LILO}$  |  |
| 1       | 0       | 0      | DC-DC converter enabled only  |  |
| 1       | 1       | 0      | Linear Regulator and DCDC enabled 1) $V_{\text{IN\_LILO}} < V_{\text{OUT\_LILO}} + 150 \text{ mV (typ.)}$ , the small NMOS device is active ( $I_{\text{MAX}} = 50 \text{ mA}$ ) and supplied by $V_{\text{IN\_LILO}}$ . 2) If $V_{\text{IN\_LILO}} > V_{\text{OUT\_LILO}} + 250 \text{ mV (typ.)}$ , the large NMOS device is active ( $I_{\text{MAX}} = 350 \text{ mA}$ ) and supplied by $V_{\text{IN\_LILO}}$ . Maxium current of DC-DC when EN_LILO = High is 250 mA <sup>(1)(2)</sup> |  |
| 1       | 1       | 1      | DC-DC converter and linear regulator active. Linear regulator starts after DC-DC converter.   |  |

The LILO is turned on via a small NMOS device supplied by V<sub>IN\_LDO</sub>. The maximum current is 50 mA when this small NMOS is ON. If higher current > 50 mA is desired the following condition must be done: EN\_DC = HIGH.

When the switcher is enabled, a transition occurs from the small NMOS to a larger NMOS. The transition occurs when V<sub>IN\_LILO</sub> > V<sub>OUT\_LILO</sub> + 250 mV. If V<sub>IN\_LILO</sub> < V<sub>OUT\_LILO</sub> + 150 mV, the LILO switches back to small NMOS (Switcher EN = low).



# 7 Evaluation Board Layout

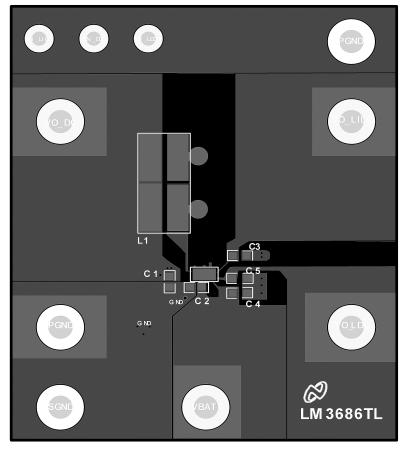


Figure 4. Top Silk Screen



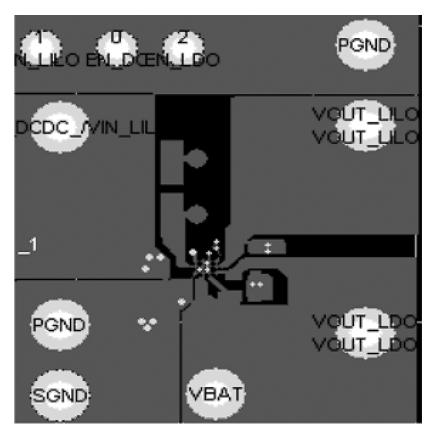


Figure 5. Top Layer

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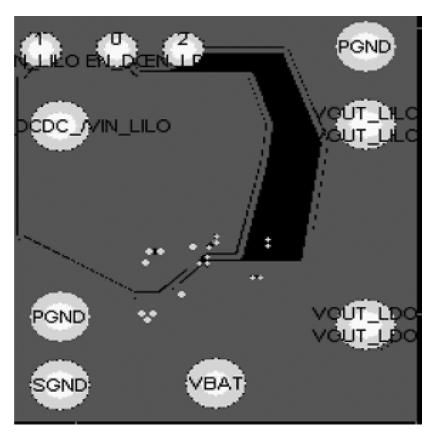


Figure 6. Mid Layer 1

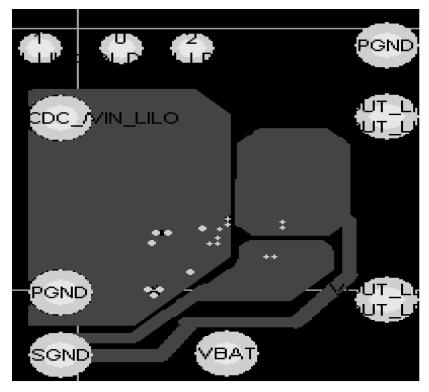


Figure 7. Mid Layer 2



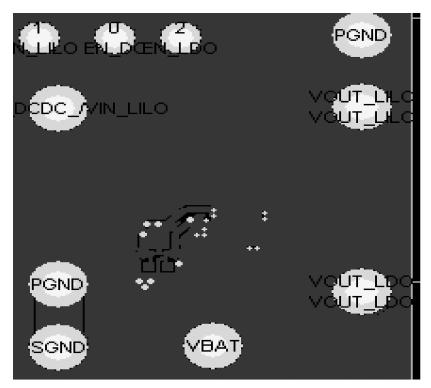


Figure 8. Bottom Layer

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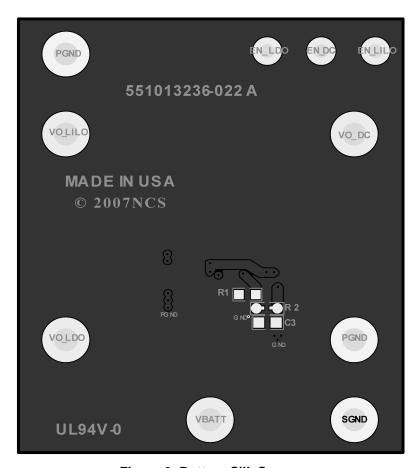


Figure 9. Bottom Silk Screen



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# 8 Bill of Materials

# Table 3. Bill of Materials for LM3686TL

| LM3686  | Manufacturer | Manufacturer No. | Description             |  |
|---|--------------|------------------|-------------------------|--|
| C <sub>IN_ BATT</sub> (C2)<br>(input capacitor)       | TDK          | C1608X5R0J475    | 4.7 μF 6.3V, 0603, 10%  |  |
| C <sub>IN_LDO</sub> (C4)<br>(LDO input capacitor)     | TDK          | C1005JB0J105KT   | 1 µF 6.3V, 0402, 10%    |  |
| C <sub>OUT_DCDC</sub> (C4)<br>(DC output capacitor)   | TDK          | C1608X5R0J106K   | 10 μF 6.3V, 0603, 10%   |  |
| C <sub>OUT_LDO</sub> (C5)<br>(LDO output capacitor)   | TDK          | C1005J105KT      | 1 µF 6.3V, 0402, 10%    |  |
| C <sub>OUT_LILO</sub> (C3)<br>(LILO output capacitor) | TDK          | C1608X5R0J225    | 2.2 μF 6.3V, 0402, 10%  |  |
| L1 (inductor)   | Taiyo Yuden  | BRL2518T1R0M     | 1 μH inductor, 1.6A sat |  |

| Common to All  | Manufacturer       | Manufacturer No. | Description                               |
|--|--------------------|------------------|---|
| V <sub>IN</sub><br>banana jack - red                                 |                    | 108-0902-001     | connector, insulated banana jack (red)    |
| V <sub>OUT_DCDC</sub> and V <sub>OUT_LILO</sub> banana jack - yellow | Johnson Components | 108-0907-001     | connector, insulated banana jack (yellow) |
| V <sub>LDO</sub> banana jack - white                                 |                    | 108-0901-001     | connector, insulated banana jack (white)  |
| GND<br>banana jack - yellow  |                    | 108-0903-001     | connector, insulated banana jack (black)  |



Application Hints www.ti.com

## 9 Application Hints

# 9.1 Evaluation Board Connection

- 1. EN\_DC\_DC, EN\_LILO and EN\_LDO can be connected to V<sub>IN</sub> for evaluation purpose.
- 2. Connect all return Ground from meters to a single PGND point on the PCB Board.
- 3. Each individual V<sub>OUT</sub> can be monitored through the meter.

## 9.2 Power Dissipation Calculation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air.

The allowable power dissipation for the device in a given package can be calculated using the following equation:

$$P_{D\_SYS} = (T_{J(MAX)} - T_A) / \theta_{JA}$$
 (1)

For the LM3686, there are three different main sources contributing to the systems power dissipation  $(P_{D SYS})$ :

- the DC-DC converter (P<sub>D DCDC</sub>)
- the linear regulator (PD LILO)
- the low noise linear regulator (P<sub>D LDO</sub>)

Neglecting switching losses and quiescent currents these two main contributors can be estimated by the following equations:

$$P_{\text{D LILO}} = (V_{\text{IN LILO}} - V_{\text{OUT LILO}}) \times I_{\text{OUT LILO}}$$
 (2)

$$P_{D\_LDO} = (V_{IN\_LDO} - V_{OUT\_LDO}) \times I_{OUT\_LDO}$$
(3)

$$P_{D DDDC} = I_{OUT DDDC}^{2} \times [(R_{DSON(P)} \times D) + (R_{DSON(N)} \times (1 - D))]$$

$$\tag{4}$$

where: duty cycle D =  $V_{OUT\ DCDC}$  /  $V_{BATT}$ 

As an example, assuming the typical post regulation application, the conversion from  $V_{BATT} = 3.6V$  to  $V_{OUT\_DCDC} = 1.8V$  and further to  $V_{OUT\_LIN} = 1.5V$ , at maximum load currents, results in following power dissipations:

$$P_{D DCDC} = (0.300A)^2 \times (0.35\Omega \times 1.8V / 3.6V + 0.15\Omega \times (1 - 1.8V / 3.6V)) = 15.6 \text{ mW}$$

$$P_{D,LIIO} = (1.8V - 1.2V) \times 0.35A = 210 \text{ mW}$$

$$P_{D_{\perp}LDO} = (3.6V - 2.8V) \times 0.3A = 240 \text{ mW}$$

$$P_{D SYS} = 466 \text{ mW}$$

With a  $\theta_{JA}$  = 120°C/W for the DSBGA 12 package, this  $P_{D\_SYS}$  will cause a rise of the junction temperature  $T_J$  of:

$$\Delta T_J = P_{D\_SYS} \times \theta_{JA} = 56K$$

For the same conditions but the LILO regulator biased from  $V_{BATT}$ , this results in a  $P_{D\_LILO}$  of 840 mW rather than 210 mW. As lower total power dissipation translates to higher efficiency this example highlights the advantage of the post regulation setup.

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