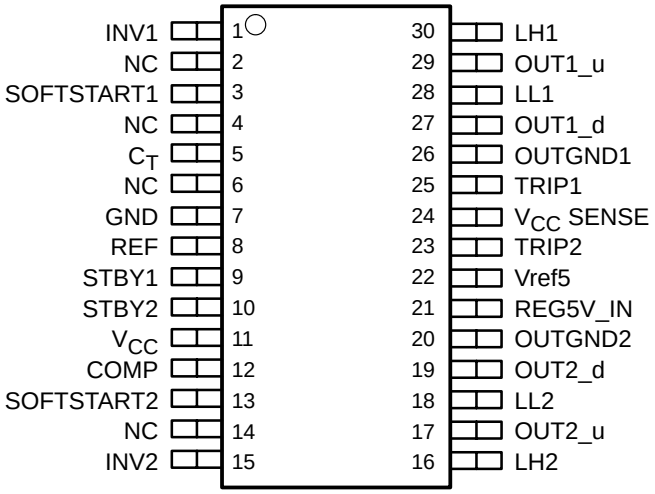
- **Independent Dual Channels**
- **Hysteretic Control for Fast Transient Response**
- **4.5-V to 25-V Input Voltage Range**
- **Adjustable Output Voltage Down to 1.2 V**
- **Synchronous Rectifier Enables Efficiencies of >95%**
- **Minimized External Component Count**
- **Separate Standby Control and Over Current Protection**
- **Low Supply Current . . . 0.8 mA Typ**
- **30-Pin TSSOP**
- **Low Standby Current (1-μA maximum)**
- **EVM Available (TPS5602EVM-121)**

DBT PACKAGE
(TOP VIEW)

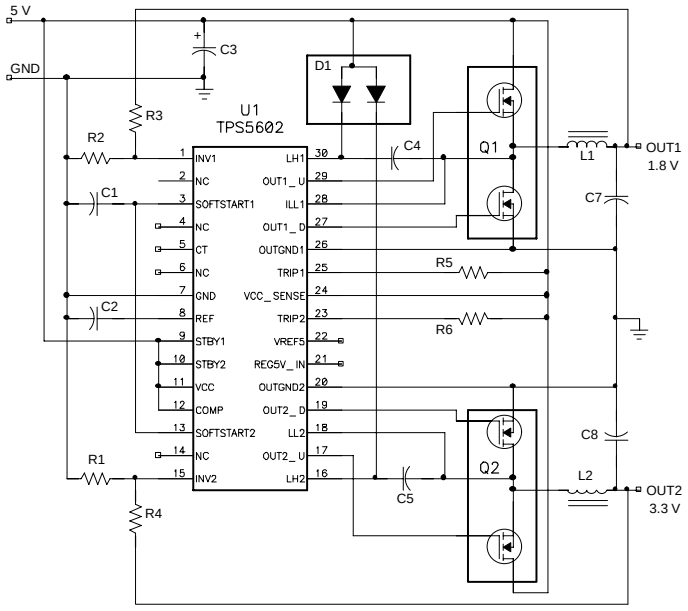


NC – No internal connection

description

The TPS5602 is a dual-channel synchronous buck switch-mode power supply controller featuring very fast feedback control and minimized component count. By using the hysteretic control method, it is ideal for high-transient current applications, such as ’C6000 and multiple ’C54x DSPs. The TPS5602 is designed specifically for DSP applications that require high efficiency. Since both channels are independent, the up and down power sequencing can be easily achieved by properly setting the standby pins. The wide input voltage and adjustable output voltage make the TPS5602 suitable for many applications.

typical design



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

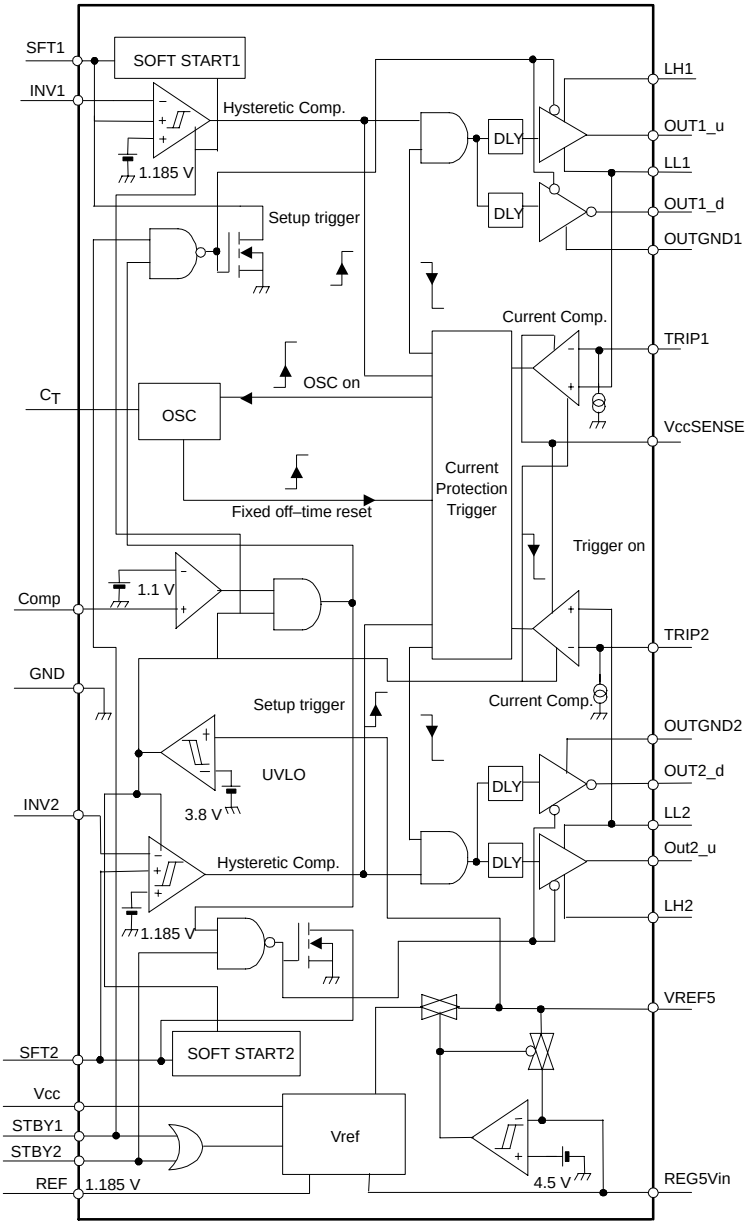
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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AVAILABLE OPTIONS

T_A	PACKAGE	
	TSSOP (DBT)	EVM
–40°C to 85°C	TPS5602IDBT	TPS5602EVM-121
	TPS5602IDBTR	

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
COMP	12	I/O	Voltage monitor comparator input
C_T	5	I/O	The oscillator frequency external capacitor connection
GND	7		Control GND
INV1	1	I	CH1 hysteretic comparator inverting input
INV2	15	I	CH2 hysteretic comparator inverting input
LH1	30	I/O	CH2 high-side gate drive boost capacitor input
LH2	16	I/O	CH1 high-side gate drive boost capacitor input
LL1	28	I/O	CH1 high-side drive and current protection
LL2	18	I/O	CH2 high-side drive and current protection
NC	2, 4, 6, 14		
OUT1_d	27	I/O	CH1 low-side gate drive output
OUT2_d	19	O	CH2 low-side gate drive output
OUT1_u	29	O	CH1 high-side switch output
OUT2_u	17	O	CH2 high-side switch output
OUTGND1	26		Output GND 1
OUTGND2	20		Output GND 2
REF	8	O	1.185-V reference voltage output
REG5V_IN	21	I	External 5-V input
SOFTSTART1	3	I/O	CH1 soft start control external capacitor connection
SOFTSTART2	13	I/O	CH2 soft start control external capacitor connection
STBY1	9	I	CH1 standby control
STBY2	10	I	CH2 standby control
TRIP1	25	I	CH1 output current control input
TRIP2	23	I	CH2 output current control input
V_{CC}	11	I	Supply voltage input
Vref5	22	O	5-V internal regulator output
V_{CC}SENSE	24	I	Supply voltage sense input

detailed description

vref (1.185 V)

The reference voltage is used for the output voltage setting and the voltage protection (COMP).

vref (5 V)

An internal linear voltage regulator offers a fixed 5-V voltage as the bootstrap voltage so that the design for the bootstrap is much easier. The tolerance is 6%. The extra current capability can also be used to power external circuitry.

5-V switch

If the internal 5-V switch senses a 5-V input from REG5V pin, the internal 5-V linear regulator will be disconnected from the MOSFET drivers. The external 5-V will be used for the low-side driver and the high-side bootstrap, thus increasing the efficiency.

detailed description (continued)

hysteretic comparator

Each channel has a hysteretic comparator to regulate the output voltage of the synchronous-buck converter. The hysteresis is set internally and is typically 8.5 mV. The total delay from the comparator input to the driver output is typically 500 ns from low to high and 350 ns from high to low.

low-side driver

The low-side driver is designed to driver low-Rds(on) n-channel MOSFETs. The maximum drive voltage is 5 V from Vref5. The current rating of the driver is typically 1 A, source and sink.

high-side driver

The high side driver is designed to drive low-Rds(on) n-channel MOSFETs. The current rating of the driver is 1 A, source and sink. When configured as a floating driver, the bias voltage to the driver is developed from the Vref5, limiting the maximum drive voltage between OUTxU and LLx to 5 V. The maximum voltage that can be applied between LHx and OUTGNDx is 30 V.

deadtime control

Deadtime control prevents shoot-through current from flowing through the main power FETs during switching transitions by actively controlling the turnon time of the MOSFETs drivers. The typical deadtime from low-side-driver-off to high-side-driver-on is 75 ns and 164 ns from high-side-driver-off to low-side-driver-on.

current protection

The current protection is achieved by sensing the high-side power MOSFET drain-to-source voltage drop during on-time through V_{CC}Sense and LLx pins. An external resistor between Vin and TRIPx pin with the internal current source connected to the current comparator negative input adjusts the current limit. The typical internal current source current is 15 μA. When the voltage on the positive pin is lower than the negative pin, the current comparator turns on the trigger, and then activates the oscillator. This oscillator repeatedly resets the trigger until the overcurrent condition is removed. The equation for the external resistor selection is:

$$Rclmt = \frac{Rds(on) \times (Itrip + Iind(p\text{-}p)/2)}{0.000015}$$

Where Rds(on) is the MOSFET turnon resistance; Itrip is the required trip current; Iind(p-p) is the peak-to-peak inductor ripple current. Itrip must be greater than 0.5×Iind(p-p). The tolerance is ±30%.

COMP

COMP is an internal comparator used for any voltage protection such as the output under-voltage protection for DSP power applications. If the core voltage is lower than the setpoint, the comparator turns off both channels to prevent the DSP from damage.

SOFT1, SOFT2

Separate soft-start terminals make it possible to set the sequencing of each output for any possibility. The capacitor value for a start-up time can be calculated by the following equation:

$$C = 2 \times T \quad (\mu F)$$

Where C is the external capacitor value, T is the required start-up time in (ms).

STBY1, STBY2

Both channels can be switched into standby mode separately by grounding the STBY pin. The standby current is less than 1 μA. The STBY pins can be used for sequencing.

UVLO

When the input voltage rises to about 3.8 V, the IC is turned on, ready to function. When the input voltage falls below the turnon value, the IC is turned off. The typical hysteresis is 149 mV.

absolute maximum ratings over operating free-air temperature (see Note 1) (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . –0.3 V to 27 V
Input voltage, V_I, INV . . . . . –0.3 V to 7 V
Softstart . . . . . –0.3 V to 7 V
COMP . . . . . –0.3 V to 6 V
REG5V_IN . . . . . –0.3 V to 6 V
STBY . . . . . –0.3 V to 15 V
TRIP . . . . . –0.3 V to 15 V
Maximum Driver current . . . . . 3 A
Output voltage, LLx . . . . . –0.3 V to 27 V
Output voltage, OUTx_u . . . . . –0.3 V to 32 V
Output voltage, OUTx_d . . . . . –0.3 V to 7 V
Power dissipation (T_A = 25°C) . . . . . See Dissipation Table
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Operating virtual junction temperature range, T_J . . . . . 125°C
Storage temperature range, T_{stg} . . . . . –55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND terminal.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER DISSIPATION	$T_A \geq$ 25°C DERATING FACTOR	T_A = 85°C POWER DISSIPATION
DBT	874 mW	6.993 mW/°C	454 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5		25	V
Input voltage, V_I	INV1/2			6	V
	COMP			6	
	SOFTSTART1/2			6	
	REG5V_IN			5.5	
	STBY1/STBY2			12	
	TRIP1/2 V_{CC_SENCE}			25	
Operation junction temperature range, T_A		–40		85	°C

electrical characteristics over recommended T_A = –40°C to 85°C temperature range, V_{CC} = 7 V (unless otherwise noted)

reference voltage

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ref}	Reference voltage	T_A = 25°C,	I_{vref} = 50 µA	1.167	1.185	1.203	V
		V_I = 4.5 V to 25 V,	I = 1 µA to 1 mA	1.155		1.215	
$VI_{(Regin)}$	Line regulation	V_{CC} = 5.5 V to 25 V,	I = 50 µA		0.2	12	mV
$VI_{(Regl)}$	Load regulation	I = 1 µA to 1 mA,			0.5	10	mV

quiescent current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Operating current without switching	Both STBY >2.5 V, No switching V_I = 4.5 V to 25 V		0.8	1.5	mA
$I_{(CCS)}$	Stand-by current	Both STBY <0.5 V, V_I = 4.5 V to 25 V		1	1000	nA

hysteretic comparator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{hys}†	Hysteresis window		5.5	8.5	11.5	mV
$V_{H(off)}$	Offset voltage			2		mV
$I_{H(bias)}$	Bias current			10		pA
$t_{(HLT)}$, $t_{(LHT)}$	Propagation delay from INV to OUTxU‡	TTL input signal		230		ns
$t_{(LH)}$		10 mV overdrive on hysteretic band signal		500	650	
$t_{(HI)}$				350	500	

† V_{hys} is assured by design.
‡ The delay time in the table includes the driver.

driver deadtime

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(DRVLH)}$	Low side to high side			90		ns
$t_{(DRVHL)}$	High side to low side			160		

standby

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_H	High-level input voltage	STBY1, STBY2	2.5			V
I_L	Low-level input voltage				0.5	V
Tturn-on	Propagation delay	Staby to driver output		7.2		µs
Tturn-off				4.8		

5 V regulator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	I = 10 mA	4.7		5.3	V
$V_{I(Regin)}$	Load regulation	V_{CC} = 5.5 V to 25 V, I = 10 mA			20	mV
$V_{I(Regl)}$		I = 1 mA to 10 mA, V_{CC} = 5.5 V			40	
I_{OS}	Short-circuit output current	Vref = 0 V		80		mA

electrical characteristics over recommended free-air temperature range, V_{CC} = 7 V (unless otherwise noted) (continued)

5-V internal switch

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TLH}	Threshold voltage		4.2		4.9	V
V_{THL}			4.1		4.7	
Rson	On-time resistance			2.5	8	Ω
V_{hys}	Hysteresis		50		250	mV

current limit

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Internal current source		10	15	20	µA
	Input offset voltage			2.5		mV

UVLO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TLH)}$	Threshold voltage		3.6		4.2	V
$V_{(THL)}$			3.5		4.1	
	Hysteresis		50		250	mV

driver output

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUT_u sink current	V_O = 3 V		0.5	1.2		A
OUT_u source current	V_O = 2 V		–1	–1.7		
OUT_d sink current	V_O = 3 V		0.5	1.2		A
OUT_d source current	V_O = 2 V		–1	–1.7		
Rise time	High side driver is GND referenced, Input: INV = 0 V – 3 V, t_r/t_f = 10 ns, Frequency = 200 kHz,	C_L = 2200 pF		25.6		ns
		C_L = 3300 pF		30.8		
Fall time	High side driver is GND referenced, Input: INV = 0 V – 3 V, t_r/t_f = 10 ns, Frequency = 200 kHz,	C_L = 2200 pF		23.2		ns
		C_L = 3300 pF		25.2		

Softstart

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(CTRL)}$	Softstart current		1.8	2.5	3	µA
	Maximum discharge current			0.92		mA

COMP†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Threshold voltage		1	1.1	1.25	V
Turn on	Propagation delay 50% duty cycle, No capacitor on COMP or OUT_u pin,	Frequency = 200 kHz		452		ns
Turn off				384		

† The delay time in the table includes the drivers.

oscillator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency without Ct			202.4		kHz
Frequency with Ct	Ct = 100 pF		67.5		kHz

TYPICAL CHARACTERISTICS

QUIESCENT CURRENT (BOTH CHANNELS ON) vs SUPPLY VOLTAGE

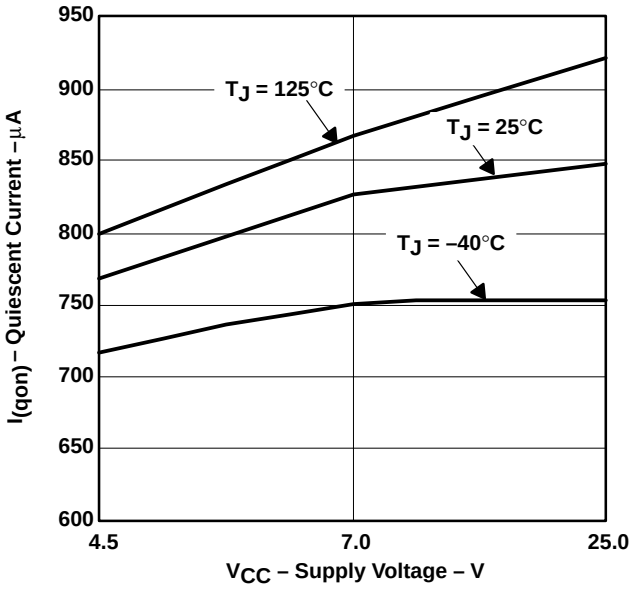


Figure 1

QUIESCENT CURRENT (BOTH CHANNEL STANDBY) vs SUPPLY VOLTAGE

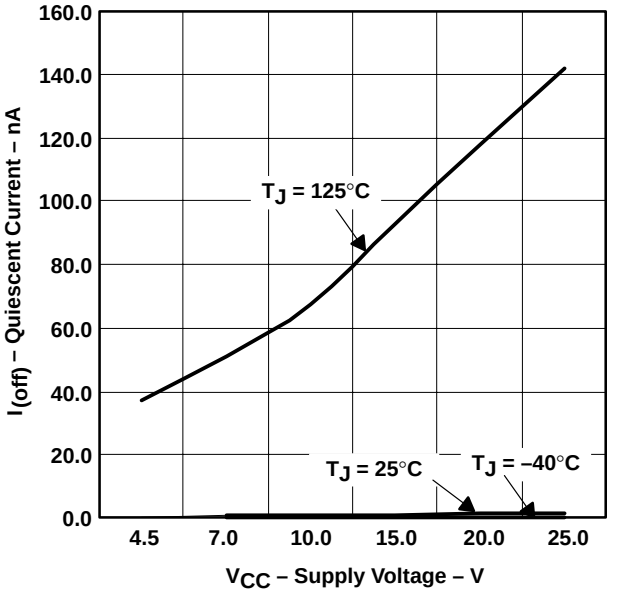


Figure 2

DRIVE OUTPUT VOLTAGE vs DRIVE CURRENT (SOURCE)

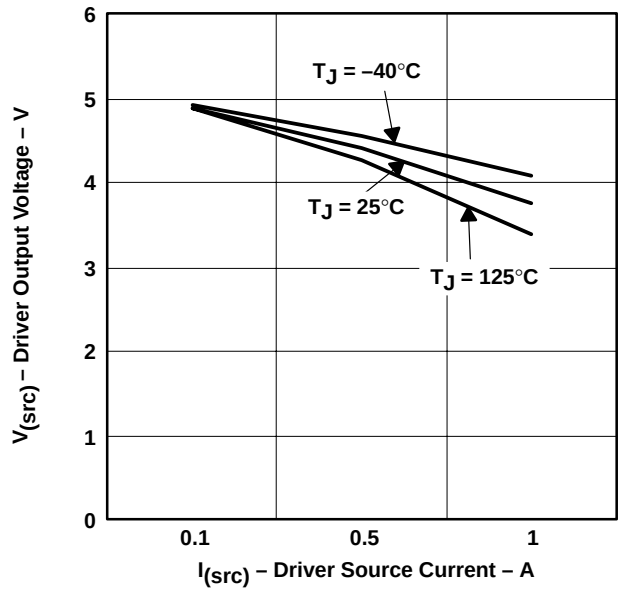


Figure 3

DRIVE VOLTAGE vs DRIVE CURRENT (SINK)

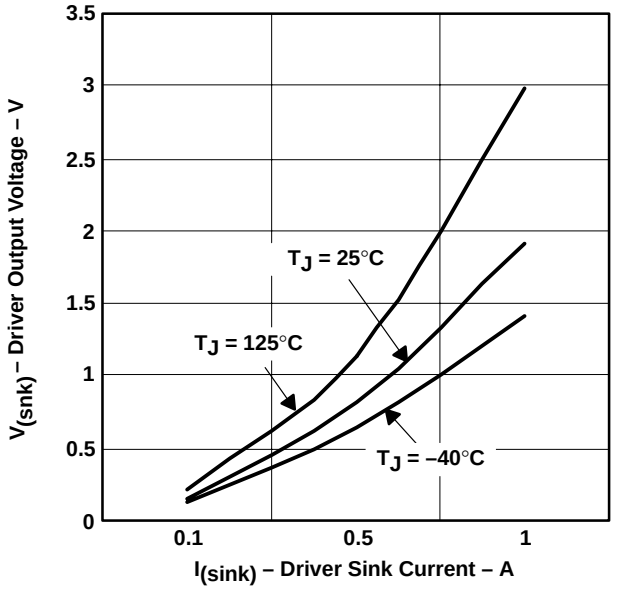


Figure 4

TYPICAL CHARACTERISTICS

SOFTSTART CAPACITANCE vs SOFTSTART TIMING

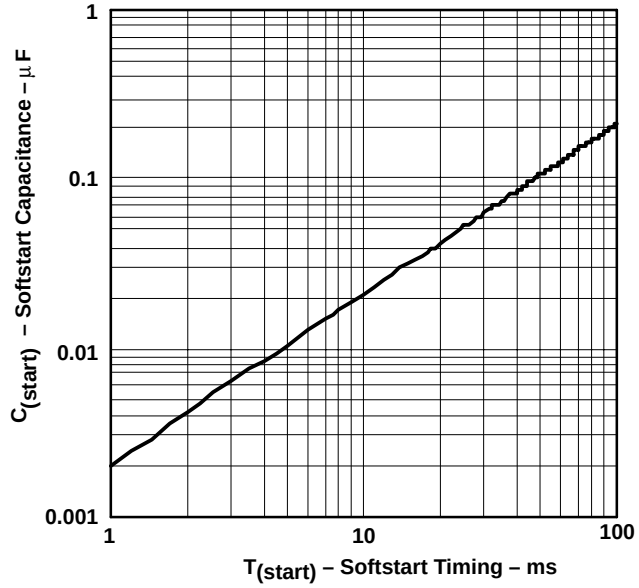


Figure 5

CURRENT-PROTECTION SOURCE CURRENT vs SUPPLY VOLTAGE

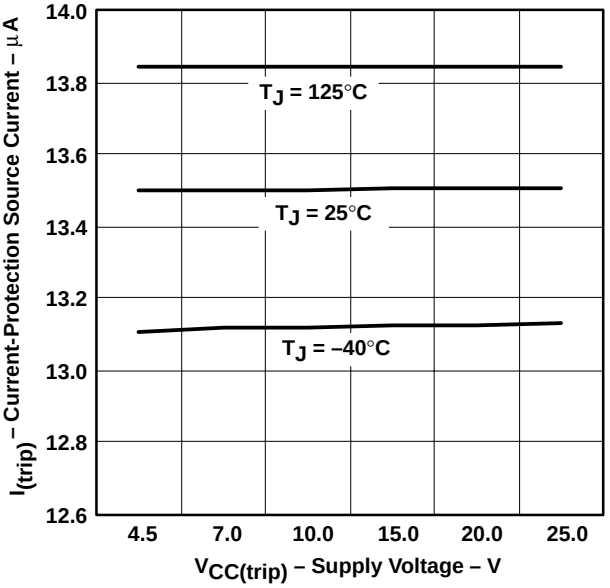


Figure 6

STANDBY THRESHOLD VOLTAGE (H–L) vs JUNCTION TEMPERATURE

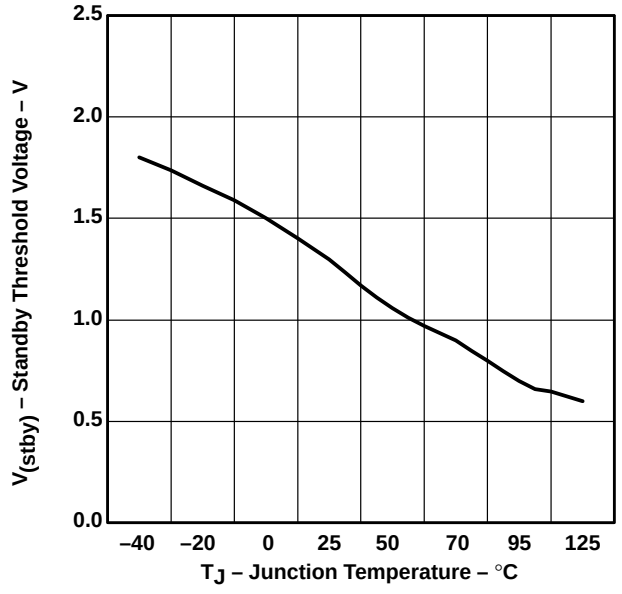


Figure 7

UVLO HYSTERESIS VOLTAGE vs JUNCTION TEMPERATURE

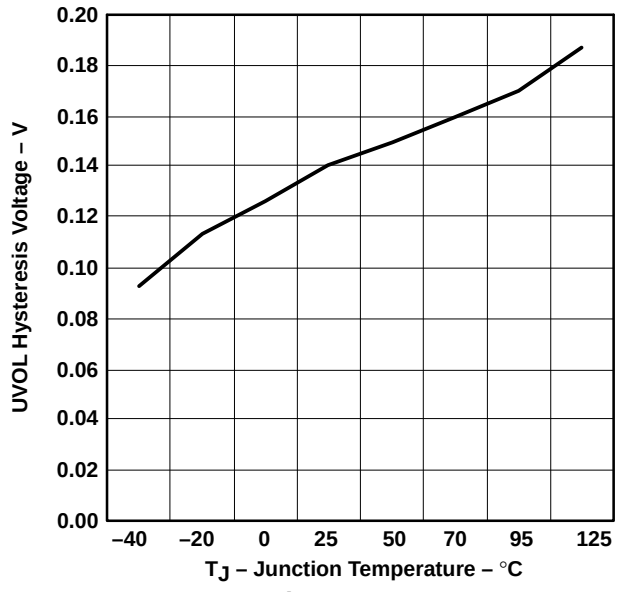


Figure 8

TYPICAL CHARACTERISTICS

UVLO THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

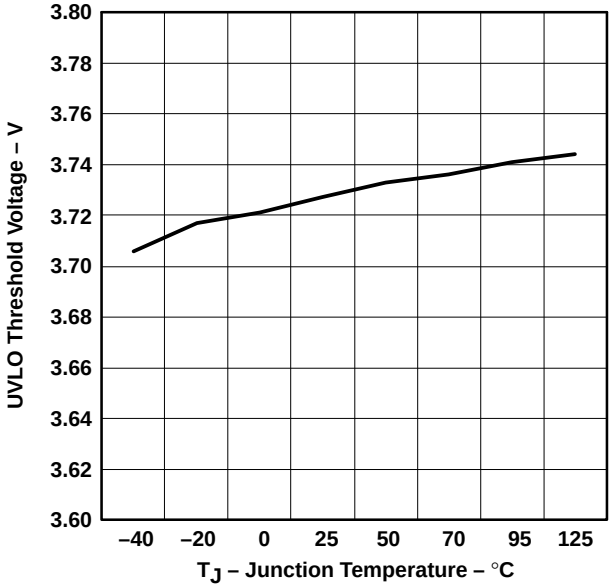


Figure 9

STANDBY THRESHOLD (L–H) vs JUNCTION TEMPERATURE

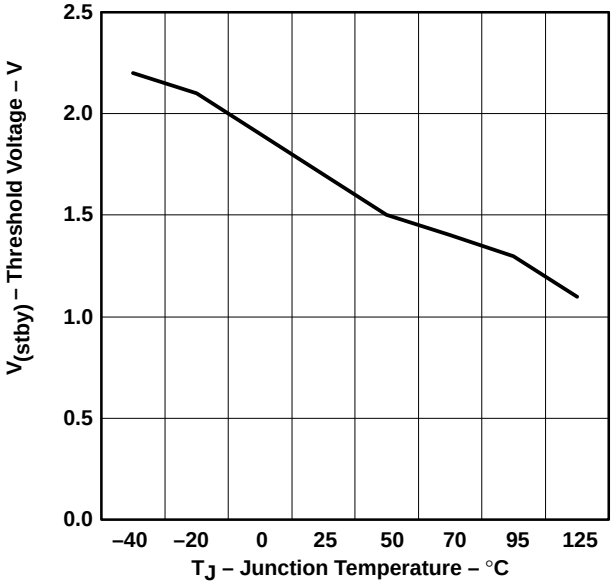


Figure 10

SOFT START CHARGE CURRENT vs JUNCTION TEMPERATURE

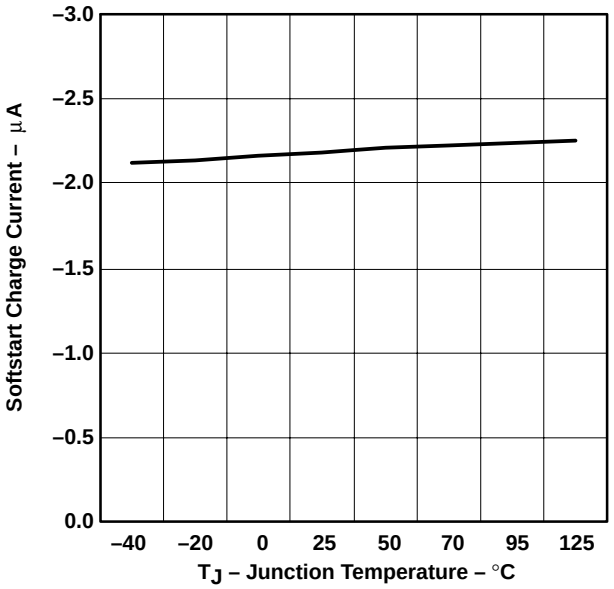


Figure 11

VREF5 VOLTAGE vs VREF5 CURRENT

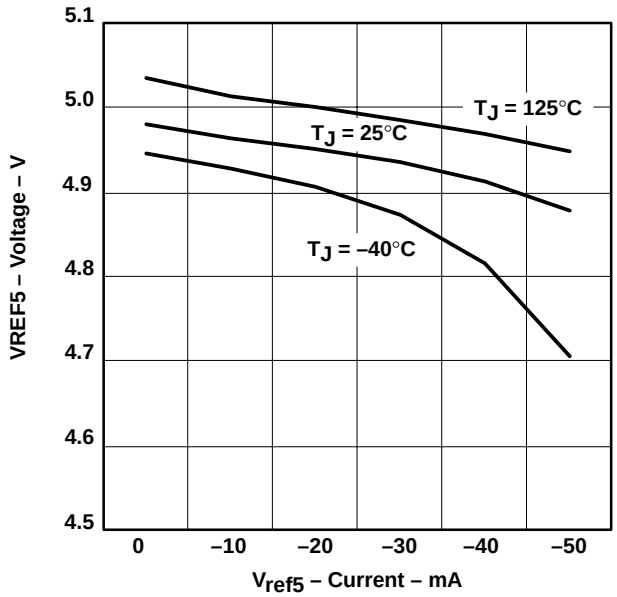


Figure 12

APPLICATION INFORMATION

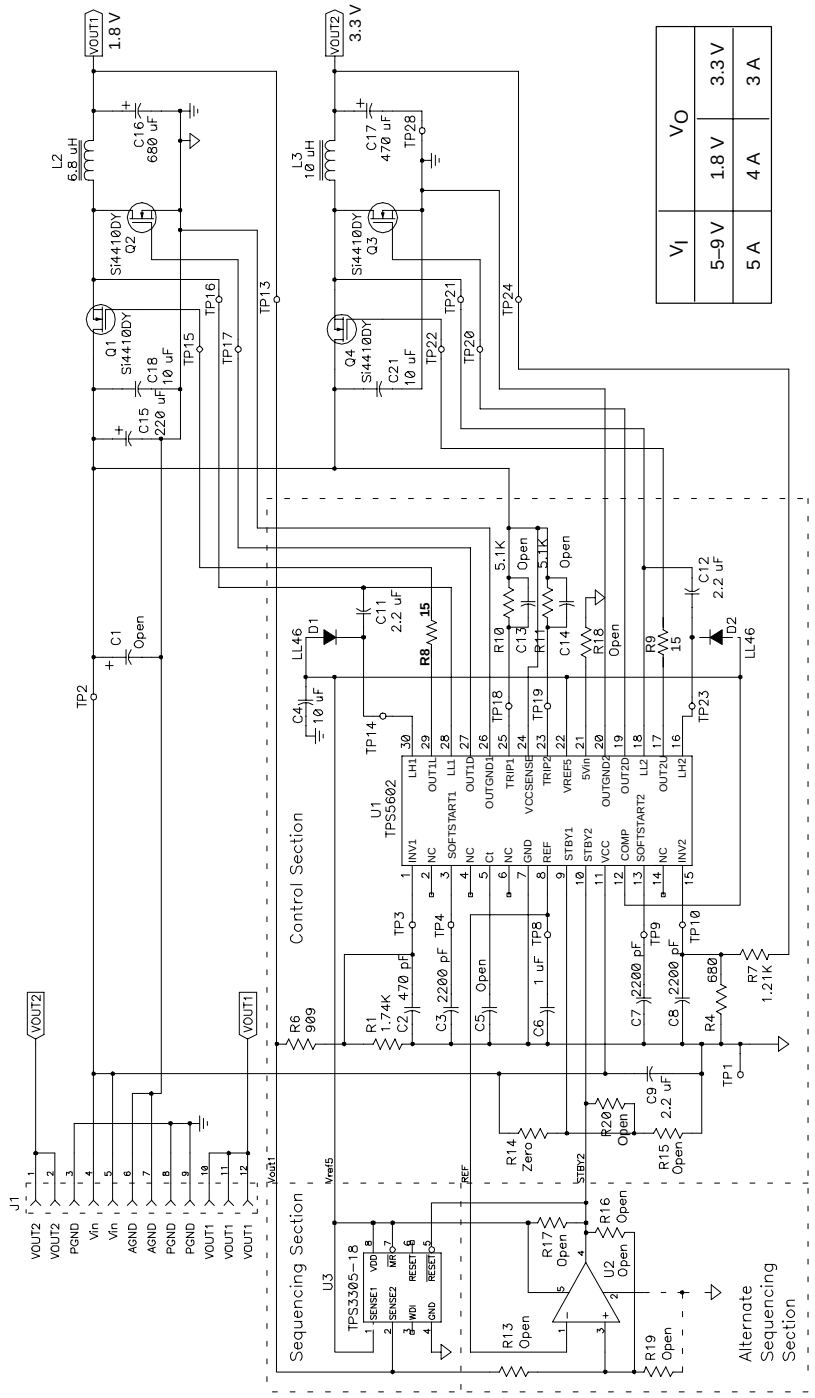


Figure 13. EVM Schematic Diagram

APPLICATION INFORMATION

application for DSP power

The design shown in this data sheet is a reference design for a DSP application. An evaluation module (EVM), TPS5602EVM-121 (SLVP121), is available for customer testing and evaluation. The intent is to allow a customer to fully evaluate the given design using the plug-in EVM supply shown here. The input voltage for this EVM is from 4.5 V to 9 V. The outputs are 1.8 V at 4 A and 3.3 V at 3 A. By changing few components this EVM can be used for different operating specifications such as high-input voltage.

This application provides the following power supply sequence: the core power goes up before the I/O supply, and if the core power is brought down by abnormal condition, the I/O power will be brought down with it.

To help the customers to design the power supply using the TPS5602, key design procedures are shown below:

switching frequency

With hysteretic control, the switching frequency is a function of the input voltage, the output voltage, the hysteresis window, the delay of the hysteresis comparator and the driver, the output inductance, the resistance in the output inductor, the output capacitance, the ESR and ESL in the output capacitor, the output current, and the turn on resistance of high side and low side MOSFET. It is a very complex equation if everything is included. To make it more useful to the designers, a simplified equation only considers the most influential factors. The tolerance of this equation is about 30%:

$$fs = \frac{Vout \times (Vin - Vout) \times \left(ESR - \left(10 \times 10^{-7} + Td\right)/Cout\right)}{Vin \times \left(Vin \times ESR \times \left(10 \times 10^{-7} + Td\right) + 0.007 \times Lout - ESL \times Vin\right)}$$

Where fs is the switching frequency (Hz); *Vout* is the output voltage (V); *Vin* is the input voltage (V); *Cout* is the output capacitance; *ESR* is the equivalent series resistance in the output capacitor (Ω); *ESL* is the equivalent series inductance in the output capacitor (H); *Lout* is the output inductance (H); and *Td* is the output feedback filter time constant (S).

Example: Vin = 5 V, Vout = 1.8 V, Cout = 680 μF: ESR = 40 mΩ; ESL = 3 nH; Lout = 6 μH; Td = 0.5 μs

Then, the frequency *fs = 122 kHz*.

output inductor ripple current

The output inductor current ripple can affect not only the efficiency and the inductor saturation, but also the output capacitor selection. The equation is exhibited below:

$$Iripple = \frac{Vin - Vout - Iout \times \left(Rdson + R_L\right)}{Lout} \times D \times Ts$$

Where *Iripple* is the peak-to-peak ripple current through the inductor (A); Vin is the input voltage (V); Vout is the output voltage (V); Iout is the output current; Rdson is the on-time resistance of MOSFET (Ω); D is the duty cycle; and Ts is the switching cycle (S). From the equation, it can be seen that the current ripple can be adjusted by changing the output inductor value.

Example: Vin = 5 V, Vout = 1.8 V, Iout = 5 A: Rdson = 10 mΩ; RL = 5 mΩ; D = 0.36; Ts = 10 mS; Lout = 6 μH

Then, the ripple current Iripple = 2 A.

APPLICATION INFORMATION

application for DSP power (continued)

output capacitor RMS current

Assuming the inductor ripple current totally goes through the output capacitor to ground, the RMS current in the output capacitor can be calculated as:

$$Io(rms) = \frac{\Delta I}{\sqrt{12}}$$

Where *Io(rms)* is the maximum RMS current in the output capacitor (A); ΔI is the peak–to–peak inductor ripple current (A).

Example: $\Delta I = 2\ A$, so *Io(rms) = 0.58 A*

input capacitor RMS current

Assuming the input ripple current totally goes into the input capacitor to the power ground, the RMS current in the input capacitor can be calculated as:

$$Ii(rms) = Io \times \left(D \times \sqrt{(1 - D)} + (1 - D) \times \sqrt{D}\right)$$

Where *Ii(rms)* is the input RMS current in the input capacitor (A); *Io* is the output current (A); D is the duty cycle. From the equation, it can be seen that the highest input RMS current usually occurs at lowest input voltage.

Example: *Io = 5 A; D = 0.36*
Then, Ii(rms) = 3.36 A

softstart

The softstart timing can be adjusted by selecting the softstart capacitor value. The equation is

$$C_{soft} = 2 \times T_{soft}$$

Where C_{soft} is the softstart capacitance (μF); T_{soft} is the start-up time pin (S).

Example: *Tsoft = 5 ms*, so *Csoft = 0.01 μF*.

current protection

The current protection in TPS5602 is set using an internal current source and an external resistor to set up the current limit. The sensed high side MOSFET drain-to-source voltage drop is compared to the set point; if the voltage drop exceeds the limit, the internal oscillator is activated, and continuously resets the current limit until the over-current condition is removed. The equation below should be used for calculating the external resistor value for current protection:

$$Rclmt = \frac{Rds(on) \times (Itrip + Iind(p\text{-}p)/2)}{0.000015}$$

Where Rclmt is the external current limit resistor (R10, R11); Rds(on) is the high side MOSFET on resistance; Itrip is the required current limit; Iind(p-p) is the peak-to-peak output inductor current.

Example: Rds(on) = *10 mΩ, Itrip = 5 A, Lind = 2 A,* so *Rclmt = 4 kΩ*.

APPLICATION INFORMATION

application for DSP power (continued)

sequencing and under voltage protection

The EVM design uses the standby pins to implement power sequencing. There are two ways to achieve the protection: one uses a voltage supervisory circuit such as the TI TPS3305-18, the other uses a low cost comparator, such as the TI TLV1391. The standby pin for the second channel is pulled low by either the supervisory circuit or the external protection comparator until the first channel output voltage is above the start-up threshold voltage. With the protection hysteresis, during the power down, if the core voltage is lower than, for example, 1.3 V, the 3.3 output will be pulled down together. During the normal operation, if the core voltage is lost, the I/O voltage will be pulled down at the same time. This protection circuit prevents the DSPs from any damage caused by the malfunctioning power supply. The equation displayed below uses the comparator for the protection setpoint:

Assuming R16 is much larger than R17, and R19 is 10 kΩ, and the R13 value is adjusted for the turnon setpoint:

$$R13 = \frac{(Von - 1.2) \times \left(R16 \parallel R19\right)}{1.2}$$

Where *Von* is the required turn on setpoint. For the turn-off setpoint, R16 is adjusted,

$$R16 = \frac{R13 \times R19 \times (1.2 - Vin)}{R19 \times (Voff - 1.2) - 1.2 \times R13}$$

By solving these equations together, or using a spreadsheet to iterate, the setpoints can be easily derived. The two equations are used for the verification:

$$Von = \frac{1.2 \times (R13 + \left(R16 \parallel R19\right)}{\left(R16 \parallel R19\right)} \quad \text{and} \qquad Voff = R13 \times \left(\frac{1.2 - Vin}{R16} + \frac{1.2}{R19} + \frac{1.2}{R13}\right)$$

Where *Von* and *Voff* are the turnon and turnoff setpoints respectively

Example can be found by using the numbers in the bill of materials.

layout considerations

Good power supply results will only occur when care is given to proper design and layout. Layout will affect noise pickup and generation and can cause a good design to perform with less than expected results. With a range of currents from milliamps to tens or even hundreds of amps, good power supply layout is much more difficult than most general PCB designs. The general design should proceed from the switching node to the output, then back to the driver section and, finally, placing the low-level components. Below are several specific points to consider *before* layout of a TPS5602 design begins.

- All sensitive analog components should be referenced to ANAGND. These include components connected to Vref5, Vref, INV, LH, and COMP.
- Analog ground and drive ground should be isolated as much as possible. Ideally, analog ground will connect to the ground side of the bulk storage capacitors on V_O, and drive ground will connect to the main ground plane close to the source of the low-side FET.
- Connections from the drivers to the gate of the power FETs should be as short and wide as possible to reduce stray inductance. This becomes more critical if external gate resistors are not being used.
- The bypass capacitor for V_{CC} should be placed close to the TPS5602.

APPLICATION INFORMATION

layout considerations (continued)

- When configuring the high-side driver as a floating driver, the connection from LL to the power FETs should be as short and as wide as possible.
- When configuring the high-side driver as a floating driver, the bootstrap capacitor (connected from LH to LL) should be placed close to the TPS5602.
- When configuring the high-side driver as a ground-referenced driver, LL should be connected to DRVGND.
- The bulk storage capacitors across V_{IN} should be placed close to the power FETs. High-frequency bypass capacitors should be placed in parallel with the bulk capacitors and connected close to the drain of the high-side FET and to the source of the low-side FET.
- High-frequency bypass capacitors should be placed across the bulk storage capacitors on V_O.
- LH and LL should be connected very close to the drain and source, respectively, of the high-side FET. LH and LL should be routed very close to each other to minimize differential-mode noise coupling to these traces. Ceramic decoupling capacitors should be placed close to where HISENSE connects to V_{IN}, to reduce high-frequency noise coupling on HISENSE.
- The output voltage sensing trace should be isolated from the switching node and/or inductor pulses by the use of a ground trace or plane.

test results

The tests are conducted at T_A = 25°C, the input voltage is 5 V (if not specifically noted).

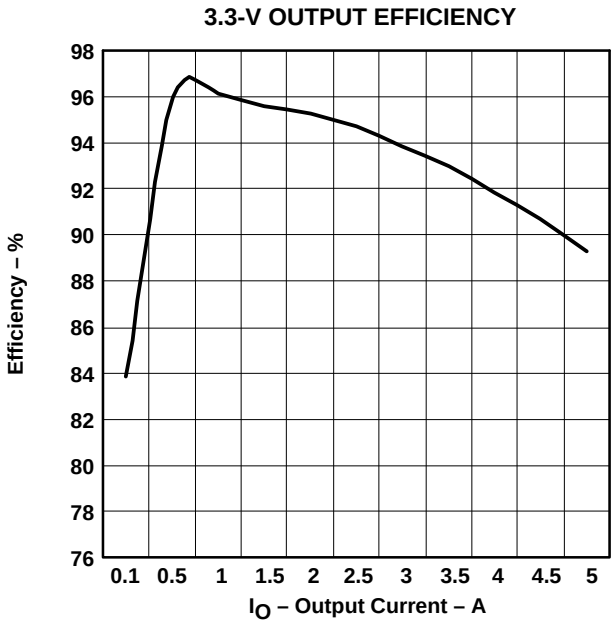


Figure 14

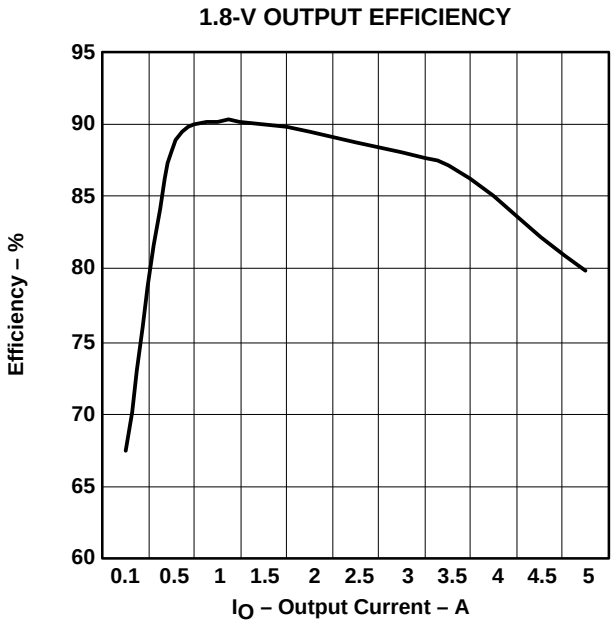


Figure 15

APPLICATION INFORMATION

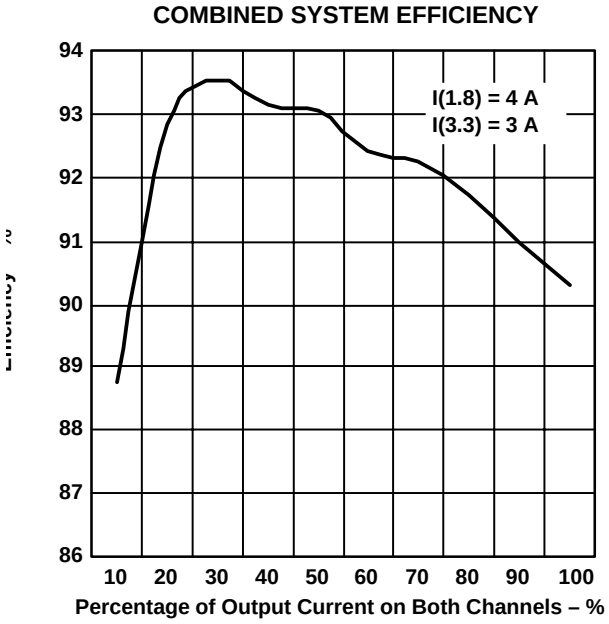


Figure 16

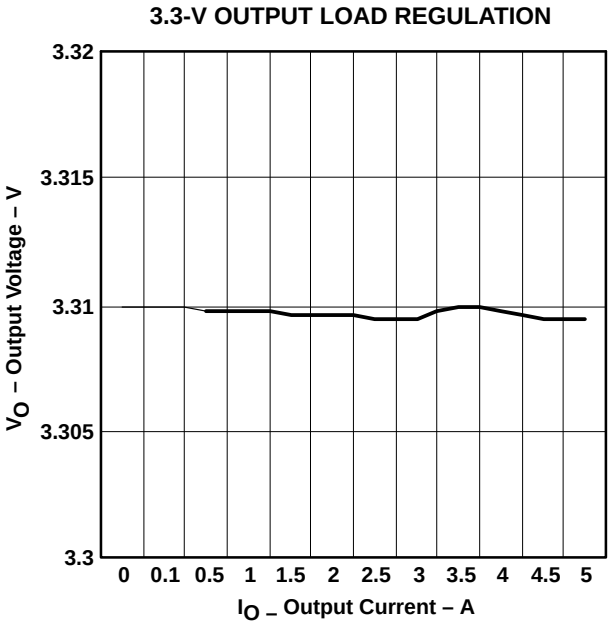


Figure 17

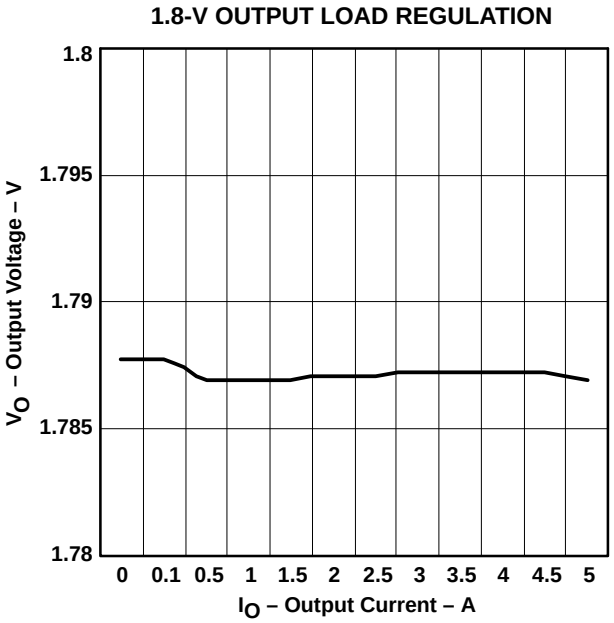


Figure 18

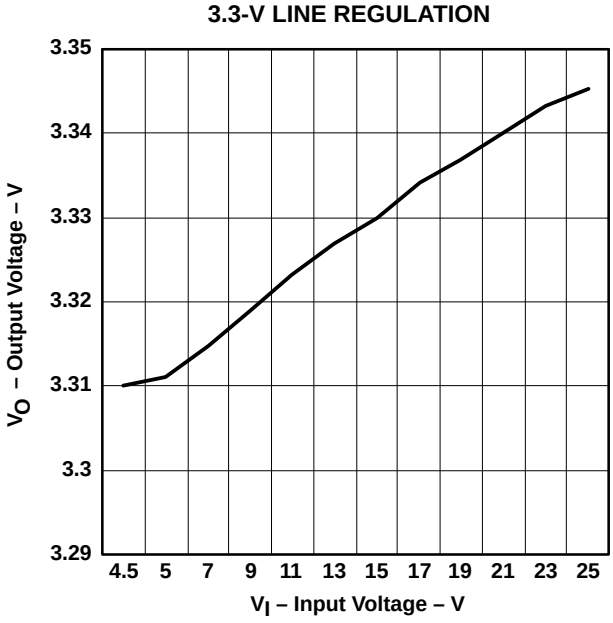


Figure 19

APPLICATION INFORMATION

1.8-V OUTPUT LINE REGULATION

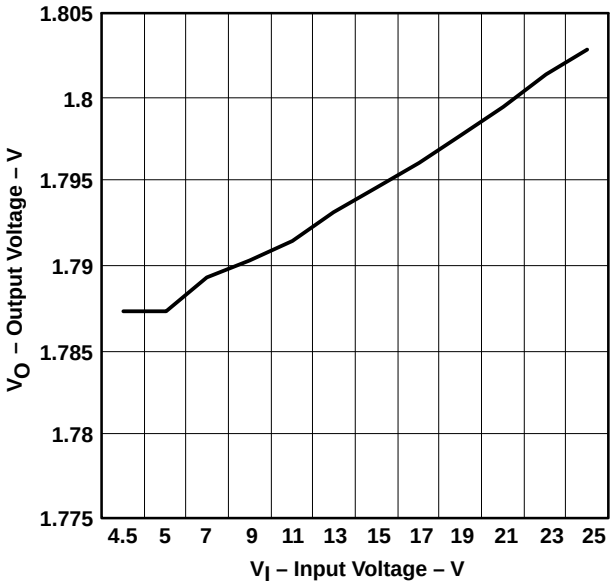


Figure 20

OUTPUT VOLTAGE RIPPLE

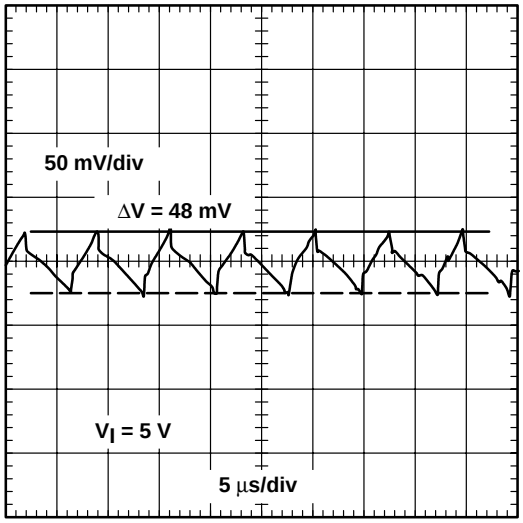


Figure 21

POWER-UP SEQUENCING

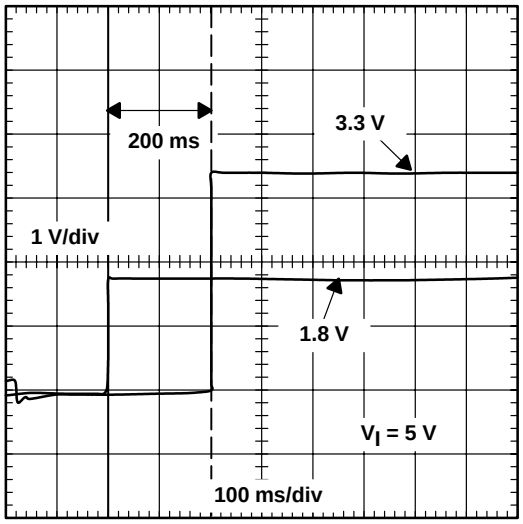


Figure 22

POWER-DOWN SEQUENCING

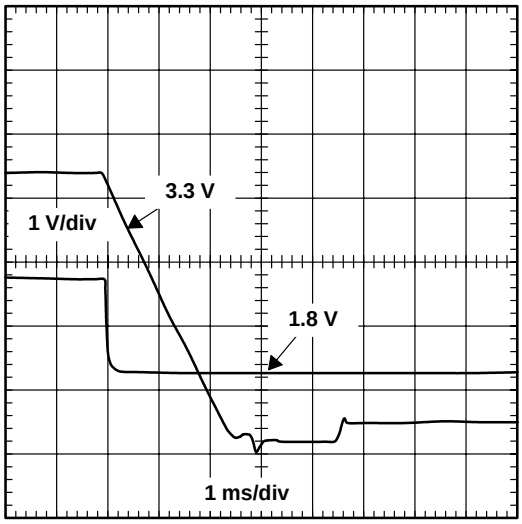


Figure 23

APPLICATION INFORMATION

TRANSIENT RESPONSE (OVERSHOOT)

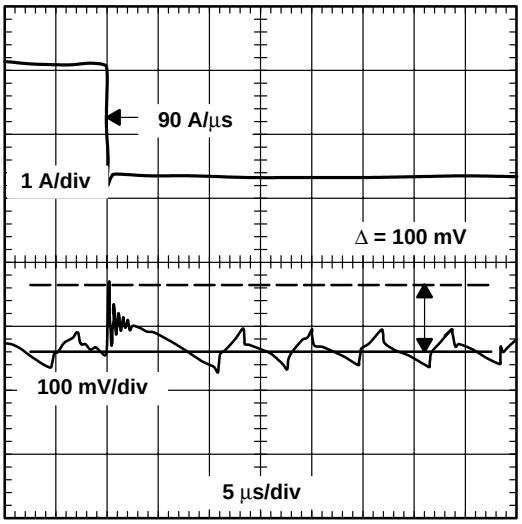


Figure 24

TRANSIENT RESPONSE (UNDERSHOOT)

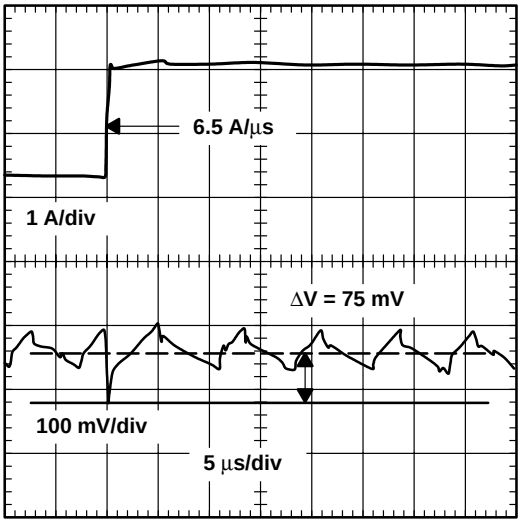


Figure 25

APPLICATION INFORMATION

Table 1. SLVP121 Bill of Materials

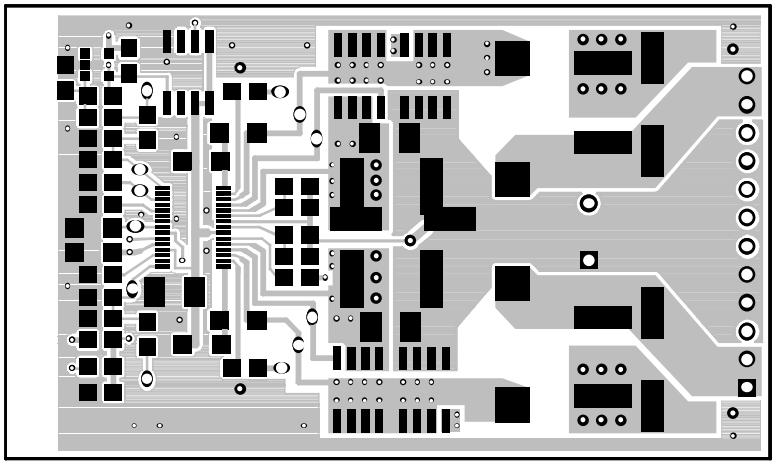
REF.	PART NUMBER	MFR.	DESCRIPTION	SIZE
C1†			Open	
C2	Std		Capacitor, ceramic, 470 pF,16 V, X7R, 20%	805
C3	Std		Capacitor, ceramic, 2200 pF,16 V, X7R, 20%	805
C4	GRM235Y5V106Z016A	muRata	Capacitor, ceramic, 10 µF, 16 V, Y5V	1210
C5†			Open	805
C6	Std		Capacitor, ceramic, 1 µF, 16 V, X7R, 20%	1206
C7	Std		Capacitor, ceramic, 2200 pF, 16 V, X7R, 20%	805
C8	Std		Capacitor, ceramic, 2200 pF, 16 V, X7R, 20%	805
C9	GRK316F225ZG	Taiyo Yuden	Capacitor, ceramic, 2.2 µF, 35 V, X7R, 20%	1206
C11	GRK316F225ZG	Taiyo Yuden	Capacitor, ceramic, 2.2 µF, 35 V, X7R, 20%	1206
C12	GRK316F225ZG	Taiyo Yuden	Capacitor, ceramic, 2.2 µF, 35 V, X7R, 20%	1206
C13†	Std		Open	805
C14†	Std		Open	805
C15	10TPB220M	SANYO	Capacitor, electrolytic, 220 µF, 10 V, 20%	10×10 mm
C16	2R5TPB680M	SANYO	Capacitor, POSCAP, 680 µF, 2.5 V, 20%	7.3×4.3 mm
C17	4TPB470M	SANYO	Capacitor, POSCAP, 470 µF, 4 V, 20%	7.3×4.3 mm
C18	GMK325F106ZH	Taiyo Yuden	Capacitor, ceramic, 10 µF, 35 V	1210
C21	GMK325F106ZH	Taiyo Yuden	Capacitor, ceramic, 10 µF, 35 V	1210
D1	SD103-AWDICT-ND	Digikey	Diode, Schottky, 40 mA, 200 mA, 400 mW	3.5×1.5 mm
D2	SD103-AWDICT-ND	Digikey	Diode, Schottky, 40 mA, 200 mA, 400 mW	3.5×1.5 mm
J1	S1132-12-ND	Sullins	Header, right angle, 12-pin, 0.1 ctrs, 0.3” pins	Digikey, S1132–12–ND
L2	DO3316P-682	Coilcraft	Inductor, 6.8 µH, 4.4 A	0.5x0.37 in
L3	DO3316P-103	Coilcraft	Inductor 10 µH, 3.9 A	0.5x0.37 in
Q1–Q4	Si441DY Rev. A	Siliconix	MOSFET, N-Ch, 30 V, 10-A, 0.013 Ω	SO–8
R1	Std		Resistor, SMD, MF, 1.74 kΩ, 1/8W, 1%	805
R4	Std		Resistor, SMD, MF, 680 Ω, 1/8W, 1%	805
R6	Std		Resistor, SMD, MF, 910 Ω, 1/8W, 1%	805
R7	Std		Resistor, SMD, MF, 1.21 kΩ, 1/8W, 1%	805
R8	Std		Resistor, SMD, MF, 15 Ω, 1/8W, 5%	805
R9	Std		Resistor, SMD, MF, 15 Ω, 1/8W, 5%	805
R10	Std		Resistor, SMD, MF, 5.1 kΩ, 1/8W, 5%	805
R11	Std		Resistor, SMD, MF, 5.1 kΩ, 1/8W, 5%	805
R13†	Std		Open, resistor, SMD, MF, 3.3 kΩ, 1/8W, 5%	805
R14	Std		Open, resistor, SMD, MF, kΩ, 1/8W, 5%	805
R15†	Std		Open, resistor, SMD, MF, 1 kΩ, 1/8W, 5%	805
R16†	Std		Open, resistor, SMD, MF, 200 kΩ, 1/8W, 5%	805
R17†	Std		Open, resistor, SMD, MF, 10 kΩ, 1/8W, 5%	805
R18†	Std		Open, resistor, SMD, MF, 1 kΩ, 1/8W, 5%	805
R19†	Std		Open, resistor, SMD, MF, 10 kΩ, 1/8W, 5%	805
R20†	Std		Open, resistor, SMD, MF, 0 kΩ	805
U1	TPS5602DBT	TI	Dual channel controller	TSSOP 30-pin
U2†	TLV1391	TI	Open, single Comparator	SOT-23
U3	TPS3305-18D	TI	Supervisor	D

NOTE: This table is for 5–9 V input voltage and 3.3 V/1.8 V only.
† Any components with † are for optional test purpose only.

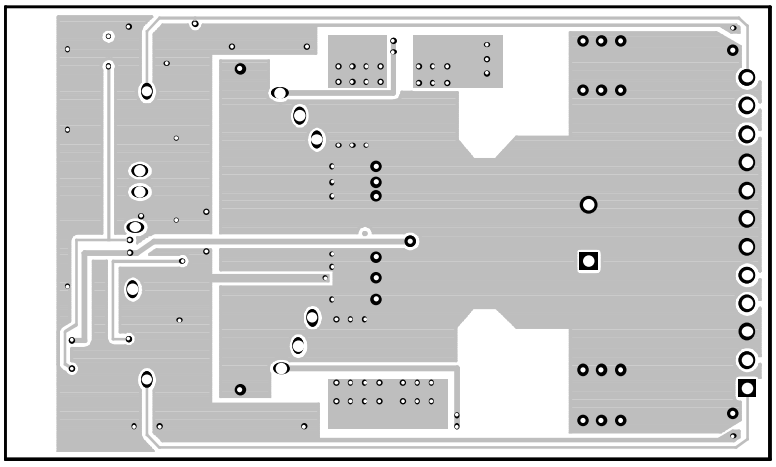
APPLICATION INFORMATION

To change the EVM operating specifications, several suggestions are shown in the following table.

HIGH INPUT VOLTAGE (TO 25 V)	2.5 V OUTPUT VOLTAGE	LOW-COST POWER SEQUENCING	COMPONENT SECOND SOURCE	
	Change R1 to 1 kΩ	Remove U3	Q1–4	IR7811 for higher efficiency
Add R15 (1 kΩ)	Change Rt to 1.2 kΩ	Add U2		
Change C15 to ELNA RV-35V221MH10-R (35 V, 220 μF)	Change U3 to TPS3305-25D	Add R13, R16, R17, R19		

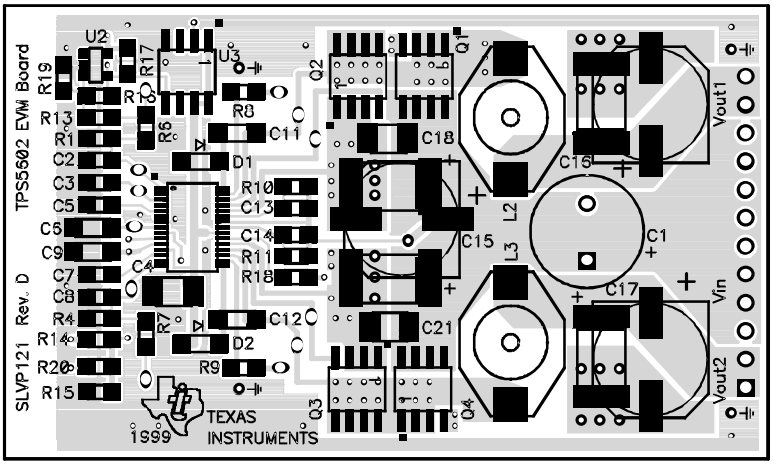


TOP SIDE



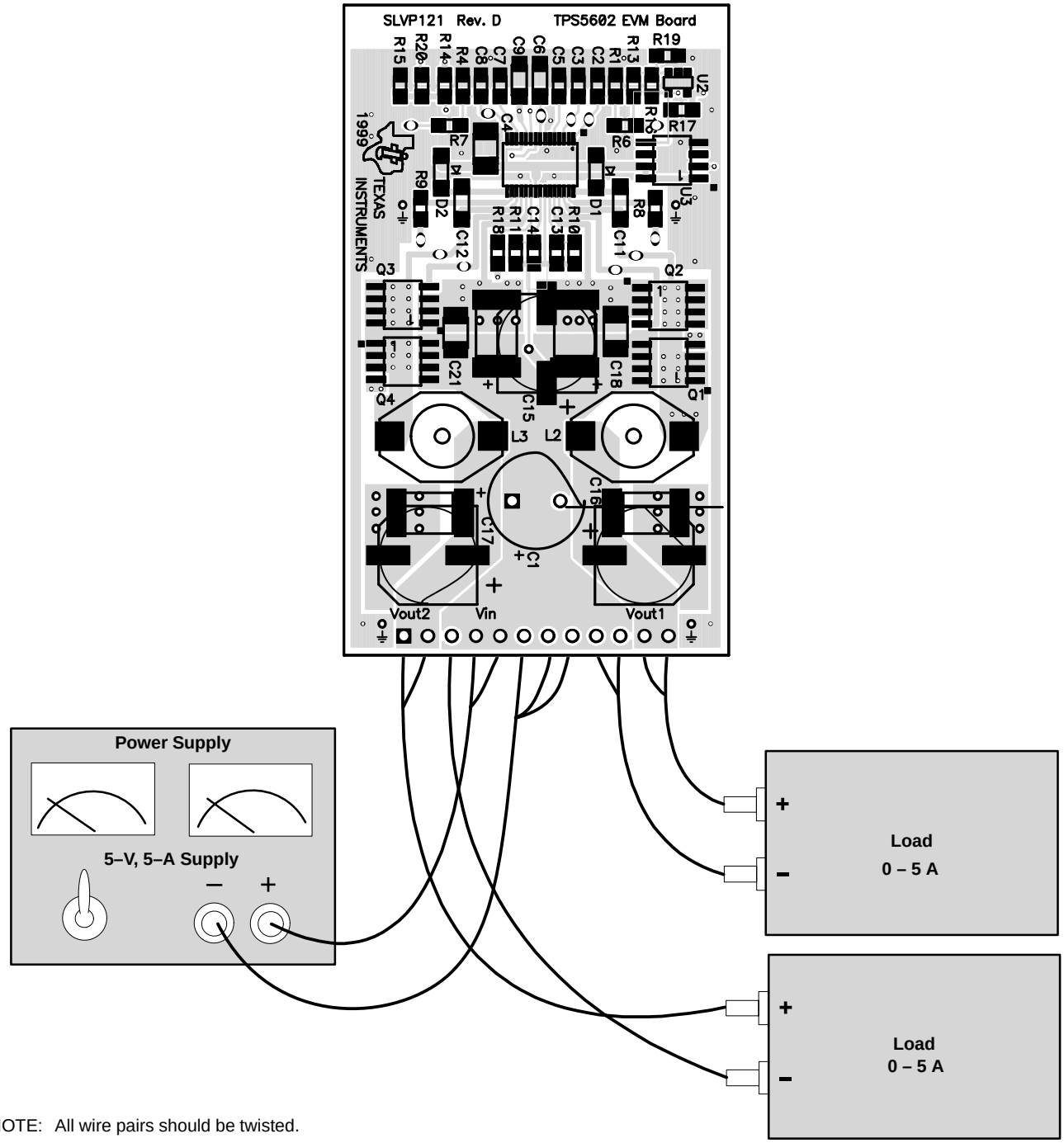
BOTTOM SIDE

APPLICATION INFORMATION



BOARD ASSEMBLY

APPLICATION INFORMATION



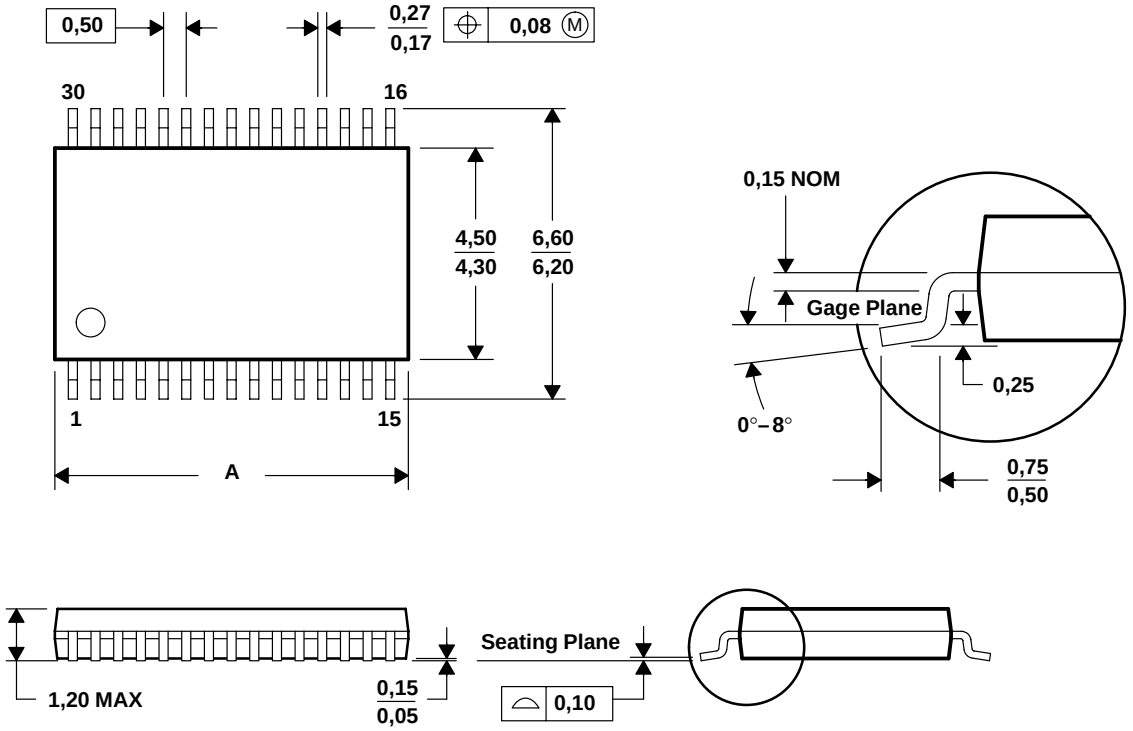
NOTE: All wire pairs should be twisted.

Figure 26. Test Setup

MECHANICAL DATA

DBT (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

30 PINS SHOWN



DIM \ PINS **	28	30	38	44	50
A MAX	7,90	7,90	9,80	11,10	12,60
A MIN	7,70	7,70	9,60	10,90	12,40

4073252/D 09/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-153 except for pin count and body length

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS5602IDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS5602IDBTG4	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS5602IDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS5602IDBTRG4	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

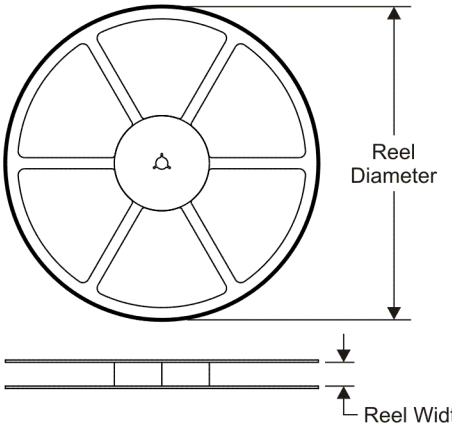
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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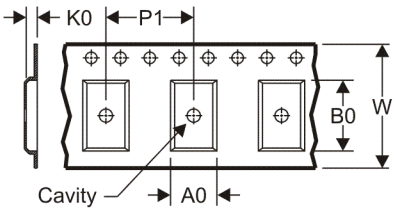
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

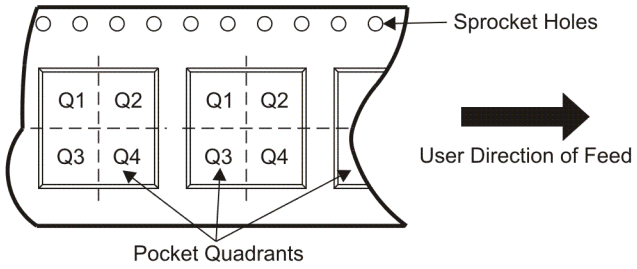


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

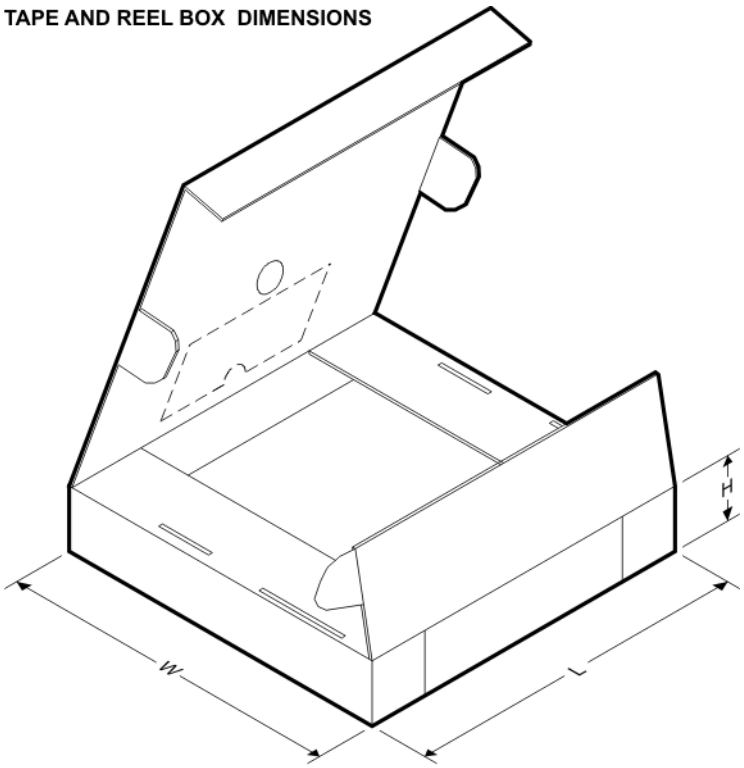
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS5602IDBTR	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS5602IDBTR	TSSOP	DBT	30	2000	346.0	346.0	33.0

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Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
RFID	www.ti-rfid.com	Video & Imaging	www.ti.com/video
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Wireless	www.ti.com/wireless

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