CSD22205L –8-V P-Channel NexFET™ Power MOSFET

1 Features

- Low Resistance
- Small Footprint 1.2 mm × 1.2 mm
- Low Profile 0.35-mm Height
- Lead Free
- Gate-Source Voltage Clamp
- Gate ESD Protection
- RoHS Compliant
- Halogen Free

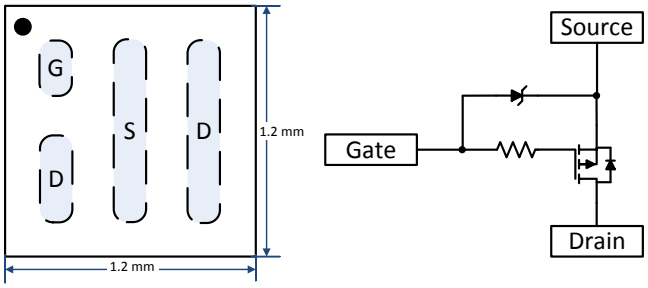
2 Applications

- Battery Management
- Load Switch
- Battery Protection

3 Description

This –8-V, 8.2-mΩ, 1.2-mm × 1.2-mm Land Grid Array (LGA) NexFET™ device has been designed to deliver the lowest on-resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra-low profile. The Land Grid Array (LGA) package is a silicon chip scale package with metal pads instead of solder balls.

Top View and Circuit Configuration



Product Summary

T_A = 25°C		VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	–8		V
Q_g	Gate Charge Total (–4.5 V)	6.5		nC
Q_{gd}	Gate Charge Gate-to-Drain	1.0		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –1.5 V	30	mΩ
		V_{GS} = –1.8 V	20	
		V_{GS} = –2.5 V	11.5	
		V_{GS} = –4.5 V	8.2	
$V_{GS(th)}$	Threshold Voltage	–0.7		V

Device Information(1)

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD22205L	3000	7-Inch Reel	1.20-mm × 1.20-mm Land Grid Array Package	Tape and Reel
CSD22205LT	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

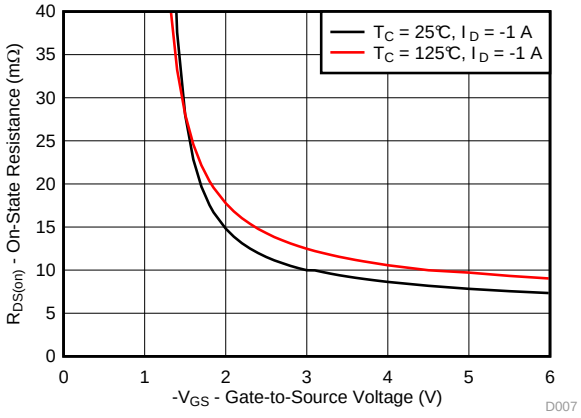
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	–8	V
V_{GS}	Gate-to-Source Voltage	–6	V
I_D	Continuous Drain Current(1)	–7.4	A
I_{DM}	Pulsed Drain Current(2)	–71	A
P_D	Power Dissipation(1)	0.6	W
T_J, T_{stg}	Operating Junction Temperature, Storage Temperature	–55 to 150	°C

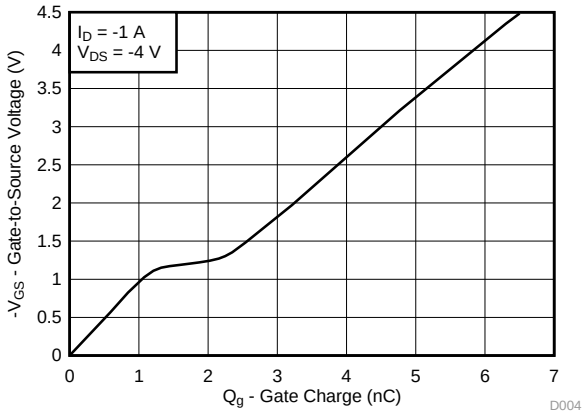
(1) Min Cu $R_{\theta JA}$ = 225°C/W.

(2) Pulse width ≤ 100 μs, duty cycle ≤ 1%.

$R_{DS(on)}$ vs V_{GS}



$R_{DS(on)}$ vs V_{GS}



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Original (May 2017) to Revision A **Page**

- Changed the units for timing parameters from µs : to ns (nanoseconds) in the *Electrical Characteristics* table ... 3

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5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

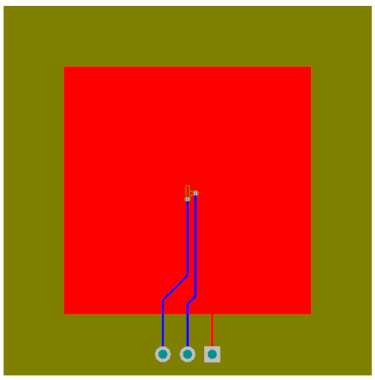
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = –250 µA	–8			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = –6.4 V			–100	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = –6 V			–100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = –250 µA	–0.4	–0.7	–1.05	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = –1.5 V, I_D = –0.2 A		30		mΩ
		V_{GS} = –1.8 V, I_D = –1 A		20	40	
		V_{GS} = –2.5 V, I_D = –1 A		11.5	15.0	
		V_{GS} = –4.5 V, I_D = –1 A		8.2	9.9	
g_{fs}	Transconductance	V_{DS} = –0.8 V, I_D = –1 A		10.4		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{DS} = –4 V, f = 1 MHz		1070	1390	pF
C_{OSS}	Output capacitance			560	730	pF
C_{RSS}	Reverse transfer capacitance			190	250	pF
R_G	Series gate resistance			30		Ω
Q_g	Gate charge total (–4.5 V)	V_{DS} = –4 V, I_D = –1 A		6.5	8.5	nC
Q_{gd}	Gate charge gate-to-drain			1.0		nC
Q_{gs}	Gate charge gate-to-source			1.2		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.7		nC
Q_{OSS}	Output charge	V_{DS} = –4 V, V_{GS} = 0 V		4.1		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = –4 V, V_{GS} = –4.5 V, I_D = –1 A , R_G = 0 Ω		30		ns
t_r	Rise time			14		ns
$t_{d(off)}$	Turnoff delay time			70		ns
t_f	Fall time			32		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_S = –1 A, V_{GS} = 0 V		–0.68	–1.0	V
Q_{rr}	Reverse recovery charge	V_{DS}= –4 V, I_F = –1 A, di/dt = 200 A/µs		16		nC
t_{rr}	Reverse recovery time			38		ns

5.2 Thermal Information

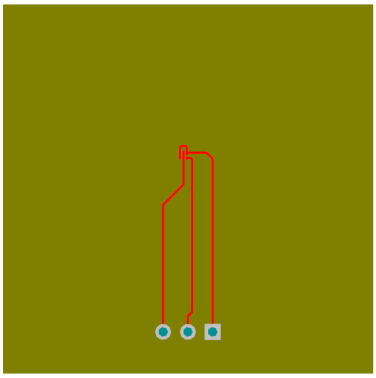
T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)		75		°C/W
	Junction-to-ambient thermal resistance(2)		225		

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.



Typ $R_{\theta JA}$ =75°C/W when mounted on 1 in^2 of 2-oz Cu.



Typ $R_{\theta JA}$ = 225°C/W when mounted on minimum pad area of 2-oz Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

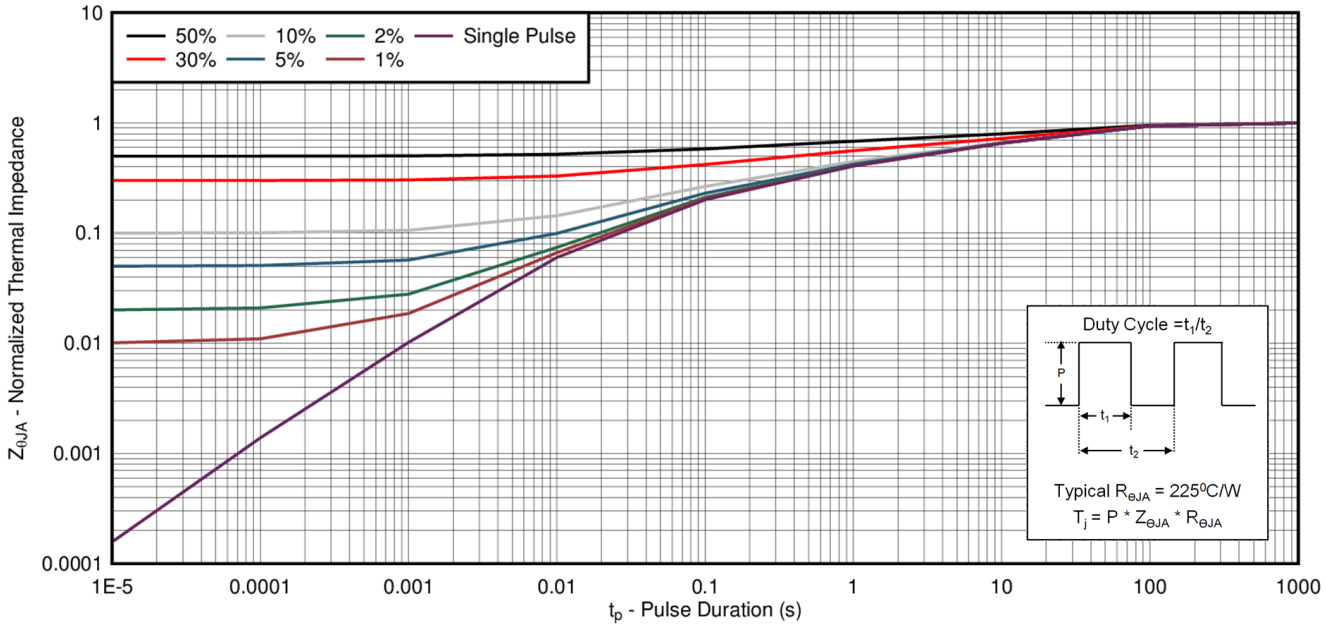


Figure 1. Transient Thermal Impedance

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Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

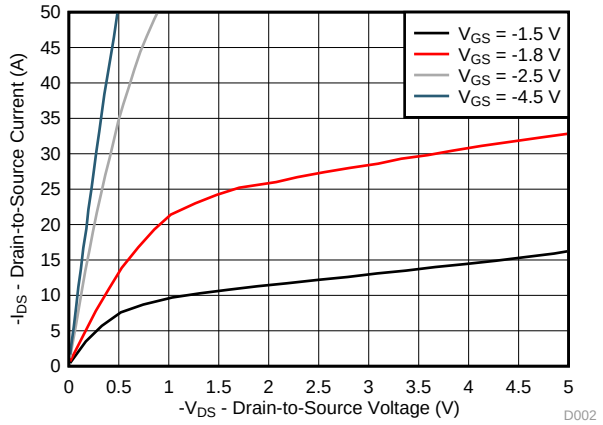


Figure 2. Saturation Characteristics

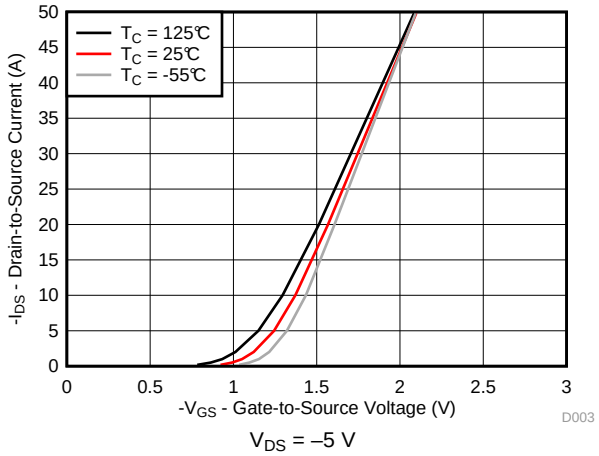


Figure 3. Transfer Characteristics

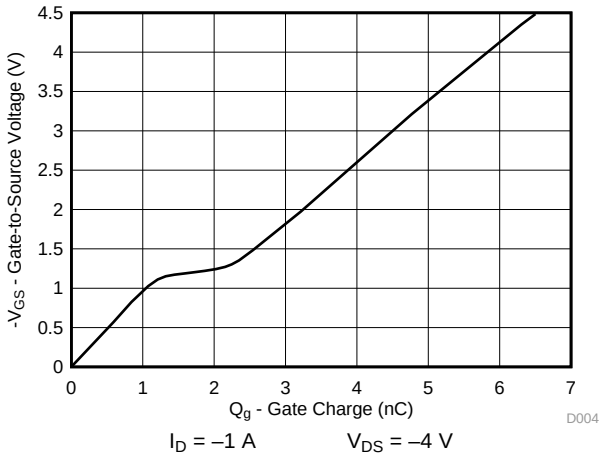


Figure 4. Gate Charge

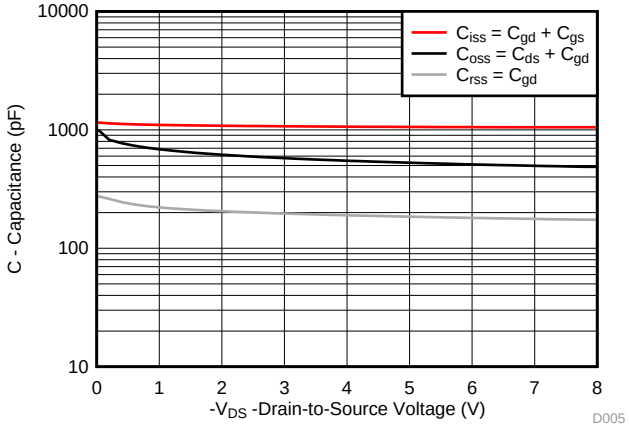


Figure 5. Capacitance

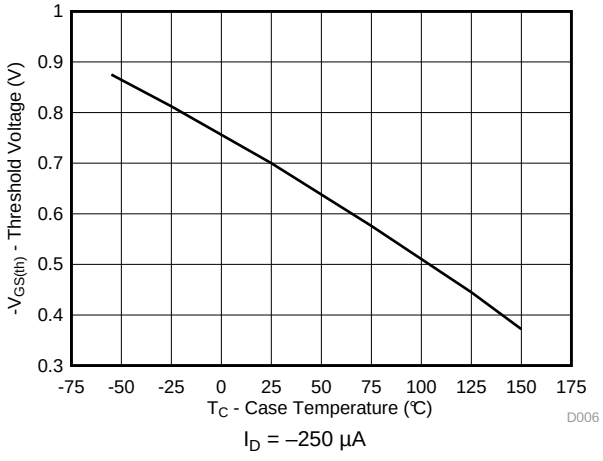


Figure 6. Threshold Voltage vs Temperature

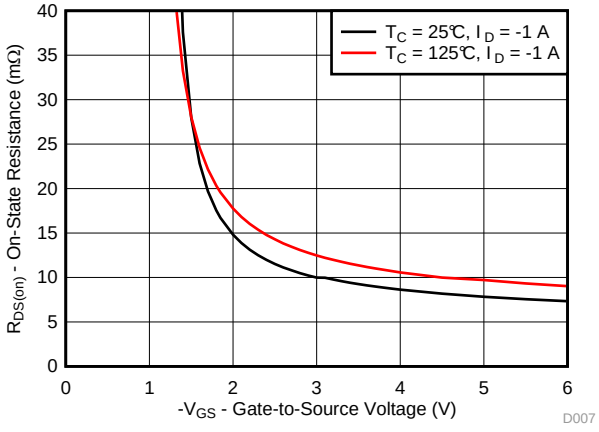
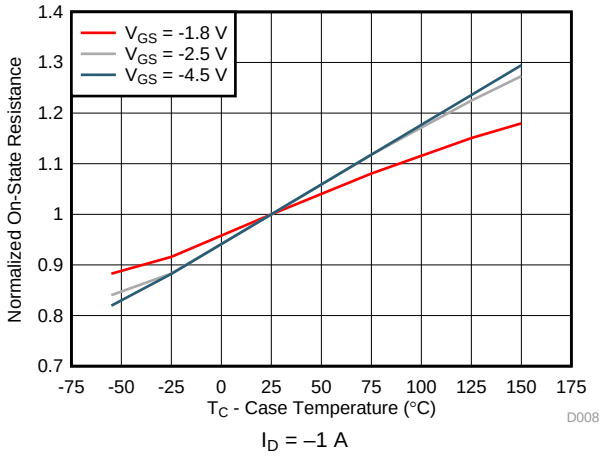


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)



I_D = –1 A

Figure 8. Normalized On-State Resistance vs Temperature

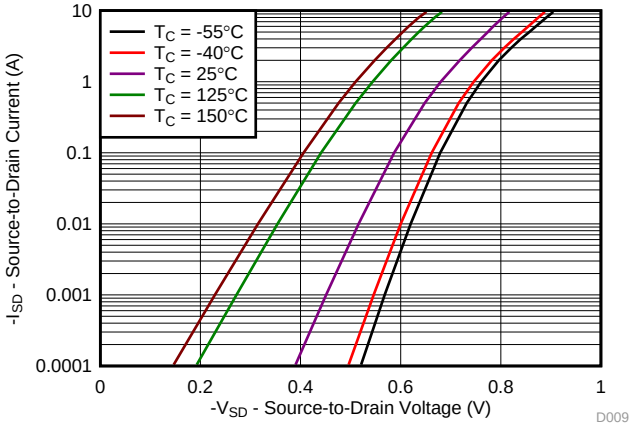
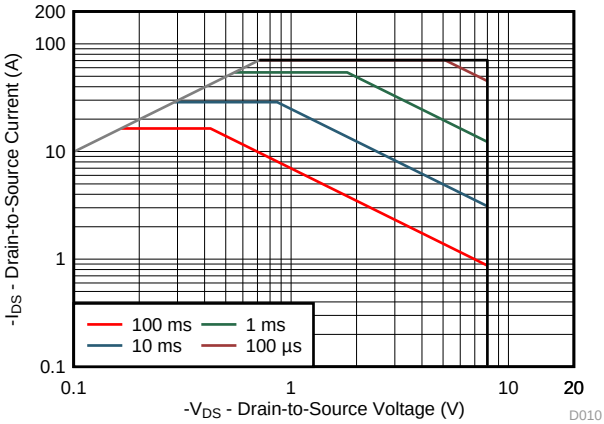


Figure 9. Typical Diode Forward Voltage



Single pulse, typical $R_{\theta JA}$ = 225°C/W

Figure 10. Maximum Safe Operating Area

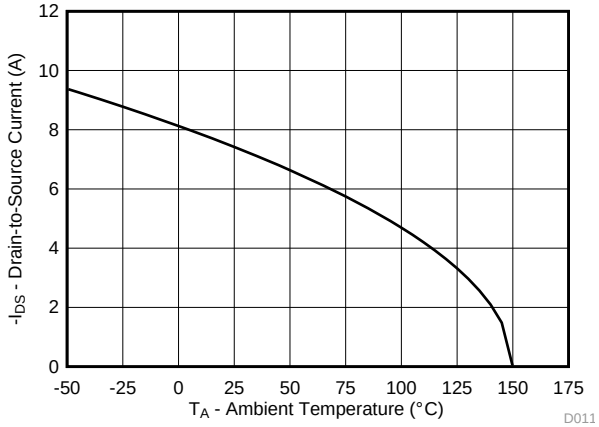


Figure 11. Maximum Drain Current vs Temperature

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6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

SLYZ022 — *TI Glossary*.

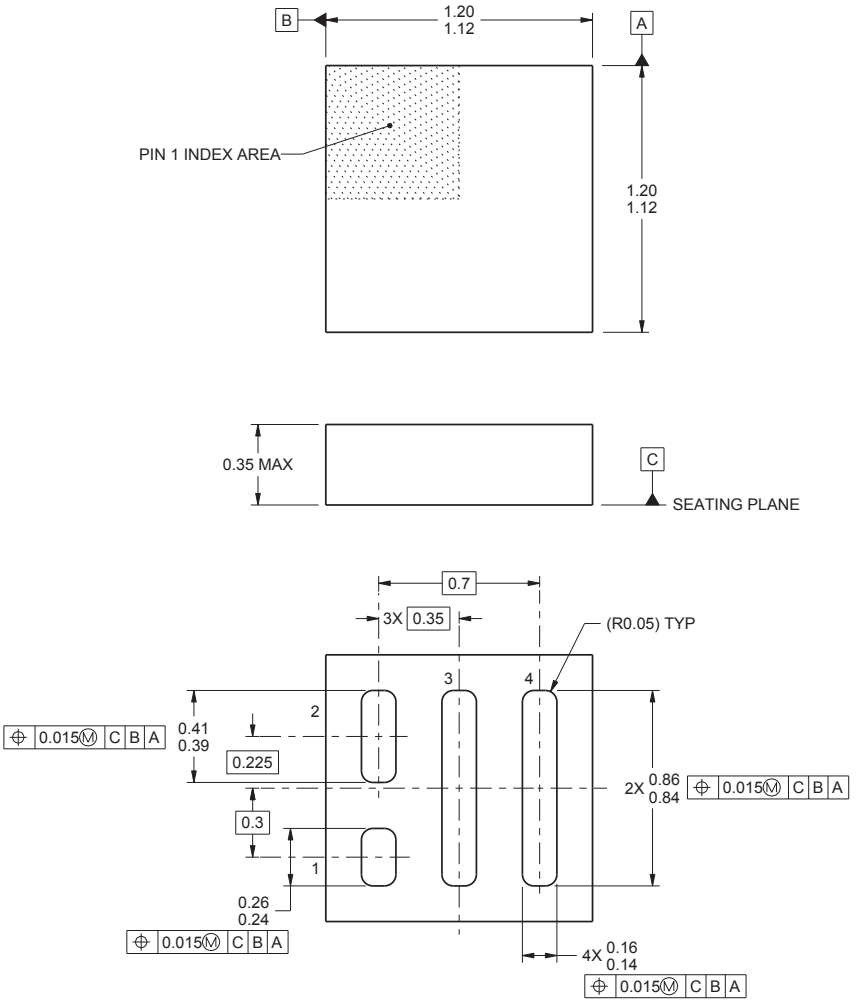
This glossary lists and explains terms, acronyms, and definitions.

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7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 CSD22205L Package Dimensions



4222872/A 04/2016

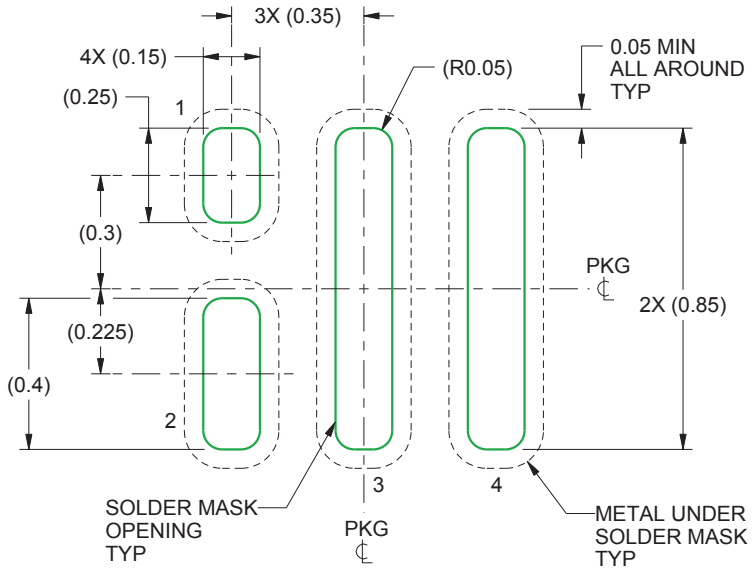
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is a lead-free bump design. Bump finish may vary. To determine the exact finish, refer to the device data sheet or contact a local TI representative.

Table 1. Pin Configuration Table

POSITION	DESIGNATION
1	Gate
2	Drain
3	Source
4	Drain

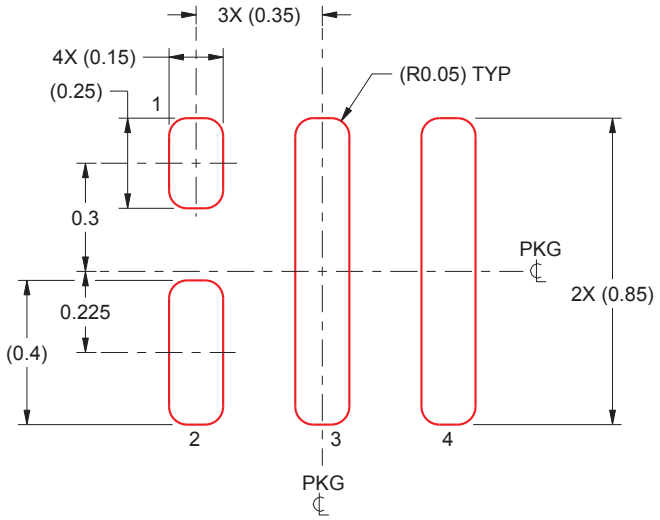
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7.2 Land Pattern Recommendation



NOTE: For more information, see *QFN/SON PCB Attachment* (SLUA271).

7.3 Stencil Recommendation



NOTE: Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

For recommended circuit layout for PCB designs, see *Reducing Ringing Through PCB Layout Techniques* (SLPA005).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD22205L	ACTIVE	PICOSTAR	YMG	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-55 to 150	205	Samples
CSD22205LT	ACTIVE	PICOSTAR	YMG	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-55 to 150	205	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

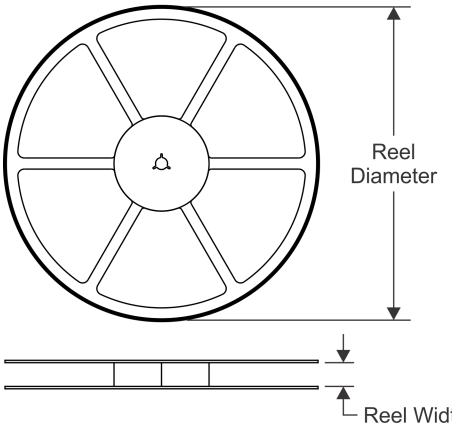
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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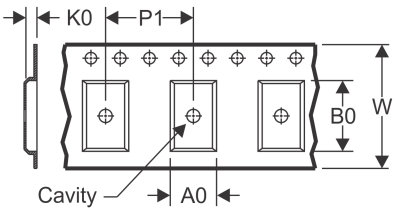
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

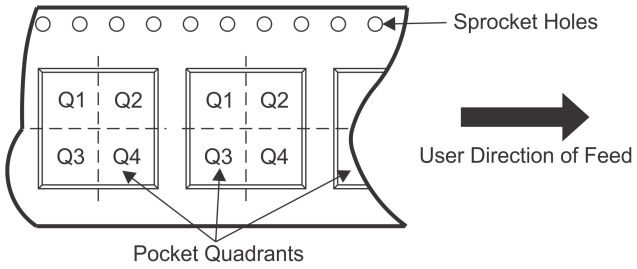


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

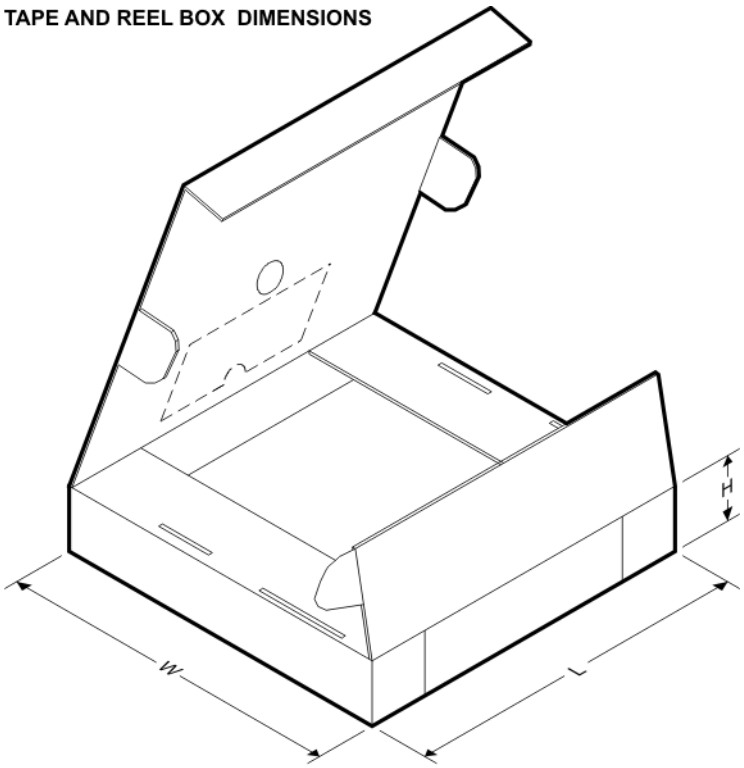
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD22205L	PICOSTAR	YMG	4	3000	180.0	8.4	1.26	1.26	0.42	4.0	8.0	Q1
CSD22205LT	PICOSTAR	YMG	4	250	180.0	8.4	1.26	1.26	0.42	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD22205L	PICOSTAR	YMG	4	3000	182.0	182.0	20.0
CSD22205LT	PICOSTAR	YMG	4	250	182.0	182.0	20.0

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