PIC32MM0064GPL036 Family Silicon Errata and Data Sheet Clarification

The PIC32MM0064GPL036 family devices that you have received conform functionally to the current Device Data Sheet (DS60001324**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC32MM0064GPL036 family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**B3**).

Data Sheet clarifications and corrections start on page 10, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC32MM0064GPL036 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)		
		B0	B2	B3
PIC32MM0016GPL020	06B04053	0004	0006	0007
PIC32MM0032GPL020	06B0C053			
PIC32MM0064GPL020	06B14053			
PIC32MM0016GPL028	06B02053			
PIC32MM0032GPL028	06B0A053			
PIC32MM0064GPL028	06B12053			
PIC32MM0016GPL036	06B06053			
PIC32MM0032GPL036	06B0B053			
PIC32MM0064GPL036	06B16053			

Note 1: The Device IDs and Revision ID (DEVID and DEVREV) are shown in hexadecimal format.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				B0	B2	B3
ADC	12-Bit Mode Conversion	1.	ADC has missing codes.	X	X	X
ADC	Format Options	2.	ADC format option is incorrect.	X	X	X
Reset	$\overline{\text{MCLR}}$ Pin	3.	$\overline{\text{MCLR}}$ Reset does not work in Retention Sleep mode.	X		
UART	Receive Buffer Overflow Detection	4.	Overflow disable feature is not functional.	X		
Primary XT and HS Oscillator (POSC)	Primary Oscillator Start-up Timer (OST)	5.	OST may indicate oscillator is ready for use and set the POSCRDY bit (CLKSTAT[2]) too early.	X	X	X
Reset	Current Consumption	6.	Current consumption in Master Clear Reset is high.	X	X	X
Reset	Configuration Mismatch Reset (CMR)	7.	An erroneous Configuration Mismatch Reset (CMR) event may occur after a POR, BOR or external device programming (ICSP™ or JTAG).	X		
Timer1	External Clock Mode	8.	External Clock Mode: Timer1 does not overflow in External Clock mode when PR1 = 1 and the prescaler is 1:1.	X	X	X
Timer1	External Clock Mode	9.	External Clock Mode: The first increment value is not visible when using External Clock mode and a 1:1 prescaler.	X	X	X
Power	Retention Sleep	10.	Retention Sleep: When the device wakes up from Retention Sleep mode, a device Reset may occur. The BOR, POR and EXTR bits in the RCON register are set erroneously for this Reset.	X		
Power	BOR	11.	BOR: The main BOR may not function.	X		
Programming	JTAG TDO Pin	12.	The JTAG TDO (RB10) pin toggles during programming when using the PGECx/PGEDx pin pairs.	X		
I/O	Schmitt Trigger Inputs	13.	Schmitt Trigger inputs may have glitches with slow signal rise/fall times.	X		
SPI	SRMT Bit	14.	In SPI Slave mode, the SRMT bit may be set if the FIFO or Shift register is not empty.	X	X	X
ICSP™ Programming	Programming	15.	Programming in Retention Sleep.	X		
ICSP Programming	Programming	16.	Self-programming after a POR or $\overline{\text{MCLR}}$ Reset.	X		
ADC	Current	17.	ADC draws additional current when enabled.	X	X	
UART	UART Transmit	18.	Stop bit is short.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B3**).

1. Module: ADC

The following codes may be missing in 12-bit mode:

- B0 silicon: 1023, 2046, 2047, 3070 and 3071
- B2 silicon: 1022, 1023, 2046, 2047, 3070 and 3071

Work around

Use 10-bit mode if all codes are desired in the application.

Affected Silicon Revisions

B0	B2	B3					
X	X	X					

2. Module: ADC

The ADC result of the 32-bit signed format option (FORM[2:0] bits = `b101`) is the same as the result of the 16-bit signed format option (FORM[2:0] = `b001`).

Work around

In the software, expand the Data Output Format bits to convert the output format from 16-bit signed integer to 32-bit signed integer.

Affected Silicon Revisions

B0	B2	B3					
X	X	X					

3. Module: Reset

$\overline{\text{MCLR}}$ is not a source of wake-up from Retention Sleep mode. Reprogramming the device may not work when the device is in Retention Sleep.

Work around

Use other wake-up sources (such as an external interrupt or Change Notification interrupt) or implement other means in the application to prevent entering into Retention Sleep mode during programming.

Affected Silicon Revisions

B0	B2	B3					
X							

4. Module: UART

The receive buffer overflow disable feature, controlled by the OVFDIS bit, is not functional.

Work around

None.

Affected Silicon Revisions

B0	B2	B3					
X							

5. Module: Primary XT and HS Oscillator (POSC)

The Primary Oscillator Start-up Timer (OST) may indicate the oscillator is ready for use and set the POSCRDY bit (CLKSTAT[2]) too early. Clocking the device before the oscillator is ready may result in incorrect execution and exceptions. This issue exists when the POSC is requested at power-on, during clock switching, when waking from Sleep or when a peripheral module requests the POSC directly. This issue affects XT and HS modes only.

Work around

Make sure that the Primary Oscillator clock is ready before using it by following these steps:

1. Running on a non-POSC source, request the POSC clock using a peripheral such as REFO.
2. Provide a delay to stabilize POSC.
3. Switch to the POSC source.

Example 1 shows a work around for the device power-on and Example 2 explains the work around when the device wakes from Sleep.

EXAMPLE 1: USING POSC AT POWER-ON

```
#pragma  config FNOSC = FRCDIV           // Oscillator Selection bits (Fast RC oscillator (FRC))
// Clock Switching Enabled (Failsafe Clock Monitor can be enabled or disabled)
#pragma  config FCKSM = CSECMD
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
void main()
{
    // configure REFO to request POSC
    REFO1CONbits.ROSEL = 2;              // POSC = 2
    REFO1CONbits.OE = 0;                 // disable output
    REFO1CONbits.ON = 1;                 // enable module

    // wait for POSC stable clock
    // this delay may vary depending on different application conditions
    // such as voltage, temperature, layout, XT or HS mode and components
    {                                    // delay for 9 ms
        unsigned int start = __builtin_mfc0(_CP0_COUNT, _CP0_COUNT_SELECT);
while((__builtin_mfc0(_CP0_COUNT, _CP0_COUNT_SELECT)) - start < (unsigned int)(0.009*8000000/2));
    }

    // unlock OSCCON
    SYSKEY = 0;
    SYSKEY = 0xAA996655;
    SYSKEY = 0x556699AA;
    // switch to POSC = 2
    OSCCONCLR = _OSCCON_NOSC_MASK | _OSCCON_CLKLOCK_MASK | _OSCCON_OSWEN_MASK;
    OSCCONSET = (2<<_OSCCON_NOSC_POSITION) | _OSCCON_OSWEN_MASK;
    while(OSCCONbits.OSWEN == 1);        // wait for switch
```

EXAMPLE 2: USING POSC WHEN WAKING FROM SLEEP

```
    // Clock Switching Enabled (Failsafe Clock Monitor can be enabled or disabled)
    #pragma config FCKSM = CSECMD
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
    // unlock OSCCON
    SYSKEY = 0;
    SYSKEY = 0xAA996655;
    SYSKEY = 0x556699AA;
    // switch to FRC = 0 before entering to sleep
    OSCCONCLR = _OSCCON_NOSC_MASK | _OSCCON_CLKLOCK_MASK | _OSCCON_OSWEN_MASK;
    OSCCONSET = (0<<_OSCCON_NOSC_POSITION) | _OSCCON_OSWEN_MASK;
    while(OSCCONbits.OSWEN == 1);                // wait for switch

    // enter sleep mode
    asm      volatile("wait");

    // configure REFO to request POSC
    REFO1CONbits.ROSEL = 2;                      // POSC = 2
    REFO1CONbits.OE = 0;                         // disable output
    REFO1CONbits.ON = 1;                         // enable module

    // wait for POSC stable clock
    // this delay may vary depending on different application conditions
    // such as voltage, temperature, layout, XT or HS mode and components
    {                                            // delay for 9 ms
        unsigned  int start = __builtin_mfc0(_CP0_COUNT, _CP0_COUNT_SELECT);
while((__builtin_mfc0(_CP0_COUNT, _CP0_COUNT_SELECT)) - start < (unsigned int)(0.009*8000000/2));
    }

    // switch to POSC = 2
    OSCCONCLR = _OSCCON_NOSC_MASK | _OSCCON_CLKLOCK_MASK | _OSCCON_OSWEN_MASK;
    OSCCONSET = (2<<_OSCCON_NOSC_POSITION) | _OSCCON_OSWEN_MASK;
    while(OSCCONbits.OSWEN == 1);                // wait for switch
```

Affected Silicon Revisions

B0	B2	B3					
X	X	X					

6. Module: Reset

When Master Clear ($\overline{MCLR}$) is asserted, the current consumption is higher than the Reset IPD specification.

Work around

Do not use $\overline{MCLR}$ to hold the device in Reset to save power.

Affected Silicon Revisions

B0	B2	B3					
X	X	X					

7. Module: Reset

An erroneous Configuration Mismatch Reset (CMR) event may occur after a POR, BOR or external device programming (ICSP™ or JTAG). This event will cause a device POR Reset and set the CMR bit in the RCON register.

Work around

Clear the CMR bit in the RCON register.

Affected Silicon Revisions

B0	B2	B3					
X							

8. Module: Timer1

Timer1 does not overflow in External Clock mode when PR1 = 1 and the prescaler is 1:1.

Work around

Use a PR1 value greater than one.

Affected Silicon Revisions

B0	B2	B3					
X	X	X					

9. Module: Timer1

The first increment value is not visible when using External Clock mode and a 1:1 prescaler.

Work around

None.

Affected Silicon Revisions

B0	B2	B3					
X	X	X					

10. Module: Power

When the device wakes up from Retention Sleep mode, a device Reset may occur. The BOR, POR and EXTR bits in the RCON register are set for this Reset.

Work around

To provide a consistent behavior when the device wakes up from the Retention Sleep mode, the software Reset sequence should be performed following the `WAIT` instruction (refer to Example 3). In this case, a Reset will always be generated when the device wakes up from Retention Sleep.

EXAMPLE 3: SOFTWARE RESET CODE EXAMPLE

```
unsigned int dummy;
SYSKEY = 0x00000000;          // write invalid key to force lock
SYSKEY = 0xAA996655;          // write key1 to SYSKEY
SYSKEY = 0x556699AA;          // write key2 to SYSKEY
RSWRSTSET = 1;                // set SWRST bit to arm reset
dummy = RSWRST;               // read RSWRST register to trigger reset
while(1);                     // prevent any unwanted code execution until reset occurs
```

Affected Silicon Revisions

B0	B2	B3					
X							

11. Module: Power

The main BOR may not occur when the operating voltage drops below the BOR trip voltage.

Work around

Ensure the device operating voltage does not violate the specified values.

Use an external supervisor circuit to reset the device if the operating voltage can be outside the specified values.

Affected Silicon Revisions

B0	B2	B3					
X							

12. Module: Programming

The JTAG TDO (RB10) pin toggles during programming when using the ICSP™ pairs.

Work around

For 20-pin devices: Do not connect external circuitry to the TDO pin (RB12) that cannot tolerate toggling when programming using the PGEC1/PGED1, PGEC2/PGED2 or PGEC3/PGED3 pins.

For 28-pin, 36-pin and 40-pin devices: Do not connect external circuitry to the TDO pin (RB10) that cannot tolerate toggling when programming using the PGEC1/PGED1 or PGEC3/PGED3 pins.

Affected Silicon Revisions

B0	B2	B3					
X							

13. Module: I/O

If the input signal rise or fall time is more than 500 nS, the I/O Schmitt Trigger output may have glitches.

Work around

The rise/fall time of the input signal must be less than 500 nS.

Affected Silicon Revisions

B0	B2	B3					
X							

14. Module: SPI

In SPI Slave mode, the SRMT bit may be set if the FIFO or Shift register is not empty.

Work around

The following work arounds can be implemented in the application to detect when the FIFO and Shift register are empty:

1. Check the SPITBF bit before checking the SRMT bit. If the SPITBF flag is cleared and the SRMT flag is set, then all data were transmitted. Example 4 demonstrates the SPITBF and SRMT bits polling.
2. Read the SRMT bit twice, back-to-back. If the SRMT bit is set two reads in a row, then the FIFO and Shift register are empty. Example 5 demonstrates the SRMT bit polling using double read.

EXAMPLE 4: EMPTY STATUS DETECTION USING SPITBF AND SRMT BITS POLLING

```
// Both flags must indicate empty status.
while(SPI1STATLbits.SPITBF);
while(!SPI1STATLbits.SRMT);
```

EXAMPLE 5: EMPTY STATUS DETECTION USING SRMT BIT POLLING WITH BACK-TO-BACK READS

```
// If SRMT bit is set two reads in a row
   then it set correctly.
asm   volatile("\n\
la    $t0, SPI1STAT;\
loop:;\
lw    $t1, 0($t0);\
lw    $t2, 0($t0);\
and   $t1, $t1, $t2;\
andi  $t1, $t2, 0x80;\
beqz  $t1, loop;");
```

Affected Silicon Revisions

B0	B2	B3					
X	X	X					

15. Module: ICSP™ Programming

After a POR or $\overline{\text{MCLR}}$ Reset, the device may fail to program if Retention Sleep is invoked within 40 ms.

Work around

Provide a delay in firmware to ensure the device does not enter Retention Sleep within 40 ms of a POR or $\overline{\text{MCLR}}$ Reset.

Affected Silicon Revisions

B0	B2	B3					
X							

16. Module: ICSP Programming

After a POR or $\overline{\text{MCLR}}$ Reset, the device may fail to program using ICSP if user firmware performs self-programming within 40 ms.

Work around

Provide a delay in firmware to ensure the device does not perform self-programming within 40 ms of a POR or $\overline{\text{MCLR}}$ Reset.

Affected Silicon Revisions

B0	B2	B3					
X							

17. Module: ADC

On some devices, the current draw may increase by up to 12 mA when the ADC is enabled. This current draw is not affected by the device Power Save modes or ADC configuration. This additional current does not affect the ADC or device performance.

Work around

Disable the ADC when it is not converting or not used in the application.

Affected Silicon Revisions

B0	B2	B3					
X	X						

18. Module: UART

The Stop bit of the transmitted data is short when data are being transmitted and data are in the TX FIFO. In BRGH = 0 mode, the Stop bit is 1/16 bit time short. In BRGH = 1 mode, the Stop bit is 1/4 bit time short.

Work around

- Add a software delay of 1/16 or 1/4 bit time (based on the BRGH setting) between writes to the TX FIFO, allowing the transmission to complete before sending the next character.
- Use a separate UART for transmit and receive. Configure the transmit UART for two Stop bits. The FIFO can be used; the combination of the first and second Stop bits will provide a Stop bit and a line idle.
- Use a timer to generate an interrupt slightly longer than the time to send a byte (1/baud rate * 10) and in the ISR, write a byte to the TX buffer.

Affected Silicon Revisions

B0	B2	B3					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001324**C**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (4/2016)

Initial release of this document; issued for silicon revision B0.

Rev B Document (6/2016)

Corrected the codes in silicon issue 2 (ADC).

Added silicon issue 5 (Primary XT and HS Oscillator (POSC)).

Rev C Document (4/2017)

Updated Table 2.

Added silicon issues 6 (Reset), 7 (Reset), 8 (Timer1), 9 (Timer1), 10 (Power), 11 (Power), 12 (Programming), 13 (I/O) and 14 (SPI).

Rev D Document (4/2018)

Added silicon revision B2.

Updated silicon issue 1 (ADC).

Added silicon issues 15 (ICSP™ Programming) and 16 (ICSP Programming).

Rev E Document (11/2018)

Added silicon issue 17 (ADC).

Rev F Document (3/2019)

Added silicon revision B3.

Added silicon issue 18 (UART).

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
═ ISO/TS 16949 ═

Trademarks

ISBN: 978-1-5224-4286-8

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-67-3636

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820