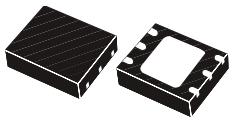
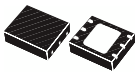
LD39050

500 mA low quiescent current and low noise voltage regulator

Datasheet - production data



DFN6 (3x3 mm)



DFN6 (2x2 mm)

Features

- Input voltage from 1.5 to 5.5 V
- Ultra low-dropout voltage (200 mV typ. at 500 mA load)
- Very low quiescent current (20 µA typ. at no load, 100 µA typ. at 500 mA load, 1 µA max. in OFF mode)
- Very low noise without bypass capacitor
- Output voltage tolerance: ± 2.0% @ 25 °C
- 500 mA guaranteed output current
- Wide range of output voltages available on request: 0.8 V to 4.5 V with 100 mV step and adjustable from 0.8 V
- Logic-controlled electronic shutdown
- Compatible with ceramic capacitor C_{OUT} = 1 µF
- Internal current and thermal limit
- Package DFN6 (3x3 mm) and DFN6 (2x2 mm)
- Temperature range: from -40 °C to 125 °C

Description

The LD39050 provides 500 mA maximum current with an input voltage range from 1.5 V to 5.5 V and a typical dropout voltage of 200 mV. Stability is given by ceramic capacitors. The ultra low drop voltage, low quiescent current and low noise features make it suitable for low power battery-powered applications. Power supply rejection is 65 dB at low frequencies and starts to roll off at 10 kHz. The enable logic control function puts the LD39050 in shutdown mode allowing a total current consumption lower than 1 µA. The device also includes short-circuit constant current limiting and thermal protection. Typical applications are mobile phones, hard disks and battery-powered systems.

This is information on a product in full production. www.st.com

Contents

1 **Diagrams** 3

2 **Pin configuration** 4

3 **Maximum ratings** 6

4 **Electrical characteristics** 7

5 **Typical performance characteristics** 11

6 **Application information** 16

6.1 Power dissipation 17

6.2 Enable function 18

6.3 Power Good function 18

7 **Package information** 19

7.1 DFN6 (3x3 mm) package information 20

7.2 DFN6 (3x3 mm) packing information 22

7.3 DFN6 (2x2 mm) package information 24

8 **Ordering information** 26

9 **Revision history** 27

1 Diagrams

Figure 1. Schematic diagram for the LD39050 (adjustable)

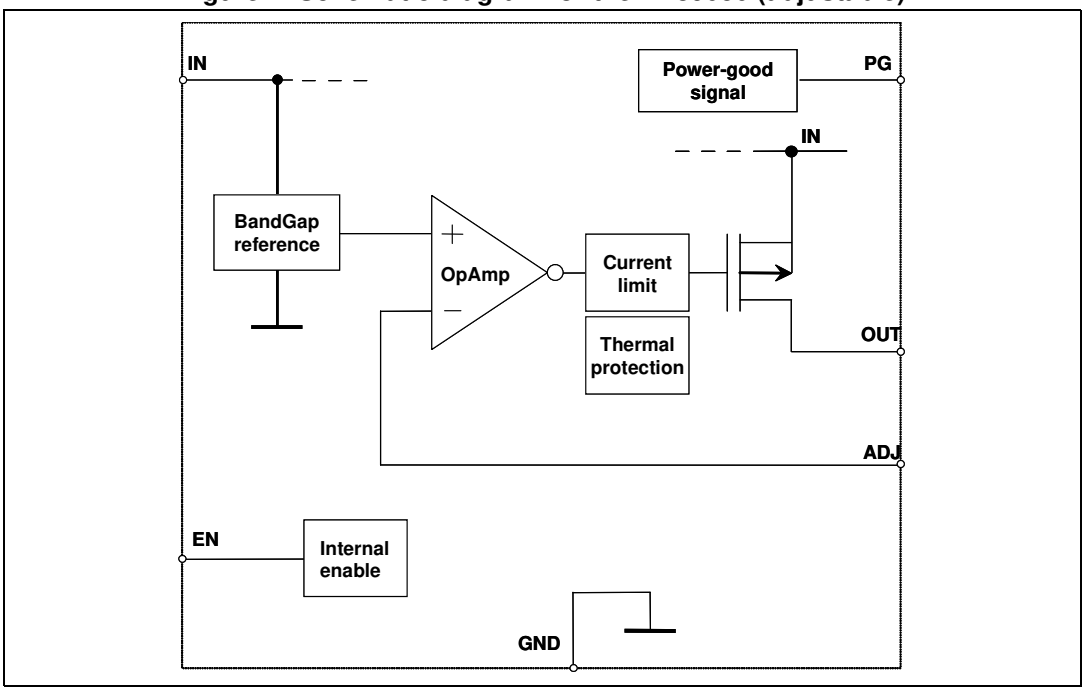
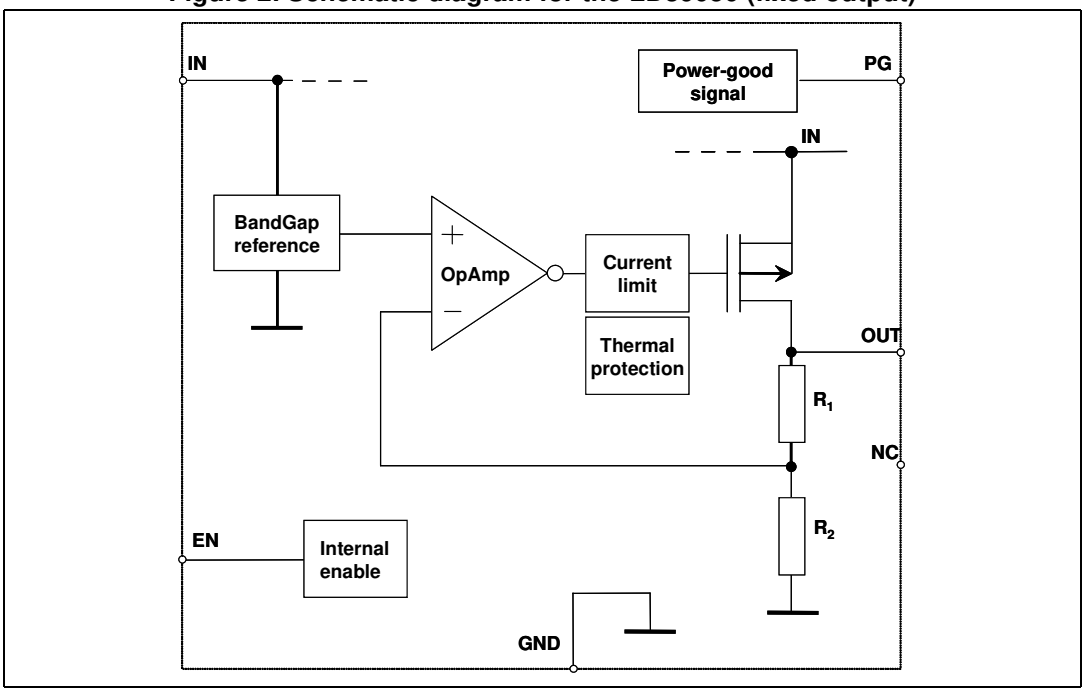


Figure 2. Schematic diagram for the LD39050 (fixed output)



2 Pin configuration

Figure 3. DFN6 (3x3 mm) pin connection (top view)

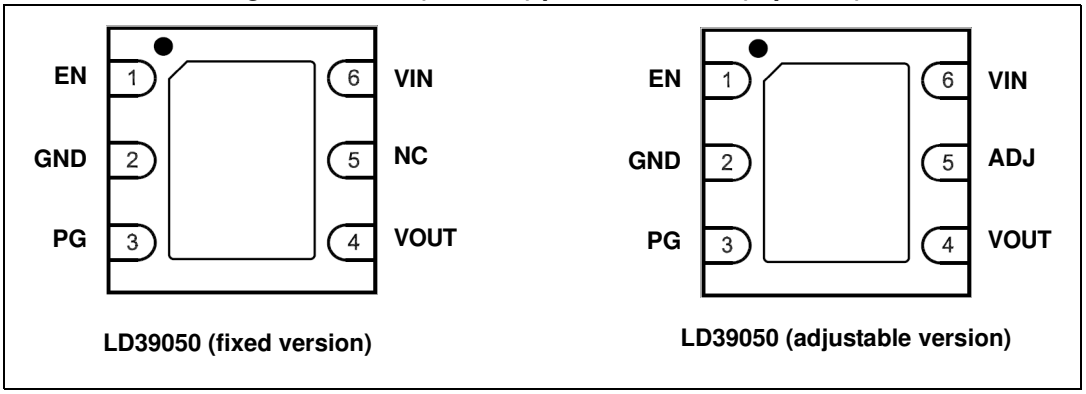


Figure 4. DFN6 (2x2 mm) pin connection (top view)

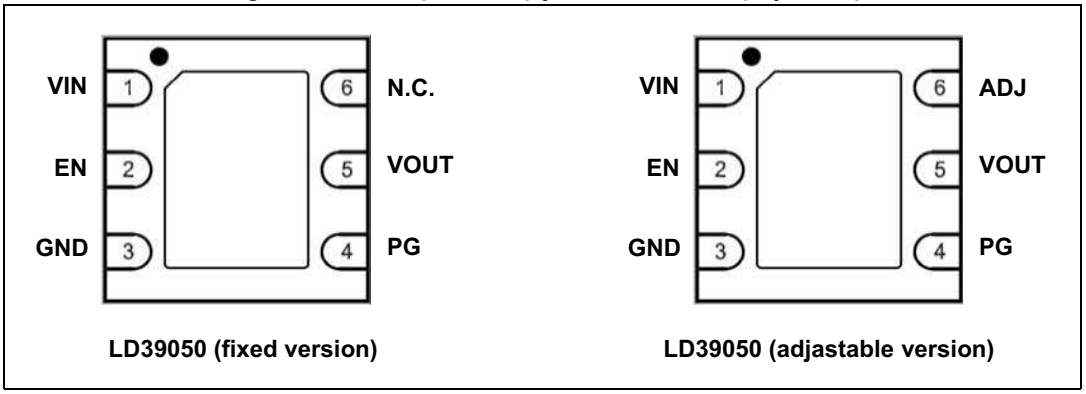


Table 1. Pin description

Symbol	Pin n° for DFN6 (3x3 mm)		Pin n° for DFN6 (2x2 mm)		Function
	LD39050 (adjustable)	LD39050 (fixed)	LD39050 (adjustable)	LD39050 (fixed)	
EN	1	1	2	2	Enable pin logic input: low = shutdown, high = active
GND	2	2	3	3	Common ground
PG	3	3	4	4	Power Good
VOUT	4	4	5	5	Output voltage
ADJ	5	-	6	-	Adjustable pin
VIN	6	6	1	1	Input voltage of the LDO
N.C.	-	5	-	6	Not connected
GND	Exposed pad		Exposed pad		Exposed pad must be connected to GND

3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	DC input voltage	-0.3 to 7	V
V_{OUT}	DC output voltage	-0.3 to V_I + 0.3 (7 V max.)	V
EN	Enable pin	-0.3 to V_I + 0.3 (7 V max.)	V
PG	Power Good pin	-0.3 to 7	V
ADJ	Adjustable pin	4	V
I_{OUT}	Output current	Internally limited	
P_D	Power dissipation	Internally limited	
T_{STG}	Storage temperature range	- 65 to 150	°C
T_{OP}	Operating junction temperature range	- 40 to 125	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		DFN6 (2x2 mm)	DFN6 (3x3 mm)	
R_{thJA}	Thermal resistance junction-ambient	65	55	°C/W
R_{thJC}	Thermal resistance junction-case	6.5	10	°C/W

Table 4. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	2	kV
		CDM	500	V
		MM	0.3	kV

4 Electrical characteristics

T_J = 25 °C, V_{IN} = 1.8 V, C_{IN} = C_{OUT} = 1 µF, I_{OUT} = 10 mA, V_{EN} = V_{IN}, unless otherwise specified.

Table 5. Electrical characteristics for the LD39050 (adjustable)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		1.5		5.5	V
V_{ADJ}	V_{ADJ} accuracy	I_{OUT} = 10 mA, T_J = 25 °C	784	800	816	mV
		I_{OUT} = 10 mA, -40 °C < T_J < 125 °C	776	800	824	
I_{ADJ}	Adjustable pin current				1	µA
ΔV_{OUT}	Static line regulation	V_{OUT} +1 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 1 mA		0.01		%/V
ΔV_{OUT}	Transient line regulation(1)	ΔV_{IN} = 500 mV, I_{OUT} = 10 mA, t_R = 5 µs		10		mVpp
		ΔV_{IN} = 500 mV, I_{OUT} = 10 mA, t_F = 5 µs		10		
ΔV_{OUT}	Static load regulation	I_{OUT} = 10 mA to 500 mA		0.002		%/mA
ΔV_{OUT}	Transient load regulation(1)	I_{OUT} = 10 mA to 500 mA, t_R = 5 µs		40		mVpp
		I_{OUT} = 10 mA to 500 mA, t_F = 5 µs		40		
V_{DROP}	Dropout voltage(2)	I_O = 500 mA, V_{OUT} fixed to 1.5 V 40 °C < T_J < 125 °C		200	400	mV
e_N	Output noise voltage	10 Hz to 100 kHz, I_{OUT} = 100 mA, V_{OUT} = 0.8 V		30		μV_{RMS}
SVR	Supply voltage rejection V_{OUT} = 0.8 V	V_{IN} = 1.8 V+/-V_{RIPPLE} V_{RIPPLE} = 0.25 V, frequency = 1 kHz I_{OUT} = 10 mA		65		dB
		V_{IN} = 1.8 V+/-V_{RIPPLE} V_{RIPPLE} = 0.25 V, frequency =10 kHz I_{OUT} = 100 mA		62		
I_Q	Quiescent current	I_{OUT} = 0 mA		20		µA
		I_{OUT} = 0 mA, -40 °C < T_J < 125 °C			50	
		I_{OUT} = 0 to 500 mA		100		
		I_{OUT} = 0 to 500 mA, -40 °C<T_J<125 °C			200	
		V_{IN} input current in OFF mode: V_{EN} = GND(3)		0.001	1	

Table 5. Electrical characteristics for the LD39050 (adjustable) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
PG	Power Good output threshold	Rising edge		0.92* V_{OUT}		V
		Falling edge		0.8* V_{OUT}		
	Power Good output voltage low	I_{sink} = 6 mA open drain output			0.4	V
I_{SC}	Short-circuit current	R_L= 0	600	800		mA
V_{EN}	Enable input logic low	V_{IN} = 1.5 V to 5.5 V, 40 °C < T_J < 125 °C			0.4	V
	Enable input logic high	V_{IN} = 1.5 V to 5.5 V, 40 °C < T_J < 125 °C	0.9			V
I_{EN}	Enable pin input current	V_{EN} = V_{IN}		0.1	100	nA
t_{ON}	Turn-on time (4)			30		µs
T_{SHDN}	Thermal shutdown			160		°C
	Hysteresis			20		
C_{OUT}	Output capacitor	Capacitance (see typical performance characteristics for stability)	1		22	µF

1. All transient values are guaranteed by design, not production tested
2. Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply to output voltages below 1.5 V
3. PG pin floating
4. Turn-on time is time measured between the enable input just exceeding V_{EN} high value and the output voltage just reaching 95% of its nominal value

T_J = 25 °C, V_{IN} = $V_{OUT(NOM)}$ + 1 V, C_{IN} = C_{OUT} = 1 µF, I_{OUT} = 10 mA, V_{EN} = V_{IN}, unless otherwise specified.

Table 6. Electrical characteristics for the LD39050 (fixed output)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		1.5		5.5	V
V_{OUT}	V_{OUT} accuracy	V_{OUT} >1.5 V, I_{OUT} = 10 mA, T_J = 25 °C	-2.0		2.0	%
		V_{OUT} >1.5 V, I_{OUT} = 10 mA, -40 °C<T_J<125 °C	-3.0		3.0	
		V_{OUT} ≤ 1.5 V, I_{OUT} = 10 mA		± 20		mV
		V_{OUT} ≤ 1.5 V, I_{OUT} = 10 mA, -40 °C<T_J<125 °C		± 30		
ΔV_{OUT}	Static line regulation	V_{OUT} +1 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 1 mA		0.01		%/V
ΔV_{OUT}	Transient line regulation (1)	ΔV_{IN} = 500 mV, I_{OUT} = 10 mA, t_R = 5 µs		10		mVpp
		ΔV_{IN} = 500 mV, I_{OUT} = 10 mA, t_F = 5 µs		10		
ΔV_{OUT}	Static load regulation	I_{OUT} = 10 mA to 500 mA		0.002		%/mA
ΔV_{OUT}	Transient load regulation (1)	I_{OUT} = 10 mA to 500 mA, t_R = 5 µs		40		mVpp
		I_{OUT} = 10 mA to 500 mA, t_F = 5 µs		40		
V_{DROP}	Dropout voltage (2)	I_{OUT} = 500 mA, V_{OUT} > 1.5 V -40 °C < T_J < 125 °C		200	400	mV
e_N	Output noise voltage	10 Hz to 100 kHz, I_O = 100 mA,		30		μV_{RMS}
SVR	Supply voltage rejection V_{OUT} = 1.5 V	V_{IN} = $V_{OUT(NOM)}$) + 0.5 V+/-V_{RIPPLE} V_{RIPPLE} = 0.1 V, freq. = 1 kHz I_{OUT} = 10 mA		65		dB
		V_{IN} = $V_{OUT(NOM)}$+ 0.5 V+/- V_{RIPPLE} V_{RIPPLE} = 0.1 V, frequency =10 kHz I_{OUT} = 100 mA		62		
I_Q	Quiescent current	I_{OUT} = 0 mA		20		µA
		I_{OUT} = 0 mA, -40 °C < T_J< 125 °C			50	
		I_{OUT} = 0 to 500 mA		100		
		I_{OUT} = 0 to 500 mA -40 °C < T_J < 125 °C			200	
		V_{IN} input current in OFF mode: V_{EN} = GND(3)		0.001	1	

Table 6. Electrical characteristics for the LD39050 (fixed output) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
PG	Power Good output threshold	Rising edge		0.92* V_{OUT}		V
		Falling edge		0.8* V_{OUT}		
	Power Good output voltage low	I_{sink} = 6 mA open drain output			0.4	V
I_{SC}	Short-circuit current	R_L = 0	600	800		mA
V_{EN}	Enable input logic low	V_{IN} = 1.5 V to 5.5 V, - 40 °C < T_J < 125 °C			0.4	V
	Enable input logic high	V_{IN} = 1.5 V to 5.5 V, -40 °C < T_J < 125 °C	0.9			V
I_{EN}	Enable pin input current	V_{EN} = V_{IN}		0.1	100	nA
t_{ON}	Turn-on time (4)			30		µs
T_{SHDN}	Thermal shutdown			160		°C
	Hysteresis			20		
C_{OUT}	Output capacitor	Capacitance (see typical performance characteristics for stability)	1		22	µF

1. All transient values are guaranteed by design, not production tested
2. Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply to output voltages below 1.5 V
3. PG pin floating
4. Turn-on time is time measured between the enable input just exceeding V_{EN} high value and the output voltage just reaching 95% of its nominal value

5 Typical performance characteristics

Figure 5. V_{ADJ} accuracy

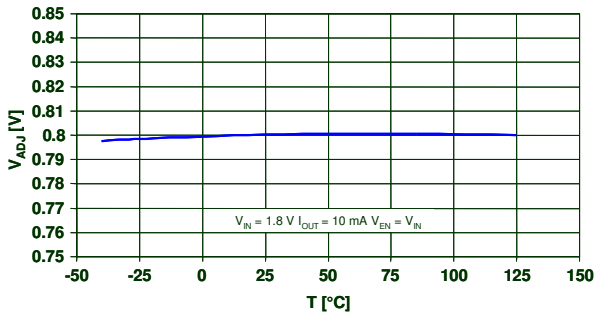


Figure 6. V_{OUT} accuracy

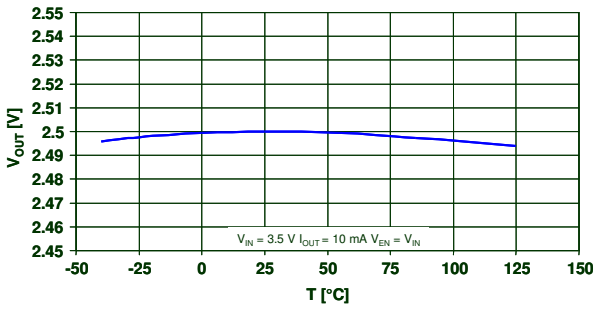


Figure 7. Dropout voltage vs. temperature (V_{OUT} = 1.5 V)

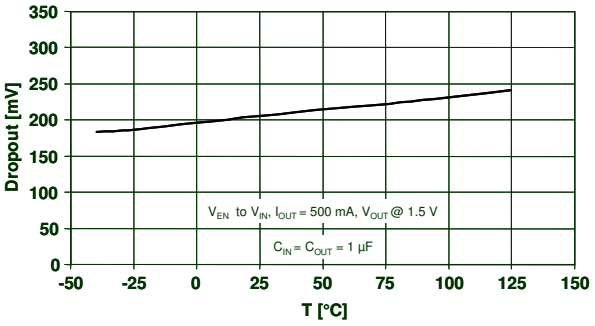


Figure 8. Dropout voltage vs. temperature (V_{OUT} = 2.5 V)

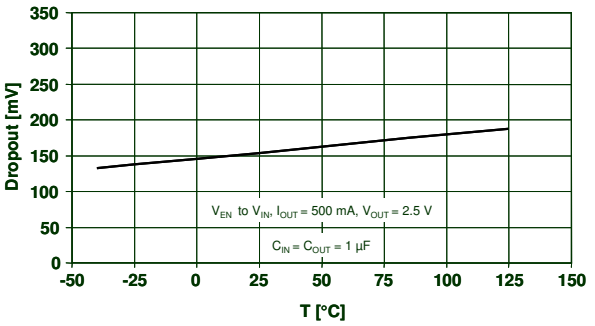


Figure 9. Dropout voltage vs. output current

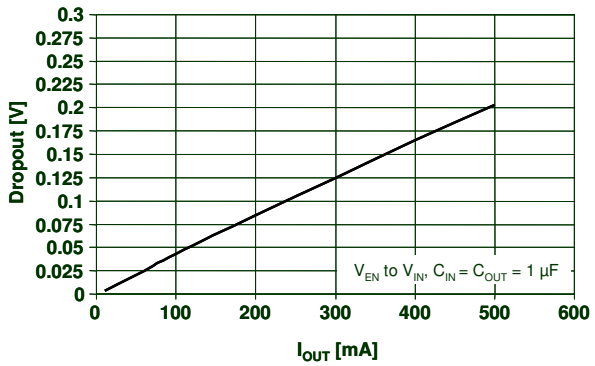


Figure 10. Short-circuit current vs. dropout voltage

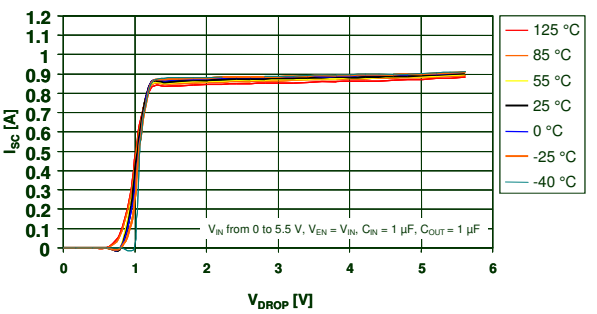


Figure 11. Output voltage vs. input voltage

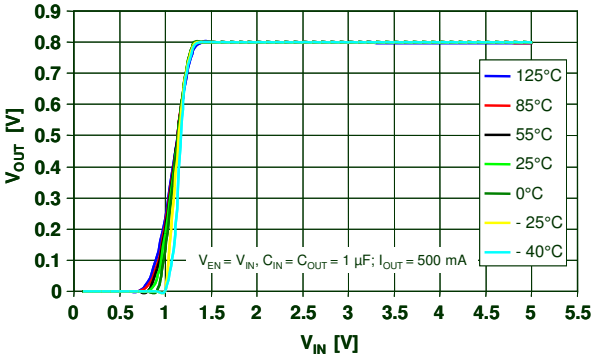


Figure 12. Quiescent current vs. temperature (V_{OUT} = 0.8 V)

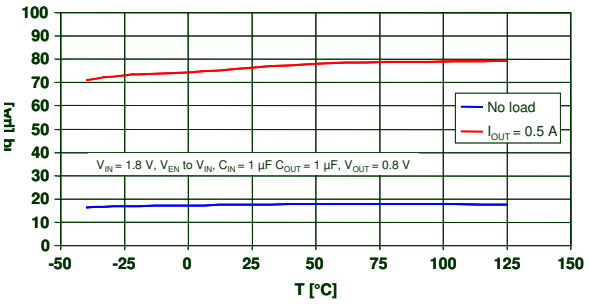


Figure 13. Quiescent current vs. temperature (V_{OUT} = 2.5 V)

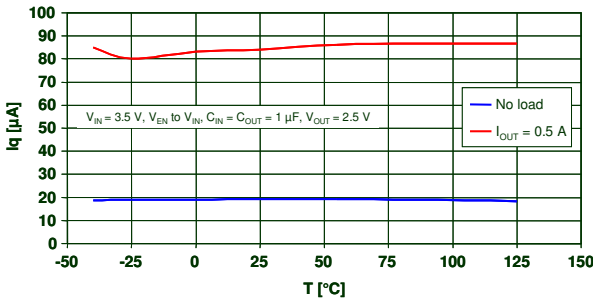


Figure 14. Quiescent current in OFF mode vs. temperature

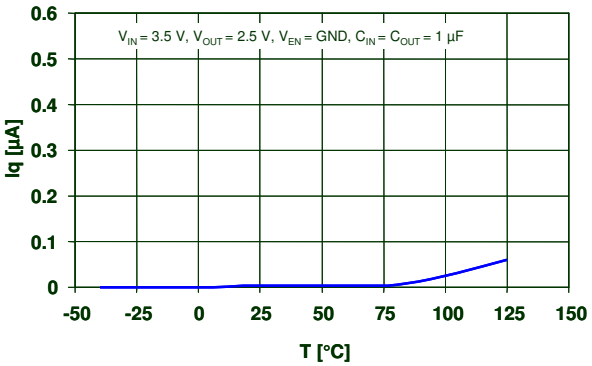


Figure 15. Load regulation

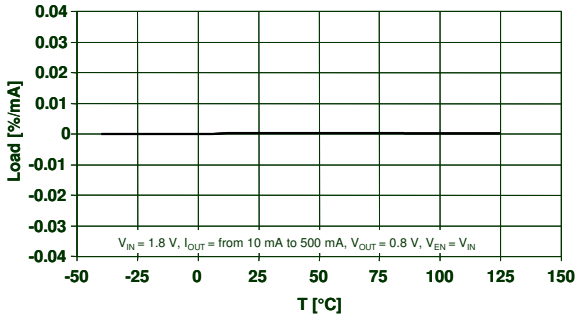


Figure 16. Line regulation (V_{OUT} = 0.8 V)

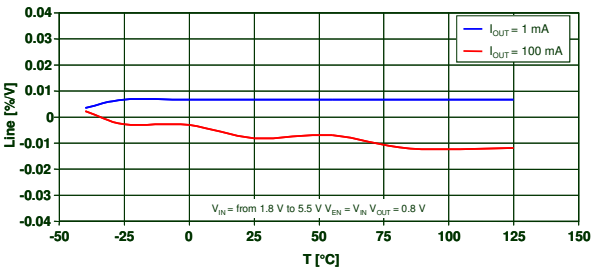


Figure 17. Line regulation (V_{OUT} = 2.5 V)

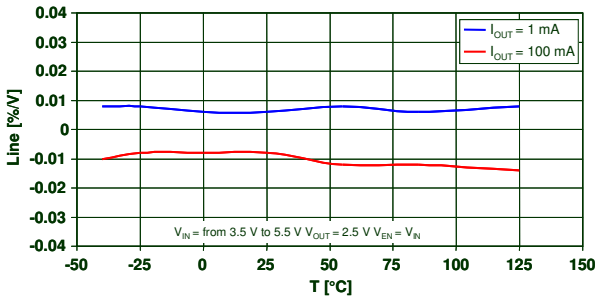


Figure 18. Supply voltage rejection vs. temperature (V_{OUT} = 0.8 V, f = 1 kHz)

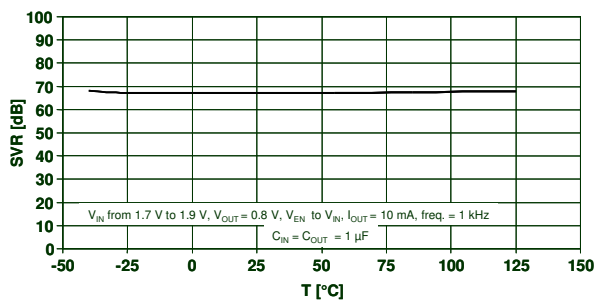


Figure 19. Supply voltage rejection vs. temperature (V_{OUT} = 0.8 V, f = 10 kHz)

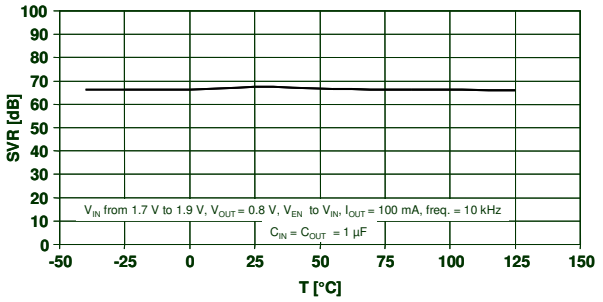


Figure 20. Supply voltage rejection vs. temperature (V_{OUT} = 2.5 V, f = 1 kHz)

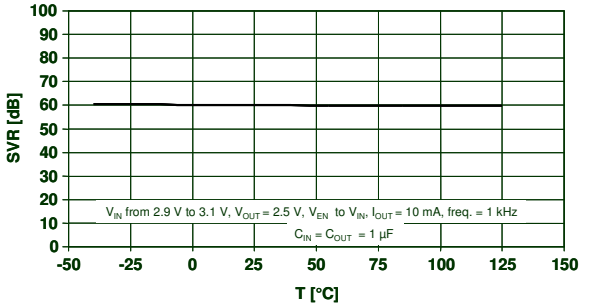


Figure 21. Supply voltage rejection vs. temperature (V_{OUT} = 2.5 V, f = 10 kHz)

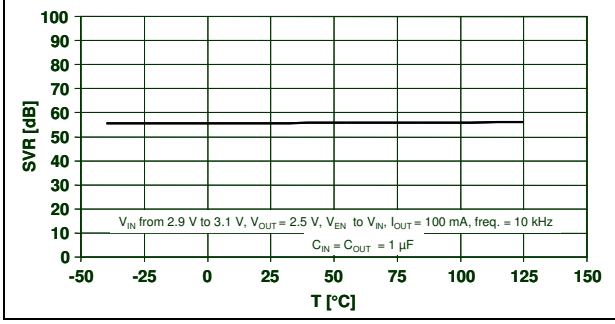


Figure 22. Supply voltage rejection vs. frequency (V_{OUT} = 0.8 V)

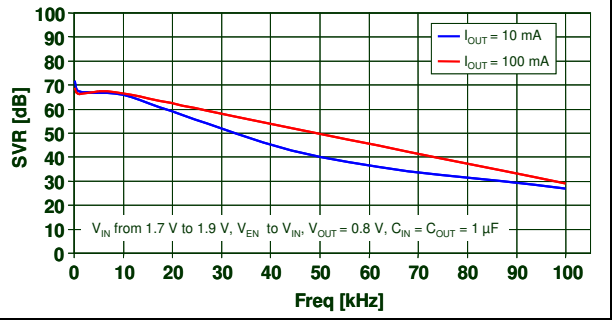


Figure 23. Supply voltage rejection vs. frequency (V_{OUT} = 2.5 V)

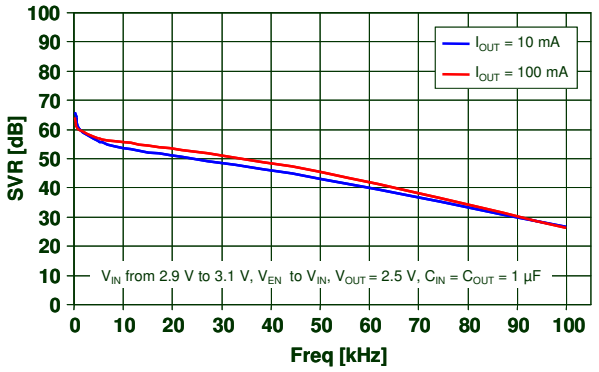
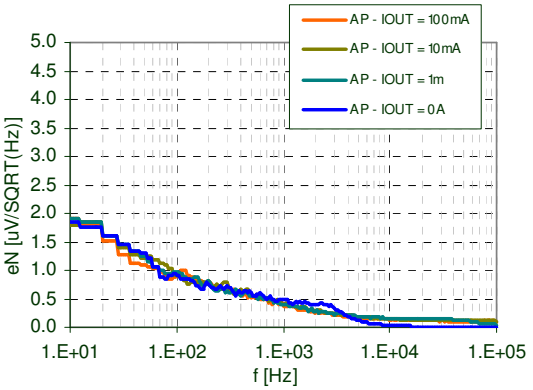


Figure 24. Noise output voltage vs. frequency



V_{IN} = 1.8 V, V_{OUT} = 0.8 V, V_{EN} = 1 V, C_{IN} = C_{OUT} = 1 µF, T_A = 25 °C

Figure 25. Enable voltage vs. temperature (V_{IN} = 3.5 V)

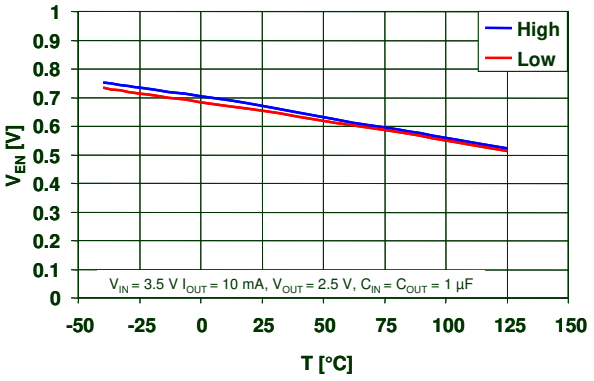


Figure 26. Enable voltage vs. temperature (V_{IN} = 5.5 V)

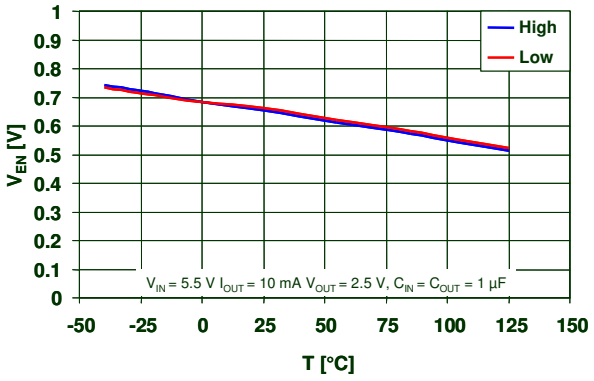
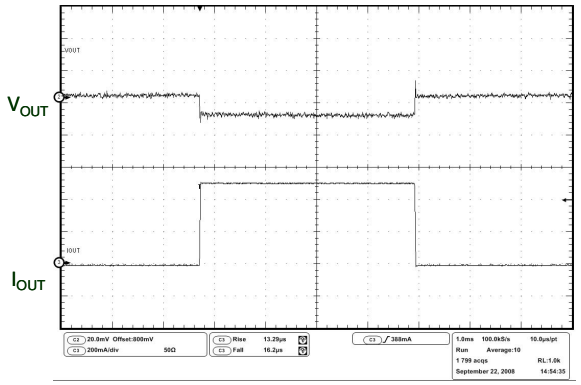
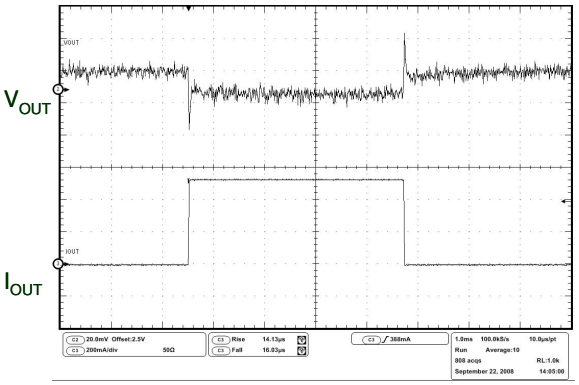


Figure 27. Load transient (V_{OUT} = 0.8 V)



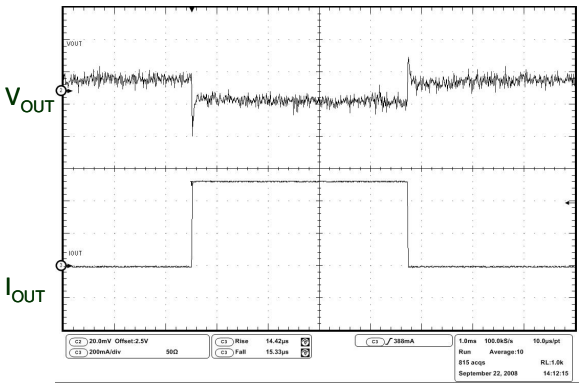
V_{EN} = V_{IN}=1.8 V, I_{OUT} = from10 mA to 0.5 A, C_{IN} = C_{OUT} = 1 µF, V_{OUT} = 0.8 V

Figure 28. Load transient (V_{OUT} = 2.5 V)



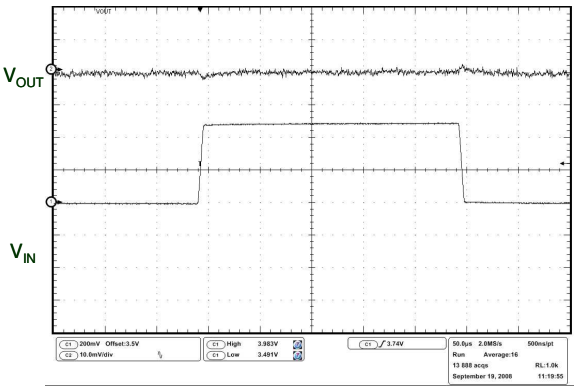
V_{EN} = V_{IN} = 3.5V, I_{OUT} from 10 mA to 0.5 A, V_{OUT} = 2.5 V, C_{IN} = C_{OUT} = 1 µF

Figure 29. Load transient (V_{OUT}=2.5 V, I_{OUT} from 0.1 A to 0.5 A)



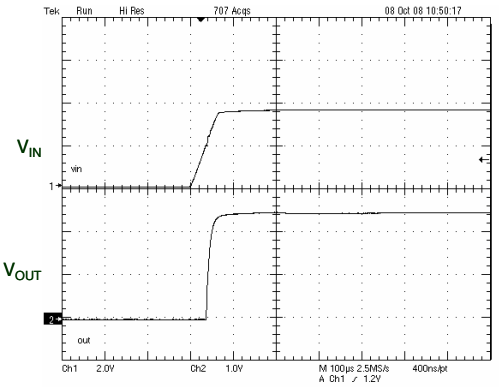
V_{EN} = V_{IN} = 3.5 V, I_{OUT} from 100 mA to 0.5 A, V_{OUT} = 2.5 V, C_{IN} = C_{OUT} = 1 µF

Figure 30. Line transient



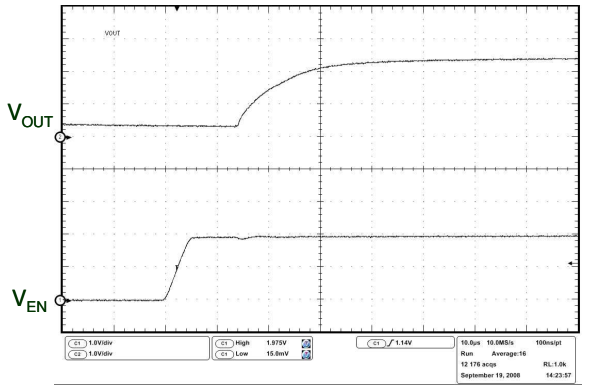
V_{EN} = V_{IN} from 4.3 V to 4.8 V, I_{OUT} = 10 mA, C_{OUT} = 1 µF, C_{IN} = NO

Figure 31. Start-up transient



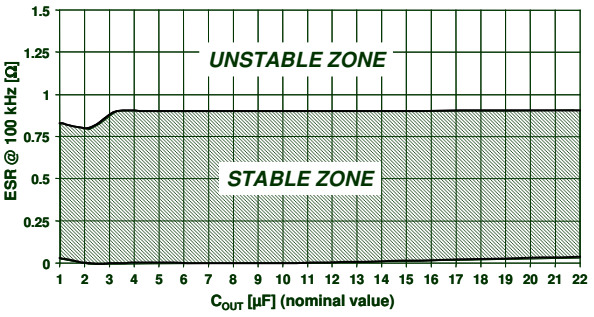
V_{EN} = V_{IN} = from 0 V to 5.5 V, I_{OUT}=10 mA, C_{IN} = C_{OUT} = 1 µF, V_{OUT} = 2.5 V

Figure 32. Enable transient



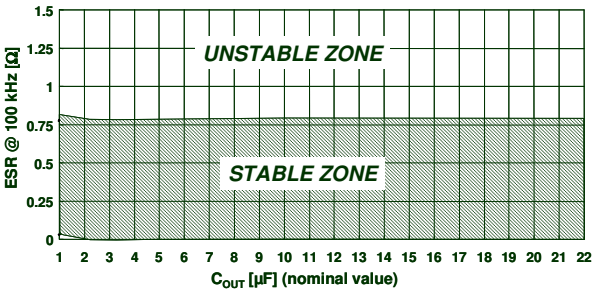
V_{EN} from 0 V to 2 V, V_{IN} = 3.5 V, V_{OUT} = 2.5 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 1µF

Figure 33. ESR required for stability with ceramic capacitors (V_{OUT} = 0.8 V)



V_{IN} = V_{EN} = from 1.8 V to 5.5 V, I_{OUT} = from 1 mA to 500 mA, V_{OUT} = 0.8 V, C_{IN} = 1 µF

Figure 34. ESR required for stability with ceramic capacitors (V_{OUT} = 2.5 V)



V_{IN} = V_{EN} = from 3.5 V to 5.5 V, I_{OUT} = from 1 mA to 500 mA, V_{OUT} = 2.5 V, C_{IN} = 1 µF

6 Application information

The LD39050 is an ultra low-dropout linear regulator. It provides up to 500 mA with a 200 mV dropout. The input voltage range is from 1.5 V to 5.5 V. The device is available in fixed and adjustable output versions.

The regulator is equipped with internal protection circuitry, such as short-circuit current limiting and thermal protection.

The regulator is designed to be stable with ceramic capacitors on the input and the output. The recommended values of the input and output ceramic capacitors are from 1 µF to 22 µF with 1 µF typical. The input capacitor must be connected within 0.5 inches of the V_{IN} terminal. The output capacitor must also be connected within 0.5 inches of output pin. There is no upper limit to the value of the input capacitor.

Figure 35 and *Figure 36* illustrate the typical application schematics:

Figure 35. Application schematic for fixed version

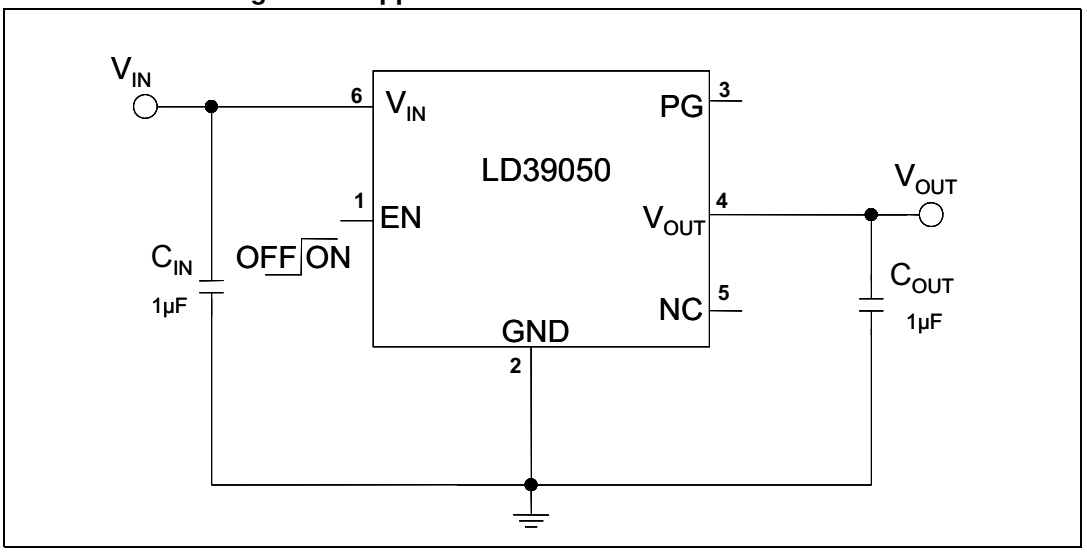
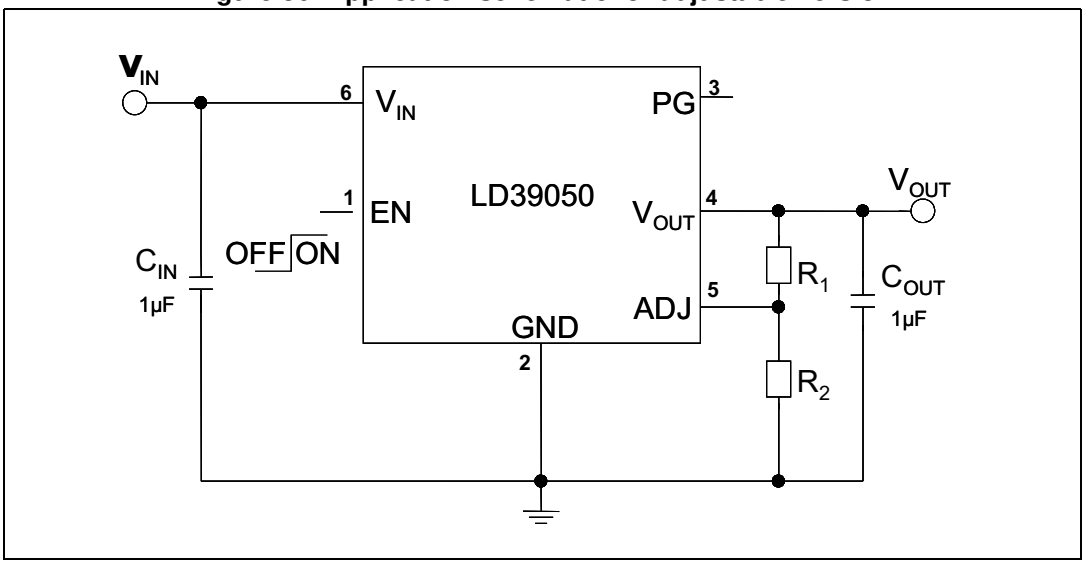


Figure 36. Application schematic for adjustable version



Regarding to the adjustable version, the output voltage can be adjusted from 0.8 V up to the input voltage minus the voltage drop across the PMOS (dropout voltage), by connecting a resistor divider between the ADJ pin and the output, thus allowing the remote voltage sensing.

The resistor divider should be selected using the following equation:

$V_{OUT} = V_{ADJ} (1 + R_1 / R_2)$ with $V_{ADJ} = 0.8$ V (typ.)

Resistors should be used with values in the range from 10 kΩ to 50 kΩ. Lower values can also be suitable, but they increase current consumption.

6.1 Power dissipation

An internal thermal feedback loop disables the output voltage if the die temperature reaches approximately 160 °C. This feature protects the device from excessive temperature and allows the user to push the limits of the power handling capability of a given board without damaging the device.

A good PC board layout should be used to maximize the power dissipation. The thermal path for the heat generated by the device goes from the die to the copper lead frame through the package leads and exposed pad to the PC board copper. The PC board copper acts as a heat sink. The footprint copper pads should be as wider as possible to spread and dissipate the heat to the surrounding ambient. Feed-through vias to inner or backside copper layers improve the overall thermal performance of the device.

The power dissipation of the device depends on the input voltage, output voltage and output current, and is given by:

$P_D = (V_{IN} - V_{OUT}) I_{OUT}$

The junction temperature of the device is:

$T_{J_MAX} = T_A + R_{thJA} \times P_D$

where:

T_{J_MAX} is the maximum junction of the die,125 °C;

T_A is the ambient temperature;

R_{thJA} is the thermal resistance junction-to-ambient.

6.2 Enable function

The LD39050 features an enable function. When the EN voltage is higher than 0.9 V the device is ON, and if it is lower than 0.4 V the device is OFF. In shutdown mode, consumption is lower than 1 µA.

The EN pin does not have an internal pull-up, therefore it cannot be left floating if it is not used.

6.3 Power Good function

Most applications require a flag showing that the output voltage is in the correct range.

The Power Good threshold depends on the adjustable voltage. When the adjustable voltage is higher than $0.92*V_{ADJ}$, the Power Good (PG) pin goes to high impedance. If it is below $0.80*V_{ADJ}$ the PG pin goes to low impedance. If the device is working well, the PG pin is at high impedance. If the output voltage is fixed using an external or internal resistor divider, the Power Good threshold is $0.92*V_{OUT}$.

The use of the Power Good function requires an external pull-up resistor, which must be connected between the PG pin and V_{IN} or V_{OUT}. The typical current capability of the PG pin is up to 6 mA. The use of a pull-up resistor for PG in the range from 100 kΩ to 1 MΩ is recommended. If the Power Good function is not used, the PG pin must remain floating.

When EN pin is in low state the power good is asserted to the high state.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com.
ECOPACK is an ST trademark.

7.1 DFN6 (3x3 mm) package information

Figure 37. DFN6 (3x3 mm) package outline

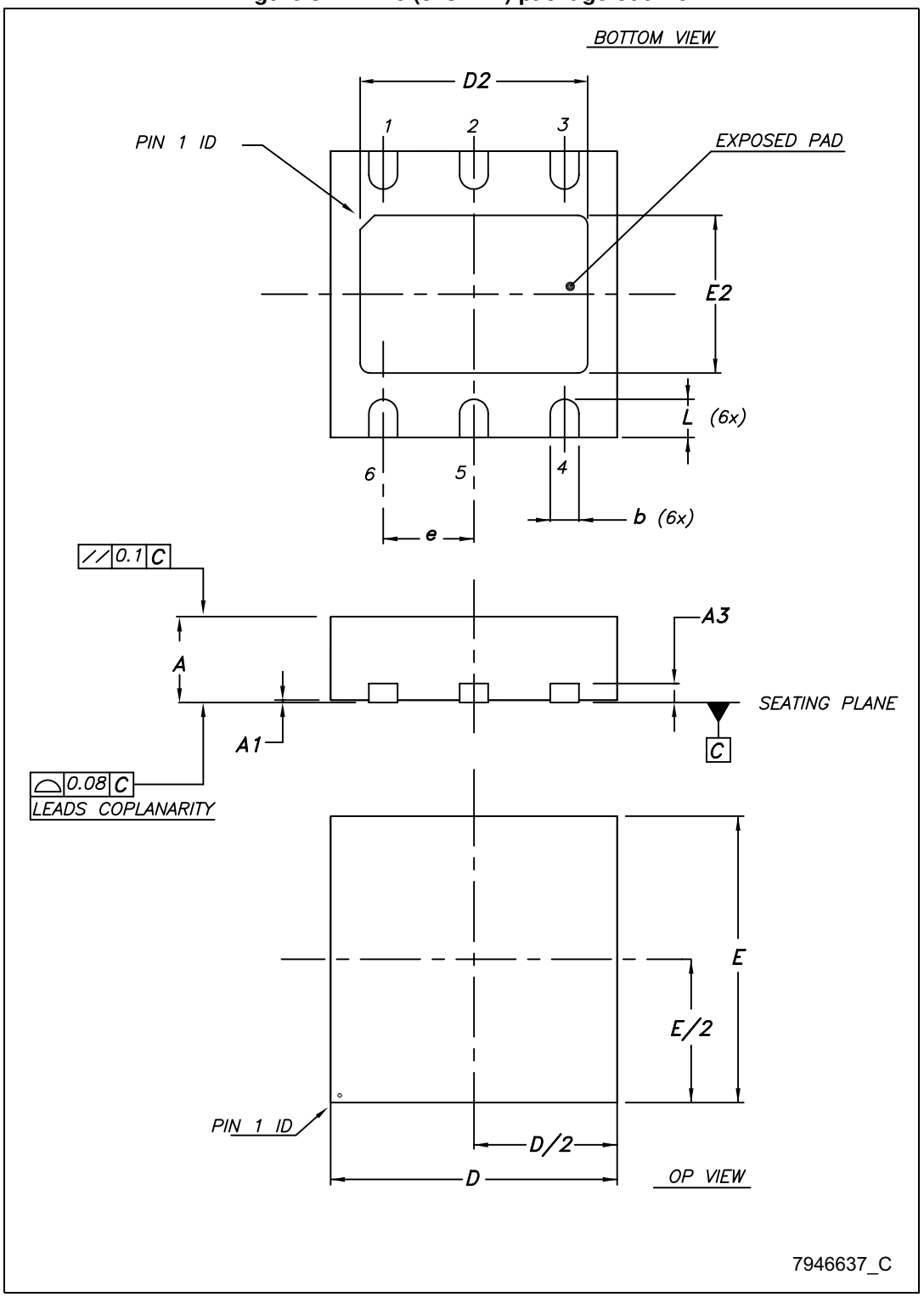
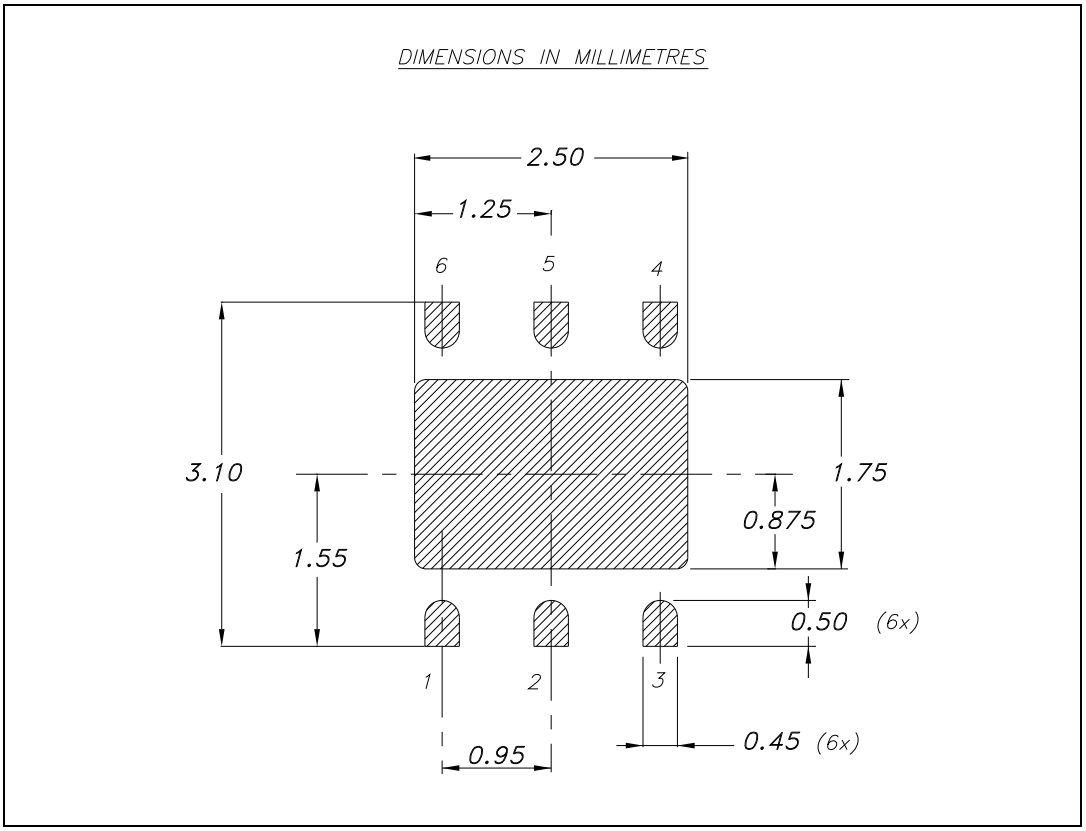


Table 7. DFN6 (3x3 mm) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1
A1	0	0.02	0.05
A3		0.20	
b	0.23		0.45
D	2.90	3	3.10
D2	2.23		2.50
E	2.90	3	3.10
E2	1.50		1.75
e		0.95	
L	0.30	0.40	0.50

Figure 38. DFN6 (3x3 mm) recommended footprint



7.2 DFN6 (3x3 mm) packing information

Figure 39. DFN6 (3x3 mm) tape outline

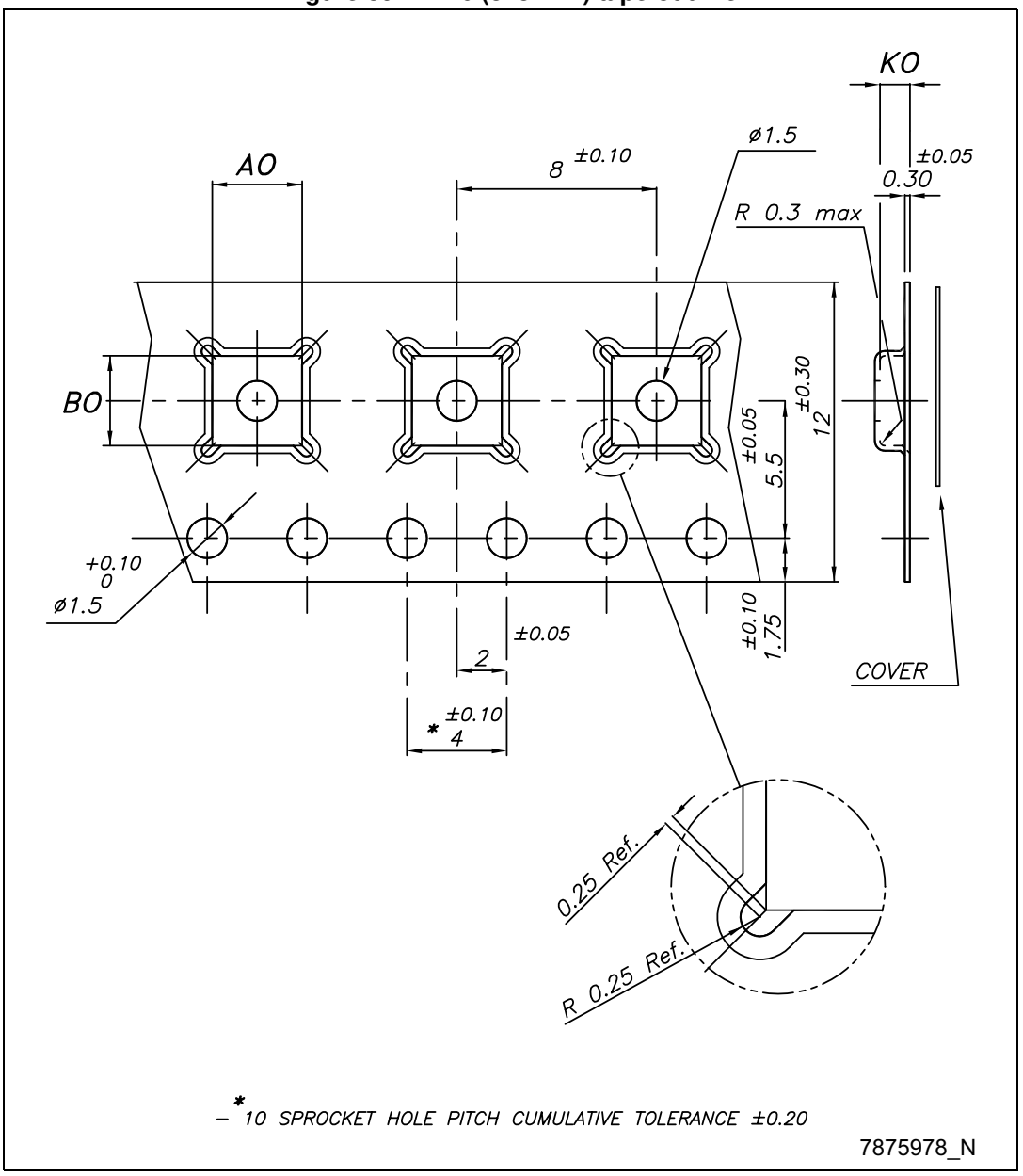


Figure 40. DFN6 (3x3 mm) reel outline

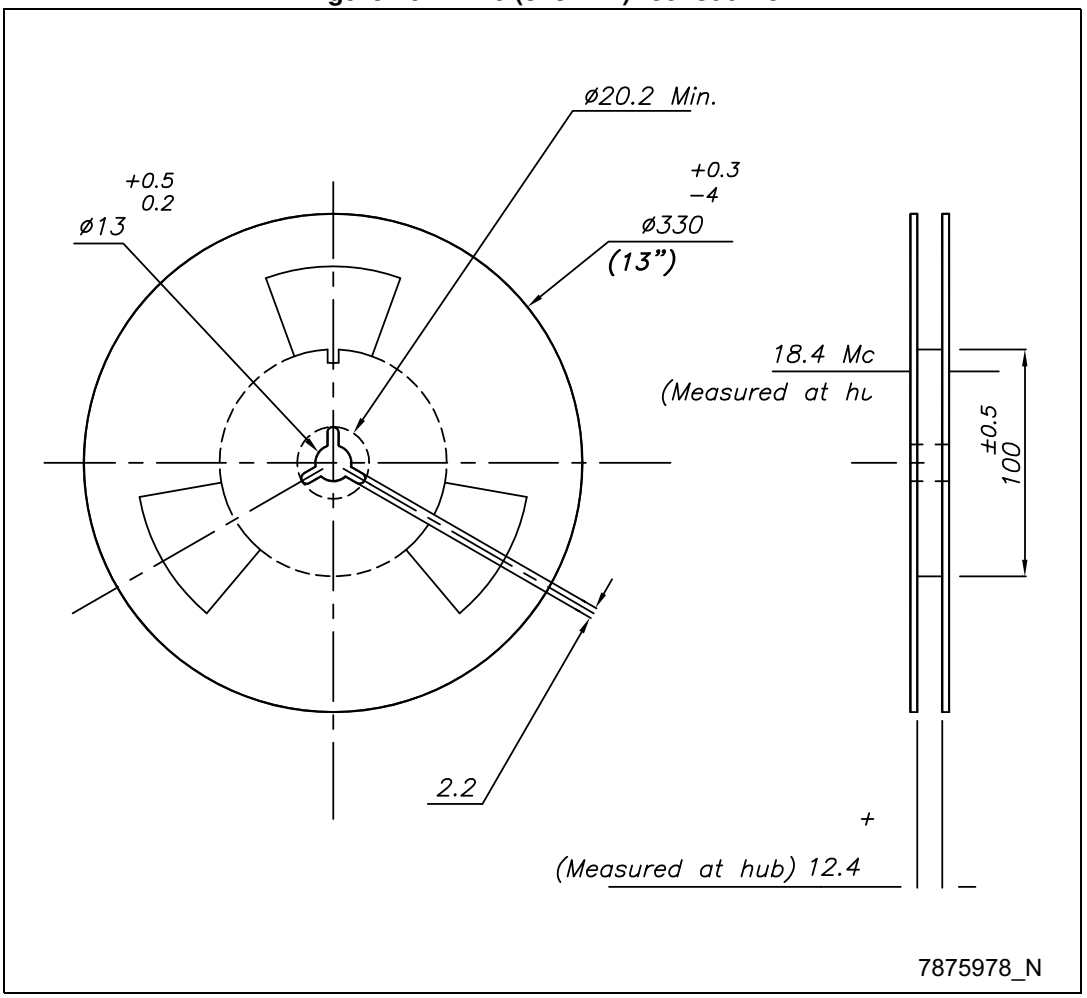


Table 8. DFN6 (3x3 mm) tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A0	3.20	3.30	3.40
B0	3.20	3.30	3.40
K0	1	1.10	1.20

7.3 DFN6 (2x2 mm) package information

Figure 41. DFN6 (2x2 mm) package outline

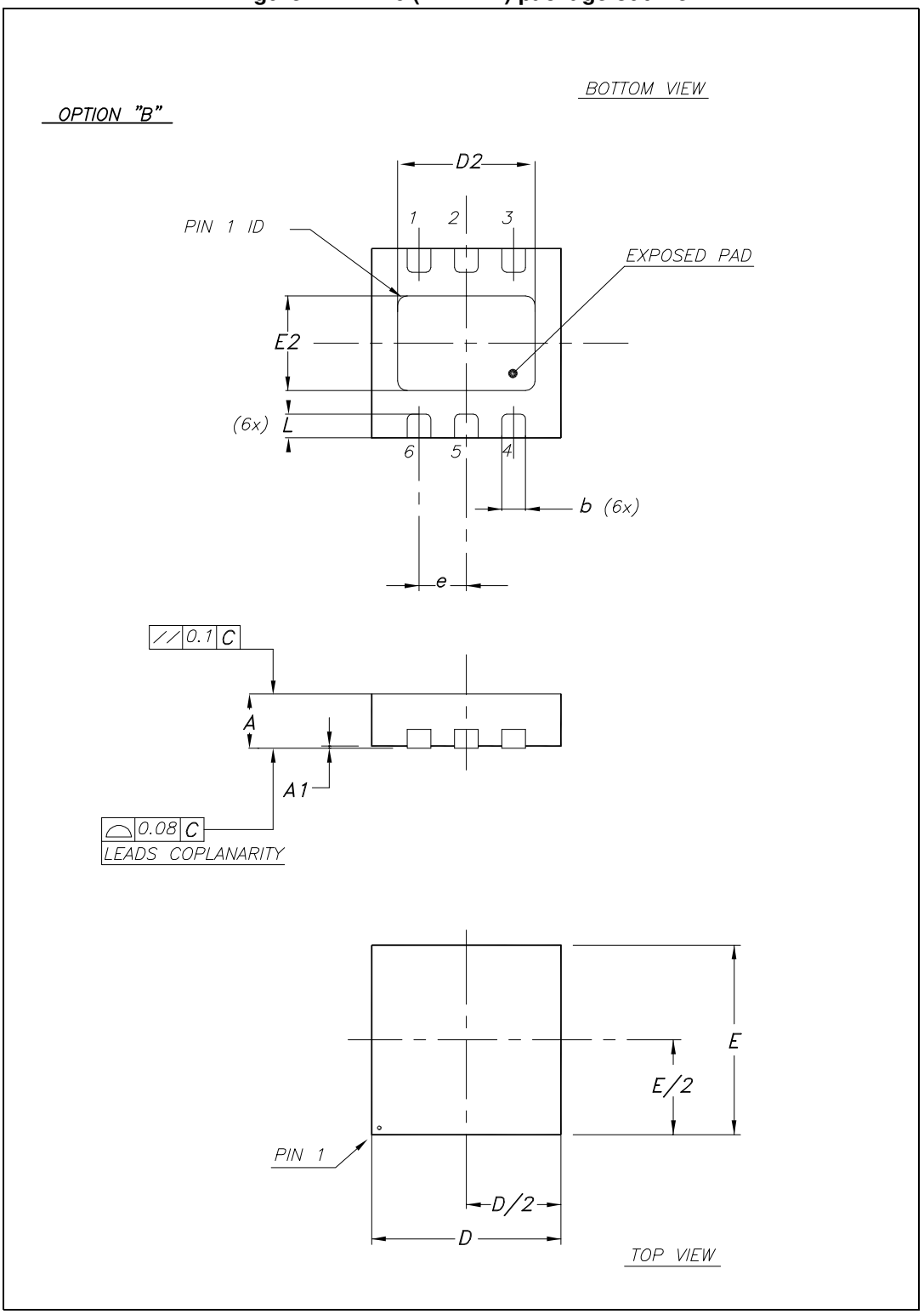
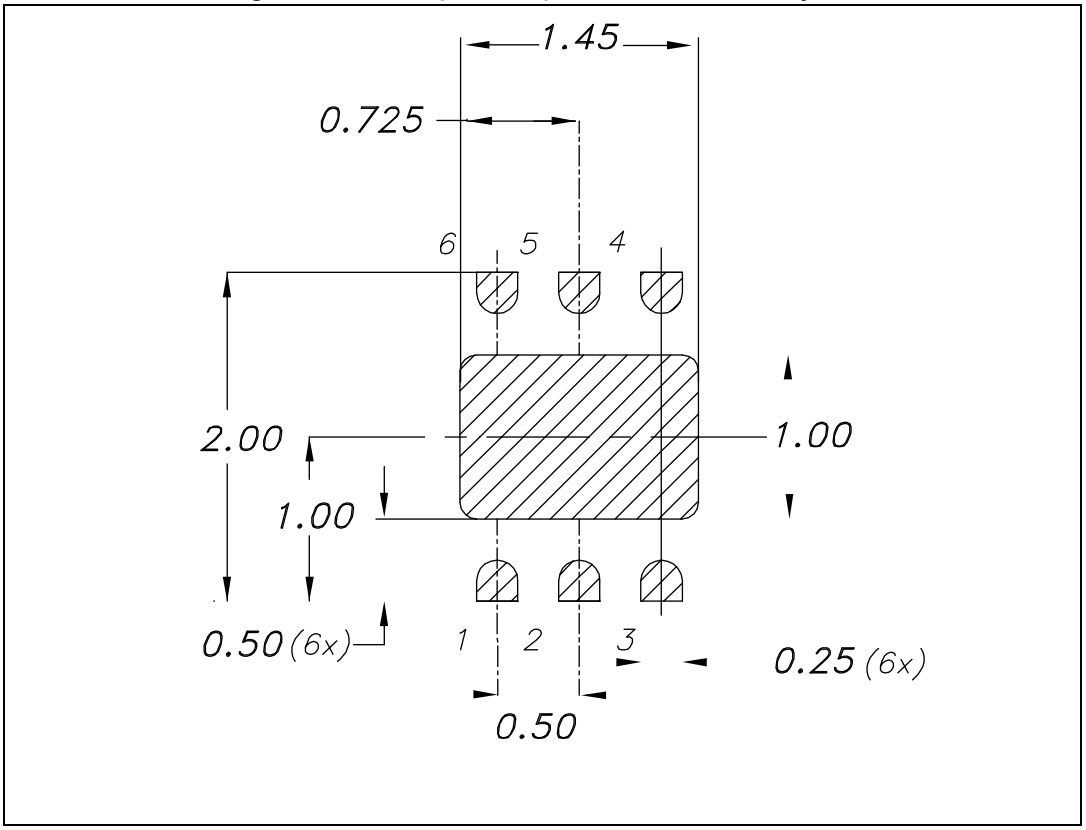


Table 9. DFN6 (2x2 mm) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.51	0.55	0.60
A1	0	0.02	0.05
b	0.18	0.25	0.30
D		2.00	
D2	1.30	1.45	1.55
E		2.00	
E2	0.85	1.00	1.10
e		0.50	
L	0.15	0.25	0.35

Figure 42. DFN6 (2x2 mm) recommended footprint



8 Ordering information

Table 10. Order code

Order code	Package	Packing	Output voltages
LD39050PUR	DFN6 (3x3 mm)	Tape and reel	Adjustable from 0.8 V
LD39050PU25R			2.5 V
LD39050PU33R			3.3 V
LD39050PV10R	DFN6 (2x2 mm)		1.0 V
LD39050PVR			Adjustable from 0.8 V

9 Revision history

Table 11. Document revision history

Date	Revision	Changes
11-Mar-2009	1	Initial release.
28-Feb-2014	2	The part number LD39050xx changed to LD39050. Updated the title in cover page, Table 10: Order code, Section 1: Diagrams, Section 2: Pin configuration, Section 4: Electrical characteristics, Section 5: Typical performance characteristics, Section 6: Application information and Section 7: Package information. Deleted order code table. Added Section 9: Revision history. Minor text changes.
26-Oct-2015	3	Added DFN6 (2x2 mm) package. Removed device summary table. Updated features and description in cover page. Updated *Section 2: Pin configuration, Table 3: Thermal data and Table 4: ESD performance.* Added *Section 8: Ordering information* Minor text changes.
29-Nov-2017	4	Updated Section 6.2: Enable function.
12-Dec-2019	5	Updated *Table 10: Order code*.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to *www.st.com/trademarks*. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2019 STMicroelectronics – All rights reserved