M41T66

Serial real-time clock with alarms

Features

- Counters for tenths/hundredths of seconds, seconds, minutes, hours, day, date, month, year, and century
- 32 KHz crystal oscillator integrating load capacitance and high crystal series resistance operation
- Oscillator stop detection monitors clock operation
- Serial interface supports I^2C bus (400 kHz)
- 525 nA timekeeping current at 3 V
- Low operating current of 35 µA (at 400 kHz)
- Timekeeping down to 1.0 V
- 1.3 V to 4.4 V I^2C bus operating voltage
  - Allows use in lithium ion rechargeable applications
- 32 KHz square wave on power-up to drive a microcontroller in low-power mode
- Programmable (1 Hz to 32 KHz) square wave
- Programmable alarm with interrupt function
- Accurate programmable watchdog (from 62.5 ms to 31 min)
- Software clock calibration to compensate deviation of crystal due to temperature
- Automatic leap year compensation
- Operating temperature of –40 to 85 °C
- Lead-free 16-pin QFN package



QFN16 3 mm x 3 mm

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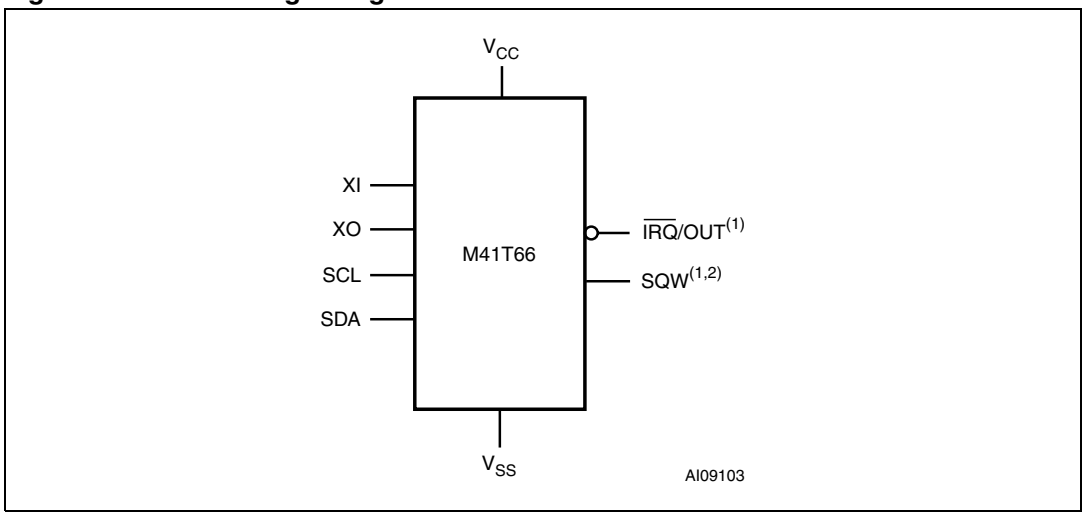
1 Description

The M41T66 is a low-power serial real-time clock (RTC) with a built-in 32.768 kHz oscillator (external crystal controlled). Eight registers are used for the clock/calendar function and are configured in binary coded decimal (BCD) format. An additional 8 registers provide status/control of alarm, square wave, calibration, and watchdog functions. Addresses and data are transferred serially via a two line, bidirectional I^2C interface. The built-in address register is incremented automatically after each WRITE or READ data byte.

Functions available to the user include a time-of-day clock/calendar, alarm interrupts, programmable square wave output, and watchdog output. The eight clock address locations contain the century, year, month, date, day, hour, minute, second and tenths/hundredths of a second in 24-hour BCD format. Corrections for 28-, 29- (leap year), 30- and 31-day months are made automatically.

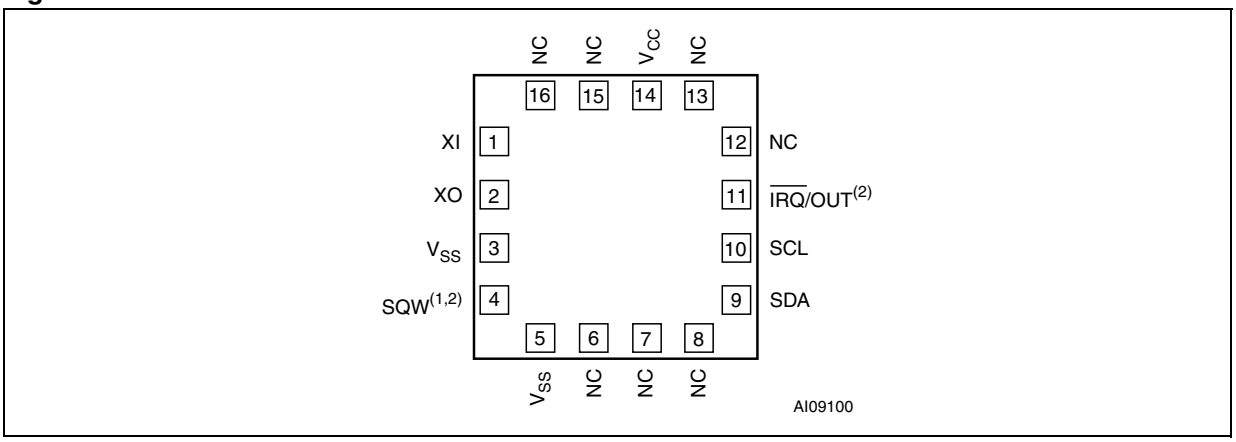
The M41T66 is supplied in a 16-pin QFN.

Figure 1. M41T66 logic diagram



1. Open drain
2. Defaults to 32 KHz on power-up

Figure 2. M41T66 connections

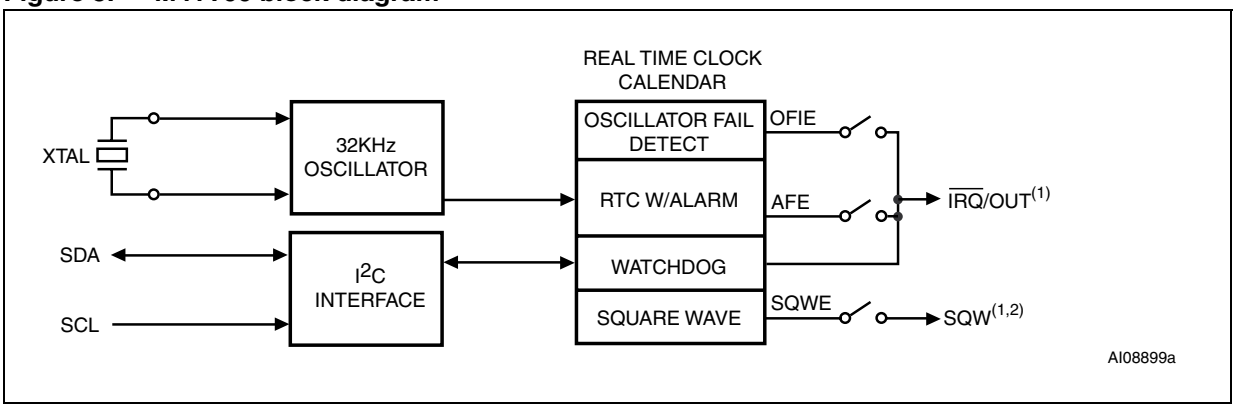


1. SQW output defaults to 32 KHz upon power-up
2. Open drain

Table 1. Signal names

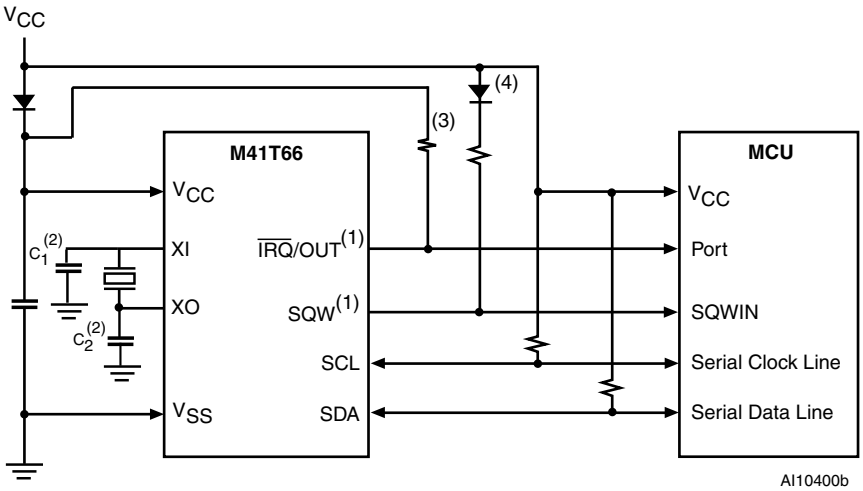
XI	Oscillator input
XO	Oscillator output
SDA	Serial data input/output
SCL	Serial clock input
$\overline{IRQ}$/OUT	Interrupt or OUT output (open drain)
SQW	Programmable square wave - defaults to 32 KHz on power-up (open drain)
V_{CC}	Supply voltage
V_{SS}	Ground

Figure 3. M41T66 block diagram



1. Open drain
2. Defaults to 32 KHz on power-up

Figure 4. Hardware hookup for SuperCap™ backup operation



1. Open drain
2. For a crystal with a load capacitance (C_L) of 12.5 pF, two parallel external 12.5 pF capacitors (C_1 and C_2) must be added to achieve better clock accuracy.
3. It can also be connected to another power supply.
4. Due to the output buffer circuitry used for the SQW output, this pin must not be taken to a voltage greater than V_{CC}. Diode required on SQW pin for SuperCap™ (or battery) backup. Low threshold BAT42 diode recommended.

2 Operation

The M41T66 clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 16 bytes contained in the device can then be accessed sequentially in the following order:

- 1st byte: tenths/hundredths of a second register
- 2nd byte: seconds register
- 3rd byte: minutes register
- 4th byte: hours register
- 5th byte: square wave/day register
- 6th byte: date register
- 7th byte: century/month register
- 8th byte: year register
- 9th byte: calibration register
- 10th byte: watchdog register
- 11th - 15th bytes: alarm registers
- 16th byte: flags register

2.1 2-wire bus characteristics

The bus is intended for communication between different ICs. It consists of two lines: a bidirectional data signal (SDA) and a clock signal (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line, while the clock line is high, will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

2.1.1 Bus not busy

Both data and clock lines remain high.

2.1.2 Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition.

2.1.3 Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.

2.1.4 Data valid

The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition a device that gives out a message is called “transmitter,” the receiving device that gets the message is called “receiver.” The device that controls the message is called “master.” The devices that are controlled by the master are called “slaves.”

2.1.5 Acknowledge

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line high to enable the master to generate the STOP condition.

Figure 5. Serial bus data transfer sequence

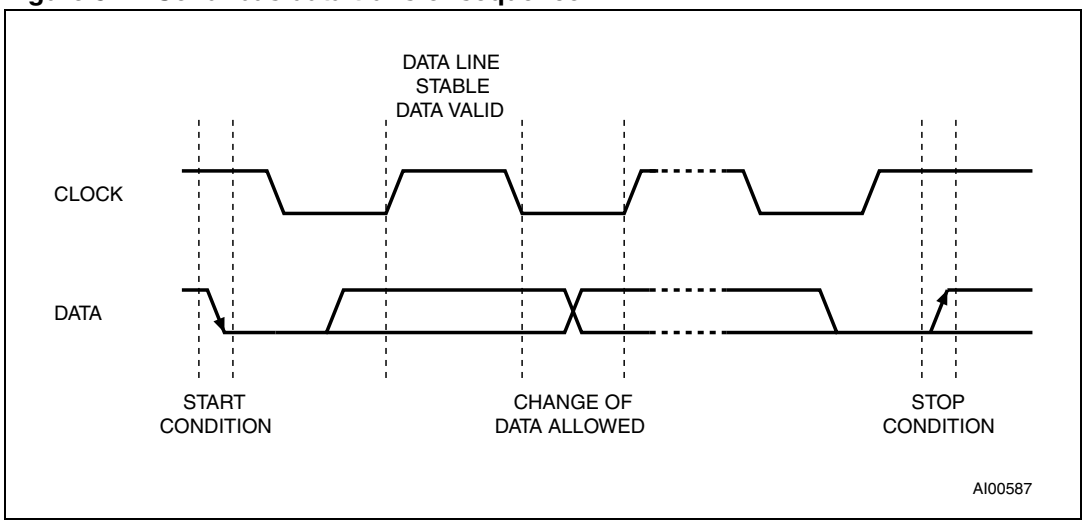
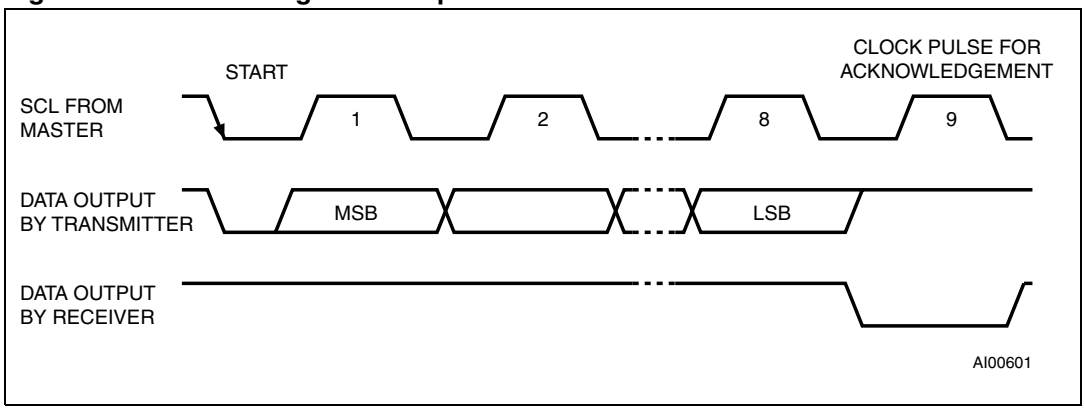


Figure 6. Acknowledgement sequence



2.2 READ mode

In this mode the master reads the M41T66 slave after setting the slave address (see *Figure 8 on page 11*). Following the WRITE mode control bit (R/$\overline{W}$=0) and the acknowledge bit, the word address 'An' is written to the on-chip address pointer. Next the START condition and slave address are repeated followed by the READ mode control bit (R/$\overline{W}$=1). At this point the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge clock. The M41T66 slave transmitter will now place the data byte at address An+1 on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to “An+2.”

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). The update will resume due to a stop condition or when the pointer increments to any non-clock address (08h-0Fh).

Note: This is true both in READ mode and WRITE mode.

An alternate READ mode may also be implemented whereby the master reads the M41T66 slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer (see *Figure 9 on page 11*).

Figure 7. Slave address location

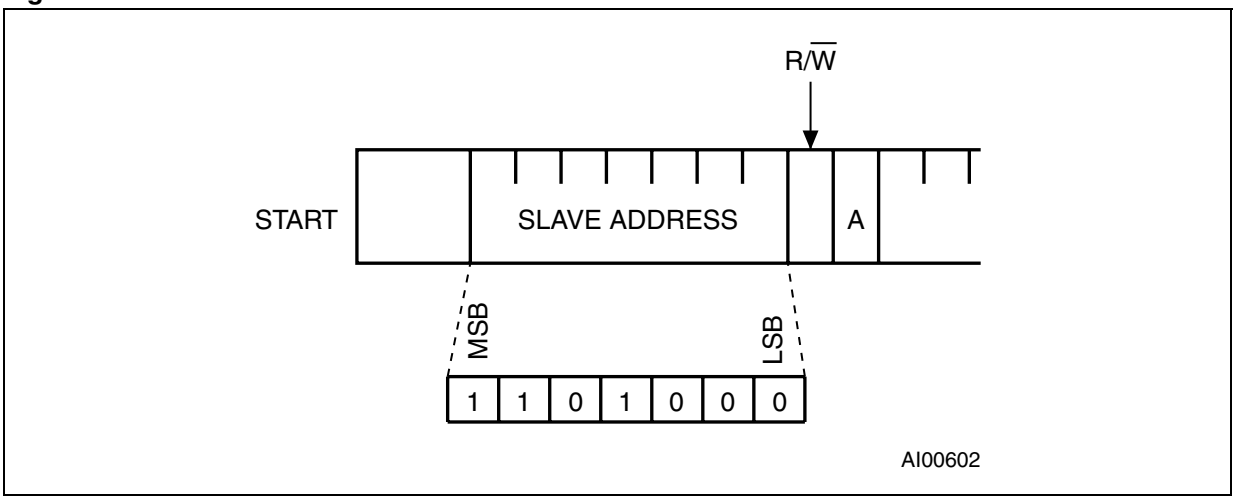


Figure 8. READ mode sequence

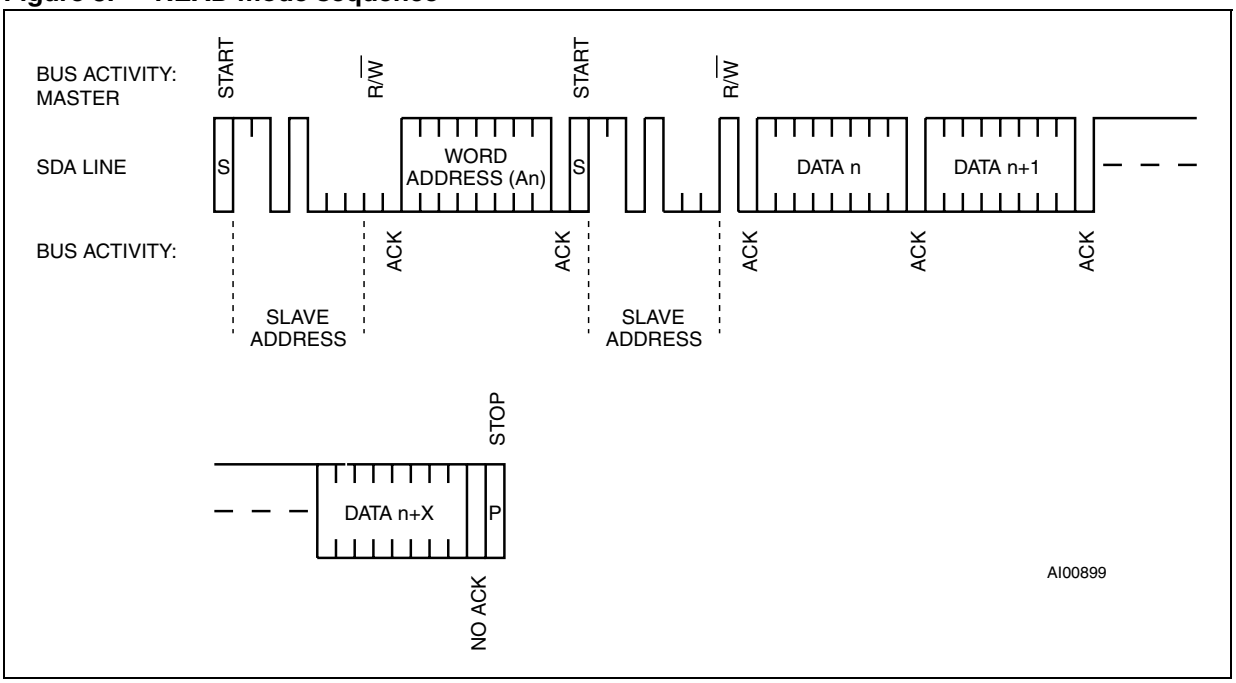
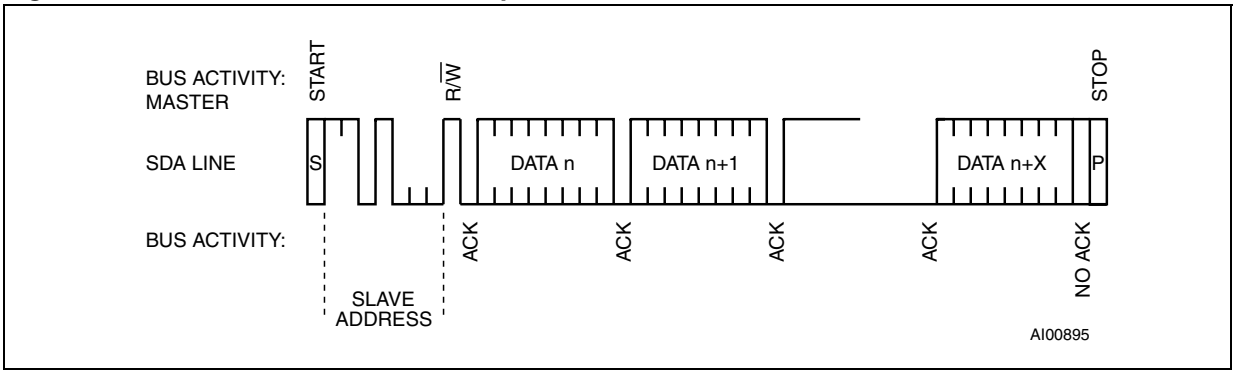


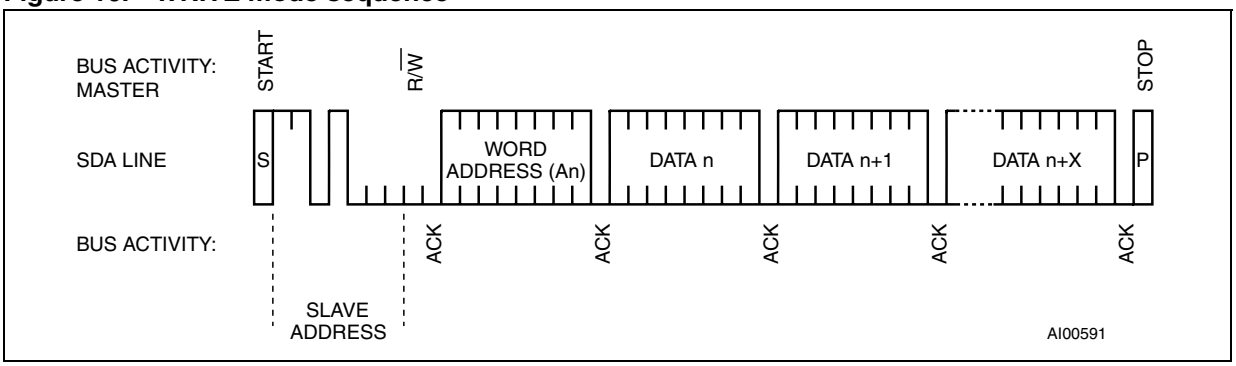
Figure 9. Alternative READ mode sequence



2.3 WRITE mode

In this mode the master transmitter transmits to the M41T66 slave receiver. Bus protocol is shown in *Figure 10*. Following the START condition and slave address, a logic '0' (R/$\overline{W}$=0) is placed on the bus and indicates to the addressed device that word address “An” will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next address location on the reception of an acknowledge clock. The M41T66 slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address see *Figure 7 on page 11* and again after it has received the word address and each data byte.

Figure 10. WRITE mode sequence



3 Clock operation

The M41T66 is driven by a quartz-controlled oscillator with a nominal frequency of 32.768 kHz. The accuracy of the real-time clock depends on the frequency of the quartz crystal that is used as the time-base for the RTC.

The eight byte clock register (see *Table 2: M41T66 register map*) is used to both set the clock and to read the date and time from the clock, in a binary coded decimal format. tenths/hundredths of seconds, seconds, minutes, and hours are contained within the first four registers.

A WRITE to any clock register will result in the tenths/hundredths of seconds being reset to “00,” and tenths/hundredths of seconds cannot be written to any value other than “00.”

Bits D0 through D2 of register 04h contain the day (day of week). Registers 05h, 06h, and 07h contain the date (day of month), month, and years. The ninth clock register is the calibration register (this is described in the clock calibration section). Bit D7 of register 01h contains the STOP bit (ST). Setting this bit to a '1' will cause the oscillator to stop. When reset to a '0' the oscillator restarts within one second (typical).

Bit D7 of register 02h (minute register) contains the oscillator fail interrupt enable bit (OFIE). When the user sets this bit to '1,' any condition which sets the oscillator fail bit (OF) (see *Oscillator stop detection on page 21*) will also generate an interrupt output.

Bits D6 and D7 of clock register 06h (century/month register) contain the CENTURY bit 0 (CB0) and CENTURY bit 1 (CB1).

A WRITE to ANY location within the first eight bytes of the clock register (00h-07h), including the OFIE bit, RS0-RS3 bit, and CB0-CB1 bits will result in an update of the system clock and a reset of the divider chain. This could result in an inadvertent change of the current time. These non-clock related bits should be written prior to setting the clock, and remain unchanged until such time as a new clock time is also written.

The eight clock registers may be read one byte at a time, or in a sequential block. Provision has been made to assure that a clock update does not occur while any of the eight clock addresses are being read. If a clock address is being read, an update of the clock registers will be halted. This will prevent a transition of data during the READ.

3.1 Clock registers

The M41T66 offers 16 internal registers which contain clock, calibration, alarm, watchdog, flags, and square wave. The clock registers are memory locations which contain external (user accessible) and internal copies of the data. The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy. The internal divider (or clock) chain will be reset upon the completion of a WRITE to any clock address (00h to 07h).

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). The update will resume either due to a stop condition or when the pointer increments to a non-clock address.

Clock and alarm registers store data in BCD format. calibration, watchdog, and square wave bits are written in a binary format.

Table 2. M41T66 register map(1)

Addr									Function/range BCD format	
	D7	D6	D5	D4	D3	D2	D1	D0		
00h	0.1 seconds				0.01 seconds				10ths/100ths of seconds	00-99
01h	ST	10 seconds			Seconds				Seconds	00-59
02h	OFIE	10 minutes			Minutes				Minutes	00-59
03h	0	0	10 hours		Hours (24 hour format)				Hours	00-23
04h	RS3	RS2	RS1	RS0	0	Day of week			Day	01-7
05h	0	0	10 date		Date: day of month				Date	01-31
06h	CB1	CB0	0	10M	Month				Century/ month	0-3/01-12
07h	10 years				Year				Year	00-99
08h	OUT	0	S	Calibration					Calibration	
09h	RB2	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	AFE	SQWE	0	Al 10M	Alarm month				Al month	01-12
0Bh	RPT4	RPT5	Al 10 date		Alarm date				Al date	01-31
0Ch	RPT3	0	Al 10 hour		Alarm hour				Al hour	00-23
0Dh	RPT2	Alarm 10 minutes			Alarm minutes				Al min	00-59
0Eh	RPT1	Alarm 10 seconds			Alarm seconds				Al sec	00-59
0Fh	WDF	AF	0	0	0	OF	0	0	Flags	

1. Keys:
0 = must be set to '0'
AF = alarm flag (read only)
AFE = alarm flag enable flag
BMB0 - BMB4 = watchdog multiplier bits
CB0-CB1 = century bits
OF = oscillator fail bit
OFIE = oscillator fail interrupt enable bit
OUT = output level
RB0 - RB2 = watchdog resolution bits
RPT1-RPT5 = alarm repeat mode bits
RS0-RS3 = SQW frequency bits
S = sign bit
SQWE = square wave enable bit
ST = stop bit
WDF = watchdog flag bit (read only)

3.2 Calibrating the clock

The M41T66 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The accuracy of the real-time clock depends on the frequency of the quartz crystal that is used as the time-base for the RTC. The accuracy of the clock is dependent upon the accuracy of the crystal, and the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. The M41T66 oscillator is designed for use with a 6 pF crystal load capacitance. When the calibration circuit is properly employed, accuracy improves to better than ±2 ppm at 25 °C. The M41T66's oscillator can drive the crystal's load capacitance that is greater than 6 pF. External capacitors must be added to achieve better clock accuracy (see *Figure 4 on page 7*).

The oscillation rate of crystals changes with temperature (see *Figure 11 on page 17*). Therefore, the M41T66 design employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in *Figure 12 on page 17*. The number of times pulses which are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in the calibration register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The calibration bits occupy the five lower order bits (D4-D0) in the calibration register (08h). These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register.

Assuming that the oscillator is running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or –5.35 seconds per day which corresponds to a total range of +5.5 or –2.75 minutes per month (see *Figure 12 on page 17*).

Two methods are available for ascertaining how much calibration the M41T66 may require:

- The first involves setting the clock, letting it run for a month and comparing it to a known accurate reference and recording deviation over a fixed period of time. Calibration values, including the number of seconds lost or gained in a given period, can be found in application note AN934, "How to use the digital calibration feature in TIMEKEEPER® and serial real-time clock (RTC) products." This allows the designer to give the end user the ability to calibrate the clock as the environment requires, even if the final product is packaged in a non-user serviceable enclosure. The designer could provide a simple utility that accesses the calibration byte.
- The second approach is better suited to a manufacturing environment, and involves the use of the SQW pin. The SQW pin will toggle at 512 Hz when RS3 = '0,' RS2 = '1,' RS1 = '1,' RS0 = '0,' SQWE = '1' and ST = '0'.

Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.010124 Hz would indicate a +20 ppm oscillator frequency error, requiring a –10 (XX001010) to be loaded into the calibration byte for correction. Note that setting or changing the calibration byte does not affect the square wave output frequency.

Figure 11. Crystal accuracy across temperature

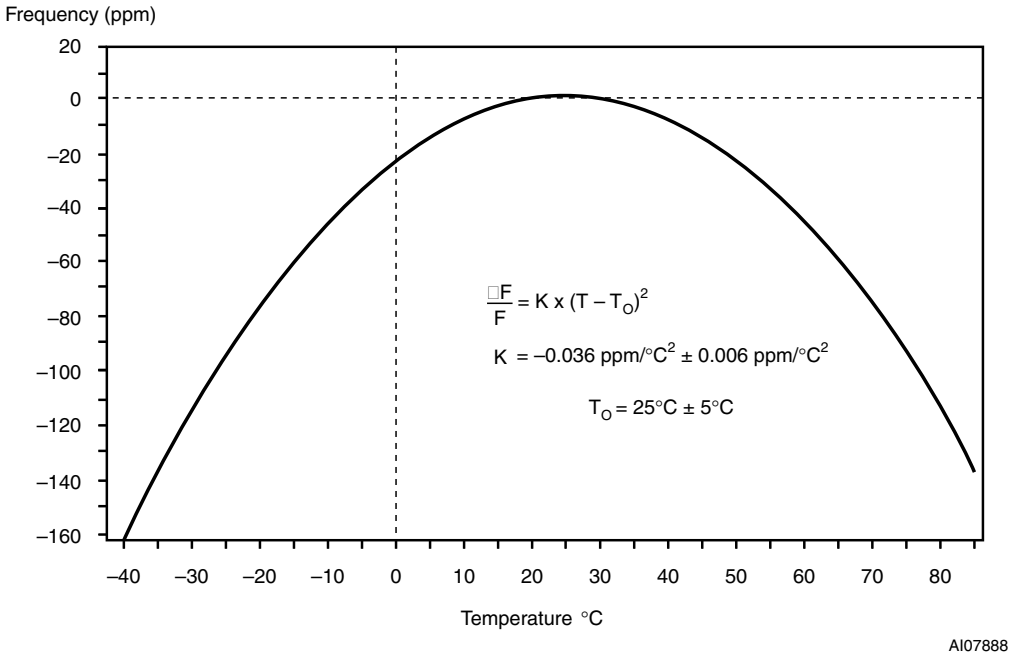
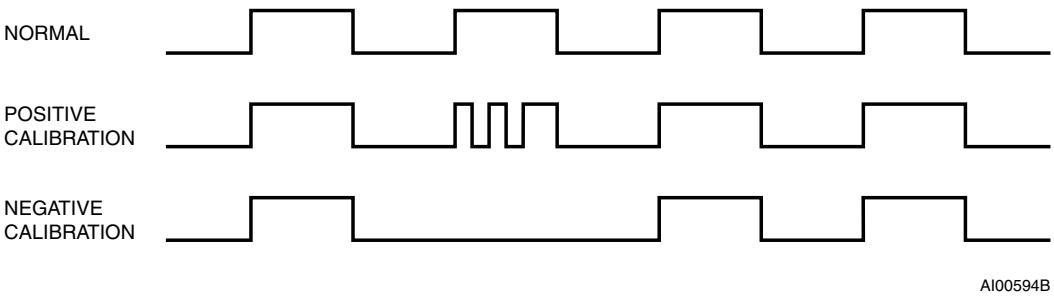


Figure 12. Calibration waveform



3.3 Setting alarm clock registers

Address locations 0Ah-0Eh contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific month, date, hour, minute, or second, or repeat every year, month, day, hour, minute, or second. Bits RPT5–RPT1 put the alarm in the repeat mode of operation. *Table 3* shows the possible configurations. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

When the clock information matches the alarm clock settings based on the match criteria defined by RPT5–RPT1, the AF (alarm flag) is set. If AFE (alarm flag enable) is also set, the alarm condition activates the $\overline{IRQ}$/OUT. To disable the alarm, write '0' to the alarm date register and to RPT5–RPT1.

Note: If the address pointer is allowed to increment to the flag register address, an alarm condition will not cause the interrupt/flag to occur until the address pointer is moved to a different address. It should also be noted that if the last address written is the "alarm seconds," the address pointer will increment to the flag address, causing this situation to occur.

The $\overline{IRQ}$/OUT output is cleared by a READ to the flags register as shown in *Figure 13*. A subsequent READ of the flags register is necessary to see that the value of the alarm flag has been reset to '0.'

Figure 13. Alarm interrupt reset waveform

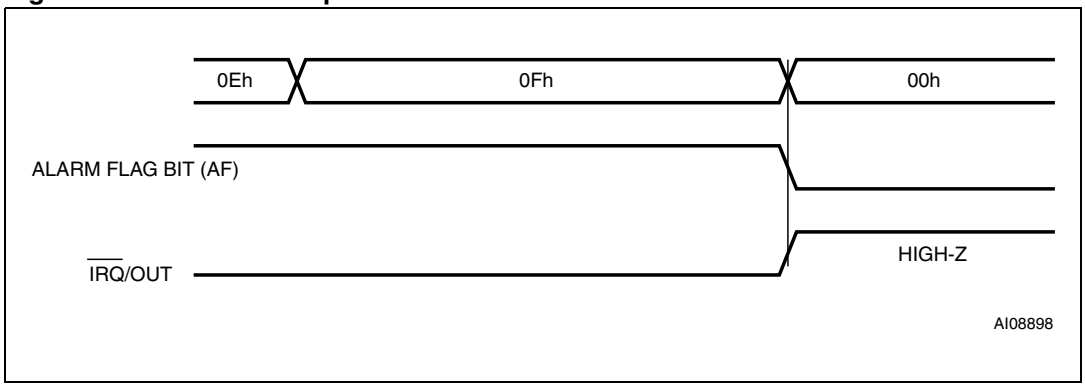


Table 3. Alarm repeat modes

RPT5	RPT4	RPT3	RPT2	RPT1	Alarm setting
1	1	1	1	1	Once per second
1	1	1	1	0	Once per minute
1	1	1	0	0	Once per hour
1	1	0	0	0	Once per day
1	0	0	0	0	Once per month
0	0	0	0	0	Once per year

3.4 Watchdog timer

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the Watchdog Register, address 09h.

Bits BMB4-BMB0 store a binary multiplier and the three bits RB2-RB0 select the resolution where:

000=1/16 second (16Hz)

001=1/4 second (4Hz)

010=1 second (1Hz)

011=4 seconds (1/4Hz) and

100 = 1 minute (1/60Hz)

Note: Invalid combinations (101, 110, and 111) will NOT enable a watchdog time-out. Setting the BMB4-BMB0 = 0 with any combination of RB2-RB0, other than 000, will result in an immediate watchdog time-out.

The amount of time-out is then determined to be the multiplication of the five-bit multiplier value with the resolution. (For example: writing 00001110 in the watchdog register = 3*1 or 3 seconds). If the processor does not reset the timer within the specified period, the M41T66 sets the WDF (watchdog flag) and generates an interrupt on the $\overline{IRQ}$/OUTpin. The watchdog timer can only be reset by having the microprocessor perform a WRITE of the watchdog register. The time-out period then starts over.

Should the watchdog timer time-out, any value may be written to the watchdog register in order to clear the $\overline{IRQ}$/OUT pin. A value of 00h will disable the watchdog function until it is again programmed to a new value. A READ of the flags register will reset the watchdog flag (bit D7; register 0Fh). The watchdog function is automatically disabled upon power-up, and the watchdog register is cleared.

Note: A WRITE to any clock register will restart the watchdog timer.

3.5 Square wave output

The M41T66 offers the user a programmable square wave function which is output on the SQW pin. RS3-RS0 bits located in 04h establish the square wave output frequency. These frequencies are listed in *Table 4*. Once the selection of the SQW frequency has been completed, the SQW pin can be turned on and off under software control with the square wave enable bit (SQWE) located in register 0Ah.

The SQW output is an open drain output driver. The initial power-up default for the SQW output is 32 KHz.

Note: When the SQW is enabled and the ST bit is set (ST = 1), the square wave output could be low or high and could drain current through the pull-up resistor.

Due to the output buffer circuitry used for the SQW output, this pin must not be taken to a voltage greater than V_{CC}. A diode is required on the SQW pin for SuperCap™ (or battery) backup. A low threshold BAT42 diode is recommended (see *Figure 4 on page 7*).

Table 4. Square wave output frequency

Square wave bits				Square wave	
RS3	RS2	RS1	RS0	Frequency	Units
0	0	0	0	None	–
0	0	0	1	32.768	kHz
0	0	1	0	8.192	kHz
0	0	1	1	4.096	kHz
0	1	0	0	2.048	kHz
0	1	0	1	1.024	kHz
0	1	1	0	512	Hz
0	1	1	1	256	Hz
1	0	0	0	128	Hz
1	0	0	1	64	Hz
1	0	1	0	32	Hz
1	0	1	1	16	Hz
1	1	0	0	8	Hz
1	1	0	1	4	Hz
1	1	1	0	2	Hz
1	1	1	1	1	Hz

3.6 Century bits

These two bits will increment in a binary fashion at the turn of the century, and handle all leap years correctly. See *Table 6 on page 22* for additional explanation.

3.7 Output driver pin

When the OFIE bit, AFE bit, and watchdog register are not set to generate an interrupt, the $\overline{IRQ}$/OUT pin becomes an output driver that reflects the contents of D7 of the calibration register. In other words, when D7 (OUT bit) is a '0,' then the $\overline{IRQ}$/OUT pin will be driven low.

Note: The $\overline{IRQ}$/OUT pin is an open drain which requires an external pull-up resistor.

3.8 Oscillator stop detection

If the oscillator fail (OF) bit is internally set to a '1,' this indicates that the oscillator has either stopped, or was stopped for some period of time and can be used to judge the validity of the clock and date data. This bit will be set to '1' any time the oscillator stops.

In the event the OF bit is found to be set to '1' at any time other than the initial power-up, the STOP bit (ST) should be written to a '1,' then immediately reset to '0.' This will restart the oscillator.

The following conditions can cause the OF bit to be set:

- The first time power is applied (defaults to a '1' on power-up).
- The voltage present on V_{CC} or battery is insufficient to support oscillation.
- The ST bit is set to '1.'
- External interference of the crystal

If the oscillator fail interrupt enable bit (OFIE) is set to a '1,' the $\overline{IRQ}$/OUTpin will also be activated. The $\overline{IRQ}$/OUT output is cleared by resetting the OFIE or OF bit to '0' (NOT by reading the flag register).

The OF bit will remain set to '1' until written to logic '0.' The oscillator must start and have run for at least 1 second before attempting to reset the OF bit to '0.' If the trigger event occurs during a power-down condition, this bit will be set correctly.

3.9 Initial power-on defaults

Upon application of power to the device, the register bits will initially power-on in the state indicated in *Table 5*.

Table 5. Initial power-on default values

Condition	ST	OF	OFIE	OUT	AFE	SQWE	RS3-1	RS0	Watchdog
Initial power-up(1)	0	1	0	1	0	1	0	1	0

1. All other control bits power-up in an undetermined state.

Table 6. Century bits examples

CB0	CB1	Leap year?	Example(1)
0	0	Yes	2000
0	1	No	2100
1	0	No	2200
1	1	No	2300

1. Leap year occurs every four years (for years evenly divisible by four), except for years evenly divisible by 100. The only exceptions are those years evenly divisible by 400 (the year 2000 was a leap year, year 2100 is not).

4 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Sym	Parameter	Conditions(1)	Value(2)	Unit
T_{STG}	Storage temperature (V_{CC} off, oscillator off)		–55 to 125	°C
V_{CC}	Supply voltage		–0.3 to 5.0	V
T_{SLD}(3)	Lead solder temperature for 10 seconds		260	°C
V_{IO}	Input or output voltages		–0.2 to V_{CC}+0.3	V
I_O	Output current		20	mA
P_D	Power dissipation		1	W
$V_{ESD(HBM)}$	Electro-static discharge voltage (human body model)	T_A = 25 °C	>1500	V
$V_{ESD(RCDM)}$	Electro-static discharge voltage (robotic charged device model)	T_A = 25 °C	>1000	V

1. Test conforms to JEDEC standard.
2. Data based on characterization results, not tested in production.
3. Reflow at peak temperature of 260 °C (total thermal budget not to exceed 245 °C for greater than 30 seconds).

5 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the measurement conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 8. Operating and AC measurement conditions(1)

Parameter	M41T66
Supply voltage (V_{CC})	1.5 V to 4.4 V
Ambient operating temperature (T_A)	–40 to 85 °C
Load capacitance (C_L)	50 pF
Input rise and fall times	≤ 5 ns
Input pulse voltages	0.2 V_{CC} to 0.8 V_{CC}
Input and output timing ref. voltages	0.3 V_{CC} to 0.7 V_{CC}

1. Output Hi-Z is defined as the point where data is no longer driven.

Figure 14. AC measurement I/O waveform

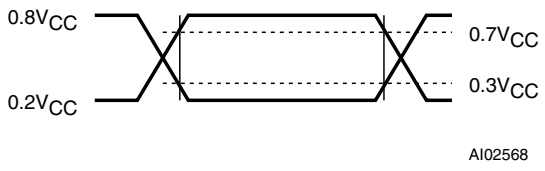
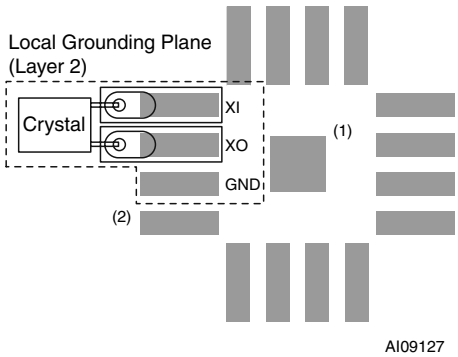


Figure 15. Crystal isolation example



1. Substrate pad should be tied to V_{SS}.
2. To avoid coupling between pin 4 (SQW) and pin 2 (XO), pin 3 (GND) should be routed adjacent to pin 4 for isolation purposes.

Table 9. Capacitance

Symbol	Parameter[1][2]	Min	Max	Unit
C_{IN}	Input capacitance		7	pF
C_{OUT}[3]	Output capacitance		10	pF
t_{LP}	Low-pass filter input time constant (SDA and SCL)		50	ns

1. Effective capacitance measured with power supply at 3.6 V; sampled only, not 100% tested.
2. At 25 °C, f = 1 MHz.
3. Outputs deselected.

Table 10. DC characteristics

Sym	Parameter	Test condition[1]		Min	Typ	Max	Unit
V_{CC}[2]	Operating voltage	Clock	0 °C to 85 °C	1.0		4.4	V
			–20 °C to 85 °C	1.3		4.4	V
			–40 °C to 85 °C	1.5		4.4	V
		I^2C bus (400 kHz)		1.3		4.4	V
I_{CC1}	Supply current	SCL = 400 kHz (no load)	4.4 V			100	µA
			3.6 V		50	70	µA
			3.0 V		35		µA
			2.5 V		30		µA
			2.0 V		20		µA
I_{CC2}	Supply current (standby)	SCL = 0 Hz, all inputs ≥ V_{CC} – 0.2 V ≤ V_{SS} + 0.2 V, SQW off	4.4 V			1100	nA
			3.6 V		550	900	nA
			3.0 V at 25 °C		525		nA
			1.8 V at 25 °C		450		nA
V_{IL}	Input low voltage			–0.2		0.3 V_{CC}	V
V_{IH}	Input high voltage			0.7V_{CC}		V_{CC}+0.3	V
V_{OL}	Output low voltage	V_{CC} = 4.4 V, I_{OL} = 1.0 mA (SQW, $\overline{IRQ}$/OUT)				0.4	V
V_{PU}	Pull-up supply voltage (open drain)	$\overline{IRQ}$/OUT				4.4	V
		SQW				V_{CC}	V
I_{LI}	Input leakage current	0V ≤ V_{IN} ≤ V_{CC}				±1	µA
I_{LO}	Output leakage current	0V ≤ V_{OUT} ≤ V_{CC}				±1	µA
	Square wave duty cycle[3]	No load		40	50	60	%

1. Valid for ambient operating temperature: T_A = –40 to 85 °C; V_{CC} = 1.5 V to 4.4 V (except where noted).
2. Oscillator startup guaranteed at 1.6 V only at 25 °C.
3. Guaranteed by design.

Table 11. Crystal electrical characteristics

Sym	Parameter[1][2]	Min	Typ	Max	Units
f_O	Resonant frequency		32.768		kHz
R_S	Series resistance (T_A = –40 to 70 °C)			75[3][4]	kΩ
C_L	Load capacitance		6		pF
			7-12.5[5]		

1. Externally supplied if using the QFN16 package. STMicroelectronics recommends the Citizen CFS-145 (1.5 x 5 mm) and the KDS DT-38 (3 x 8 mm) for thru-hole, or the KDS DMX-26S (3.2 x 8 mm) for surface-mount, tuning fork-type quartz crystals. KDS can be contacted at http://www.kds.info/index_en.htm. Citizen can be contacted at http://www.citizencrystal.com.
2. Load capacitors are integrated within the M41T66. Circuit board layout considerations for the 32.768 kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.
3. Guaranteed by design.
4. $R_{S\ (max)}$ = 65 kΩ for T_A = –40 to 85 °C and oscillator startup at 1.7 V.
5. External capactors must be added to achieve better clock accuracy.

Table 12. Oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{STA}	Oscillator start voltage	at 25 °C	1.6			V
t_{STA}	Oscillator start time	V_{CC} = 1.6 V at 25 °C		500		ms
		V_{CC} = 3.0 V			1	s
C_g	XIN			12		pF
C_d	XOUT			12		pF
	IC-to-IC frequency variation [1]		–10		+10	ppm

1. Reference value. T_A = 25 °C, V_{CC} = 3.0 V, CMJ-145 (C_L = 6 pF, 32,768 Hz) manufactured by Citizen.

Figure 16. Bus timing requirements sequence

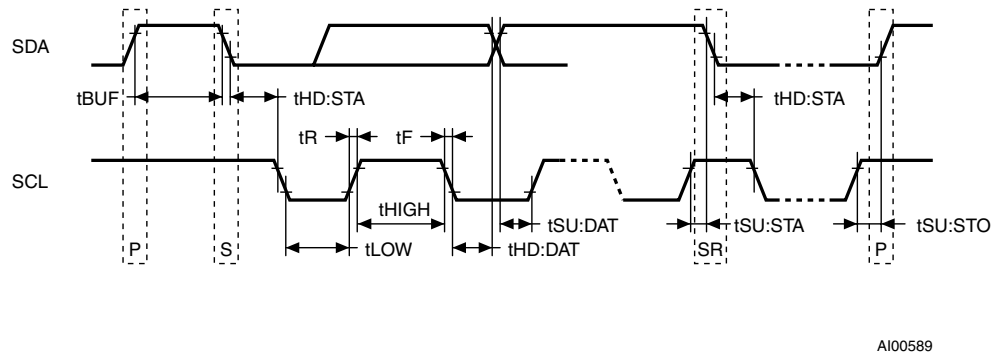


Table 13. AC characteristics

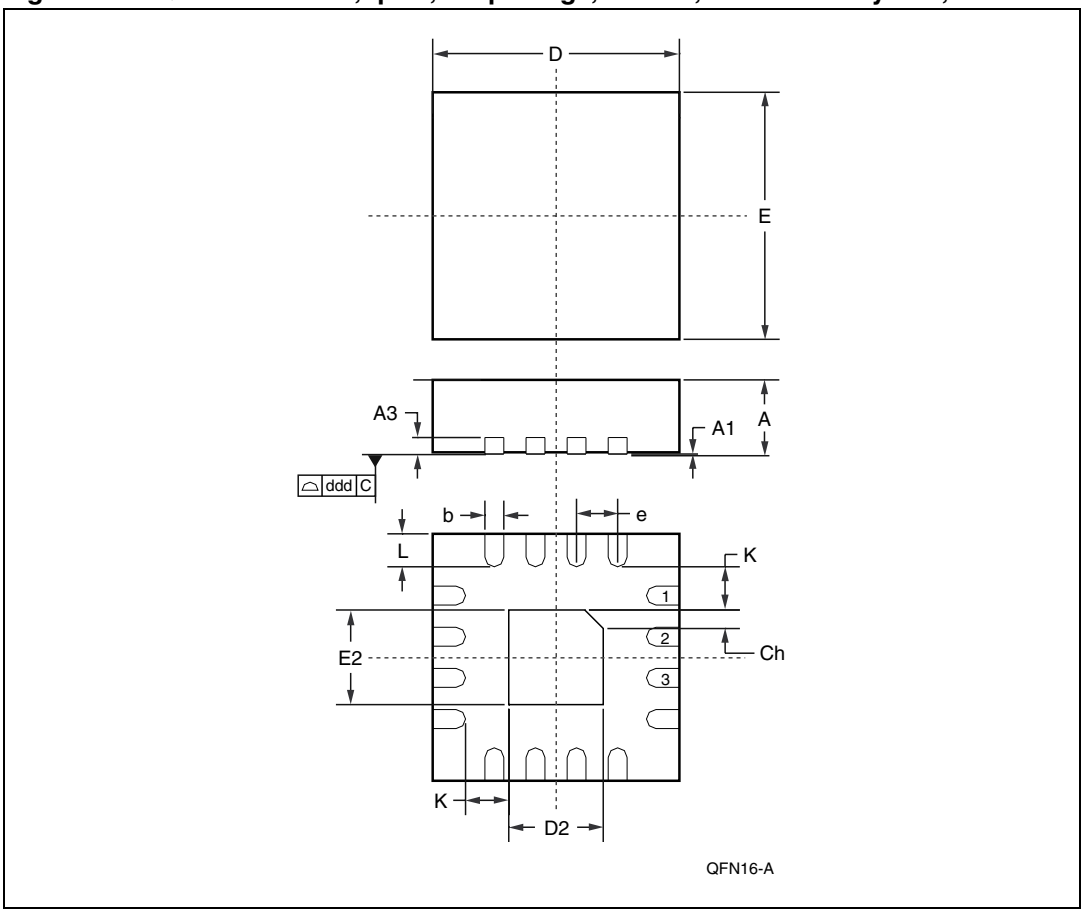
Sym	Parameter[1]	Min	Typ	Max	Units
f_{SCL}	SCL clock frequency	0		400	kHz
t_{LOW}	Clock low period	1.3			µs
t_{HIGH}	Clock high period	600			ns
t_R	SDA and SCL rise time			300	ns
t_F	SDA and SCL fall time			300	ns
$t_{HD:STA}$	START condition hold time (after this period the first clock pulse is generated)	600			ns
$t_{SU:STA}$	START condition setup time (only relevant for a repeated start condition)	600			ns
$t_{SU:DAT}$[2]	Data setup time	100			ns
$t_{HD:DAT}$	Data hold time	0			µs
$t_{SU:STO}$	STOP condition setup time	600			ns
t_{BUF}	Time the bus must be free before a new transmission can start	1.3			µs

1. Valid for ambient operating temperature: T_A = –40 to 85 °C; V_{CC} = 1.5 to 4.4 V (except where noted).
2. Transmitter must internally provide a hold time to bridge the undefined region (300 ns max) of the falling edge of SCL.

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 17. QFN16 – 16-lead, quad, flat package, no lead, 3 x 3 mm body size, outline

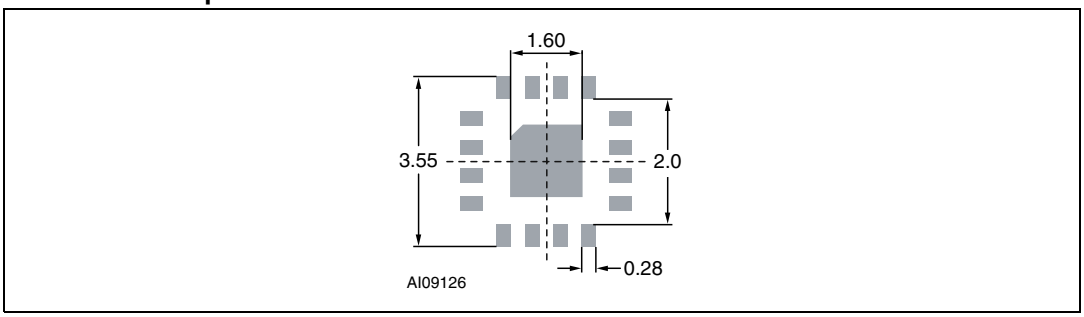


1. Drawing is not to scale.

Table 14. QFN16 – 16-lead, quad, flat package, no lead, 3 x 3 mm body size, mech. data

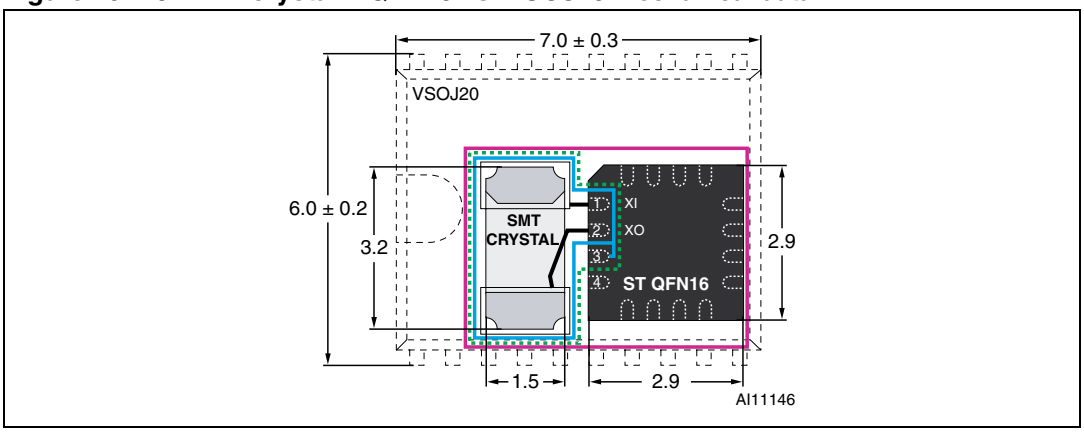
Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	0.90	0.80	1.00	0.035	0.032	0.039
A1	0.02	0.00	0.05	0.001	0.000	0.002
A3	0.20	–	–	0.008	–	–
b	0.25	0.18	0.30	0.010	0.007	0.012
D	3.00	2.90	3.10	0.118	0.114	0.122
D2	1.70	1.55	1.80	0.067	0.061	0.071
E	3.00	2.90	3.10	0.118	0.114	0.122
E2	1.70	1.55	1.80	0.067	0.061	0.071
e	0.50	–	–	0.020	–	–
K	0.20	–	–	0.008	–	–
L	0.40	0.30	0.50	0.016	0.012	0.020
ddd	–	0.08	–	–	0.003	–
Ch	–	0.33	–	–	0.013	–
N	16			16		

Figure 18. QFN16 – 16-lead, quad, flat package, no lead, 3 x 3 mm, recommended footprint



1. Dimensions shown are in millimeters (mm).

Figure 19. 32 KHz crystal + QFN16 vs. VSOJ20 mechanical data



1. Dimensions shown are in millimeters (mm).

Figure 20. Carrier tape for QFN16 (3 mm x 3 mm) package

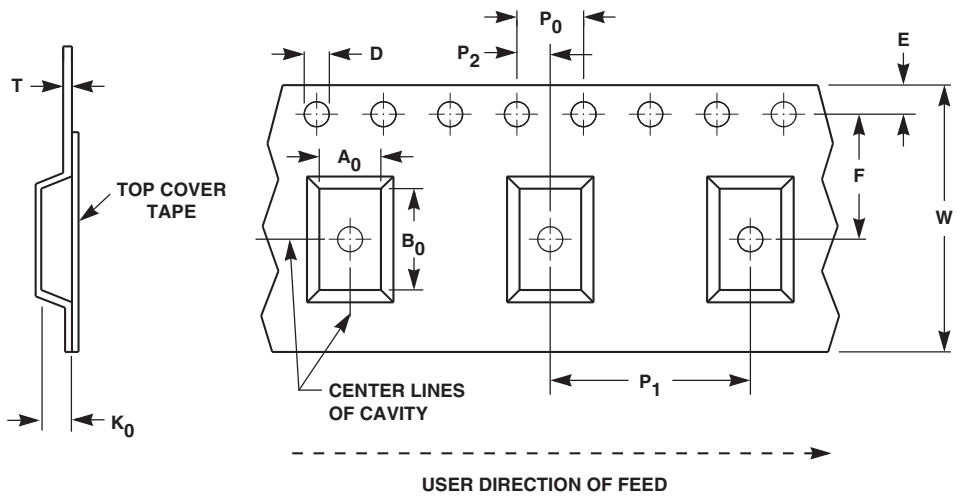


Table 15. Carrier tape dimensions for QFN16 (3 mm x 3 mm) package

Package	W	D	E	P_0	P_2	F	A_0	B_0	K_0	P_1	T	Unit	Bulk Qty
QFN16	12.00 ±0.30	1.50 +0.10 /-0.00	1.75 ±0.10	4.00 ±0.10	2.00 ±0.10	5.50 ±0.05	3.30 ±0.10	3.30 ±0.10	1.10 ±0.10	8.00 ±0.10	0.30 ±0.05	mm	3000

Figure 21. Reel schematic

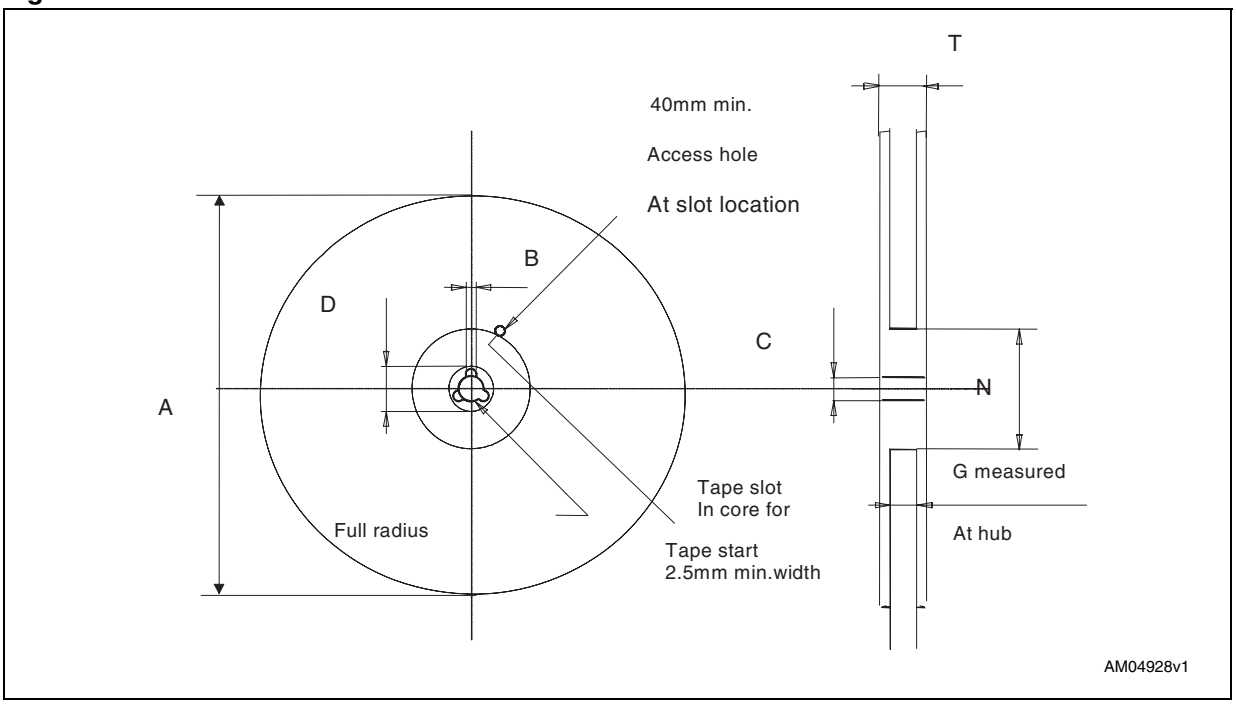


Table 16. Reel dimensions for 12 mm carrier tape - QFN16 package

A (max)	B (min)	C	D (min)	N (min)	G	T (max)
330 mm (13-inch)	1.5 mm	13 mm ± 0.2 mm	20.2 mm	60 mm	12.4 mm + 2/–0 mm	18.4 mm

Note: The dimensions given in Table 16 incorporate tolerances that cover all variations on critical parameters.

7 Part numbering

Table 17. Ordering information scheme

Example: M41T 66 Q 6 F

Device family

M41T

Device type and supply voltage

66 = V_{CC} = 1.5 V to 4.4 V

Package

Q = QFN16 (3 mm x 3 mm)

Temperature range

6 = –40 °C to 85 °C

Shipping method

F = ECOPACK® package, tape & reel

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

8 Revision history

Table 18. Document revision history

Date	Revision	Changes
22-Oct-2008	1	Initial release
25-Oct-2011	2	Updated title; minor textual updates; updated ECOPACK® text in *Section 6: Package mechanical data*; added *Figure 20*, *21*, *Table 15*, *16*

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