3.3-V DUAL-PLL MULTICLOCK GENERATOR

Check for Samples: PLL1707-Q1

FEATURES

- **Qualified for Automotive Applications**
- **27-MHz Master Clock Input**
- **Generated Audio System Clock**
  - **SCKO0: 768 f_S (f_S = 44.1 kHz)**
  - **SCKO1: 768 f_S, 512 f_S (f_S = 48 kHz)**
  - **SCKO2: 256 f_S (f_S = 32, 44.1, 48, 64, 88.2, 96 kHz)**
  - **SCKO3: 384 f_S (f_S = 32, 44.1, 48, 64, 88.2, 96 kHz)**
- **Zero PPM Error Output Clocks**
- **Low Clock Jitter: 50 ps (Typical)**
- **Multiple Sampling Frequencies: f_S = 32, 44.1, 48, 64, 88.2, 96 kHz**
- **3.3-V Single Power Supply**
- **Parallel Control**
- **Package: 20-Pin SSOP (150 mil), Lead-Free Product**

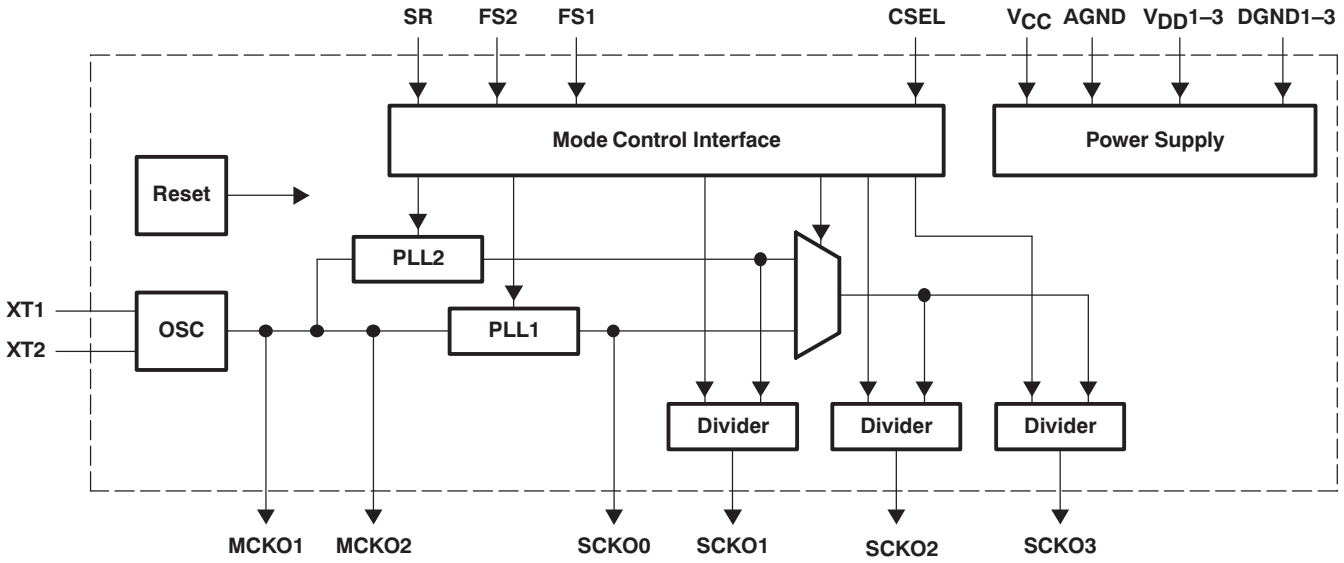
APPLICATIONS

- **HDD + DVD Recorders**
- **DVD Recorders**
- **HDD Recorders**
- **DVD Players**
- **DVD Add-On Cards for Multimedia PCs**
- **Digital HDTV Systems**
- **Set-Top Boxes**

DESCRIPTION

The PLL1707 is a low-cost phase-locked loop (PLL) multiclock generator. The PLL1707 can generate four system clocks from a 27-MHz reference input frequency. The clock outputs of the PLL1707 can be controlled by sampling frequency-control pins. The device gives customers both cost and space savings by eliminating external components and enables customers to achieve the very low-jitter performance needed for high performance audio DACs and/or ADCs. The PLL1707 is ideal for MPEG-2 applications that use a 27-MHz master clock such as DVD recorders, HDD recorders, DVD add-on cards for multimedia PCs, digital HDTV systems, and set-top boxes.

FUNCTIONAL BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP - DBQ	Reel of 2500	PLL1707IDBQRQ1	PLL1707I

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

V_{CC}	Supply voltage: $V_{DD}1$-$V_{DD}3$	4 V
ΔV_{CC}	Supply voltage differences: $V_{DD}1$-$V_{DD}3$	±0.1 V
	Ground voltage differences: AGND, DGND1-DGND3	±0.1 V
V_I	Digital input voltage: FS1, FS2, SR, CSEL	-0.3 V to (V_{DD} + 0.3) V
V_I	Analog input voltage, XT1, XT2	-0.3 V to (V_{CC} + 0.3) V
I_I	Input current (any pins except supplies)	±10 mA
T_A	Ambient temperature range	-40°C to 85°C
T_{stg}	Storage temperature	-55°C to 150°C
T_J	Junction temperature	150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, $V_{DD}1$-$V_{DD}3$ (= V_{DD}) = V_{CC} = 3.3 V, f_M = 27 MHz, crystal oscillation, f_S = 48 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT						
Logic input			CMOS compatible			
V_{IH}	Input logic level(1)		0.7 V_{DD}		3.6	Vdc
V_{IL}					0.3 V_{DD}	Vdc
I_{IH}	Input logic current(1)	V_{IN} = V_{DD}		65	100	µA
I_{IL}		V_{IN} = 0 V			±10	µA
Logic output			CMOS			
V_{OH}	Output logic level(2)(3)	I_{OH} = -4 mA	V_{DD} - 0.4			Vdc
V_{OL}		I_{OL} = 4 mA			0.4	Vdc
Sampling frequency		Standard f_S	32	44.1	48	kHz
		Double f_S	64	88.2	96	kHz

(1) Pins 5, 6, 7, 12: FS1, FS2, SR, CSEL (Schmitt-trigger input with internal pulldown, 3.3-V tolerant)
(2) Pins 2, 3, 14, 15, 18, 19: SCKO2, SCKO3, MCKO1, MCKO2, SCKO0, SCKO1
(3) Not production tested

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ELECTRICAL CHARACTERISTICS (continued)

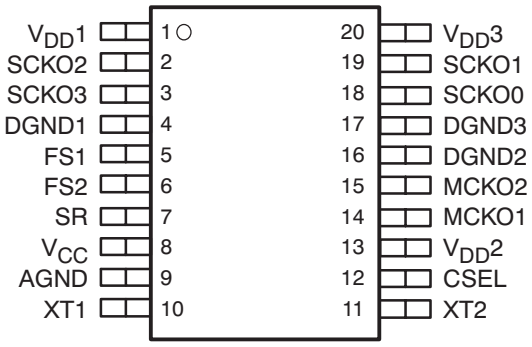
T_A = 25°C, $V_{DD}1$-$V_{DD}3$ (= V_{DD}) = V_{CC} = 3.3 V, f_M = 27 MHz, crystal oscillation, f_S = 48 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MASTER CLOCK (MCKO1, MCKO2) (f_M = 27 MHz, C1 = C2 = 15 pF, C_L = 20 pF on measurement pin)						
	Master clock frequency		26.73	27	27.27	MHz
V_{IH}	Input level(4)(5)		0.7 V_{CC}			V
V_{IL}					0.3 V_{CC}	
I_{IH}	Input current(4)	V_{IN} = V_{CC}			±10	µA
I_{IL}		V_{IN} = 0 V			±10	
	Output voltage(6)			3.5		Vp-p
	Output rise time	20% to 80% of V_{DD}		2		ns
	Output fall time	80% to 20% of V_{DD}		2		ns
	Duty cycle	For crystal oscillation	45	51	55	%
		For external clock		50		
	Clock jitter(7)			50		ps
	Power-up time(8)			0.5	1.5	ms
PLL AC CHARACTERISTICS (SCKO0-SCKO3) (f_M = 27 MHz, C_L = 20 pF on measurement pin)						
SCKO0	Output system clock frequency(9)	Fixed		33.8688		MHz
SCKO1		Selectable for 48 kHz	24.576		36.864	
SCKO2		256 f_S	8.192	12.288	24.576	
SCKO3		384 f_S	12.288	18.432	36.864	
	Output rise time	20% to 80% of V_{DD}		2		ns
	Output fall time	80% to 20% of V_{DD}		2		ns
	Output duty cycle		45	50	55	%
	Output clock jitter(7)(5)	SCKO0, SCKO1		58	100	ps
		SCKO2, SCKO3		50	100	ps
	Frequency settling time(10)	To stated output frequency		50	150	ns
	Power-up time(11)	To stated output frequency		3	6	ms
POWER SUPPLY						
V_{CC}, V_{DD}	Supply voltage		2.7	3.3	3.6	V
I_{DD} + I_{CC}	Supply current(12)	V_{DD} = V_{CC} = 3.3 V, f_S = 48 kHz		19	35	mA
	Power dissipation	V_{DD} = V_{CC} = 3.3 V, f_S = 48 kHz		63	130	mW
TEMPERATURE						
	Operating temperature		-40		85	°C
θ_{JA}	Thermal resistance			150		°C/W

(4) Pin 10: XT1
(5) Not production tested
(6) Pin 11: XT2
(7) Jitter performance is specified as standard deviation of jitter for 27-MHz crystal oscillation and default SCKO frequency setting. Jitter performance varies with master clock mode, SCKO frequency setting and load capacitance on each clock output.
(8) The delay time from power on to oscillation
(9) The MIN and MAX values are the low and high selectable frequencies based on frequency (f_S) selected (see Table 2 through Table 4)
(10) The settling time when the sampling frequency is changed
(11) The delay time from power on to lockup
(12) f_M = 27-MHz crystal oscillation, no load on MCKO1, MCKO2, SCKO0, SCKO1, SCKO2, SCKO3. Power supply current varies with sampling frequency selection and load condition.

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DBQ PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	9	-	Analog ground
CSEL	12	I	SCKO1 frequency selection control(1)
DGND1	4	-	Digital ground 1
DGND2	16	-	Digital ground 2
DGND3	17	-	Digital ground 3
FS1	5	I	Sampling frequency group control 1(1)
FS2	6	I	Sampling frequency group control 2(1)
MCKO1	14	O	27-MHz master clock output 1
MCKO2	15	O	27-MHz master clock output 2
SCKO0	18	O	System clock output 0 (33.8688 MHz fixed)
SCKO1	19	O	System clock output 1 (selectable for 48 kHz)
SCKO2	2	O	System clock output 2 (256 f_S selectable)
SCKO3	3	O	System clock output 3 (384 f_S selectable)
SR	7	I	Sampling rate control(1)
V_{CC}	8	-	Analog power supply, 3.3 V
VDD1	1	-	Digital power supply 1, 3.3 V
VDD2	13	-	Digital power supply 2, 3.3 V
VDD3	20	-	Digital power supply 3, 3.3 V
XT1	10	I	27-MHz crystal oscillator, or external clock input
XT2	11	O	27-MHz crystal oscillator, must be OPEN for external clock input mode

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TYPICAL PERFORMANCE CURVES

All specifications at T_A = 25°C, V_{DD}1-3 (= V_{DD}) = V_{CC} = +3.3 V, f_M = 27 MHz, crystal oscillation, C1, C2 = 15 pF, default frequency (33.8688 MHz for SCKO0, 36.864 MHz for SCKO1, 256 f_S and 384 f_S of 48 kHz for SCKO2 and SCKO3), C_L = 20 pF on measurement pin, unless otherwise noted.

JITTER
vs
SAMPLING FREQUENCY

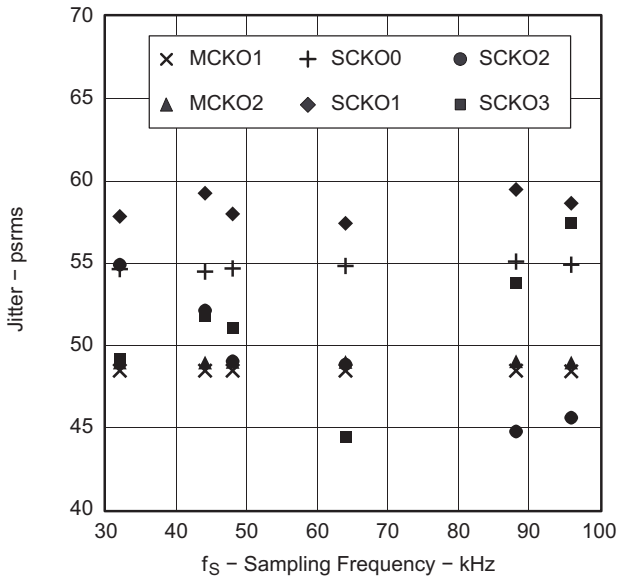


Figure 1.

JITTER
vs
LOAD CAPACITANCE

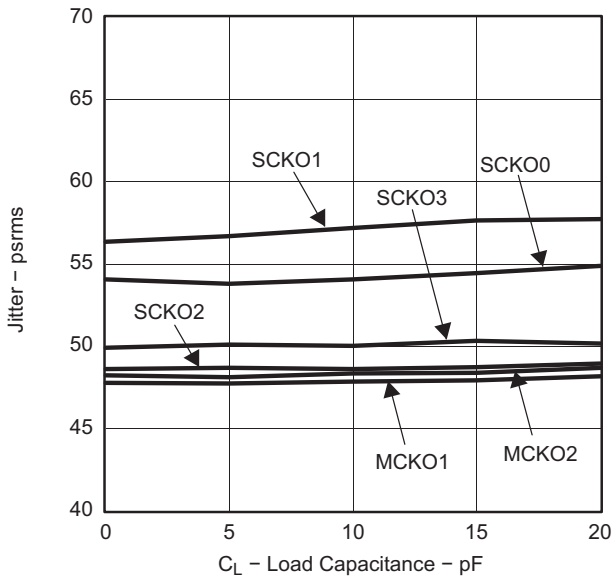


Figure 2.

JITTER
vs
SUPPLY VOLTAGE

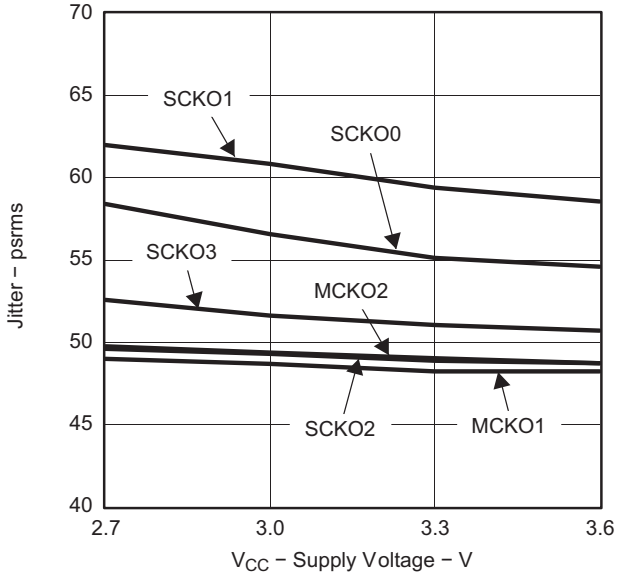


Figure 3.

JITTER
vs
FREE-AIR TEMPERATURE

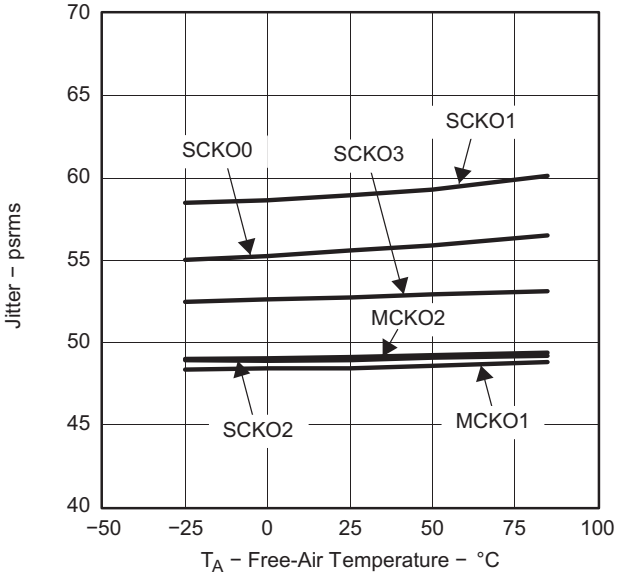


Figure 4.

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TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{DD}1-3 (= V_{DD}) = V_{CC} = +3.3 V, f_M = 27 MHz, crystal oscillation, C1, C2 = 15 pF, default frequency (33.8688 MHz for SCKO0, 36.864 MHz for SCKO1, 256 f_S and 384 f_S of 48 kHz for SCKO2 and SCKO3), C_L = 20 pF on measurement pin, unless otherwise noted.

DUTY CYCLE
vs
SUPPLY VOLTAGE

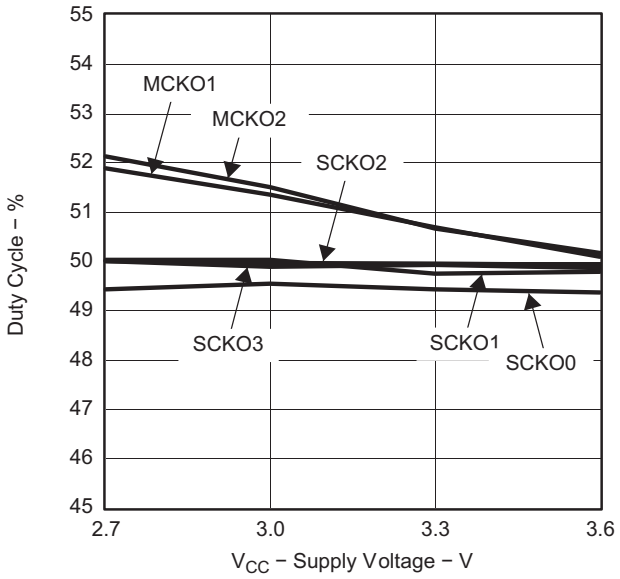


Figure 5.

DUTY CYCLE
vs
FREE-AIR TEMPERATURE

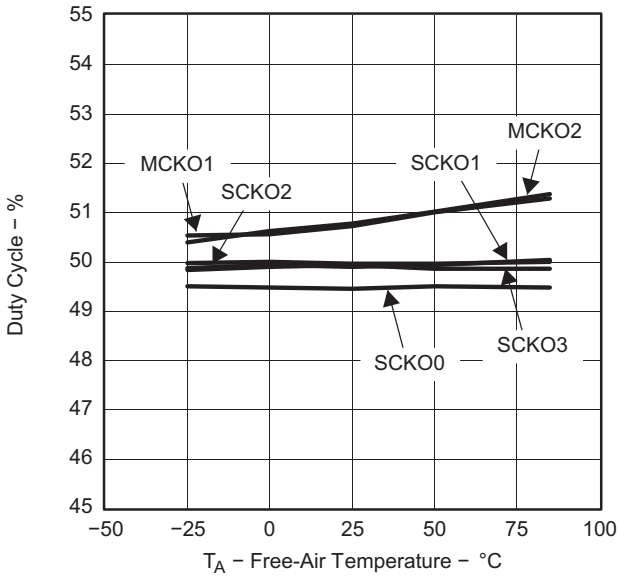


Figure 6.

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THEORY OF OPERATION

Master Clock and System Clock Output

The PLL1707 consists of a dual PLL clock and master clock generator which generates four system clocks and two buffered 27-MHz clocks from a 27-MHz master clock. Figure 7 shows the block diagram of the PLL1707. The PLL is designed to accept a 27-MHz master clock.

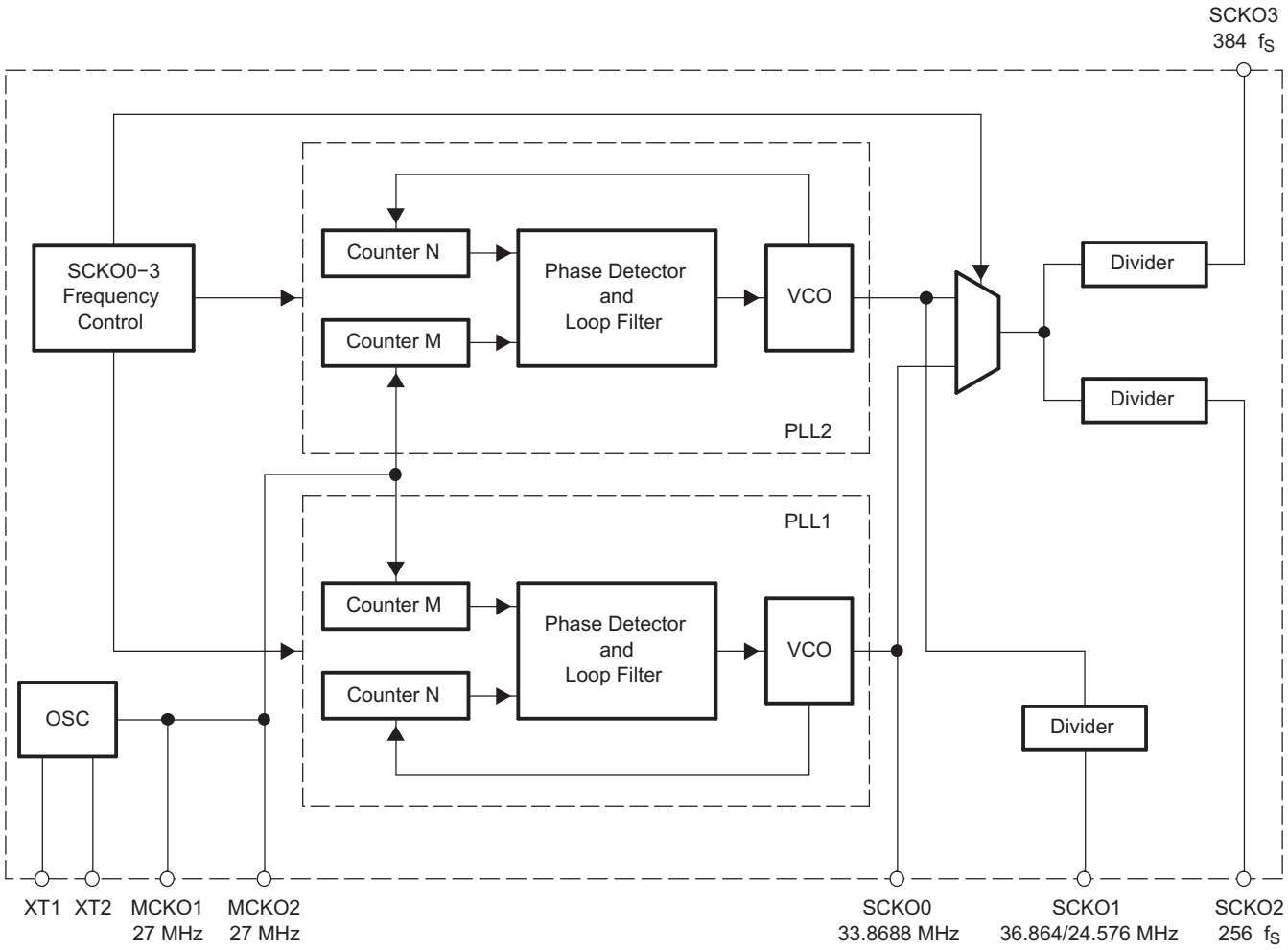


Figure 7. Block Diagram

The master clock can be either a crystal oscillator placed between XT1 (pin 10) and XT2 (pin 11), or an external input to XT1. If an external master clock is used, XT2 must be open. Figure 8 illustrates possible system clock connection options, and Figure 9 illustrates the 27-MHz master clock timing requirement.

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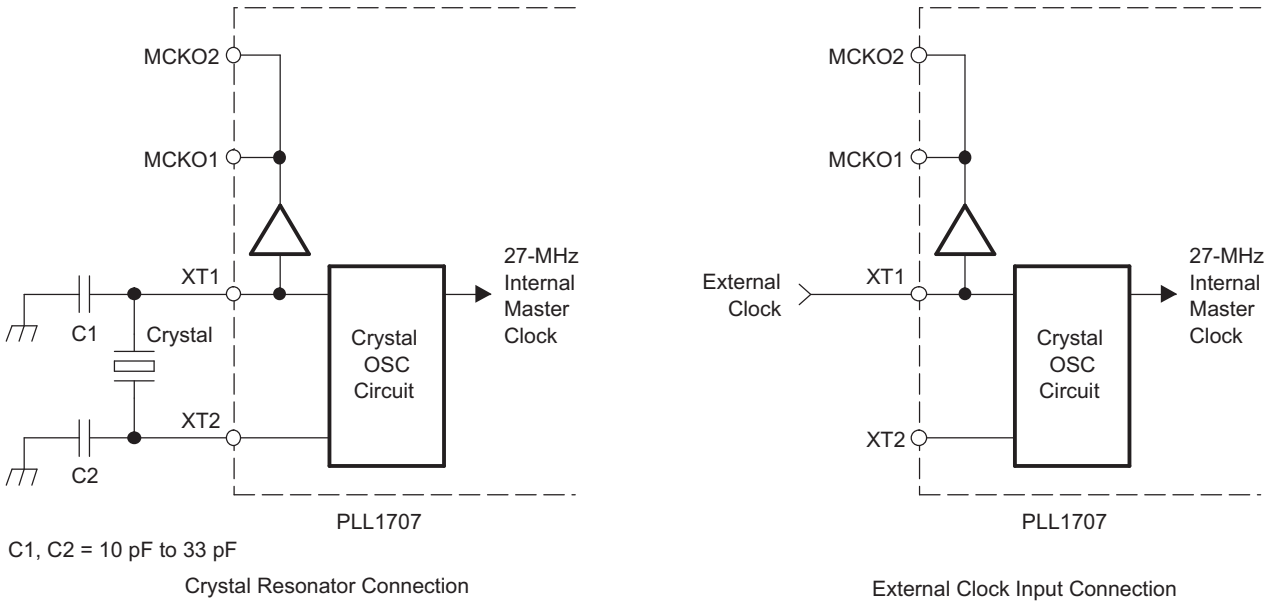


Figure 8. Master Clock Generator Connection Diagram

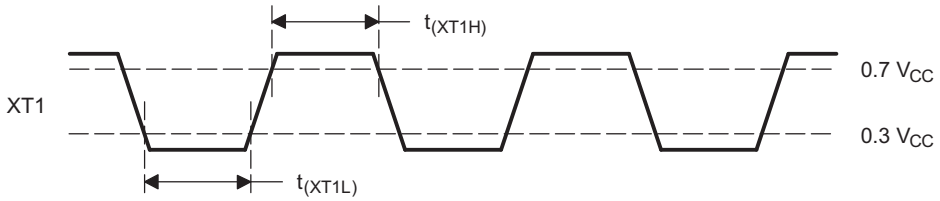


Figure 9. External Master Clock Timing Requirements

Table 1. External Master Clock Timing Requirements

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
Master clock pulse duration HIGH	$t_{(XT1H)}$	10		ns
Master clock pulse duration LOW	$t_{(XT1L)}$	10		ns

The PLL1707 provides a very low-jitter high-accuracy clock. SCKO0 outputs a fixed 33.8688-MHz clock, SCKO1 outputs 512 f_S or 768 f_S (f_S = 48 kHz), which is selected by hardware or software control (see Table 2). The output frequency of the remaining clocks is determined by the sampling frequency (f_S) under hardware or software control. SCKO2 and SCKO3 output 256-fS and 384-fS system clocks, respectively. Table 3 shows each sampling frequency which can be programmed. The system clock output frequencies for programmed sampling frequencies are shown in Table 4.

Table 2. Generated System Clock SCKO1 Frequency

f_S	SCKO1 FREQUENCY
512 f_S	24.576 MHz
768 f_S	36.864 MHz

Table 3. Sampling Frequencies

SAMPLING RATE	SAMPLING FREQUENCY (kHz)		
Standard sampling frequencies	32	44.1	48
Double sampling frequencies	64	88.2	96

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Table 4. Sampling Frequencies and System Clock Output Frequencies

SAMPLING FREQUENCY (kHz)	SAMPLING RATE	256 f_S SCKO2 (MHZ)	384 f_S SCKO3 (MHZ)
32	Standard	8.192	12.288
44.1	Standard	11.2896	16.9344
48	Standard	12.288	18.432
64	Double	16.384	24.576
88.2	Double	22.5792	33.8688
96	Double	24.576	36.864

Response time from power on (or applying the clock to XT1) to SCKO settling time is typically 3 ms. Delay time from sampling frequency change to SCKO settling is 300 ns maximum.

The delay time for hardware control to use SR, FS2, FS1, or CSEL is 150 ns maximum. Figure 10 illustrates SCKO transient timing in the PLL1707. Clock transient timing is not synchronized with the SCKOs. External buffers are recommended on all output clocks in order to avoid degrading the jitter performance of the PLL1707.

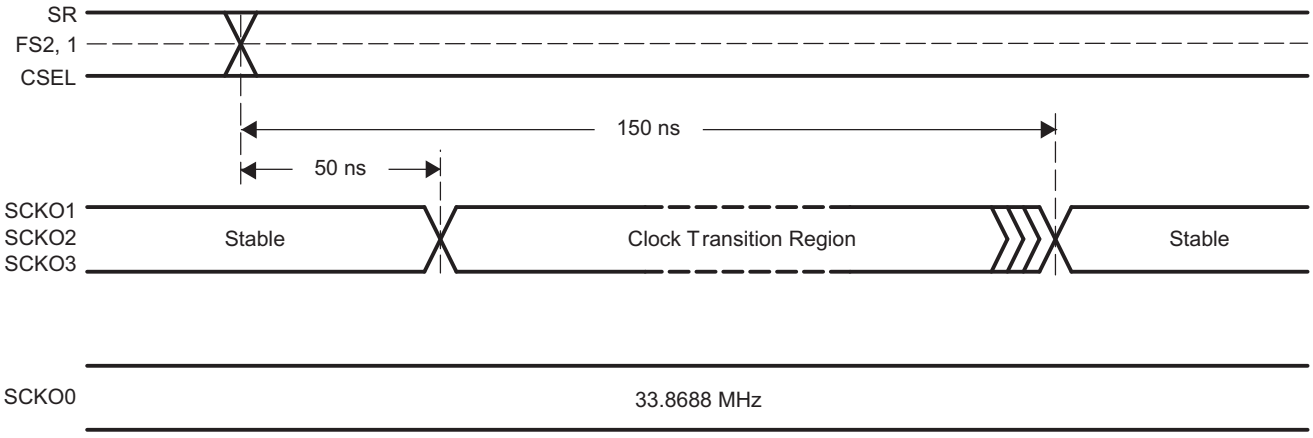


Figure 10. SCKO Transient Timing

Power-On Reset

The PLL1707 has an internal power-on reset circuit. Throughout the reset period, all clock outputs are enabled with the default settings after power-up time. Initialization by internal power-on reset is done automatically during 1024 master clocks at V_{DD} > 2.0 V (TYP). Power-on reset timing is shown in Figure 11.

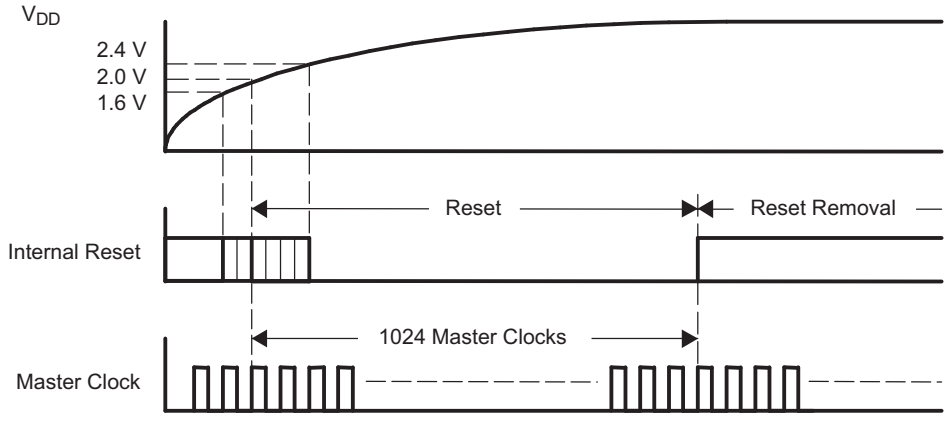


Figure 11. Power-On Reset Timing

Functional Control

The built-in functions of the PLL1707 can be controlled in the parallel mode (hardware mode), which uses SR (pin 7), FS1 (pin 5) and FS2 (pin 6). The selectable functions are shown in Table 5.

Table 5. Selectable Functions

SELECTABLE FUNCTION	PARALLEL MODE
Sampling frequency select (32 kHz, 44.1 kHz, 48 kHz)	Yes
Sampling rate select (standard/double)	Yes

PLL1707 (Parallel Mode)

In the parallel mode, the following functions can be selected:

Sampling Frequency Group Select

The sampling frequency group can be selected by FS1 (pin 5) and FS2 (pin 6).

Table 6. Sampling Frequency Group Select

FS2 (PIN 6)	FS1 (PIN 5)	SAMPLING FREQUENCY
LOW	LOW	48 kHz
LOW	HIGH	44.1 kHz
HIGH	LOW	32 kHz
HIGH	HIGH	Reserved

Sampling Rate Select

The sampling rate can be selected by SR (pin 7)

Table 7. Sampling Rate Select

SR (PIN 7)	SAMPLING RATE
LOW	Standard
HIGH	Double

System Clock SCKO1 Frequency Select

System clock SCKO1 frequency can be selected by CSEL (pin 12).

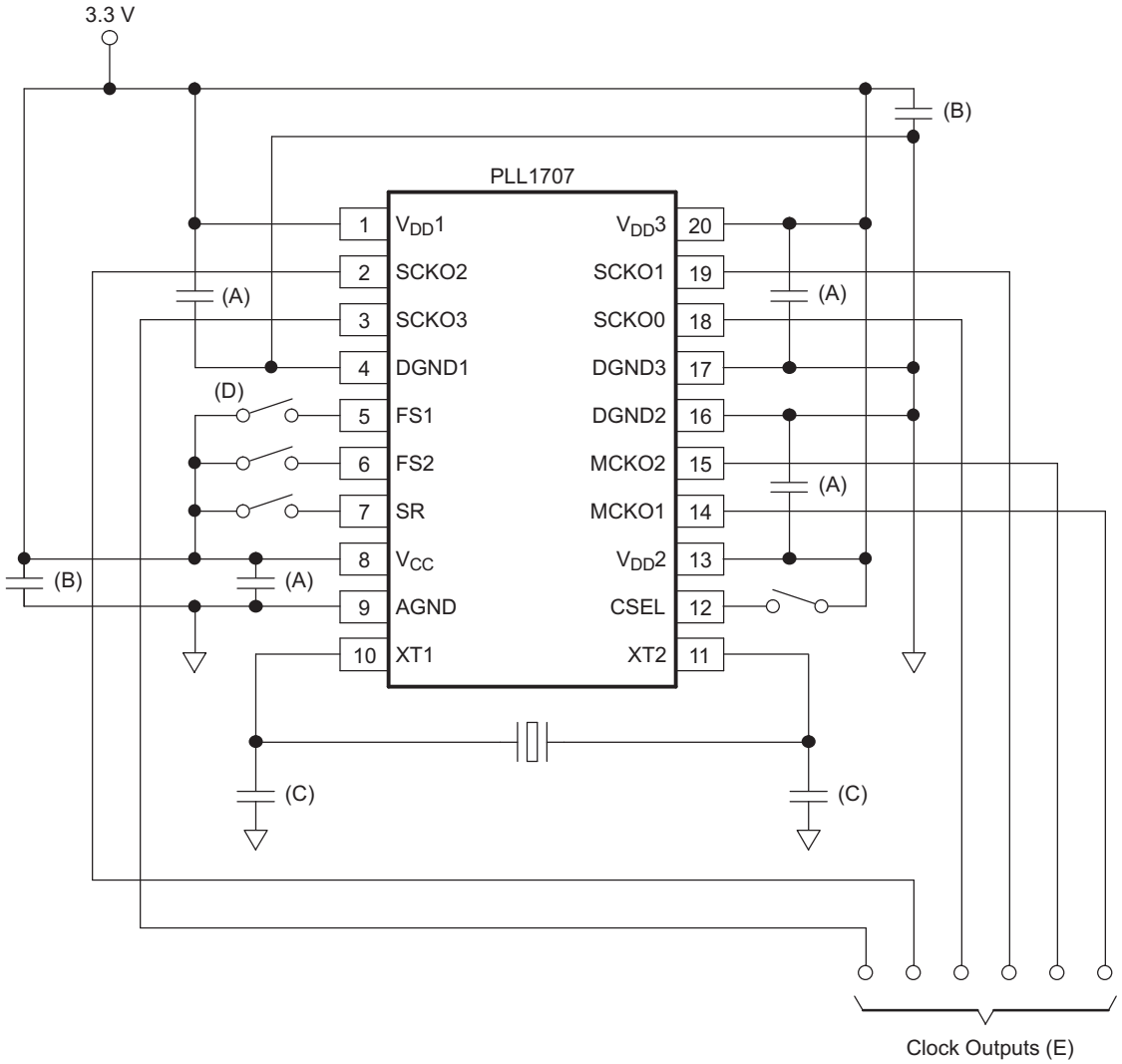
Table 8. System Clock SCKO1 Frequency Select

CSEL (PIN 12)	SCKO1 FREQUENCY
LOW	36.864 MHz
HIGH	24.576 MHz

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Connection Diagram

Figure 12 shows the typical connection circuit for the PLL1707. There are four grounds for digital and analog power supplies. However, the use of one common ground connection is recommended to avoid latch-up or other power-supply-related troubles. Power supplies should be bypassed as close as possible to the device.



A. 0.1-μF ceramic capacitor typical, depending on quality of power supply and pattern layout

B. 10-μF aluminum electrolytic capacitor typical, depending on quality of power supply and pattern layout

C. 27-MHz quartz crystal and 10 pF to 33 pF × 2 ceramic capacitors, which generate the appropriate amplitude of oscillation on XT1/XT2

D. This connection is for PLL1707 (parallel mode)

E. For good jitter performance, minimize the load capacitance on the clock output. It is recommended to drive the clock outputs through buffers, especially if there are heavy loads on SCKO0 and SCKO1, and to minimize mutual interference by separating them or inserting a guard pattern between them.

Figure 12. Typical Connection Diagram

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MPEG-2 Applications

Typical applications for the PLL1707 are MPEG-2 based systems such as DVD recorders, HDD recorders, DVD players, DVD add-on cards for multimedia PCs, digital HDTV systems, and set-top boxes. The PLL1707 provides audio system clocks for a CD-DA DSP, DVD DSP, Karaoke DSP, ADC(s), and DAC(s) from a 27-MHz video clock.

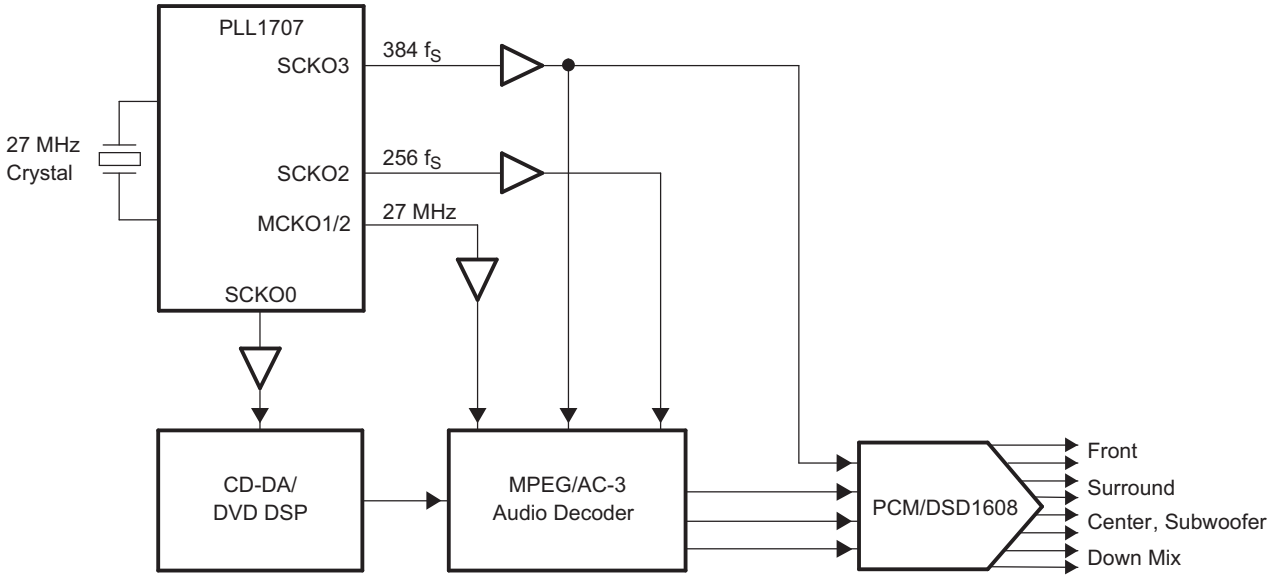


Figure 13. Block Diagram of DVD Player Application

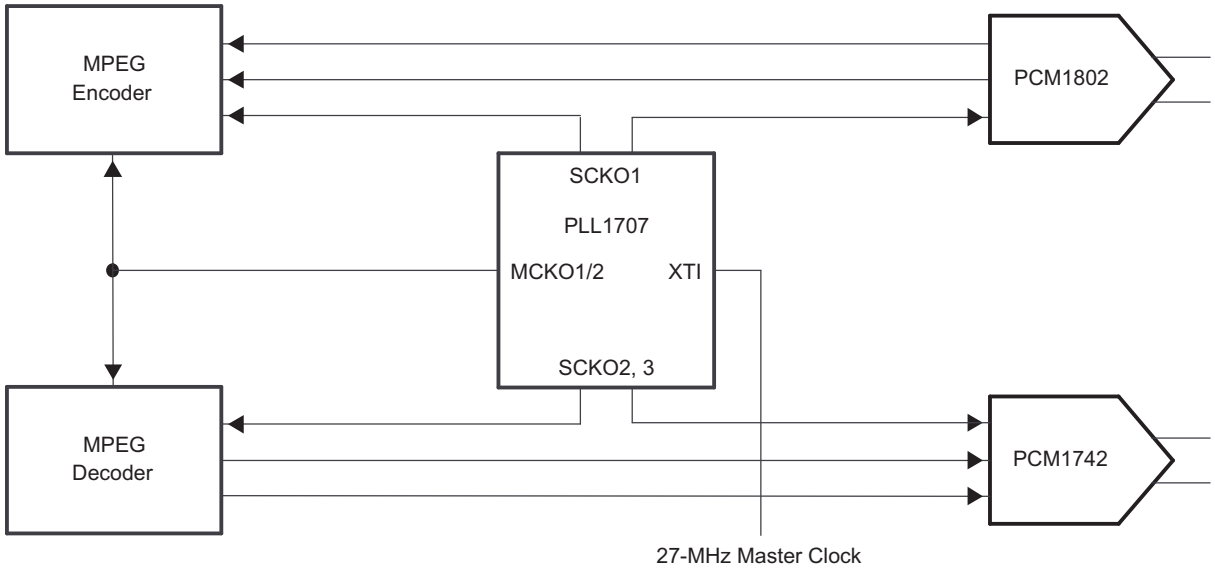


Figure 14. Block Diagram of HDD+DVD Recorder Application

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PLL1707IDBQRQ1	ACTIVE	SSOP	DBQ	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PLL1707I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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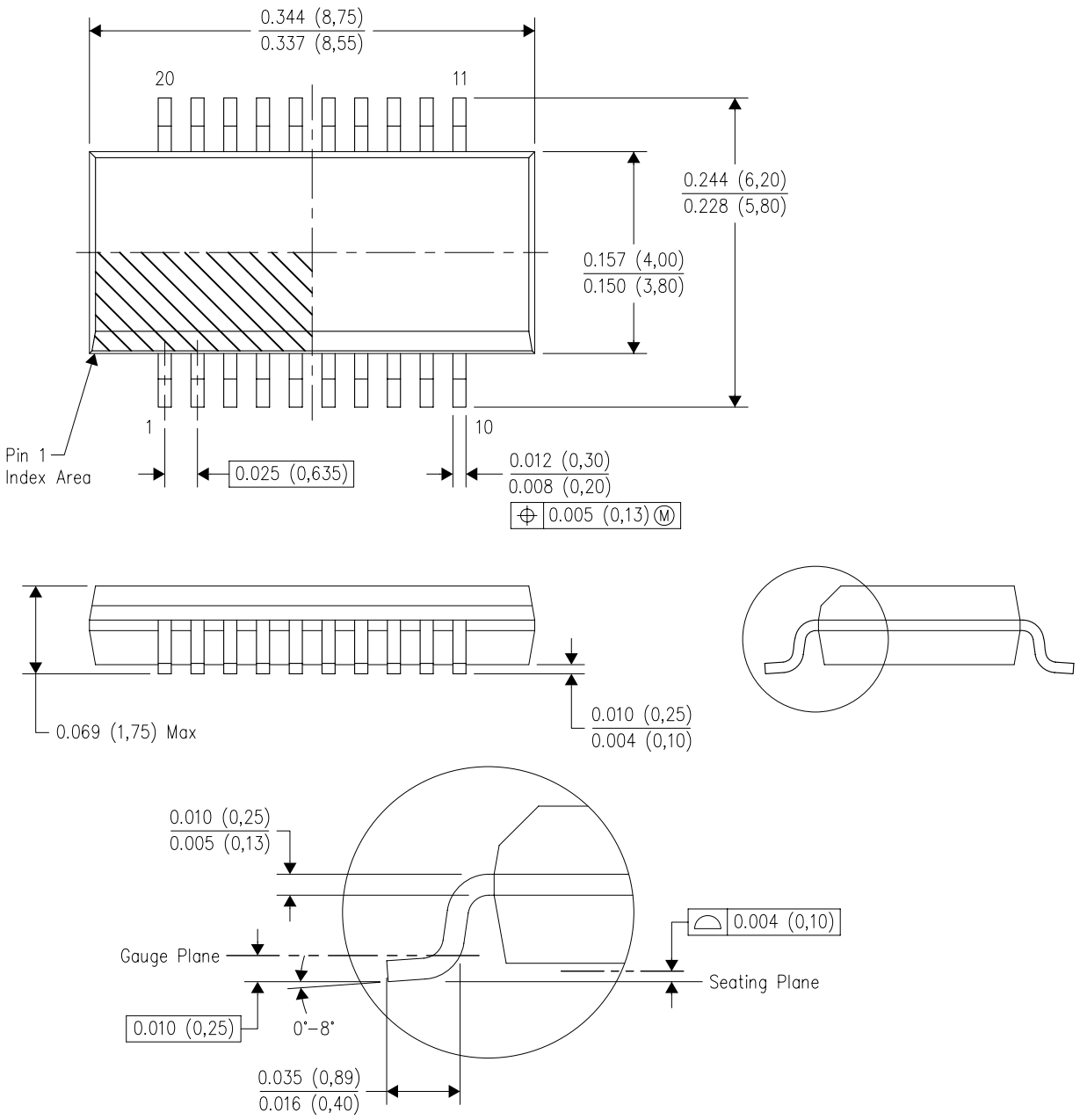
OTHER QUALIFIED VERSIONS OF PLL1707-Q1 :

- Catalog: PLL1707

NOTE: Qualified Version Definitions:

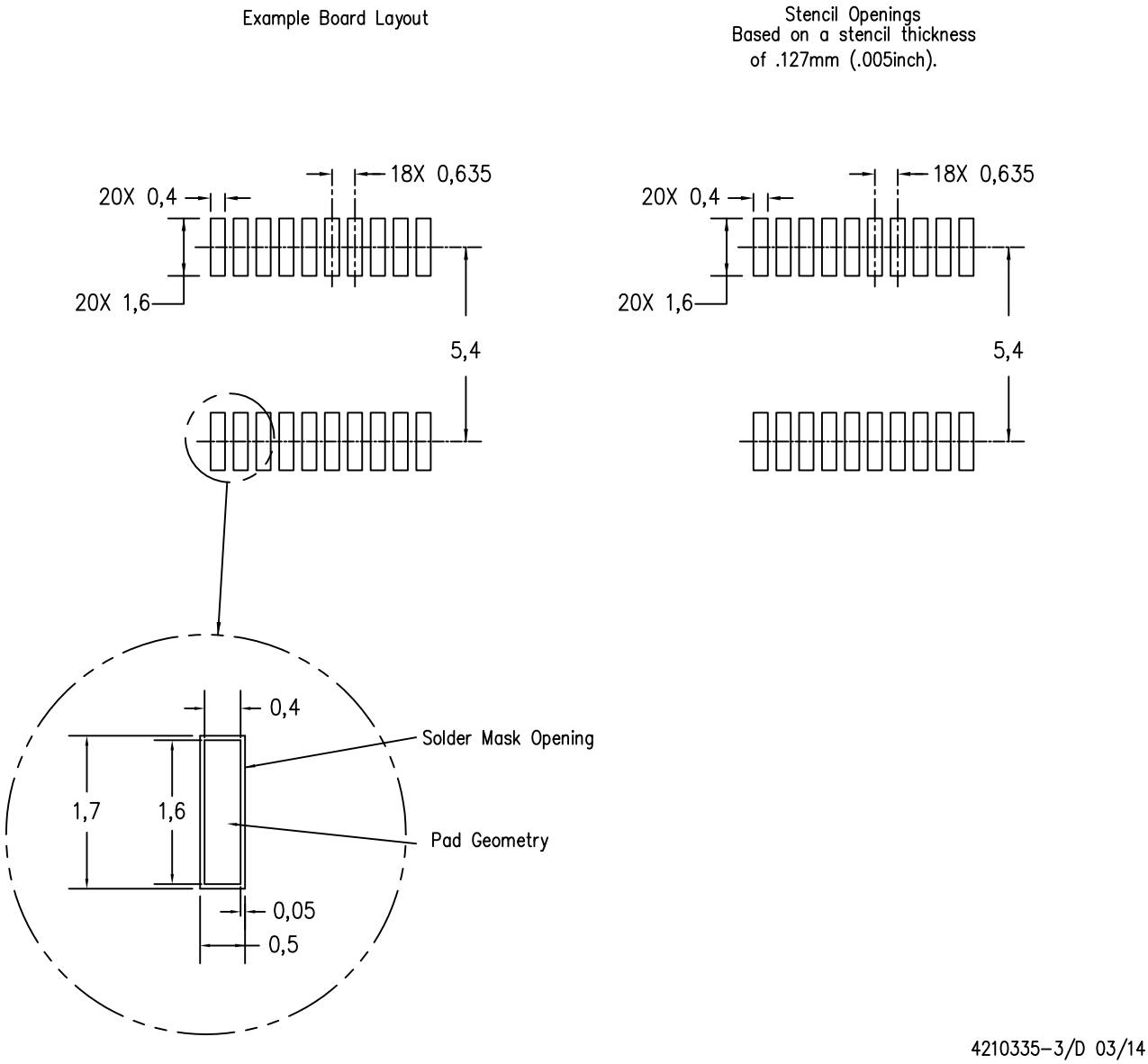
- Catalog - TI's standard catalog product

DBQ (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AD.

DBQ (R–PDSO–G20) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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