Document Number: A3G26H501W17S
Rev. 2, 01/2020

RoHS

RF Power GaN Transistor

A3G26H501W17S

2496–2690 MHz, 56 W AVG., 48 V AIRFAST RF POWER GaN TRANSISTOR

This 56 W asymmetrical Doherty RF power GaN transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 2496 to 2690 MHz.

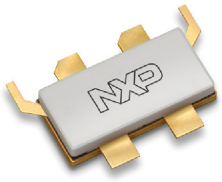
This part is characterized and performance is guaranteed for applications operating in the 2496 to 2690 MHz band. There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

2600 MHz

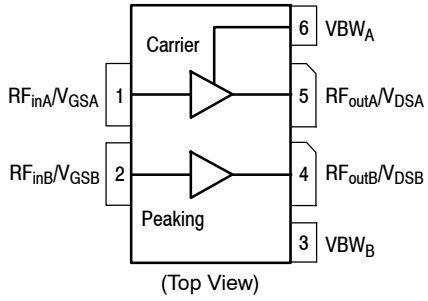
- Typical Doherty Single-Carrier W-CDMA Characterization Performance: V_{DD} = 48 Vdc, I_{DQA} = 350 mA, V_{GSB} = −5.0 Vdc, P_{out} = 56 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. (1)

Frequency	G_{ps} (dB)	η_D (%)	P3dB (dBm)(2)	ACPR (dBc)
2496 MHz	14.0	46.3	56.6	–35.4
2590 MHz	14.5	45.1	57.1	–36.6
2690 MHz	14.4	47.4	56.0	–33.2

1. All data measured in fixture with device soldered to heatsink.
2. Data measured at pulsed CW, 10 μsec(on), 10% duty cycle.



NI-780S-4S2S



(Top View)

Figure 1. Pin Connections

Features

- High terminal impedances for optimal broadband performance
- Advanced high performance in-package Doherty
- Improved linearized error vector magnitude with next generation signal
- Able to withstand extremely high output VSWR and broadband operating conditions

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	125	Vdc
Gate-Source Voltage	V_{GS}	–8, 0	Vdc
Operating Voltage	V_{DD}	0 to +55	Vdc
Maximum Forward Gate Current, $I_{G\ (A+B)}$, @ T_C = 25°C	I_{GMAX}	66	mA
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–55 to +150	°C
Operating Active Die Surface Temperature Range	T_J	–55 to +225	°C
Maximum Channel Temperature (1)	T_{CH}	275	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance by Infrared Measurement, Active Die Surface-to-Case Case Temperature 93°C, P_D = 80 W	$R_{\theta JC}$ (IR)	0.90 (2)	°C/W
Thermal Resistance by Finite Element Analysis, Channel-to-Case Case Temperature 90°C, P_D = 80 W	$R_{\theta CHC}$ (FEA)	1.23 (3)	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JS-001-2017)	1C
Charge Device Model (per JS-002-2014)	C3

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Drain-Source Breakdown Voltage (V_{GS} = –8 Vdc, I_D = 24 mAdc) Carrier (V_{GS} = –8 Vdc, I_D = 42 mAdc) Peaking	$V_{(BR)DSS}$	 150 150	—	—	Vdc
On Characteristics — Side A, Carrier					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 20 mAdc)	$V_{GS(th)}$	–3.5	–2.8	–2.3	Vdc
Gate Quiescent Voltage (V_{DD} = 48 Vdc, I_{DA} = 350 mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	–3.1	–2.7	–2.4	Vdc
Gate-Source Leakage Current (V_{DS} = 150 Vdc, V_{GS} = –8 Vdc)	I_{GSS}	–9.9	—	—	mAdc
On Characteristics — Side B, Peaking					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 20 mAdc)	$V_{GS(th)}$	–3.8	–3.3	–2.3	Vdc
Gate-Source Leakage Current (V_{DS} = 150 Vdc, V_{GS} = –8 Vdc)	I_{GSS}	–9.9	—	—	mAdc

1. Reliability tests were conducted at 225°C. Operations with T_{CH} at 275°C will reduce median time to failure.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
3. $R_{\theta CHC}$ (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression MTTF (hours) = $10^{[A + B/(T + 273)]}$, where T is the channel temperature in degrees Celsius, A = –11.1 and B = 8366.
4. Each side of device measured separately.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1) (In NXP Doherty Production Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, I_{DQA} = 350 mA, V_{GSB} = −5 Vdc, P_{out} = 56 W Avg., f = 2690 MHz, Single−Carrier W−CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset. **[See note on correct biasing sequence.]**					
Power Gain	G_{ps}	12.7	13.7	15.7	dB
Drain Efficiency	η_D	37.0	40.7	—	%
P_{out} @ 3 dB Compression Point, CW	P3dB	55.5	56.4	—	dBm
Adjacent Channel Power Ratio	ACPR	—	−33.2	−29.0	dBc
Wideband Ruggedness (In NXP Doherty Production Test Fixture, 50 ohm system) I_{DQA} = 350 mA, V_{GSB} = −5 Vdc, f = 2590 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR					
ISBW of 400 MHz at 55 Vdc, 194 W Avg. Modulated Output Power (8 dB Input Overdrive from 56 W Avg. Modulated Output Power)	No Device Degradation				
Typical Performance (In NXP Doherty Production Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, I_{DQA} = 350 mA, V_{GSB} = −5 Vdc, 2496−2690 MHz Bandwidth					
P_{out} @ 3 dB Compression Point (2)	P3dB	—	500	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2496−2690 MHz bandwidth)	Φ	—	−12	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	160	—	MHz
Gain Flatness in 194 MHz Bandwidth @ P_{out} = 56 W Avg.	G_F	—	0.4	—	dB
Gain Variation over Temperature (−40°C to +85°C)	ΔG	—	0.018	—	dB/°C
Output Power Variation over Temperature (−40°C to +85°C)	ΔP1dB	—	0.008	—	dB/°C

Table 5. Ordering Information

Device	Tape and Reel Information	Package
A3G26H501W17SR3	R3 Suffix = 250 Units, 44 mm Tape Width, 13−inch Reel	NI−780S−4S2S

1. Part internally input matched.
2. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W−CDMA single−carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

NOTE: Correct Biasing Sequence for GaN Depletion Mode Transistors

Turning the device ON

1. Set V_{GS} to −5 V
2. Turn on V_{DS} to nominal supply voltage (48 V)
3. Increase V_{GS} until I_{DS} current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce V_{GS} down to −5 V
3. Reduce V_{DS} down to 0 V (Adequate time must be allowed for V_{DS} to reduce to 0 V to prevent severe damage to device.)
4. Turn off V_{GS}

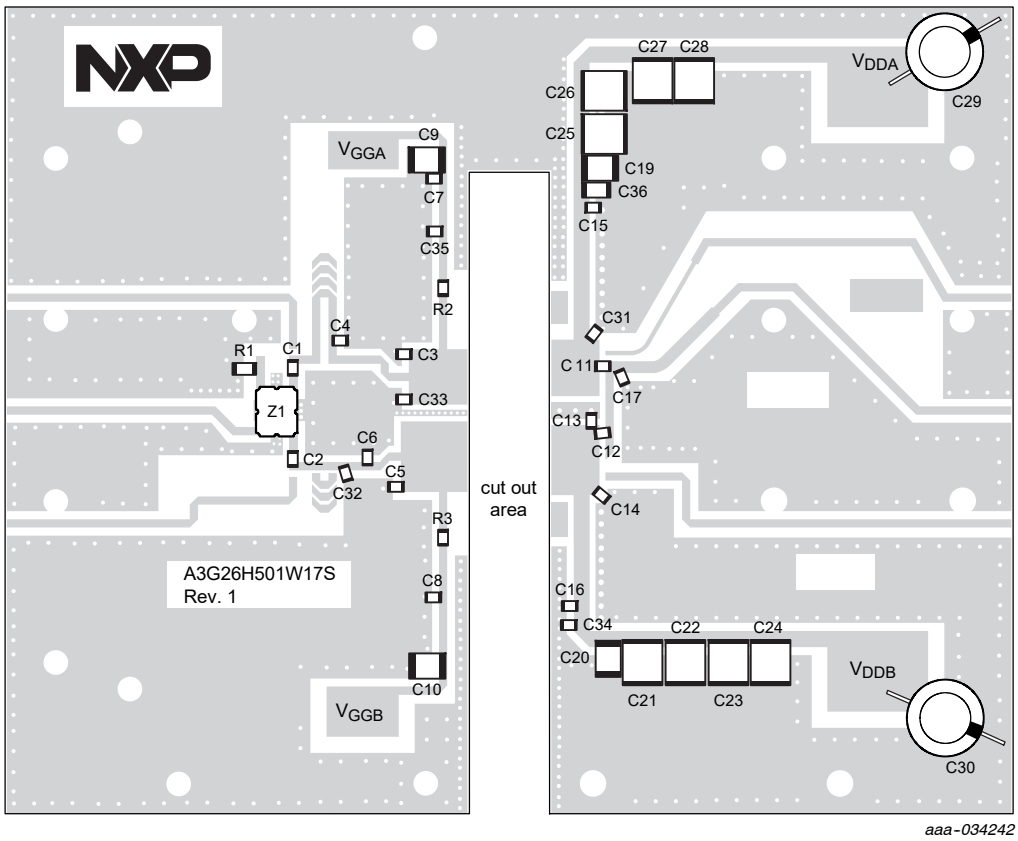
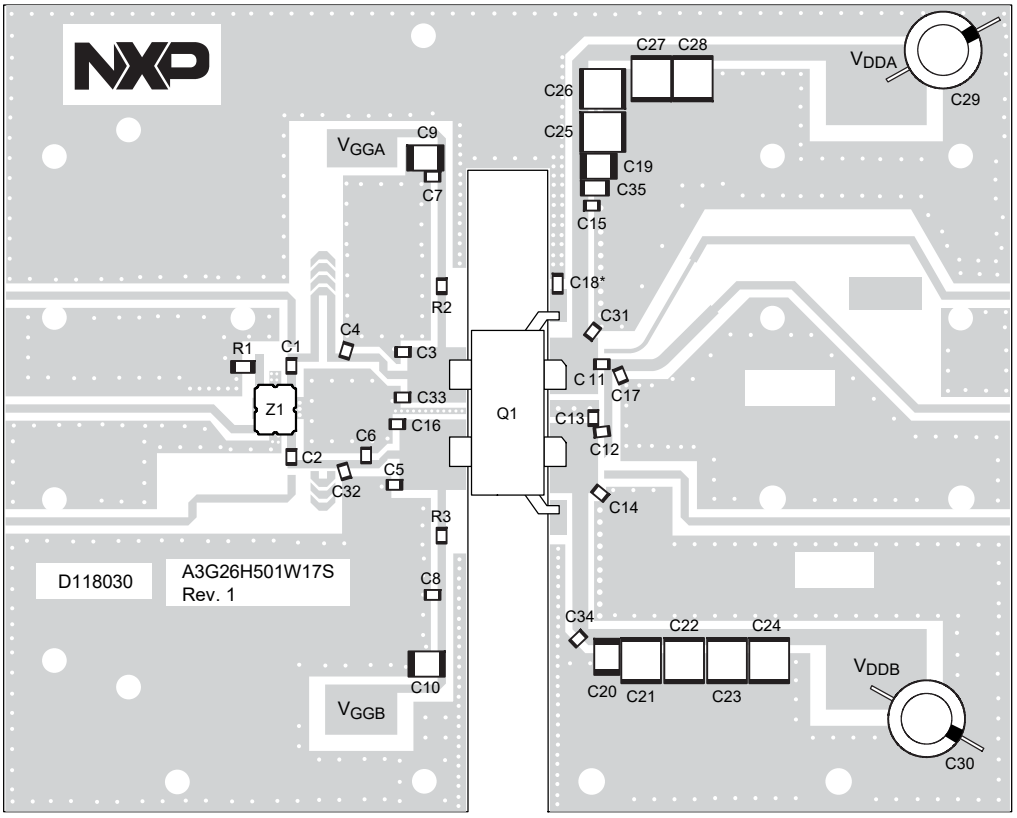


Figure 2. A3G26H501W17S Production Test Circuit Component Layout

Table 6. A3G26H501W17S Production Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C7, C8, C15, C16, C35	6.8 pF Chip Capacitor	GQM2195C2E6R8BB12D	Murata
C3, C33	0.8 pF Chip Capacitor	GQM2195C2ER80BB12D	Murata
C4	1.2 pF Chip Capacitor	GQM2195C2E1R2BB12D	Murata
C5	1.6 pF Chip Capacitor	GQM2195C2E1R6BB12D	Murata
C6	1.5 pF Chip Capacitor	GQM2195C2E1R5BB12D	Murata
C9, C10	2.2 μF Chip Capacitor	GRM31CR71H225KA88L	Murata
C11	3.9 pF Chip Capacitor	GQM2195C2E3R9BB12D	Murata
C12	2.2 pF Chip Capacitor	GQM2195C2E2R2BB12D	Murata
C13	0.6 pF Chip Capacitor	GQM2195C2ER60BB12D	Murata
C14	0.5 pF Chip Capacitor	GQM2195C2ER50BB12D	Murata
C17, C31	0.2 pF Chip Capacitor	GQM2195C2ER20BB12D	Murata
C19, C20	4.7 μF Chip Capacitor	C4532X7S2A475M	TDK
C21, C22, C23, C24, C25, C26, C27, C28	15 μF Chip Capacitor	C5750X7S2A156M	TDK
C29, C30	220 μF, 100 V Electrolytic Capacitor	MCGPR100V227M16X26	Multicomp
C32	1.0 pF Chip Capacitor	GQM2195C2E1R0BB12D	Murata
C34	8.2 pF Chip Capacitor	GQM2195C2E8R2BB12D	Murata
C36	15 nF Chip Capacitor	C3225CH2A153J	TDK
R1	50 Ω, 8 W Termination Chip Resistor	C8A50Z4A	Anaren
R2, R3	3.3 Ω, 1/4 W Chip Resistor	CRCW08053R30JNEA	Vishay
Z1	2300–2700 MHz Band, 5 dB Directional Coupler	X3C25P1-05S	Anaren
PCB	Rogers RO3035, 0.020″, ε_r = 3.6	—	MTL

Note: Component number C18 is intentionally omitted.



*C18 is mounted vertically.

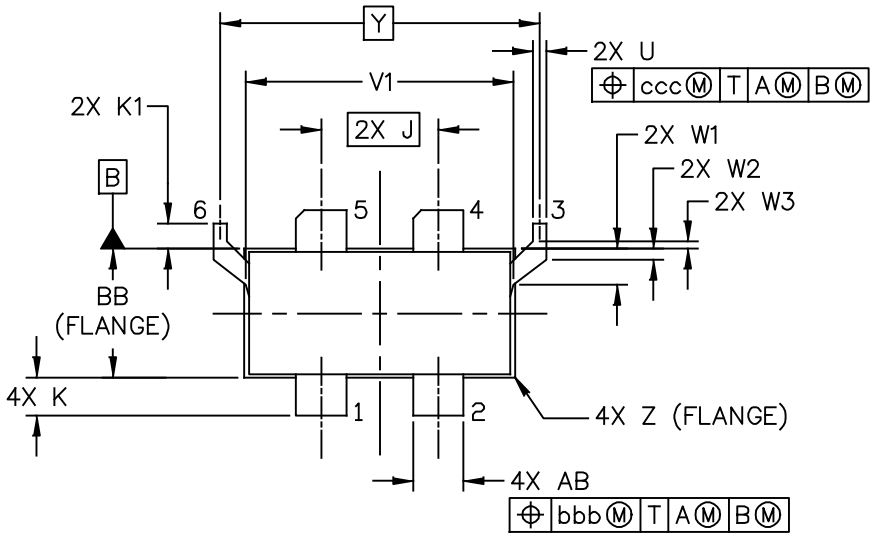
Note: All data measured in fixture with device soldered to heatsink.

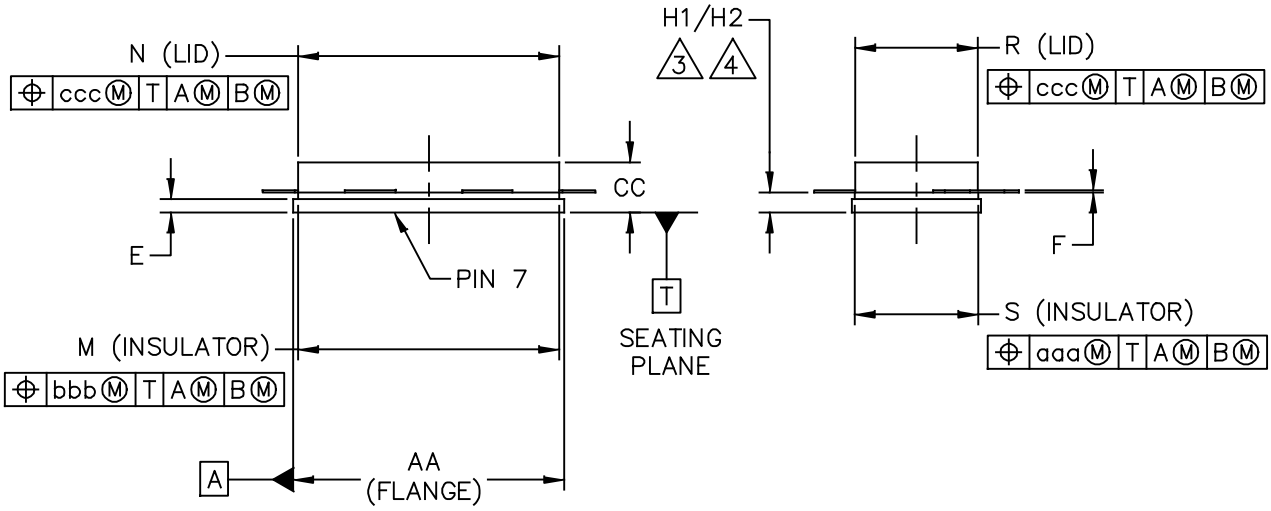
Figure 3. A3G26H501W17S Characterization Test Circuit Component Layout

Table 7. A3G26H501W17S Characterization Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C7, C8, C15	6.8 pF Chip Capacitor	GQM2195C2E6R8BB12D	Murata
C3, C33	0.8 pF Chip Capacitor	GQM2195C2ER80BB12D	Murata
C4	1.2 pF Chip Capacitor	GQM2195C2E1R2BB12D	Murata
C5	1.6 pF Chip Capacitor	GQM2195C2E1R6BB12D	Murata
C6	1.5 pF Chip Capacitor	GQM2195C2E1R5BB12D	Murata
C9, C10	2.2 μF Chip Capacitor	GRM31CR71H225KA88L	Murata
C11	3.9 pF Chip Capacitor	GQM2195C2E3R9BB12D	Murata
C12	5.6 pF Chip Capacitor	GQM2195C2E2R2BB12D	Murata
C13	0.6 pF Chip Capacitor	GQM2195C2ER60BB12D	Murata
C14	0.5 pF Chip Capacitor	GQM2195C2ER50BB12D	Murata
C16	0.3 pF Chip Capacitor	GQM2195C2ER30BB12D	Murata
C17, C31	0.2 pF Chip Capacitor	GQM2195C2ER20BB12D	Murata
C18, C19, C20	4.7 μF Chip Capacitor	C4532X7S2A475M	TDK
C21, C22, C23, C24, C25, C26, C27, C28	15 μF Chip Capacitor	C5750X7S2A156M	TDK
C29, 30	220 μF, 100 V Electrolytic Capacitor	MCGPR100V227M16X26	Multicomp
C32	1.0 pF Chip Capacitor	GQM2195C2E1R0BB12D	Murata
C34	8.2 pF Chip Capacitor	GQM2195C2E8R2BB12D	Murata
C35	15 nF Chip Capacitor	C3225CH2A153J	TDK
Q1	RF Power LDMOS Transistor	A3G26H501W17S	NXP
R1	50 Ω, 8 W Termination Chip Resistor	C8A50Z4A	Anaren
R2, R3	3.3 Ω, 1/4 W Chip Resistor	CRCW08053R30JNEA	Vishay
Z1	2300–2700 MHz Band, 5 dB Directional Coupler	X3C25P1-05S	Anaren
PCB	Rogers RO3035, 0.020″, ε_r = 3.6	D118030	MTL

PACKAGE DIMENSIONS





© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: NI-780S-4S2S	DOCUMENT NO: 98ASA01208D	REV: O
	STANDARD: NON-JEDEC	
	SOT1799-6	14 AUG 2018

NOTES:

1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B TO CLEAR EPOXY FLOW OUT. H1 APPLIES TO PINS 1, 2, 4 & 5. H2 APPLIES TO PINS 3 & 6.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.805	.815	20.45	20.70	R	.365	.375	9.27	9.53
BB	.380	.390	9.65	9.91	S	.365	.375	9.27	9.53
CC	.125	.170	3.18	4.32	U	.035	.045	0.89	1.14
E	.035	.045	0.89	1.14	V1	.795	.805	20.19	20.45
F	.004	.007	0.10	0.18	W1	.0975	.1175	2.48	2.98
H1	.057	.067	1.45	1.70	W2	.0225	.0425	0.57	1.08
H2	.054	.070	1.37	1.78	W3	.0125	.0325	0.32	0.83
J	.350 BSC		8.89 BSC		Y	.956 BSC		24.28 BSC	
K	.0995	.1295	2.53	3.29	Z	R.000	R.040	R0.00	R1.02
K1	.070	.090	1.78	2.29	AB	.145	.155	3.68	3.94
M	.774	.786	19.66	19.96	aaa	.005		0.13	
N	.772	.788	19.61	20.02	bbb	.010		0.25	
					ccc	.015		0.38	

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASA01208D	REV: O
NI–780S–4S2S	STANDARD: NON–JEDEC	
	SOT1799–6	14 AUG 2018

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1908: Solder Reflow Attach Method for High Power RF Devices in Air Cavity Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- .s2p File

Development Tools

- Printed Circuit Boards

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	June 2019	• Initial release of data sheet
1	Aug. 2019	• Fig. 2, Production Test Circuit Component Layout: C18 component omitted, p. 4 • Table 6, Production Test Circuit Component Layout Parts List: C18 component omitted, updated the part number and description for R1, added note, p. 4 • Table 7, Characterization Component Layout Parts List: updated the part number and description for R1, p. 5
2	Jan. 2020	• Functional Tests table: updated Drain Efficiency Min value from 35.5% to 37.0% to reflect tightened minimum test specification limit, p. 3

How to Reach Us:

Home Page:
nxp.com

Web Support:
nxp.com/support

Document Number: A3G26H501W17S
Rev. 2, 01/2020