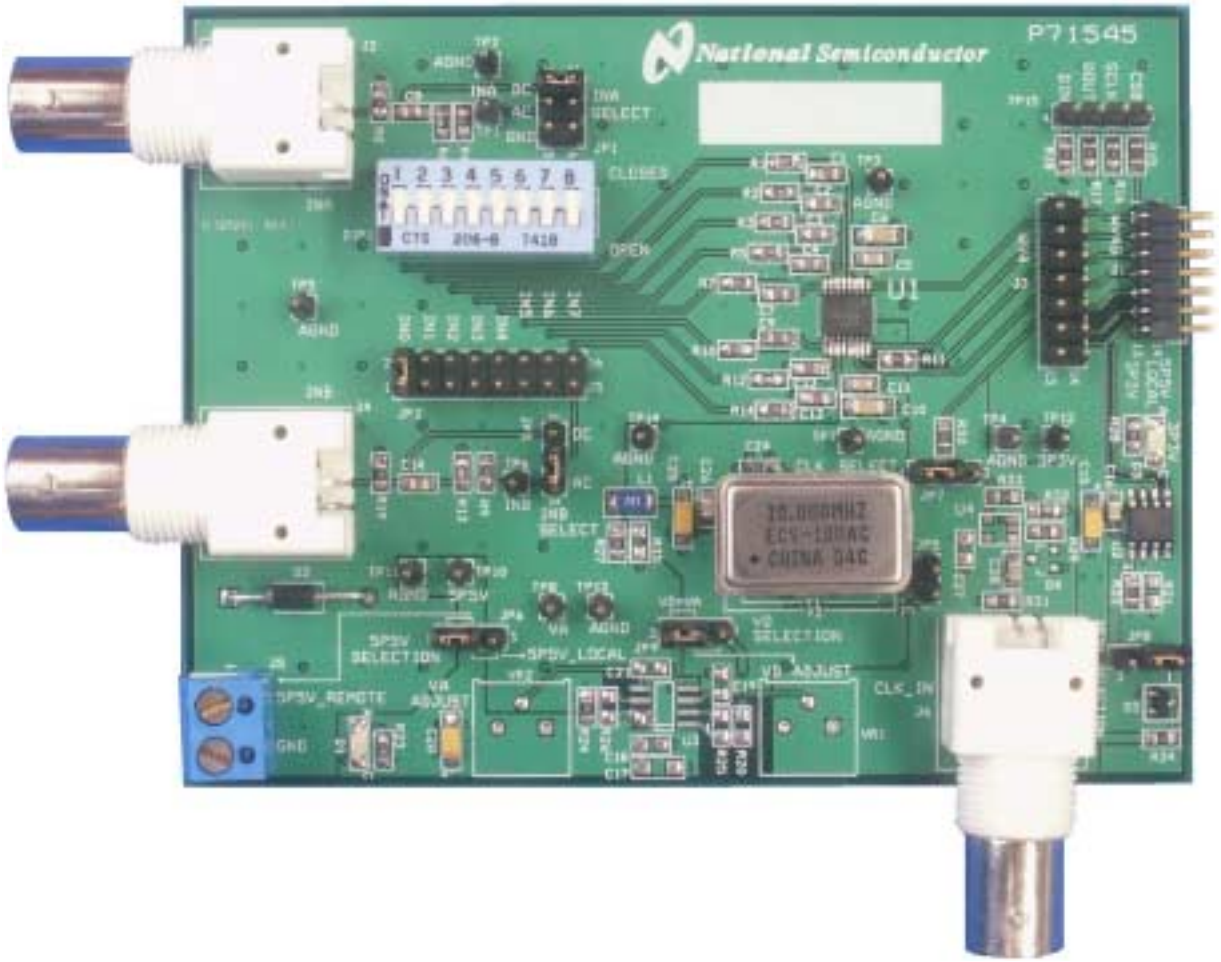
National Semiconductor

February 14, 2006
Rev -2.0
CS

Evaluation Board User's Guide

	8-bit	10-bit	12-bit
50KSPS - 200kSPS	ADC088S022	ADC108S022	ADC128S022
200KSPS - 500KSPS	ADC088S052	ADC108S052	ADC128S052
500KSPS - 1MSPS	ADC088S102	ADC108S102	ADC128S102

Low Power, Eight-Channel CMOS Analog-to-Digital Converter Family



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1.0 Introduction

The ADC128S102EVAL Design Kit (consisting of the ADC128S102 Evaluation Board and this User's Guide) is designed to ease evaluation and design-in of National Semiconductor's eight-channel, low-power CMOS Analog-to-Digital Converters (ADC128S102, ADC108S102, ADC088S102, ADC128S052, ADC108S052, ADC088S052, ADC128S022, ADC108S022, and ADC088S022). This family of pin-compatible ADCs will be referenced throughout this document as the ADC128S102.

The evaluation board can be used in one of two modes; Stand-alone or Computer mode.

In Stand-alone mode, suitable test equipment, such as a function generator and logic analyzer, can be used with the board to evaluate the ADC128S102.

In the Computer mode, data capture and evaluation is simplified by connecting this board to National Semiconductor's Data Capture Board (order number WAVEVSN BRD 4.0) with a 14-pin ribbon cable (order number WV4ADCIFCABLE). The Data Capture (WV4) Board is connected to a personal computer running WaveVision software through a USB port. The WaveVision4 software runs on Microsoft Windows™ and the latest version can be downloaded from the web at http://www.national.com/adc.

Note: WaveVision Software version 4.2 or later is required to evaluate this part with the WV4 Evaluation System.

The Analog input signal enters the Analog-to-Digital Converter through one of its eight selectable input channels and is converted into a digital stream of bits by U1, the ADC128S102. The WV4 system captures and displays the digitized signal on a PC monitor in the time and frequency domains.

The software will perform an FFT on the captured data upon command. This FFT plot shows dynamic performance in the form of SNR, SINAD, THD, SFDR and ENOB. A histogram of the captured data is also available.

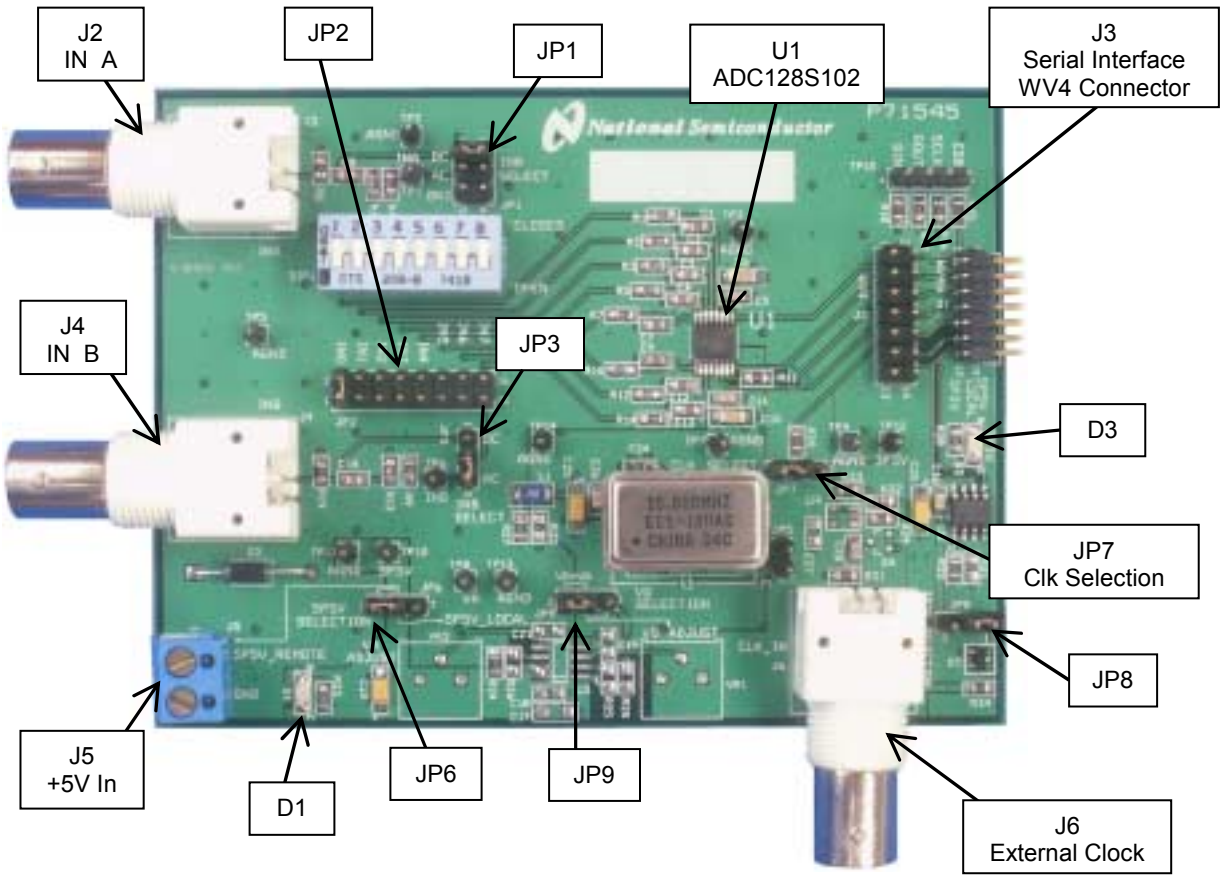


Figure 1: Component and Test Point Locations

2.0 Board Assembly

The ADC128S102 evaluation board comes fully assembled and ready for use. Refer to the Bill of Materials for a description of components, to *Figure 1* for major component placement, and to *Figure 3* for the Evaluation Board schematic.

3.0 Quick Start

The ADC128S102 evaluation board may be used in the Stand-Alone mode to capture data with a logic analyzer or other third-party equipment. It may also be used in the Computer Mode with a WV4 Board. In both cases, the captured data can be analyzed with National Semiconductor's WaveVision4 software.

3.1 Stand Alone Mode

Refer to *Figure 1* for locations of test points and major components.

1. Open all the DIP switches at DIP1 and configure the board's jumpers according to *Table 1* below.

	Pin1	Pin2	Pin3	Pin4
JP1 (INA Coupling)	o	o	o	o
JP2 (INB Select)	o	o	o	o
JP3 (INB Coupling)	o	o	o	
JP6 (5P5V Select)	o	o	o	
JP7 (SCLK Select)				
JP8 (3P3V Select)	o	o	o	
JP9 (VD Select)	o	o	o	

Table 1: Quick Start Jumper Configuration

2. Connect a clean analog (not switching) +5V power source to Power Connector J5.
3. Connect a single-ended source of 4.8 V_{P-P} amplitude from a suitable 50-Ohm source to IN_B (BNC J4). This signal should be applied through a bandpass filter to eliminate the noise and harmonics commonly associated with signal sources. To accurately evaluate the performance of the ADC128S102, the source must be better than 90dB THD.

   Note: For a time-varying DC input signal, DC couple the input by placing the jumper at JP3 across pins 1 & 2 instead of pins 2 & 3.
4. The digital inputs and outputs are available at header J3. Refer to *Figure 2* for connection details. The source used to create signals SCLK, CSB, and D_{IN} must meet the digital input characteristics in the ADC128S102 datasheet.

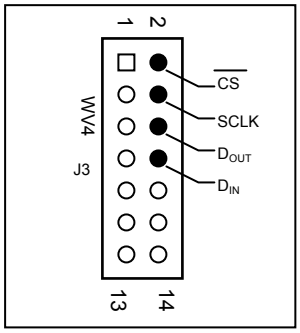


Figure 2: J3 WaveVision4 Serial Interface Header

5. Finally, import the Data taken with a Logic Analyzer or other third-party equipment into the WaveVision4 Software. Refer to WaveVision4 Manual for data analysis techniques.

3.2 Computer Mode

Refer to *Figure 1* for locations of test points and major components.

1. Run the WaveVision4 program. While the program is loading, continue below.
2. Install the appropriate crystal oscillator into socket Y2 and short pins 1 & 2 of JP7 (See *Table 1*). Alternatively, connect a low-jitter square wave generator with an amplitude between 2.5 V_{P-P} and 5 V_{P-P} to BNC connector J6 and short pins 2 & 3 of JP7.

   If using an external source, remove the oscillator from Y2. If using an oscillator at Y2, remove the signal source from J6. The presence of a second oscillator source could add noise to the conversion process.
2. Perform steps 1 and 2 of section 3.1.
3. Connect the 14-pin ribbon cable between J3 of the ADC128S102 evaluation board and J3 of the WV4 board.
4. Connect a clean analog (not switching) +5V power source to Power Connector J1 on the WV4 board.
5. Connect a USB cable between the WaveVision4 Data Capture Board and the PC running the WaveVision4 program. *See Section 4.5 for detailed Power Supply Information.*
6. Refer to section 5.0 on Software Operation and Settings.

4.0 Functional Description

Table 2 describes the function of the various jumpers on the ADC128S102 evaluation board. The Evaluation Board schematic is shown in *Figure 3*.

Jumper	Function		
DIP1	Routes IN_A to each of the eight ADC channels. E.g. Switch 1 routes IN_A to channel 0 while switch 4 routes IN_A to channel 3.		
JP1	Pins 1 & 2	Pins 3 & 4	Pins 5 & 6
	DC couple IN_A	AC couple IN_A	Ground IN_A
JP2	Routes IN_B to each of the eight ADC channels. E.g. Pins 1 & 2 route IN_B to channel 0 while pins 15 and 16 route IN_B to channel 7.		
JP3	Pins 1& 2	Pins 2 & 3	
	DC couple IN_B	AC couple IN_B	
JP5	Not Used		
JP6	Pins 1& 2	Pins 2 & 3	
	5P5V_REMOTE	5P5V_LOCAL	
JP7	Pins 1& 2	Pins 2 & 3	
	Select on-board clock oscillator Y2	Select clock oscillator at BNC J6	
JP8	Pins 1& 2	Pins 2 & 3	
	Select on-board +3.3V	Select +3.3V from WV4S board	
JP9	Pins 1& 2	Pins 2 & 3	
	Not Used	Set V_D=V_A	

Table 2: Jumper Functions

4.1 The Signal Input

The input signal to be digitized can be applied through the BNC connector at J2 (IN_A) or J4 (IN_B). Two inputs allow the user to utilize multiple channels of the eight-channel ADC128S102 at the same time.

Both IN_A and IN_B can be AC coupled or DC coupled. To digitize a time-varying DC signal, place a jumper across pins 1 and 2 of JP1 for IN_A, or place a jumper across pins 1 and 2 of JP3 for IN_B. If the AC component of an input signal is to be evaluated, place a jumper across pins 3 and 4 of JP1 for IN_A, or place a jumper across pins 2 and 3 of JP3 for IN_B. Additionally, IN_A can be grounded by shorting pins 5 and 6 of JP1.

Both IN_A and IN_B of the ADC128S102 Evaluation board can be routed to any number of the Analog-to-Digital converter's eight channels. For IN_A, simply close the DIP switches corresponding to the desired ADC128S102 input channels. For example, to route IN_A to input channels 0 and 5, close dip switches 1 and 6. For IN_B, simply place jumpers across JP2 to select input channels. For example, to route IN_B to input channels 0 and 3, short pins 1 and 2 as well as pins 7 and 8 of JP2.

4.2 ADC Reference Circuitry

The ADC128S102 family gets its reference voltage from the analog supply (V_A). Hence, a clean analog supply must be used to guarantee the performance of the ADC128S102.

4.3 ADC Clock Circuit

In Computer mode, the ADC128S102 Evaluation board sends a clock signal to the WV4 Data capture board. This clock signal is used to derive the digital signals that drive the ADC128S102.

The crystal-based oscillator provided on the evaluation board is selected by shorting pins 1 & 2 of JP7. It is best to remove any external signal generator when using this oscillator to reduce any unnecessary noise.

This board will also accept a clock signal from an external source by connecting that source to BNC J6 and shorting pins 2 & 3 of JP7. An ac-coupling circuit together with a DC-biased resistive divider is provided so the board can accept a 50 Ohm signal source in the range of 2.5 to 5.0V_{P-P} to drive this input. It is best to remove the oscillator at Y2 when using an external clock source to reduce any unnecessary noise.

If the Evaluation board is used in Stand-alone mode, the onboard oscillator and signal applied to J6 do not drive the SCLK pin. Rather, an external source such as a pattern generator must supply the digital signals (CSB, SCLK, D_{IN}) to drive the ADC128S102. These signals must be applied at J3, the Serial Interface Header (See *Figure 2*).

Note: SCLK, CSB, & D_{IN} must be driven between 0 and V_A to prevent damage to the ADC.

4.4 Digital Data Output

The serial data output from this board may be monitored at TP15 or J3. Note: The TP15 test points are current limited by 1kΩ resistors which will cause some slewing of the digital waveforms. For data capture with the WaveVision4 Software, refer to section 3.2. Detailed timing diagrams can be found in the datasheet.

4.5 Power Supply Connections

The ADC128S102 Evaluation Board has three independent supplies; V_A, V_D, and 3P3V. V_A serves as the analog reference for the Analog to Digital Converter and must be driven by a clean source to maximize the performance of the ADC128S102. The voltage applied to V_A can be any value between 2.7V and 5.25V. V_D sets the digital output level of the device and can be any value between 2.7V and the voltage applied to pin V_A. 3P3V supplies power to the on-board EEPROM

and is automatically generated on the evaluation board when pins 1 & 2 are shorted on JP8. This voltage is only used by U2 when operating the evaluation board in computer mode.

If desired, V_D and V_A can be tied together by placing a jumper across pins 2 and 3 of JP9. Otherwise, V_D can be driven independently of V_A by removing the jumper at JP9 and driving pin 2 of JP9 directly. In either case, the supply voltage for V_A must be supplied to connector J5, labeled 5P5V, or directly to TP10. A jumper must be placed across pins 1 and 2 of JP6.

5.0 Software Operation and Settings

The WaveVision4 software is included with the WV4 board and the latest version can be downloaded for free from National's web site at http://www.national.com/adc. WaveVision Software version 4.2 or later is required to evaluate this part with the WV4 Evaluation System.

To install this software, follow the procedure in the WAVEVSN BRD 4 User's Guide. Once the software is installed, set it up as follows:

1. Follow the steps outlined in Section 3.2 “Computer Mode Quick Start”.
2. From the WaveVision main menu, go to Settings, then Board Settings and do the following:

   Select the following from the WaveVision4 main menu:
   - WaveVision 4.0 (USB)
   - # of Samples: 2K to 32K, as desired
3. Apply power as specified in Section 4.5, click on the **"Test"** button and await the firmware to download.
4. Click on the **"Accept"** button.
5. Click on ‘Acquire’ then ‘Samples’ from the Main Menu (you can also press the *F1* shortcut key). If a dialog box opens, select ‘Discard’ or press the *Escape* key to start collecting new updated samples.

A plot of the selected number of samples will be displayed. Make sure there is no clipping of data samples. The Samples may be further analyzed by clicking on the magnifying glass icon, then clicking and dragging across a specific area of the plot for better data inspection. See the WaveVision4 Board User's Guide for details.

To view an FFT of the data captured, click on the ‘FFT’ tab. This plot may also be zoomed in on. A display of dynamic performance parameters in the form of SINAD, SNR, THD, SFDR and ENOB will be displayed at the top right hand corner of the FFT plot.

To view a Histogram of the data, click on the “Software Histogram” tab. This plot may be zoomed in on like the data plot. If the input signal is clipping, the ‘zero’ and ‘full-scale’ codes will be very abundant. The number of missing codes will be displayed at the top right hand corner of the plot.

Acquired data may be saved to a file. Plots may also be exported as graphics.

Please refer to the WaveVision4 Data Capture Board User's Guide for further details.

6.0 Evaluation Board Specifications

Board Size:	3.25" x 4.19" (8.25 cm x 10.65 cm)	
Power Requirements	Min: +2.7V, 100mA	Max: +5.25V, 100 mA
Clock Frequency Range:	ADCXX8S102	8MHz to 16MHz
	ADCXX8S052	3.2MHz to 8MHz
	ADCXX8S022	800kHz to 3.2MHz
Analog Input		
Nominal Voltage Range:	$4.9V_{P-P}$ Low: +0.05V High: (V_A-0.05V)	
Impedance:	50 Ohms	

7.0 Hardware Schematic

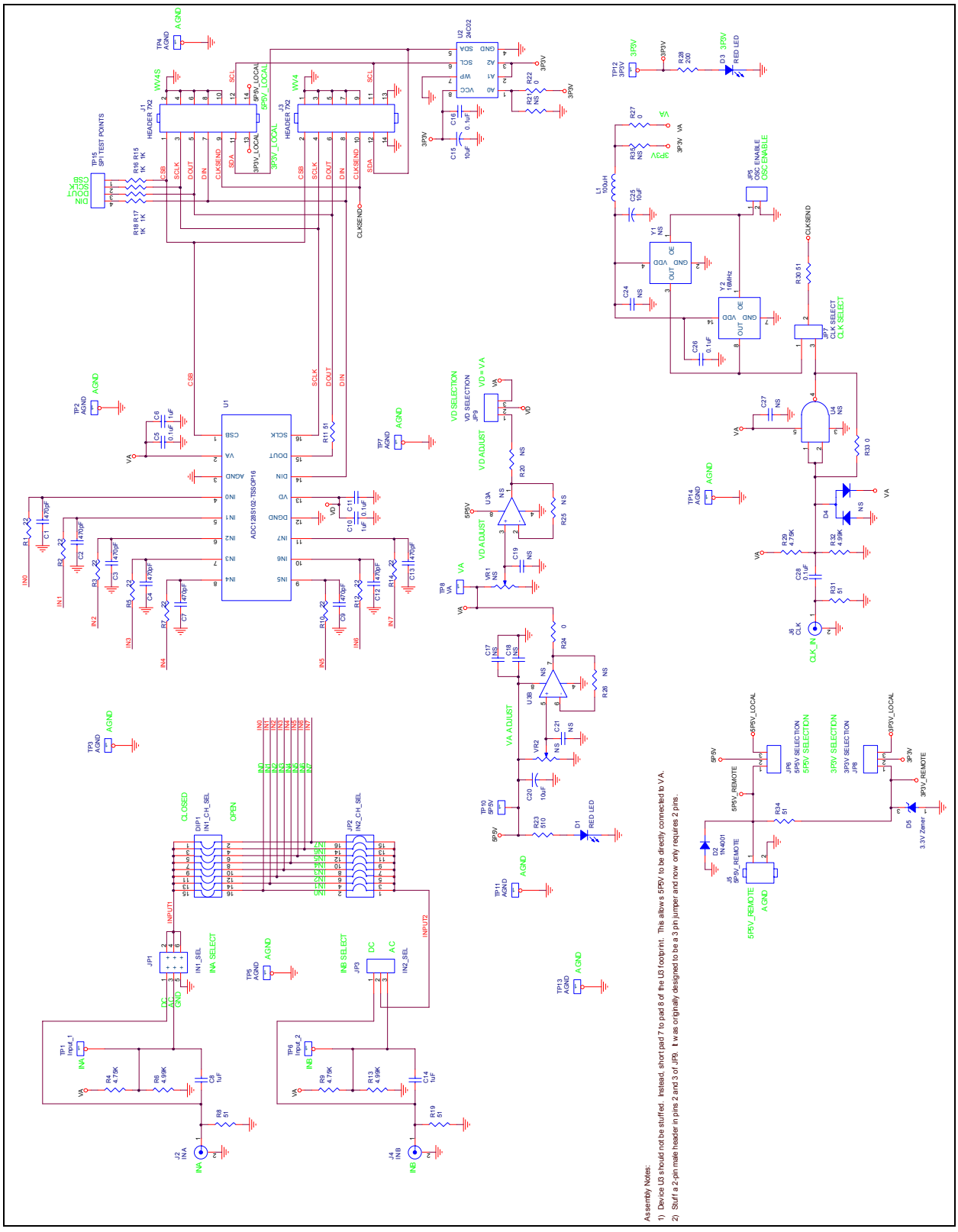


Figure 3: ADC128S102 Evaluation Board Schematic

8.0 Evaluation Board Bill of Materials

Qty.	Reference	PCB Footprint	Source	Source Part #	Rating	Value
8	C1,C2,C3,C4,C7, C9, C12, C13	sm/c_0805			10V	470pF
5	C5,C11,C16,C26, C28	sm/c_0805			10V	0.1uF
2	C10,C6	sm/c_1206			10V	1uF
2	C14,C8	sm/c_0805			10V	1uF
3	C15,C20,C25	sm/ct_3216_12			10V	10uF
1	C17	sm/c_1206			10V	NS
5	C18,C19,C21, C24,C27	sm/c_0805			10V	NS
1	DIP1	dip.100/16/w.300/l.900	Digikey	CT2068-ND		IN1_CH_SEL
2	D3,D1	sm/led_21	Digikey	516-1440-1-ND		RED LED
1	D2	DAX2/DO41	Digikey	1N4001GICT-ND		1N4001
1	D4	sm/sot23_123/nat	Digikey	BAT54SLT1OSCT-ND		NS
1	D5	sm/SOT23	Digikey	MMBZ5226BLT1OSCT-ND		3.3V Zener
1	JP1	blkcon.100/vh/tm2oe/w.200/6	Digikey	A26529-40-ND		IN1_SEL
1	JP2	blkcon.100/vh/tm2oe/w.200/16	Digikey	A26529-40-ND		IN2_CH_SEL
1	JP3	blkcon.100/vh/tm1sq/w.100/3	Digikey	A26513-40-ND		IN2_SEL
1	JP5	blkcon.100/vh/tm1sq/w.100/2	Digikey	A26513-40-ND		OSC ENABLE
1	JP6	blkcon.100/vh/tm1sq/w.100/3	Digikey	A26513-40-ND		5P5V SELECTION
1	JP7	blkcon.100/vh/tm1sq/w.100/3	Digikey	A26513-40-ND		CLK SELECT
1	JP8	blkcon.100/vh/tm1sq/w.100/3	Digikey	A26513-40-ND		3P3V SELECTION
1	JP9	blkcon.100/vh/tm1sq/w.100/3	Digikey	A26513-40-ND		VD SELECTION
1	J1	blkcon/2mm/ra/tm2oe/w2mm/14	Digikey	S2200-07-ND		HEADER 7X2
1	J2	rf/bnc/r1.350_21	Digikey	ARF1177-ND		INA
1	J3	blkcon.100/vh/tm2oe/w.200/14	Digikey	A26529-40-ND		HEADER 7X2
1	J4	rf/bnc/r1.350_21	Digikey	ARF1177-ND		INB
1	J5	term_block/.200/2pos	Digikey	ED1609-ND		5P5V_REMOTE
1	J6	rf/bnc/r1.350_21	Digikey	ARF1177-ND		CLK
1	L1	sm/l_1210	Digikey	445-1155-1-ND		100uH
8	R1,R2,R3,R5,R7, R10,R12, R14	sm/r_0805				22
3	R4,R9,R29	sm/r_0805				4.75K
3	R6,R13,R32	sm/r_0805				4.99K
6	R8,R11,R19,R30, R31,R34	sm/r_0805				51
4	R15,R16,R17,R18	sm/r_0805				1K
5	R20,R21,R25, R26,R35	sm/r_0805				NS
4	R22,R24,R27,R33	sm/r_0805				0
1	R23	sm/r_0805				510
1	R28	sm/r_0805				200
1	TP1	blkcon.100/vh/tm1sq/w.100/1	Digikey	5011K-ND		Input_1
6	TP2,TP3,TP4, TP5,TP7,TP11	blkcon.100/vh/tm1sq/w.100/1	Digikey	5011K-ND		AGND
2	TP13, TP14	blkcon.100/vh/tm1sq/w.100/1	Digikey	5011K-ND		AGND

1	TP6	blkcon.100/vh/tm1sq/w.100/1	Digikey	5011K-ND		Input_2
1	TP8	blkcon.100/vh/tm1sq/w.100/1	Digikey	5011K-ND		VA
1	TP10	blkcon.100/vh/tm1sq/w.100/1	Digikey	5011K-ND		5P5V
1	TP12	blkcon.100/vh/tm1sq/w.100/1	Digikey	5011K-ND		3P3V
1	TP15	blkcon.100/vh/tm1sq/w.100/4	Digikey	A26513-40-ND		SPI TEST POINTS
1	U1	sog.65m/16/wg6.40/l5.10				ADCxx8Sxx2
1	U2	sog.050/8/wg.244/l.200				24C02
1	U3	sog.050/8/wg.244/l.200	Digikey	LMC6492AEMX		NS
1	U4	sm/SOT23-5	Digikey	NC7SZ00M5CT-ND		NS
2	VR2,VR1	vres4	Digikey	3386F-103-ND		NS
1	Y1	SOJ.100/4/WG8.80MM/L.550				NS
1	Y2	crystal_socket	Digikey	A400-ND		socket
1	Y2	oscillator	Digikey	CTX116-ND		16.0MHz OSC (thru-hole)
1	PCB	ADC128S102 evaluation board				
	J1		Digikey	S2200-07-ND		HEADER 7X2

APPENDIX

A1.0 Summary Tables of Test Points, Jumpers, and Connectors

Test Points on the ADC128S102 Evaluation Board

TP1: IN_A	IN_A test point. Located near the top left of the board.
TP2: AGND	Ground. Located near the top left of the board.
TP3: AGND	Ground. Located near the top of the board. Just above U1.
TP4: AGND	Ground. Located at the right edge of the board.
TP5: AGND	Ground. Located between the BNC connectors on the left side of the board.
TP6: IN_B	IN_B test point. Located near the middle of the board.
TP7: AGND	Ground. Located just above the oscillator socket.
TP8: V_A	V_A supply test point. Located near the bottom edge of the board.
TP10: 5P5V	5P5V supply test point. Located near the bottom left of the board.
TP11: AGND	Ground. Located near the bottom left of the board.
TP12: 3P3V	3.3V test point. Located at the right edge of the board.
TP13: AGND	Ground. Located near the bottom edge of the board.
TP14: AGND	Ground. Located near the center of the board.
TP15:	Warning: Do not attempt to drive the chip via these test points, they are isolated by 1kΩ resistors and for probing only. Instead, use the header J3 as shown in *Figure 2.*
Pin 1: CSB	Chip Select test point.
Pin 2: SCLK	Serial Clock test point.
Pin 3: DOUT	Data Out test point.
Pin 4: DIN	Data In test point.

Connectors on the ADC128S102 Evaluation Board

J1: WV4S	WV4S 14-Pin Right-angle Header
J2: IN_A Input	BNC Connector
J3: WV4	WV4 14-Pin Header
J4: IN_B Input	BNC Connector
J5: VA_REMOTE	Two Position Power connector terminal block.
J6: External Clock	BNC Connector

Selection Jumpers on the ADC128S102 Evaluation Board (Refer to Table 2, Section 4.0 for configuration details)

DIP1: IN_A Channel Selection	Routes Input A to the ADC's eight input channels.
JP1: IN_A Coupling	Selects AC coupling, DC coupling, or simply grounds Input A
JP2: IN_B Channel Selection	Routes Input B to the ADC's eight input channels.
JP3: IN_B Coupling	Selects AC coupling, DC coupling, or simply grounds Input B
JP5: Oscillator Enable	Enables or disables the on-board oscillator.
JP6: 5P5V Select	Selects local or remote source of 5P5V supply.
JP6: Osc Enable	Not Used
JP7: Clock Select	Selects internal or external clock source.
JP8: 3P3V Select	Selects local or remote source of 3P3V supply.
JP9: V_D Select	Sets the digital supply (V_D) equal to the analog supply (V_A).

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REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of this Product in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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西新宿三井ビル
http://www.tij.co.jp

EVALUATION BOARD/KIT/MODULE (EVM)
WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

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TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

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