

DAC38RF8xEVM

The DAC38RF8xEVM is the family of circuit boards for evaluating the DAC38RFxx family of high-speed digital-to-analog converters (DACs) from Texas Instruments. The DAC38RF8xEVM family consists of the DAC38RF80EVM, DAC38RF87EVM, DAC38RF82EVM, DAC38RF86EVM, and DAC38RF89EVM. This user's guide is applicable to all the EVMs in the DAC38RF8xEVM family. This document is intended to guide the DAC38RF8xEVM user through the process of setting up the EVM successfully. For other information on the DAC38RFxx device family, refer to the device datasheet ([SLASEA3](#), [SLASEA6](#), and [SLASEF4](#)). Throughout this document, *italics* are used to refer to names of controls on graphical user interfaces (GUI).

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1 Introduction

1.1 Required Hardware and Software

The following hardware and software are required to evaluate the DAC38RF8x device:

1. DAC38RF8xEVM: Main circuit board containing the DAC to be evaluated
2. DAC38RF8xEVM Graphical User Interface (GUI): Software that controls the DAC EVM:
<http://www.ti.com/tool/TSW14J56EVM>
3. TSW14J56 EVM: Hardware that generates digital patterns for the DAC:
<http://www.ti.com/tool/TSW14J56EVM>
4. HSDC Pro software: Software interface that controls the TSW14J56 EVM. Version 4.50 or higher is recommended: <http://www.ti.com/tool/dataconverterpro-sw>

1.2 Hardware Description

Figure 1 illustrates the EVM block diagram.

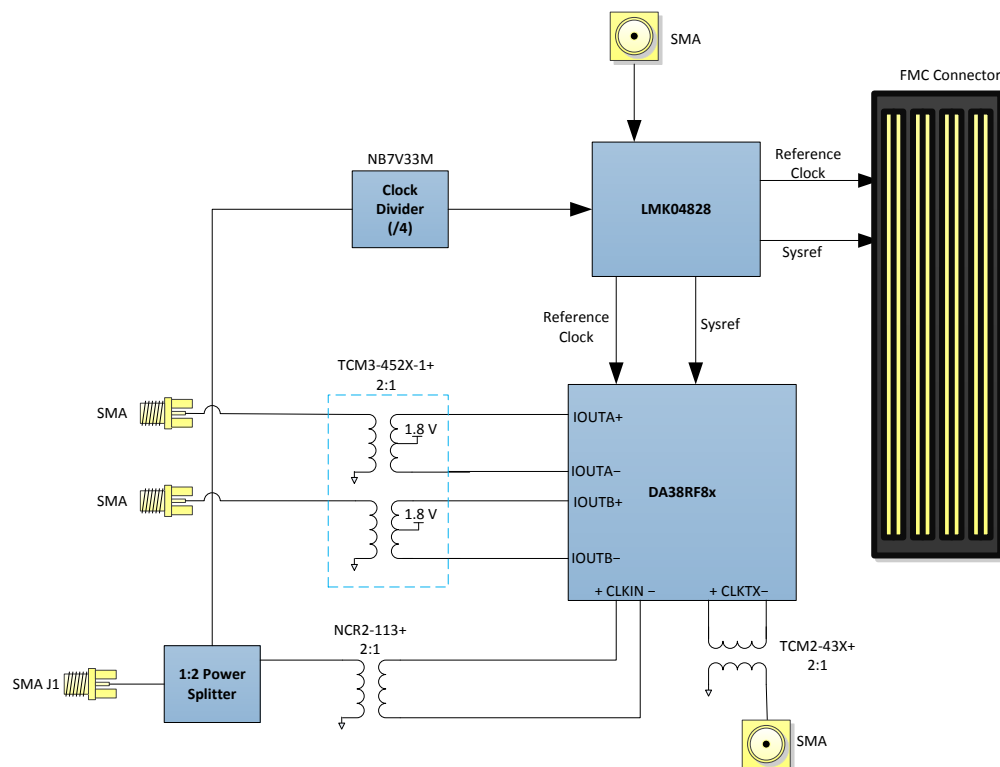


Figure 1. DAC38RF8xEVM Block Diagram

Table 1. DAC38RF8xEVM Component Description

Part	Description
DAC38RF8x	9 Gbps dual-channel DAC with JESD204B interface
FMC Connector	Interface to connect DAC evaluation board to pattern generators (for example, TSW14J56)
LMK04828	JESD204B-compliant clock generator. Used to generate SYSREF and device clock to pattern generator. Also generates SYSREF and PLL reference clock to DAC38RF8x.
NB7V33M	10 GHz divide by 4 clock divider
TCM3-452X-1+	2:1 impedance ratio transformer. Used for (1) impedance matching to 50-Ω load, (2) differential to single-ended conversion, (3) DC biasing of DAC output.
TCM2-43X+	2:1 impedance ratio transformer. Used to convert CLKTX from differential to single ended. CLKTX is divided by 3 or 4 output of the DAC sampling clock.
NCR2-113+	2:1 impedance ratio transformer. Used to convert single-ended input clock to differential for the DAC.

Table 2. Jumpers on DAC38RF8xEVM

Jumper	Default Position	Description
JP1	Shunt pin 2-3	shunt pin1-2: Put some DAC internal blocks in sleep mode. Shunt pin2-3: Take DAC out of sleep mode
JP2	Shunt pin 2-3	shunt pin1-2- Enable DAC output. Shunt pin2-3-disable DAC output
JP3	Open	Open: Disables power to the on-board 122.88 MHz VCXO (Y1). Leave open when VCXO is not used Closed: Enables power to the on-board 122.88 MHz VCXO
JP8	Open	Open: Enables VDDD1G1 supply (U37). Closed: disables VDDD1G1 supply (U37)
JP9	Open	Open: Enables VEE18N supply (U19). Closed: disables VEE18N supply (U19)
JP10	Shunt pin 1-2	Closed: Enable external clock mode Open: Enable on-chip PLL clock mode
J11	Open	Not used
J22	Open	Provides access to externally monitor ATEST pin
J23	Shunt pin 1-2, 3-4, 5-6, 7-8	Connects DAC SPI interface to FT232H (U4) spi interface.

1.2.1 Clocking Modes

The DAC38RF8xEVM may be configured into one of five clocking modes. These clocking modes are:

1. Direct External clock mode with high amplitude clock
2. Direct External clock mode with low amplitude clock (less than 7 dBm)
3. On-chip PLL clock mode
4. On-board VCXO clock mode
5. LMF = 413 or 823, 12-bits clock mode

1.2.1.1 Direct External Clock Mode With High Amplitude Clock (CMODE1)

This mode is intended for use with signal generators that can output 16 dBm or higher. Examples are Keysight E8257D or R&S SMA100. To use this mode, the only modification from the default EVM configuration is to connect a shunt between pin 1 and 2 of jumper JP10. Then, provide a 16-dBm clock to SMA J1. This is shown in [Figure 2](#). By default, the EVM is configured to use the single-ended clock input of the DAC in this mode. For best spurious performance, also install C1, C333, and C334 on the EVM to switch to differential clock input of DAC. Refer to the schematics and BOM of the EVM for the component values ([SLAC734](#)).

1.2.1.2 Direct External Clock Mode With Low Amplitude Clock (CMODE2)

The purpose of this mode is for use with monolithic clock synthesizers like the [LMX259x](#). Clock power in the range of 3 dBm to 7 dBm is recommended in this mode. Note that when using the LMX2592 with the frequency doubler enabled, an external filter is required to attenuate the sub-harmonic at half the clock frequency to –50 dBc or better. To configure the EVM in this mode from the default configuration:

1. Install SMA J27
2. Remove C2, C3, R215, R211
3. Install R323, R324, C449, C450 (refer to the schematics and BOM of the EVM for the component values ([SLAC734](#)))
4. Connect the positive and negative output of clock synthesizer to SMA J27 and SMA J1, respectively
5. Remove jumper JP10
6. Use a second signal generator to provide a clock to SMA J4 and set the amplitude to 6 dBm. The frequency of this clock is one-fourth of the sampling rate (or $F_s/4$). This clock is used to provide the reference clock of the FPGA and SYSREF.
7. Connect SMA J24 to the reference input of the clock synthesizer. The frequency at SMA J24 is set from the EVM GUI in a later step.

1.2.1.3 On-Chip PLL Clock Mode (CMODE3)

This mode is for evaluating the DAC performance with a low-frequency reference clock and the internal PLL/VCO as the sampling clock. To use this mode, connect a clock at 6 dBm to SMA J4 and remove the shunt connecting pin1 and 2 of jumper JP10. Keep all other hardware settings in the default configuration. The frequency of the clock at SMA J4 is determined from the EVM GUI in a later step.

1.2.1.4 On-Board VCXO Clock Mode (CMODE4)

This mode allows the DAC to be evaluated without providing any external clock. The on-board VCXO running at a fixed 122.88-MHz frequency can be used to provide a reference clock to the LMK04828 PLL. The high-frequency clock generated by the LMK04828 PLL is subsequently divided down and used to source reference clock and SYSREF to the DAC internal PLL and the FPGA on TSW14J56 EVM. To use this mode, connect a shunt between pins 1 and 2 of jumper JP3. Keep all other hardware settings in the default configuration.

1.2.1.5 LMF = 413 or 823, 12-Bits Clock Mode (CMODE5)

This mode is used to generate the required clocks for evaluating the DAC in 12-bits mode, LMF = 413 or 823 only. Two signal generators with their 10-MHz reference connected together are required in this mode. The setup involves:

1. Provide an external sampling clock to SMA J1
2. Provide a second clock to SMA J4 with an amplitude of 6 dBm. The frequency of this clock will be determined by the EVM GUI in a later step. Connect the reference of the two signal generators together.
3. Remove the shunt on pins 1 and 2 of jumper JP10

2 Quick Start

The following examples use an external clock and the on-chip PLL to evaluate the performance of the DAC38RF8xEVM. The frequency of the clock is arbitrarily selected as 6144 Mps but the procedure outlined is applicable to any external clock frequency and any supported on-chip PLL frequency.

The external clock path includes a balun for single-ended to differential conversion. [Appendix B](#) shows the insertion loss, amplitude, and phase un-balance of this balun.

2.1 TSW14J56 and DAC38RF8xEVM

This section covers details on the TSW14J56 and DAC38RF8xEVM.

1. Make sure both boards are not powered and not connected to the USB port of the PC.
2. Connect the FMC connector of TSW14J56 EVM (J4) to FMC connector of DAC38RF8xEVM (J20).

2.1.1 TSW14J56

1. Connect a 5-V power supply to connector J11 (+5 V IN).
2. Connect a USB cable to the USB connector (J9).
3. Flip the power switch (SW6) to the "ON" position.

2.1.2 DAC38RF8xEVM Configuration With Direct External Clock(CMODE1)

Skip this section if the on-chip PLL is used as the DAC clock source.

NOTE: Shunt pin 1 and pin 2 of the 2-pin jumper labeled JP10 to enable external clock mode. This is shown in [Figure 2](#). Other hardware changes may be required depending on the external clocking mode. These changes are described in [Section 1.2.1](#).

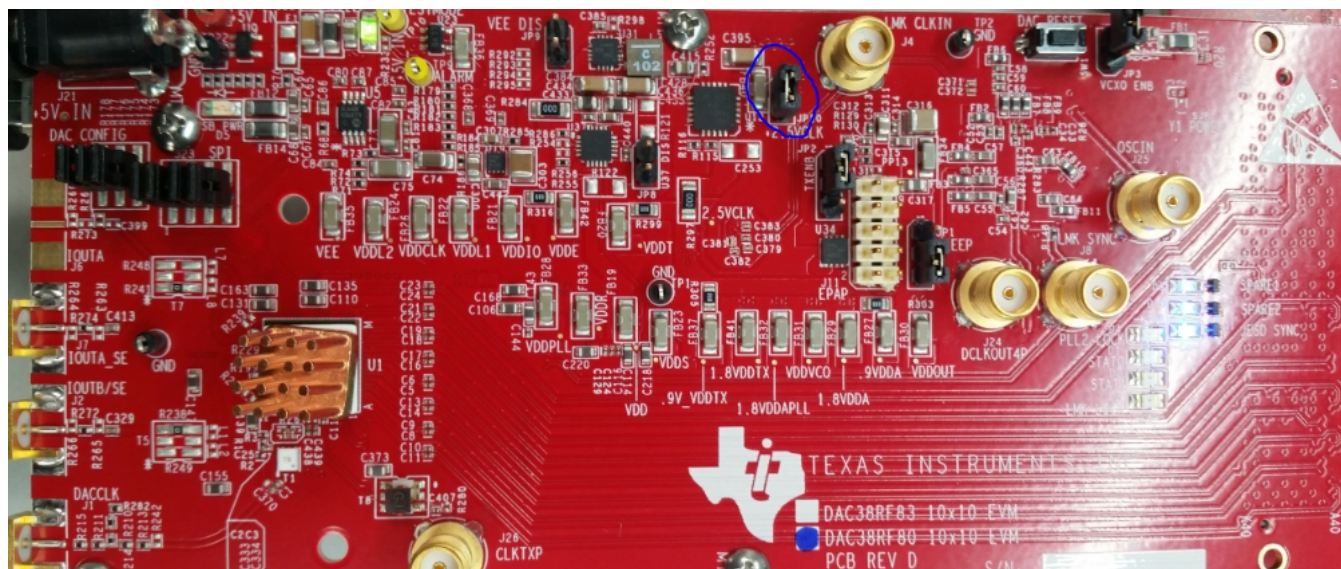


Figure 2. Shunt Pin 1 and Pin 2 of JP10 Jumper Enabling External Clock Mode

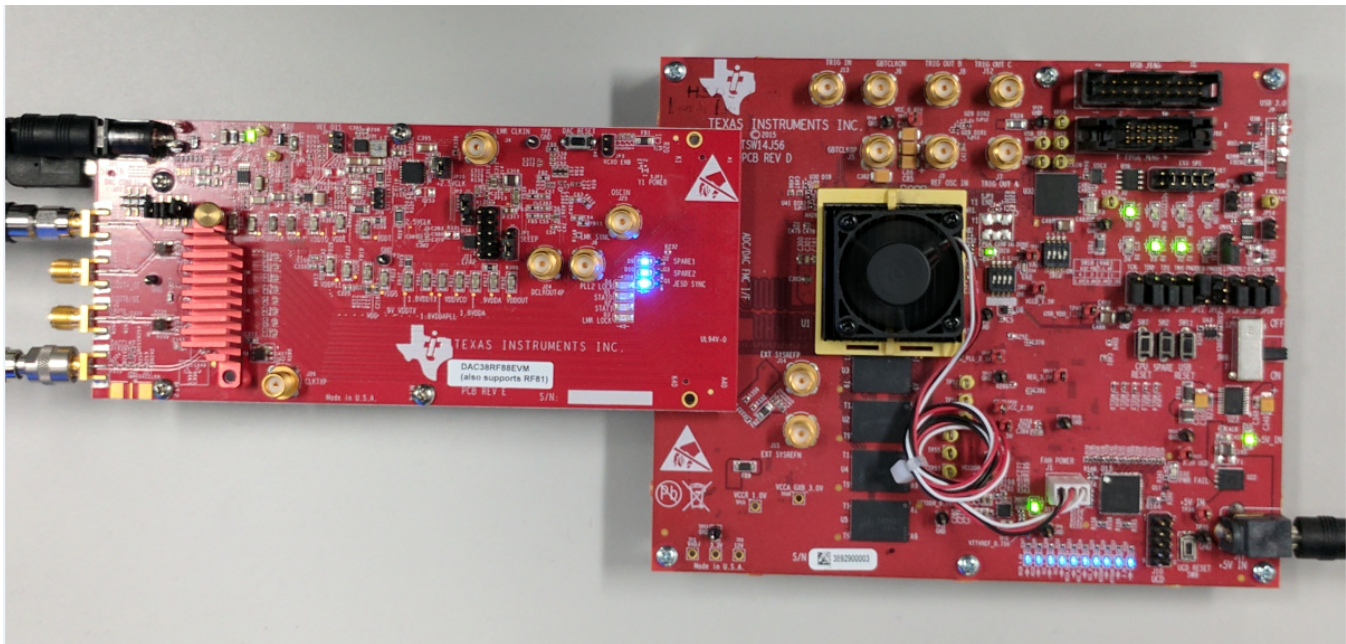


Figure 3. DAC38RF83 EVM Setup for External Clock Mode

1. Connect a 5-V power supply to connector J21 (+5V_IN).
2. Connect a USB cable to the USB connector (J16).
3. Provide a 16-dBm, 6144-MHz, external DAC sampling clock to the clock balun input at J1.
4. Connect a spectrum analyzer to the DAC output SMA connector:
 - For DAC38RF83: Connect spectrum analyzer to J6 (DAC A output) or J2 (DAC B output).
 - For DAC38RF80: Connect a spectrum analyzer to J7 (DAC A output) or J2 (DAC B output).

2.1.3 DAC38RF8x Graphical User Interface (GUI)

Follow these steps to use the DAC38RF8x GUI:

1. Start the DAC38RF8xEVM GUI, then navigate to the quick start page as shown in [Figure 4](#).
2. Verify that the green **USB Status** indicator on the top right corner is lit. If it is not lit, click the **Reconnect FTDI?** button and check the **USB Status** indicator again.
3. From the **Quick Start** tab, in the **SELECT DEVICE** drop down menu, choose from the list of available devices. The device list is automatically populated based on the type of EVM connected.
4. On the **Quick Start** tab, toggle the **DAC RESETB Pin** button and then click on the **Load Default** button. The software automatically configures the DAC to its default state.
5. Enter the desired DAC clock frequency (6144 MHz in this example) and specify the desired number of DACs (Dual DAC), number of IQ pairs (1 IQ pair), number of lanes (4 lanes), and interpolation (16x) as shown in [Figure 4](#).
6. Note the messages displayed for information about the SerDes rate, maximum allowed sample rate for the selected mode, and the HSDC Pro ini file to select (see the section on [HSDC Pro](#) for more information). If the DAC clock frequency entered is not supported for the selected mode, the DAC clock frequency box blinks.

The screenshot shows the 'Quick Start' page for the DAC38RF8xEVM. The top navigation bar includes 'Quick Start', 'DAC38RF8x', 'LMK04828', and 'Low Level V'. A 'Reconnect?' button is in the top right. The main area is titled 'SELECT DEVICE' and shows 'DAC38RF82' selected. Below this are buttons for 'DAC RESETB Pin' (Not in RESET, LOAD DEFAULT) and a 'Quick Start Procedure' section. The 'DAC MODE' section includes fields for 'DAC Clock Frequency (MHz)' (6144), '# of DACs' (Dual DAC), '# of IQ pairs per DAC' (1 IQ pair), '# of serdes lanes per DAC' (4 Lanes), and 'Desired Interpolation' (16x). A 'CONFIGURE DAC' button is present. The 'On-chip PLL' section has a 'PLL Enable' checkbox, 'M' (6), 'N' (1), 'Ref Freq (MHz)' (375), and 'SMA J4 CLK (MHz)' (1125). A 'PLL AUTO TUNE' button is also there. A text box displays current settings: 'Current Serdes Lane Rate = 3840.00MHz', 'Maximum sample rate for Dual DAC, 1 IQ pair, 4 Lanes, 16x interpolation is 9000', 'Serdes Configured to Half Rate', 'Serdes clock predivider = 4', 'Serdes PLL Vrange = 1', 'Serdes PLL Multiplier = 5', and 'HSDCPR0 ini file: DAC38RF8x_LMF_841'. A 'Reset DAC JESD Core & SYSREF TRIGGER' button is at the bottom. A status bar at the bottom shows 'Idle', 'HARDWARE CONNECTED', and the Texas Instruments logo.

Figure 4. DAC38RF8xEVM GUI Quick Start Page Configured for External Clock Mode

- Click on the **CONFIGURE DAC** button to load the DAC configuration data.

NOTE: When using [CMODE2](#) and after configuring the DAC in the preceding step 6, navigate to DAC38RF8x>>Clocking tab and de-select the *External Clock Select* checkbox.

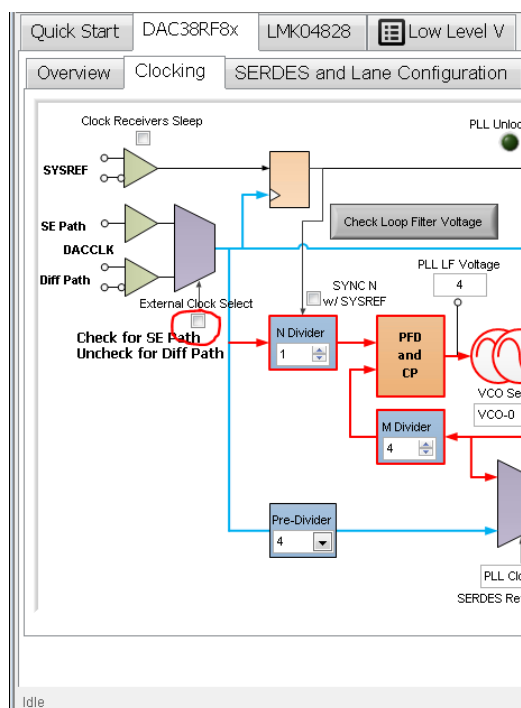


Figure 5. DAC38RF8xEVM GUI External Clock Select Checkbox

8. Click on the **Reset DAC JESD Core** button and the **Trigger LMK04828 SYSREF** button.

2.1.4 DAC38RF8xEVM Configuration With On-Chip PLL(CMODE3)

Skip this section if using an external clock such as the DAC clock source.

NOTE: The 2-pin jumper labeled JP10 must be open to enable on-chip PLL clock mode. This is shown in [Figure 6](#). Other hardware changes may be required depending on the on-chip PLL clocking mode selected. These changes are described in [Section 1.2.1](#).

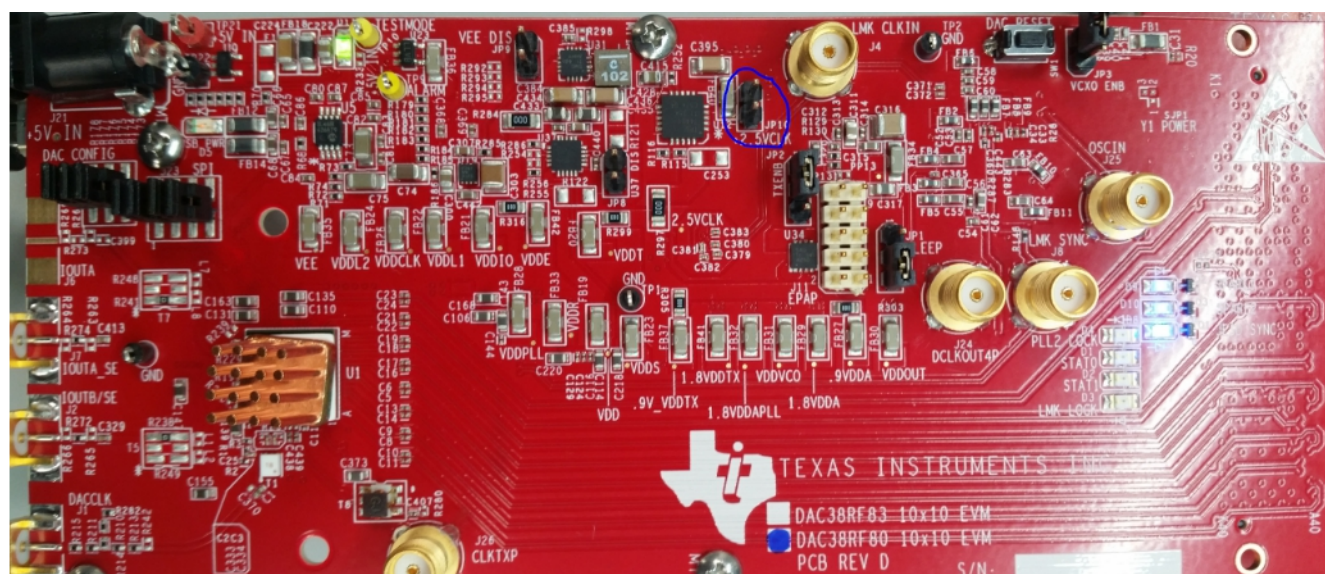


Figure 6. Open Pin 1 and Pin 2 of JP10 Jumper to Enable On-Chip PLL Clock Mode

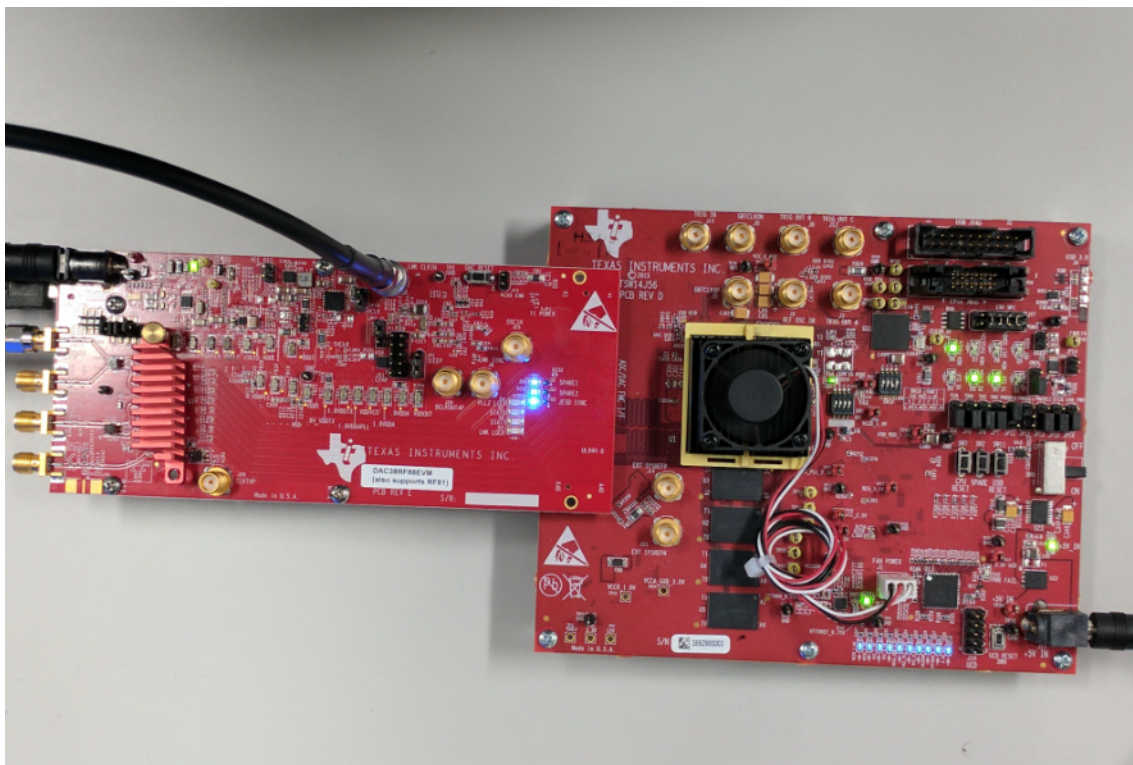


Figure 7. DAC38RF83 EVM Setup for On-Chip PLL Mode

1. Connect a 5-V power supply to connector J21 (+5 V IN).
2. Connect a USB cable to the USB connector (J16).
3. Provide a 4–8 dBm external reference clock to SMA J4 as shown in Figure 7. The frequency of this reference clock is set in a later step.
4. Connect a spectrum analyzer to the DAC output SMA connector.

2.1.5 DAC38RF8x Graphical User Interface (GUI)

1. Start the DAC38RF8xEVM GUI then navigate to the quick start page as shown in Figure 8.
2. Verify that the green USB Status indicator on the top right corner is lit. If it is not lit, click the **Reconnect FTDI?** button and check the *USB Status* indicator again.
3. On the *Quick Start* tab, toggle the **DAC RESETB Pin** button and then click the **Load Default** button. The software automatically configures the DAC to its default state.
4. Check the *PLL Enable* box and enter the desired on-chip PLL reference clock frequency.

NOTE: The *DAC Clock Frequency* box automatically updates based on the M, N, and Ref Freq values entered. If the calculated DAC clock frequency is not supported by the on-chip PLL, the *DAC Clock Frequency* box blinks.

For this example:

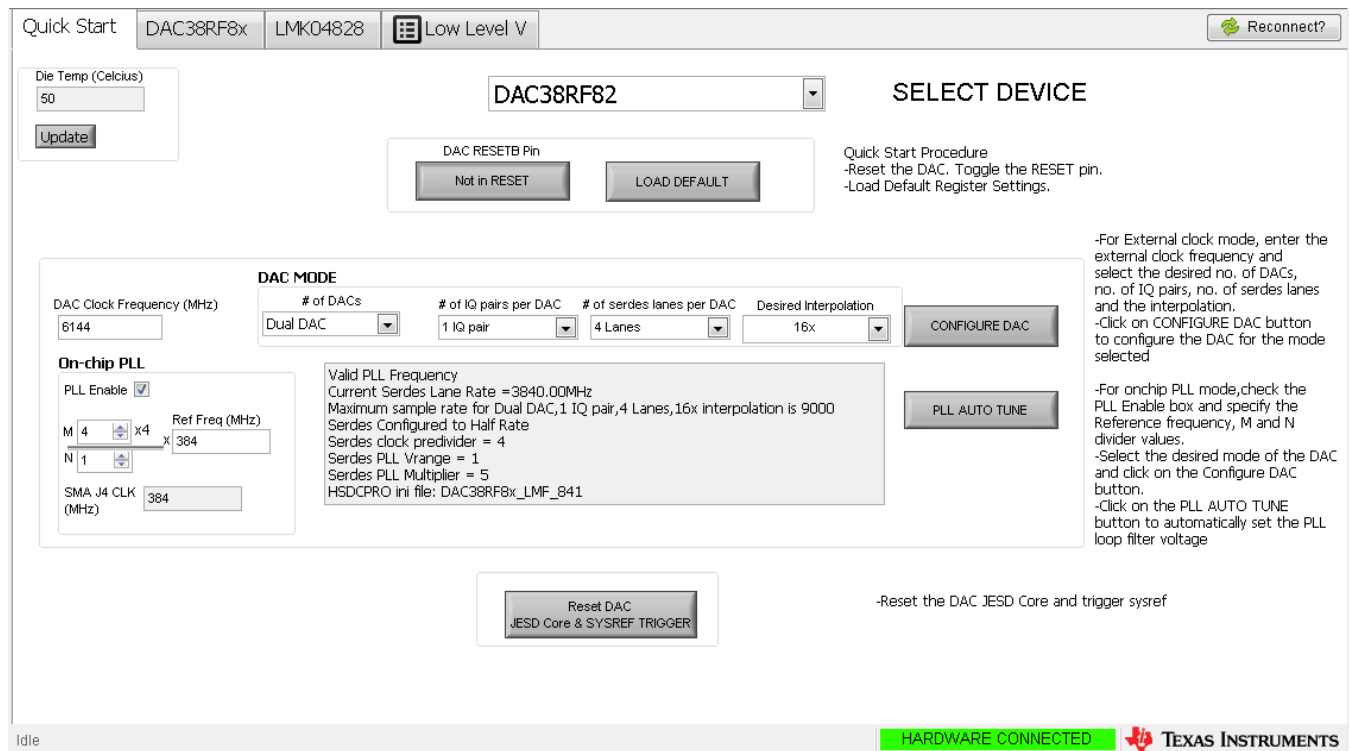
- (a) If using DAC38RF80EVM, DAC38RF87EVM, or DAC38RF82EVM set the reference frequency to 384 MHz, M = 4 and N = 1. The DAC PLL clock frequency is 6144 MHz.
- (b) If using DAC38RF86EVM, set the reference frequency to 368.64 MHz, M = 6 and N = 1. The DAC PLL clock frequency is 8847.36 MHz.
- (c) If using DAC38RF89EVM, set the reference frequency to 307.2 MHz, M = 4 and N = 1. The DAC PLL clock frequency is 4915.2 MHz.

5. Specify the desired number of DACs (Dual DAC), number of IQ pairs (1 IQ pair), number of lanes (4

lanes) and interpolation (16x), as shown in [Figure 8](#).

NOTE: It is important to record the calculated value of 'SMA J4 CLK' and set the frequency of the signal generator connected to SMA J4 to this frequency.

- Note the messages displayed for information about the SerDes rate, maximum allowed sample rate for the selected mode, and which HSDC Pro ini file to select (see the section on [HSDC Pro](#) for more information). If the DAC clock frequency is not supported for the selected mode, the *DAC Clock Frequency* box blinks.



Quick Start | DAC38RF8x | LMK04828 | Low Level V | Reconnect?

Die Temp (Celsius): 50 | Update

DAC38RF82 | SELECT DEVICE

DAC RESETB Pin: Not in RESET | LOAD DEFAULT

Quick Start Procedure:
-Reset the DAC. Toggle the RESET pin.
-Load Default Register Settings.

DAC MODE

DAC Clock Frequency (MHz): 6144

of DACs: Dual DAC | # of IQ pairs per DAC: 1 IQ pair | # of serdes lanes per DAC: 4 Lanes | Desired Interpolation: 16x | CONFIGURE DAC

On-chip PLL

PLL Enable: ☒ | Ref Freq (MHz): 384 | M: 4 | N: 1 | SMA J4 CLK (MHz): 384

Valid PLL Frequency
Current Serdes Lane Rate = 3840.00MHz
Maximum sample rate for Dual DAC, 1 IQ pair, 4 Lanes, 16x interpolation is 9000
Serdes Configured to Half Rate
Serdes clock predivider = 4
Serdes PLL Vrange = 1
Serdes PLL Multiplier = 5
HSDCPRO ini file: DAC38RF8x_LMF_841

PLL AUTO TUNE

Reset DAC JESD Core & SYSREF TRIGGER

-Reset the DAC JESD Core and trigger sysref

Idle | HARDWARE CONNECTED | TEXAS INSTRUMENTS

Figure 8. DAC38RF8xEVM GUI Quick Start Page Configured for On-Chip PLL Mode

- Click on **CONFIGURE DAC** button to load the DAC configuration data.
- Click on the **PLL AUTO TUNE** button to automatically search for the correct PLL loop filter voltage setting. If desired, the PLL may be manually tuned by stepping through the VCO tune control until the PLL LF voltage is either 3 or 4. Both the VCO tune control and PLL LF voltage indicator are available on the DAC38RF8x → Clocking tab.
- Click on **Reset DAC JESD Core & SYSREF TRIGGER** button.

2.1.6 High Speed Data Converter Pro (HSDC Pro)

- Open High Speed Data Converter Pro by going to *Start Menu → All Programs → Texas Instruments → High Speed Data Converter Pro*.
- Select the *DAC* tab.
- Use the *Select DAC* drop-down menu at the top left corner and select the appropriate .ini file (for this example, the ini file is DAC38RF8x_LMF_841). Check the DAC38RF8x GUI message box on the quick start page for the appropriate .ini file to use based on the DAC mode selected.
- When prompted to update the firmware for the DAC, click "Yes" and wait for the firmware to download to the TSW14J56.

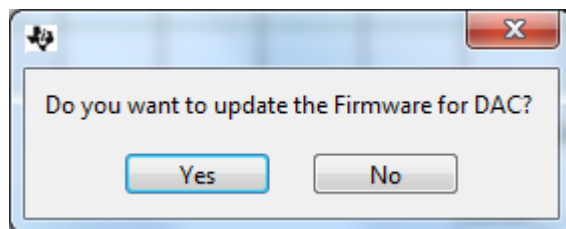


Figure 9. Load Firmware to the TSW14J56

- For this example enter "384M" in the *Data Rate (SPS)* field if using DAC38RF80EVM, DAC38RF87EVM, or DAC38RF82EVM. Data rate = Sampling frequency / Interpolation

NOTE: For this example

- If using DAC38RF86EVM, enter "552.96M" in the *Data Rate (SPS)* field
- If using DAC38RF89EVM, enter "307.2M" in the *Data Rate (SPS)* field

- Choose "2's Complement" in the *DAC Option* drop-down menu.
- Set up the *I/Q Multitone Generator* to generate a single tone at "100 k" as shown in Figure 10. Ensure that the *Tone Selection* box is set to "Complex" and then click the **Create Tones** button.

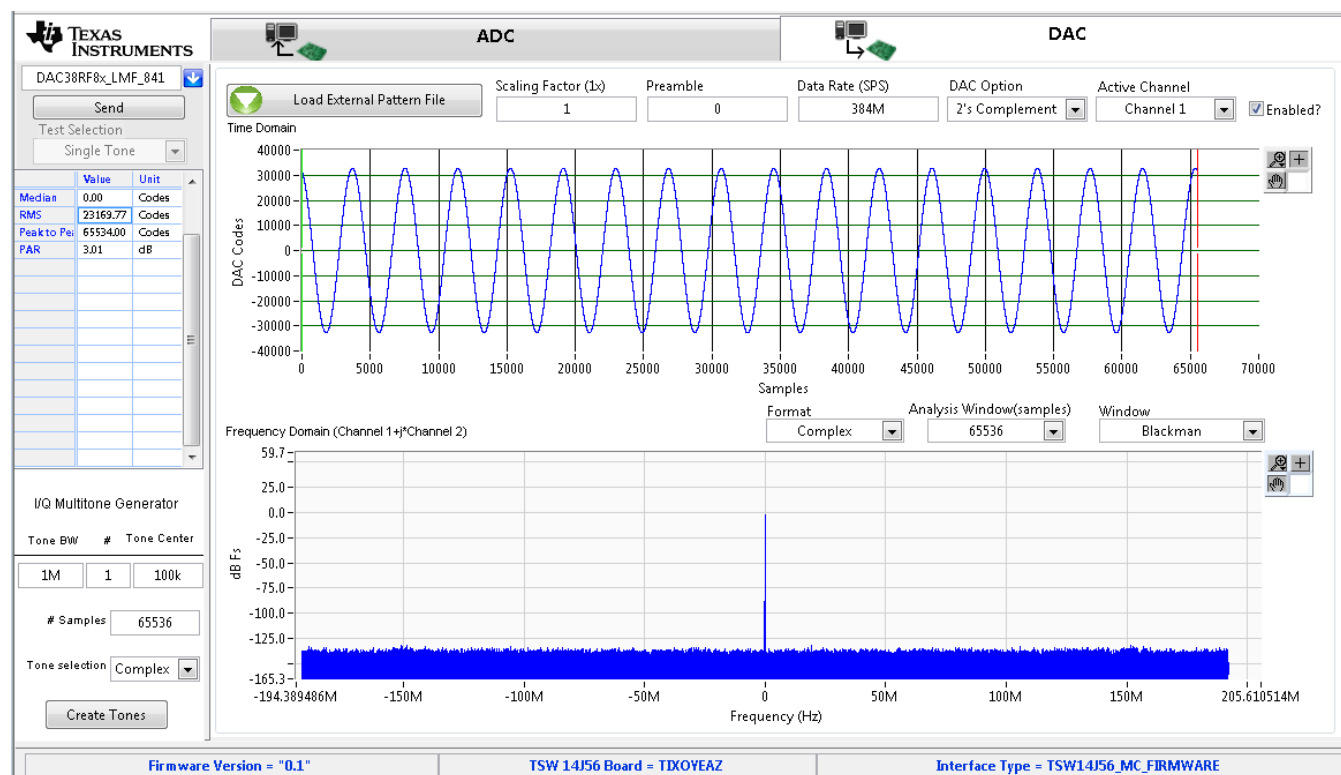


Figure 10. Complex, Single Tone Generation at 100 kHz in HSDC Pro

- Click the **Send** button to load the generated pattern to TSW14J56 EVM.
- Switch back to the DAC38RF8x GUI, and from the *Quick Start* page, click the **Reset DAC JESD Core** button to reset the RFDAC JESD204B core and also select the **Trigger LMK04828 SYSREF** button to trigger the SYSREF signal.

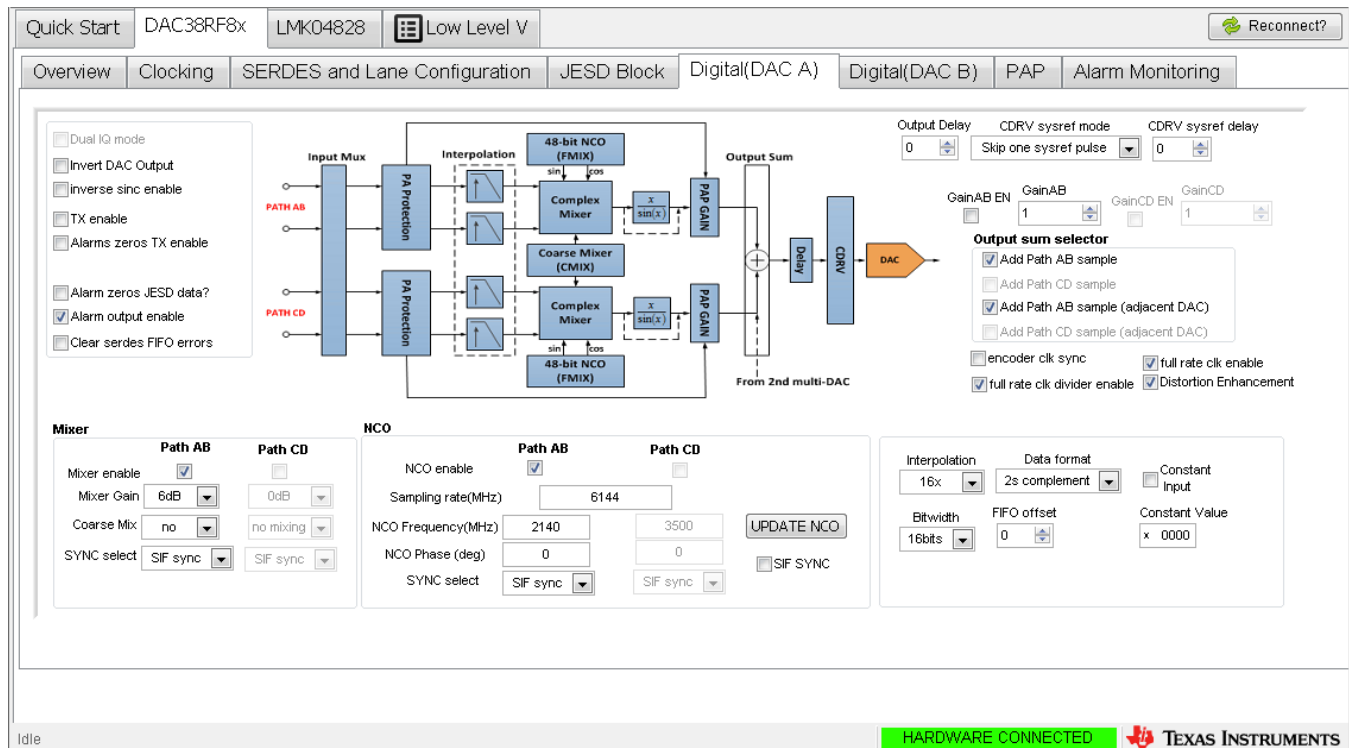


Figure 11. DAC A Digital Control Tab of the DAC38RF8x GUI

10. Navigate to the DAC38RF8x → Digital(DAC A) tab as shown in [Figure 11](#).
11. To use the coarse mixer only, check the *Mixer enable* box for path AB and select the desired coarse mixer option from the *Coarse Mix* box for path AB.
To use the NCO and mixer, check both the *Mixer enable* and *NCO enable* boxes for path AB. Also specify the DAC *Sampling rate (MHz)* and the desired *NCO frequency (MHz)*. Click the **UPDATE NCO** button to configure the NCO.

NOTE: For this example:

- (a) If using DAC38RF80EVM, DAC38RF87EVM, or DAC38RF82EVM, the sampling rate = 6144 MHz and the NCO Frequency = 2140 MHz.
- (b) If using DAC38RF86EVM, the sampling rate = 8847.36 MHz and the NCO Frequency = 2140 MHz.
- (c) If using DAC38RF89EVM, the sampling rate = 4915.2 MHz and the NCO Frequency = 2140 MHz.

12. Navigate to the DAC38RF8x tab → *Digital (DAC B)* and repeat step 11. Set the *NCO frequency (MHz)* to 1960 MHz for DAC B.
13. At this point, there should be a tone at 2140.1 MHz at the DAC A output, and another tone at 1960.1 MHz at the DAC B output. These should be visible on a spectrum analyzer connected to the respective outputs.
The *Output sum selector* of the DAC can be used to add both signals at 1960.1 MHz and 2141 MHz and output through DAC A as shown in [Figure 12](#).

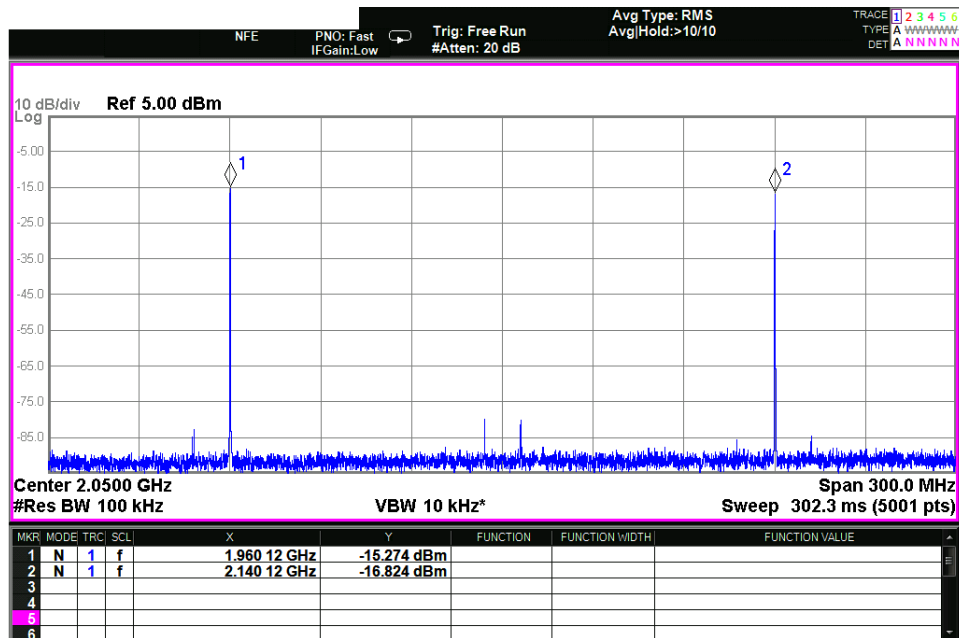


Figure 12. DAC A Output at 1960 MHz and 2140 MHz, Mixer Gain Off, Dummy Data Enabled

2.1.7 Typical Performance

Figure 13 and Figure 14 provide typical performance examples.

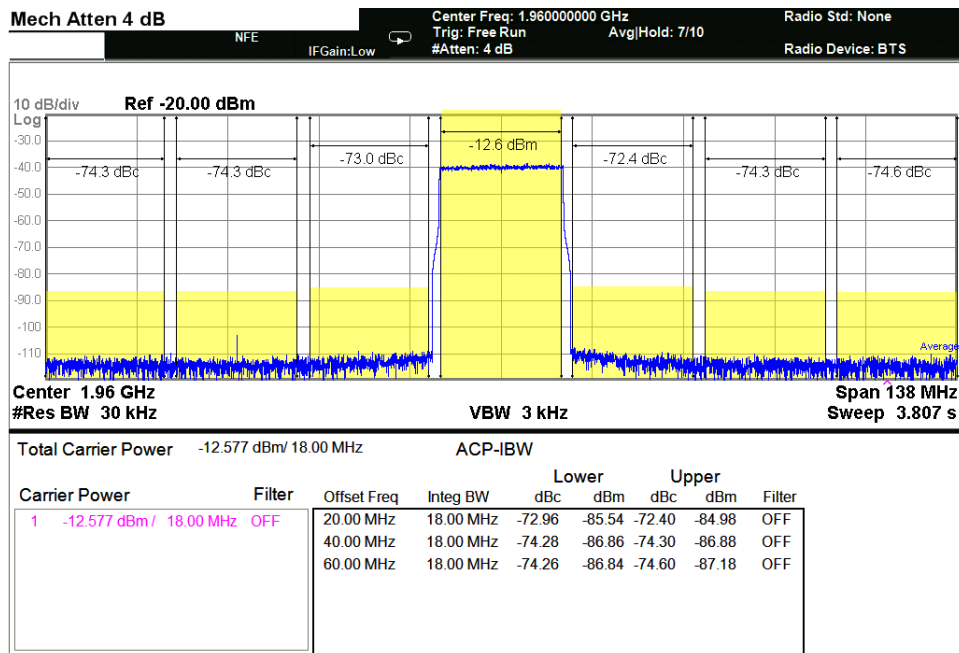


Figure 13. 1x20 MHz LTE, TM3.1, Center Frequency = 1960 MHz, DAC Coarse Gain = 10, External Clock

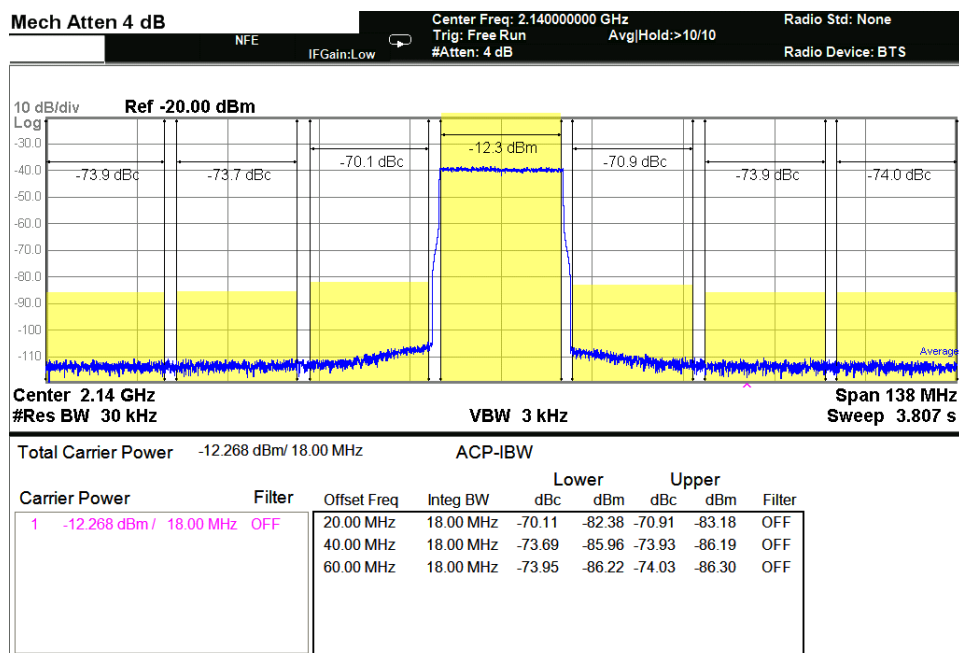


Figure 14. 1x20 MHz LTE, TM3.1, Center Frequency = 2140 MHz, DAC Coarse Gain = 10, External Clock

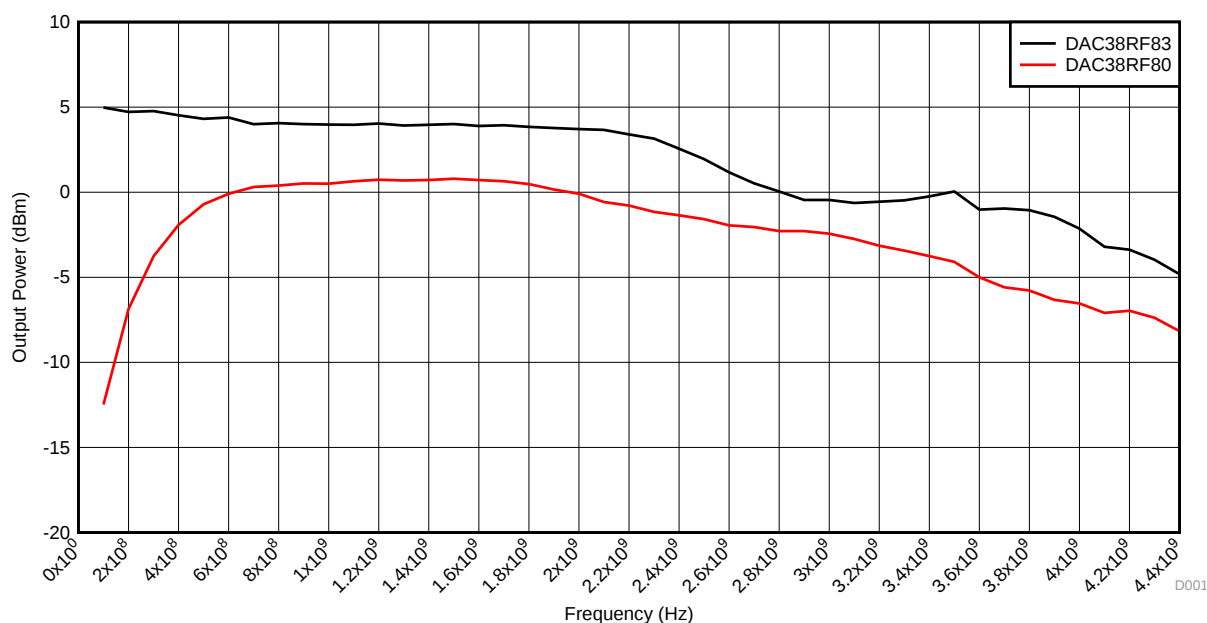


Figure 15. DAC Output Power vs Frequency (Fsampling = 8847.36 Msps)

3 Generating Configuration Files for Custom Boards

Normally, after the evaluation process, it may be necessary to transfer the DAC configuration settings to a custom board. The following steps outline the features of the DAC38RF8xEVM GUI that can facilitate this process.

3.1 Status Log

The status log can be used to determine information about the register address and data of every control on the EVM GUI. To access the status log, double click inside the lower left corner of the EVM GUI as shown in [Figure 16](#). In the following example, the *Coarse DAC Gain* control on the EVM GUI will be used to show how to use the status log:

- Bring up the status log by doubling clicking inside the lower left corner of EVM GUI ([Figure 16](#)). Once opened, right click anywhere inside the status log window and select "clear log" to clear the log window.
- Navigate to the DAC38RF8x>>Overview tab and change the value of Coarse DAC Gain control to 11. Check the status log for information on the SPI address (0x0D), page (0x4) and data (0xB000) associated with the *Coarse DAC Gain* control. The information in the status log can be interpreted as follows:
Write Register: DAC38RF8x.config* [0x4-bits page address,8-bits register address]-[16-bits data]

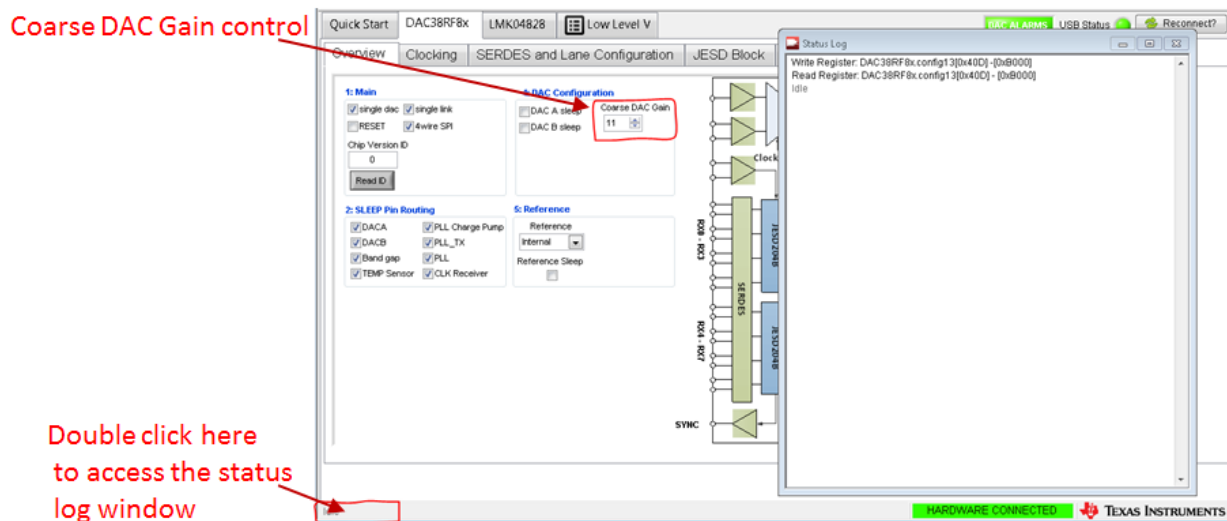


Figure 16. DAC38RF8xEVM GUI Status Log

3.2 Low Level View

The low Level View tab can be used to perform the following functions:

1. Read and Save configuration file
To save all the register configuration information for the current session, from the low level view tab, click on the "read all" button (or icon) to update the register information in the GUI. Afterwards, click on the "save all" button (or icon) and enter a desired name to be used to save the configuration file. The DAC38RF8x configuration registers are saved in the following format:
[4-bits page address (in hex), 8-bits register address (in hex)] 16bits data (in hex)
2. Access a specific register
In the *Register Map* window on the *Low Level View*, click on any desired register name to highlight the register. The *Register Description* window provides detailed description of the highlighted register. Also, read and write actions can be performed on this specific register using the **Write Register** and **Read Register** buttons in the lower right corner of the GUI (see [Figure 17](#)).



Figure 18 illustrates the DAC output circuit schematic.

Figure 18. DAC Output Circuit Schematic

Figure 19. TCM3-452X-1+ Frequency Response

B.1 Clock Balun Characteristics

Figure 20 illustrates the clock input path circuit schematic.

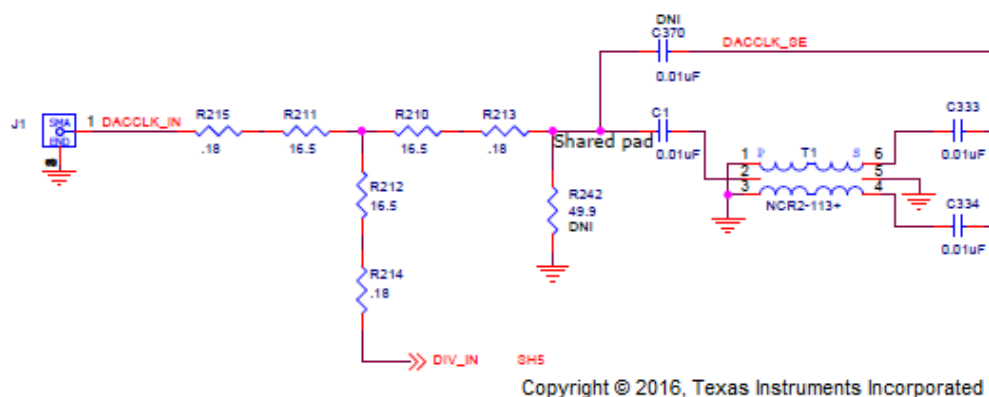


Figure 20. Clock Input Path Circuit Diagram

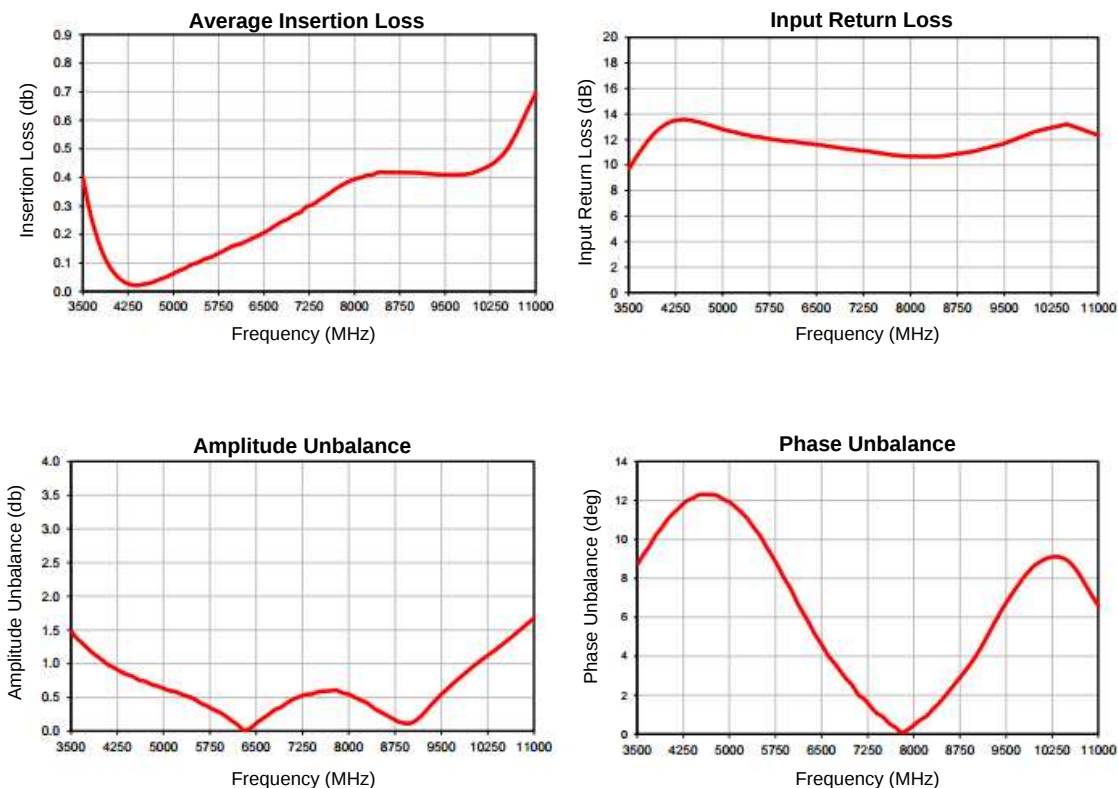


Figure 21. NCR2-113+ Frequency Response

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2016) to A Revision	Page
• Modified abstract to specify all the EVMs part of DAC38RF8xEVM family.	1
• Removed instructions for installing HSDCPRO patch.	2
• Removed HSDCPRO patch from the list of required software in the <i>Required Hardware and Software</i> section.	2
• Added information on various jumpers on EVM in Table 2	3
• Added information on the various available clocking options on EVM in Section 1.2.1	3
• Updated Figure 4	7
• Added new figure in Figure 5	7
• Updated Figure 8	10
• Updated Figure 11	12
• Included information on configuration file generation in Section 3	15
• Added Removed <i>Known Issues</i> section from before <i>Appendix A</i>	17

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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