MX575ABC100M000

Ultra-Low Jitter 100MHz LVCMOS XO

ClockWorks® FUSION

General Description

The MX575ABC100M000 is an ultra-low phase jitter XO with LVCMOS output optimized for high line rate applications.

Applications

- PCI-Express Gen 1/2/3/4
- Storage

Features

- 100MHz LVCMOS
- Typical phase noise:
  - 100fs (Integration range: 1.875MHz-20MHz)
- ±50ppm total frequency stability
- -40°C to +85°C temperature range
- Industry standard 6-Pin 7mm x 5mm LGA package

Absolute Maximum Ratings

Supply Voltage (VIN).....+4.6V
Lead Temperature (soldering, 10s).....260°C
Storage Temperature (T_S).....125°C
ESD Rating (HBM).....2kV

Operating Ratings

Supply Voltage (VIN).....+2.375V to +3.63V
Ambient Temperature (TA).....-40°C to +85°C

Electrical Characteristics

VDD = 2.375 - 3.63V, TA = -40°C to +85°C, output terminated with 50 Ohms to VDD/2.[1]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDD	Supply Current				95	mA
F0	Center Frequency			100		MHz
	Frequency Stability	Note 2			±50	ppm
Øj	Phase Noise	Integration Range (12kHz to 20MHz) Integration Range (1.875MHz to 20MHz)		149 100		fsRMS
Tstart	Start-Up Time				20	ms
TR/TF	Rise/Fall time		100		500	ps
	Duty Cycle		45		55	%
VIH	Input High Voltage	3.3V Operation	2		VDD + 0.3	V
VIL	Input Low Voltage	3.3V Operation	-0.3		0.8	V
VOH	Output High Voltage	LVCMOS output levels	VDD - 0.8			V
VOL	Output Low Voltage	LVCMOS output levels			0.6	V

Notes:
1. Guaranteed after thermal equilibrium.
2. Inclusive of initial accuracy, temperature drift, aging, shock, vibration.

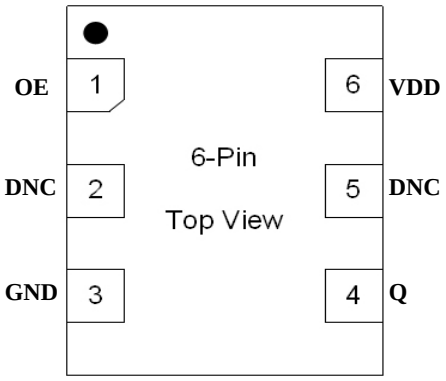
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Ordering Information

Ordering Part Number	Marking Line 1	Marking Line 3	Shipping	Package
MX575ABC100M000	MX575AB	C100M000	Tube	6-Pin 7mm x 5mm LGA
MX575ABC100M000-TR	MX575AB	C100M000	Tape and Reel	6-Pin 7mm x 5mm LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	OE	I, SE	LVCMOS	Output Enable, disables output to tri-state, 0 = Disabled, 1 = Enabled, 50k Ohms Pull-Up
2	DNC			Make no connection, leave floating.
3	GND	PWR		Power Supply Ground
4, 5	Q, DNC	O, SE	LVCMOS	Clock Output Frequency = 100MHz
6	VDD	PWR		Power Supply

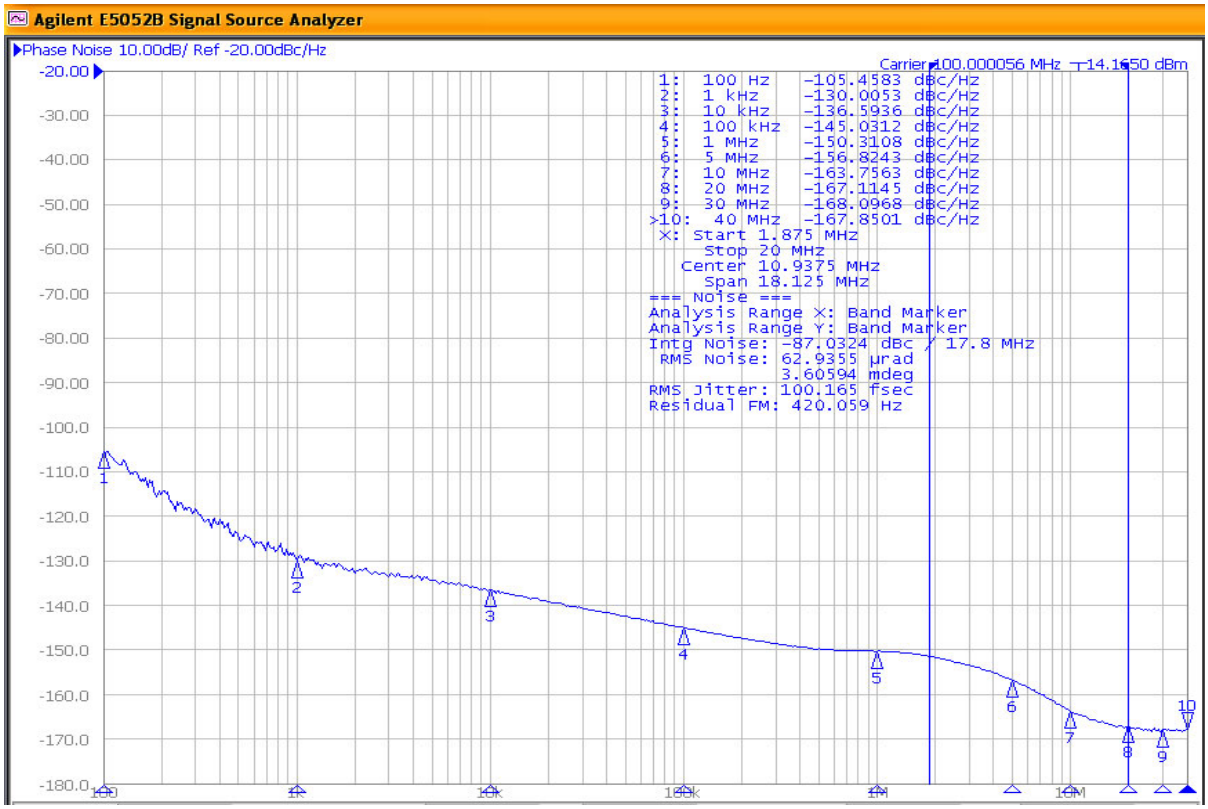


Figure 1. LVCMOS Output 100MHz 1.875MHz-20MHz 100fs

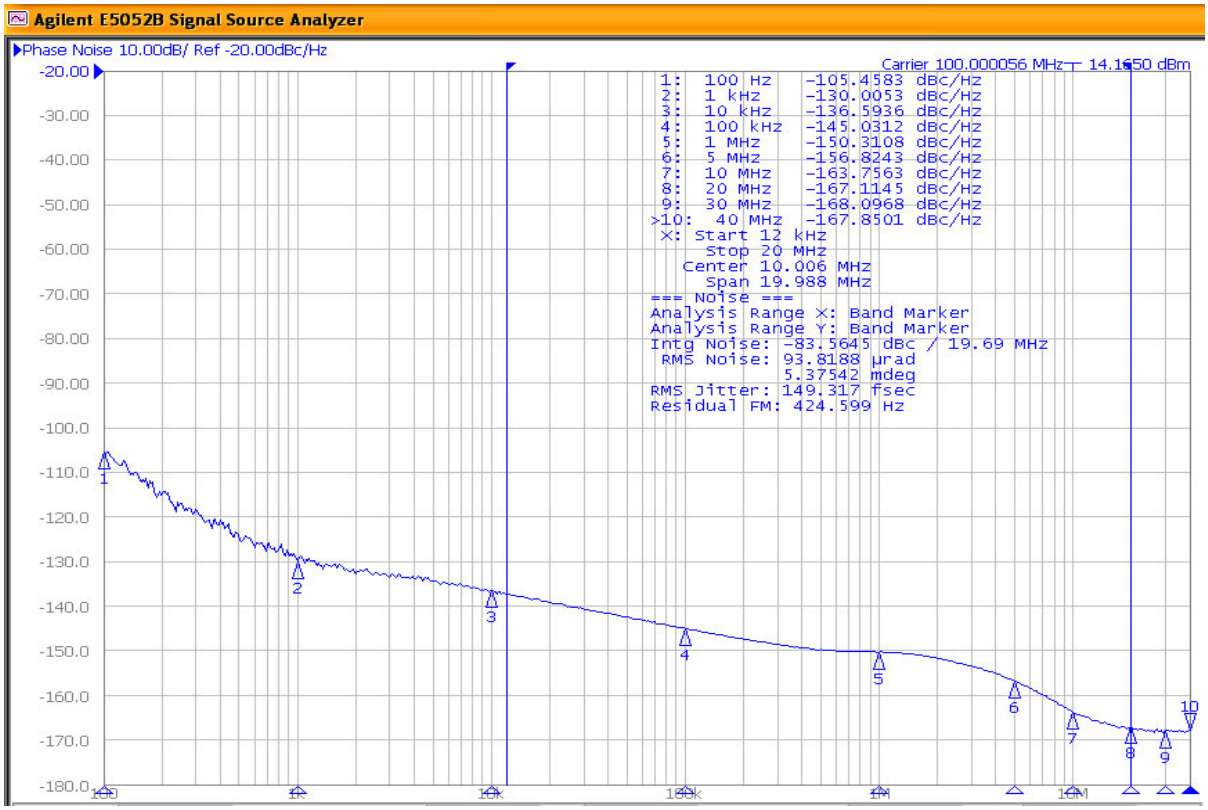


Figure 2. LVCMOS Output 100MHz 12kHz-20MHz 149fs

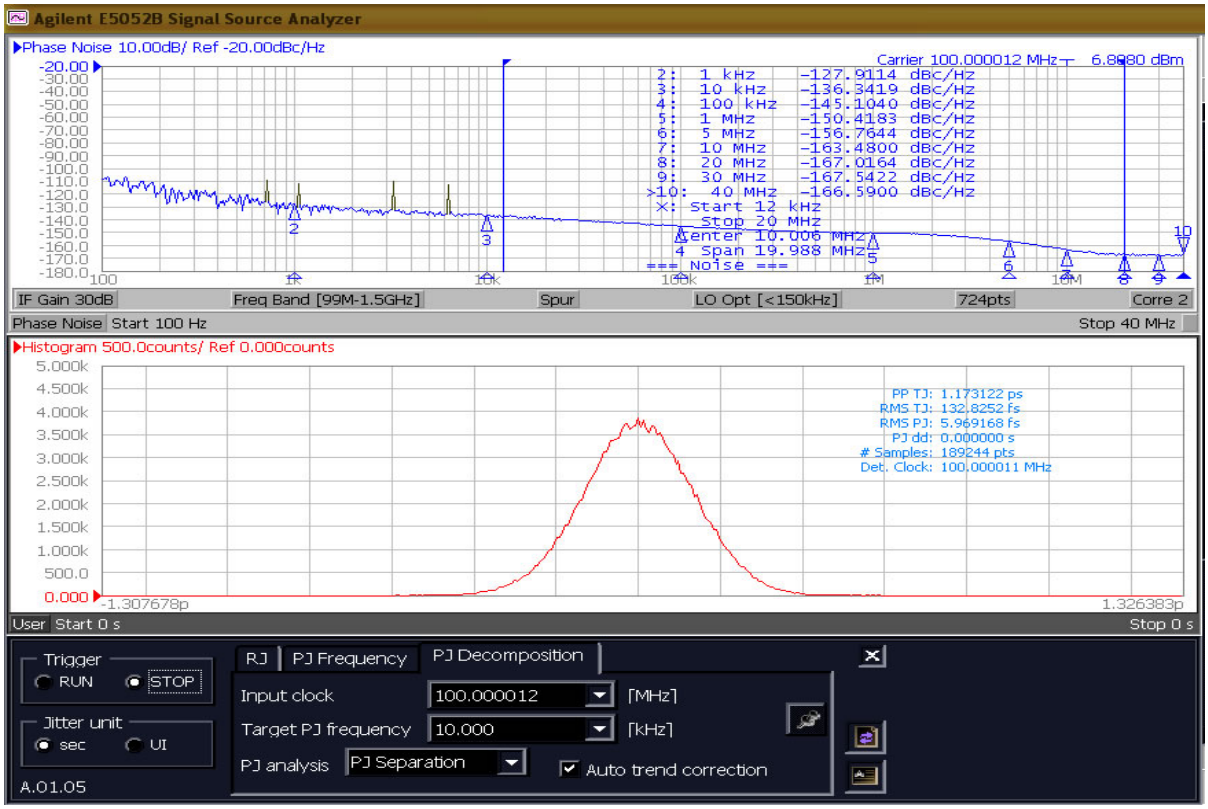
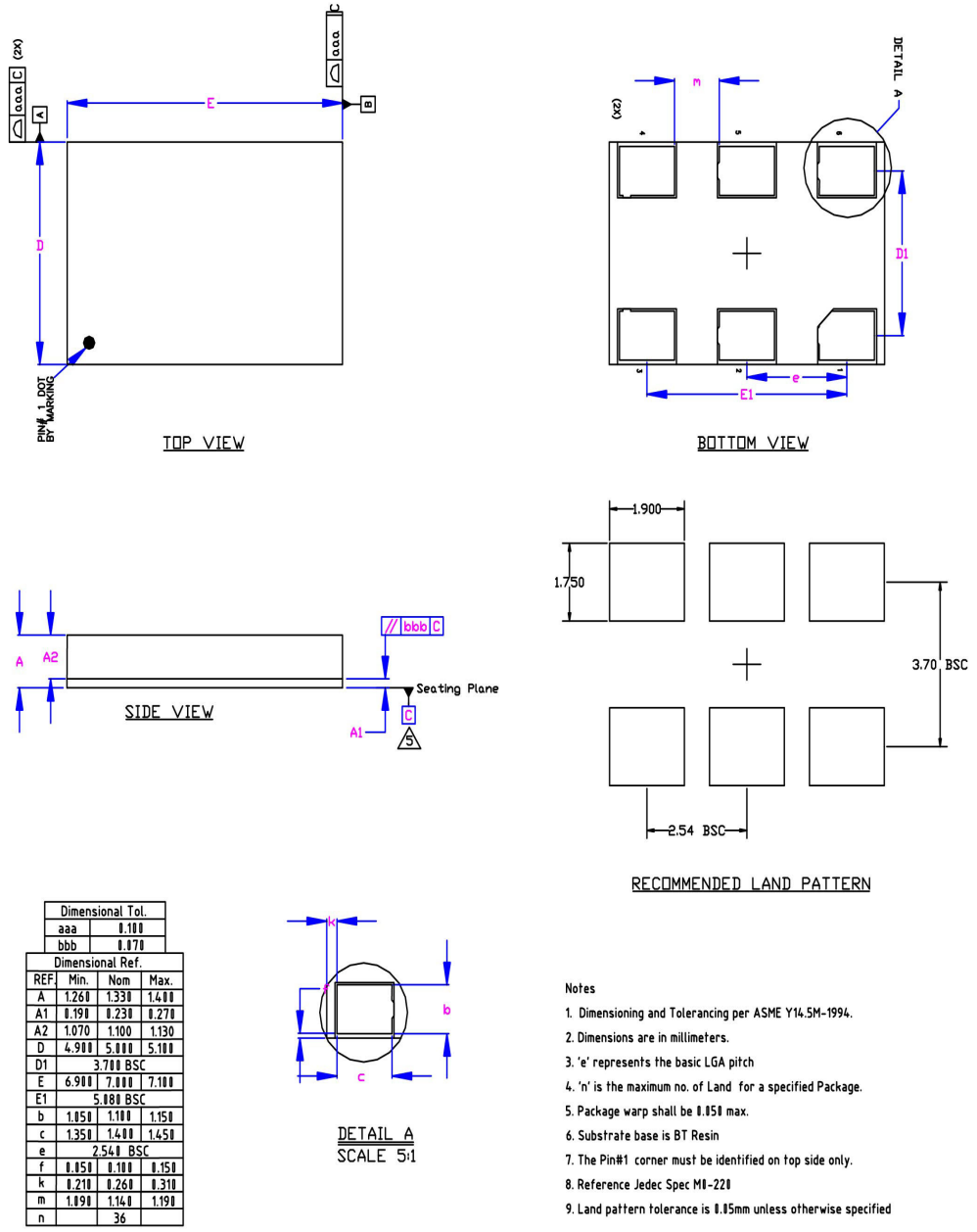


Figure 3. E5001A Period Jitter @ 100MHz LVCMOS, RMS TJ: 132.8fs, Pk-Pk TJ: 1.17ps

Package Information and Recommended Land Pattern for 6-Pin LGA[3]



Dimensional Tol.	
aaa	0.100
bbb	0.070

Dimensional Ref.			
REF.	Min.	Nom	Max.
A	1.260	1.330	1.400
A1	0.190	0.230	0.270
A2	1.070	1.100	1.130
D	4.900	5.000	5.100
D1	3.700 BSC		
E	6.900	7.000	7.100
E1	5.080 BSC		
b	1.050	1.100	1.150
c	1.350	1.400	1.450
e	2.540 BSC		
f	0.050	0.100	0.150
k	0.210	0.260	0.310
m	1.090	1.140	1.190
n		36	

Notes

1. Dimensioning and Tolerancing per ASME Y14.5M-1994.
2. Dimensions are in millimeters.
3. 'e' represents the basic LGA pitch
4. 'n' is the maximum no. of Land for a specified Package.
5. Package warp shall be 0.050 max.
6. Substrate base is BT Resin
7. The Pin#1 corner must be identified on top side only.
8. Reference Jedec Spec MO-220
9. Land pattern tolerance is 0.05mm unless otherwise specified

6-Pin LGA (7x5mm)

Note:

3. Package information is correct as of the publication date. For updates and most current information, go to www.microchip.com.

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