KSZ9031MNX

KSZ9031MNX Silicon Errata & Data Sheet Clarification

This document describes known silicon errata for the Microchip KSZ9031MNX device, which include the following variants:

- KSZ9031MNXCA
- KSZ9031MNXCC
- KSZ9031MNXIA
- KSZ9031MNXIC

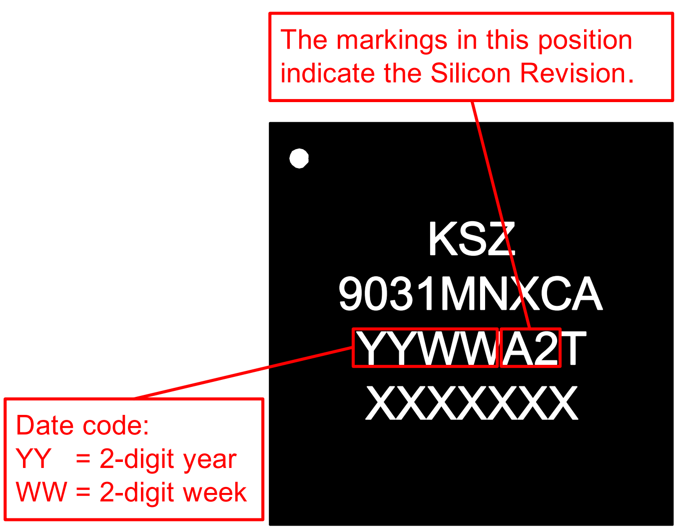
The silicon errata discussed in this document are for silicon revisions as listed in Table 1. The silicon revision can be determined by the device's top marking as indicated in Figure 1. A summary of KSZ9031MNX silicon errata is provided in Table 2.

TABLE 1: AFFECTED SILICON REVISIONS

Part Numbers	Silicon Revision
KSZ9031MNXCA, KSZ9031MNXCC, KSZ9031MNXIA, KSZ9031MNXIC	A, A2, A4

Note: All future orders will be transitioning to silicon revision A4. Contact your local sales representative for additional information.

FIGURE 1: TOP MARKING DATE CODE INDICATION



Note: The purpose of Figure 1 is to detail the top markings of an example part and highlight the location of the silicon revision code. Other top marking values may differ (lot codes, location of manufacture, etc.).

TABLE 2: SILICON ISSUE SUMMARY

Item Number	Silicon Issue Summary	Affected Silicon Revisions
1.	Device fails to link after Asymmetric Pause capability is set	A, A2, A4
2.	Duty cycle variation for optional 125MHz reference output clock	A, A2, A4
3.	LED toggle is not visible for Tri-color Dual-LED Mode	A, A2, A4
4.	Auto-Negotiation link-up failure / long link-up time due to default FLP interval setting	A, A2, A4
5.	Link failure after repeated unplugging/plugging of cable in forced 100BASE-TX mode	A, A2, A4
6.	1000BASE-T Transmitter Jitter fails to meet IEEE compliance specification	A, A2, A4
7.	1000BASE-T Transmitter Distortion fails to meet IEEE compliance specification	A, A2, A4
8.	Transmitter common mode voltage drift at cold temperature	A, A2

Silicon Errata Issues

Module 1: Device fails to link after Asymmetric Pause capability is set

DESCRIPTION

Whenever the device's Asymmetric Pause capability (Register 4h, Bit [11]) is set to 1, link-up may fail after a link-up to link-down transition (e.g., a cable disconnect).

END USER IMPLICATIONS

The device may fail to establish link when the Asymmetric Pause capability bit is set to 1.

Work around

Do not enable (set to 1) the Asymmetric Pause capability bit. If enabling this bit is required, a second link-up attempt (e.g., disconnect and reconnect cable) is required to establish link.

PLAN

This erratum will not be corrected in a future revision.

Module 2: Duty cycle variation for optional 125MHz reference output clock

DESCRIPTION

When the device links in the 1000BASE-T slave mode only, the optional 125MHz reference output clock (CLK125_NDO, Pin 55) has wide duty cycle variation.

END USER IMPLICATIONS

The optional CLK125_NDO clock does not meet the RGMII 45/55 percent (min/max) duty cycle requirement and therefore cannot be used directly by the MAC side for clocking applications that have setup/hold time requirements on rising and falling clock edges (e.g., to clock out RGMII transmit data from MAC to PHY (KSZ9031MNX device)).

Work around

Use an alternative external clock source for the MAC.

If an alternative clock source is not available, the CLK125_NDO clock can be used with limitations. One solution requires the MAC side clock input to include an on-chip PLL that locks on the rising or falling edge of the CLK125_NDO clock. Another solution requires the device to always operate in master mode (Register 9h, Bits [12:11] = '11') whenever there is 1000BASE-T link-up, which is workable only in those applications where the link partner is known and can always be configured to slave mode for 1000BASE-T.

PLAN

This erratum will not be corrected in a future revision.

Module 3: LED toggle is not visible for Tri-color Dual-LED Mode

DESCRIPTION

In Tri-color Dual-LED mode, the LED[2:1] pin outputs toggle high pulses for transmit/receive activity indication. The high pulse width incorrectly tracks the activity data rate. At low data rate (e.g., one frame per second), the LED pin drives high (OFF) with a narrow high pulse width of about 640ns.

END USER IMPLICATIONS

Typically, the LED toggle rate should be <10Hz (100ms clock period or 50ms high pulse width) to be visible to the human eye. A 640ns pulse is not visible.

Work around

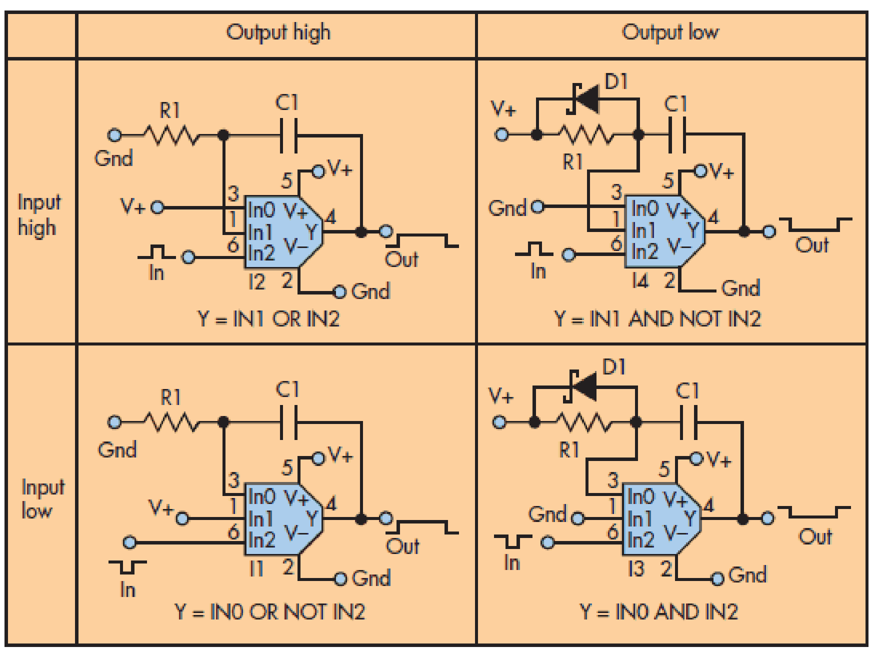
Use the Single-LED mode instead.

If Tri-color Dual-LED mode must be used, use a pulse stretching circuit to detect high narrow pulse widths down to 500ns and stretch them to the visible width (e.g., >50ms). The following Electronic Design web link article has a sample pulse stretching circuit:

http://electronicdesign.com/lighting/configurable-logic-chip-stretches-pulses-brighten-led-flash

Use the Input high / Output high configuration, as shown in Figure 2 from the Electronic Design link. The output high stretch time is set by the time constant (R1 * C1).

FIGURE 2: LED CONFIGURATION



A configurable logic chip, the SN74LVC1G97, can serve as a "pulse stretcher" when the original (input) pulse is too short to perform the required task. The designer can wire the circuit in four configurations.

PLAN

This erratum will not be corrected in a future revision.

Module 4: Auto-Negotiation link-up failure / long link-up time due to default FLP interval setting

DESCRIPTION

The device's Auto-Negotiation FLP (Fast Link Pulse) burst-to-burst timing defaults to 8ms. IEEE Standard specifies this timing to be 16ms +/-8ms. Some link partners, such as Intel G-PHY controllers, were observed in bench tests to have tighter timing requirements that need to detect the FLP interval timing centered at 16ms.

END USER IMPLICATIONS

With the default 8ms FLP interval setting, intermittent link failure and long link-up time can occur with some link partners.

Work around

After device power-up/reset, change the FLP interval to 16ms using the following programming sequence to set MMD - Device Address 0h, Register 4h = 0x0006 and MMD - Device Address 0h, Register 3h = 0x1A80:

a) Write Register Dh = 0x0000 //Set up register address for MMD - Device Address 0h
b) Write Register Eh = 0x0004 //Select Register 4h of MMD - Device Address 0h
c) Write Register Dh = 0x4000 //Select register data for MMD - Device Address 0h, Register 4h
d) Write Register Eh = 0x0006 //Write value 0x0006 to MMD - Device Address 0h, Register 4h
e) Write Register Dh = 0x0000 //Set up register address for MMD - Device Address 0h
f) Write Register Eh = 0x0003 //Select Register 3h of MMD - Device Address 0h
g) Write Register Dh = 0x4000 //Select register data for MMD - Device Address 0h, Register 3h
h) Write Register Eh = 0x1A80 //Write value 0x1A80 to MMD - Device Address 0h, Register 3h

Then restart Auto-Negotiation for the 16ms FLP interval setting to take effect.

PLAN

This erratum will not be corrected in a future revision.

Module 5: Link failure after repeated unplugging/plugging of cable in forced 100BASE-TX mode

DESCRIPTION

With Auto-Negotiation disabled and the speed set to forced 100BASE-TX mode, the device can sometimes run into a failed link-up state where the device is in the link-down state and its link partner is in the link-up state. This link failure occurs if the device receive circuit does not get properly reset when the link status changes from link-up to link-down (e.g. cable is unplug), causing the next link-up attempt to fail when the cable is reconnected.

END USER IMPLICATIONS

When the device is set to forced 100BASE-TX mode, intermittent link failure can occur after repeated unplugging/ plugging of the cable.

Work around

Force a restart of the link-up process by causing the link partner to drop link and thereby cease its 100BASE-TX signal transmission to the device. When the 100BASE-TX receive signal is no longer detected, the device automatically generates a reset to its receive circuit to exit the link failure state and restart the link-up process.

PLAN

This erratum will not be corrected in a future revision.

Module 6: 1000BASE-T Transmitter Jitter fails to meet IEEE compliance specification

DESCRIPTION

The device's 1000BASE-T Transmitter Jitter, Master Filtered (No TX_TCLK Access) is in the 500-600ps range, versus the <300ps indicated in the IEEE specification.

END USER IMPLICATIONS

The device consumes an additional 200-300ps of the system's total jitter budget.

Link partners in properly designed systems that follow good Gigabit PHY design practices will not experience link drop and packet errors/losses that are attributed directly to the transmit jitter of the device. In lab testing and field testing, the device has shown to have neither link drop nor packet error/loss in continuous overnight runs (>12 hours) with 1000Mbps full-duplex traffic at 100% utilization. Table 3 provides a sampling of the overnight test results.

TABLE 3: SAMPLE OVERNIGHT TEST RESULTS

Link Partners	Continuous Overnight Run (>12 hours)	
	Short Cable (2 feet)	Long cable (100 meters)
KSZ9031 <=> KSZ9031	No packet error/loss	No packet error/loss
KSZ9031 <=> KSZ9021	No packet error/loss	No packet error/loss
KSZ9031 <=> LAN7800	No packet error/loss	No packet error/loss
KSZ9031 <=> LAN8810	No packet error/loss	No packet error/loss
KSZ9031 <=> Netgear GS105	No packet error/loss	No packet error/loss

Link partners in poorly designed systems will also typically exhibit poor receiver jitter tolerance. Here, link drops and packet errors/losses may be attributed to the receiver jitter tolerances of the link partners, not necessarily the transmit jitter of the device.

Work around

None.

PLAN

This erratum will not be corrected in a future revision.

Module 7: 1000BASE-T Transmitter Distortion fails to meet IEEE compliance specification

DESCRIPTION

The device's 1000BASE-T Transmitter Distortion is in the 8-20mV range, versus the <10mV indicated in the IEEE specification.

END USER IMPLICATIONS

It is unlikely this specification failure will impact system performance. The following link to the Gigabit Transmit Distortion Testing document on the IEEE802.org website also questions the validity of this measurement:

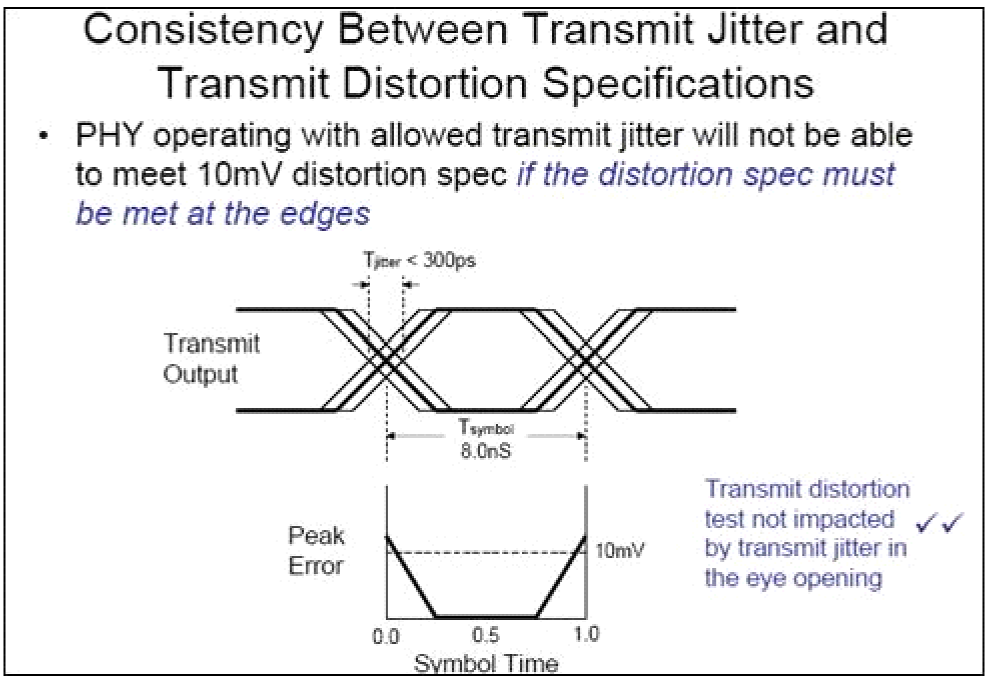
http://www.ieee802.org/3/axay/public/may_07/sefidvash_1_0507.pdf

IEEE testing calls for <10mV peak transmitter distortion for at least 60% of the UI within the eye opening. However, this measurement might not be valid, as the transmit distortion test is sensitive to transmit jitter. Refer to the explanation below, taken from the aforementioned IEEE document.

The Gigabit Transmit Distortion Testing document indicates:

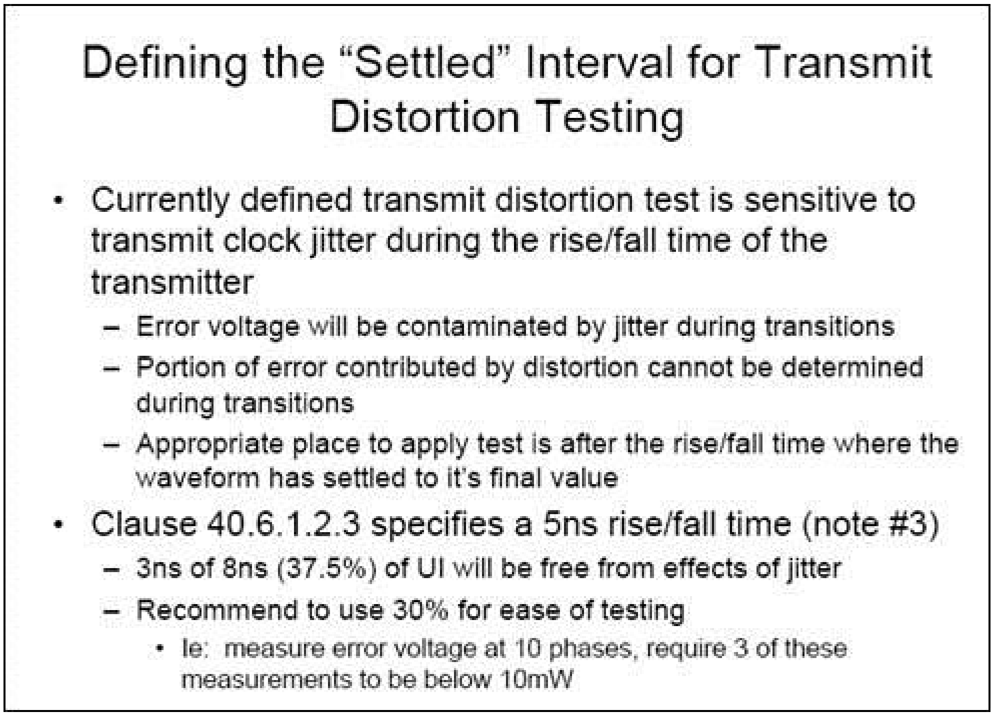
- On page 6, a contradiction between Transmit Jitter and Transmit Distortion requirements:

FIGURE 3: IEEE DOCUMENT PAGE 6



- On page 7:
  - The transmit distortion test is sensitive to transmit clock jitter during the rise/fall time.
  - It is recommended to change the requirement to use at least 30%, instead of at least 60%, of the UI within the eye opening for the <10mV peak transmitter distortion.

FIGURE 4: IEEE DOCUMENT PAGE 7



Extensive testing has been performed to ensure the device can inter-operate with different Gigabit PHY link partners. The following is a partial list of some of the Gigabit PHY link partners that have tested against the device and have passed interoperability testing.

TABLE 4: TESTED GIGABIT PHY LINK PARTNERS

Link Partner
3Comm Corp. SuperStack 3 4050
3Comm Corp. SuperStack II 4900
Agere Systems ET1310-EVB NIC
Atheros AR8314 Switch
Atheros AR8316 Switch
Avaya 9640G IP Phone
Broadcom BCM53115
Broadcom BCM56218
Broadcom BCM5650
Coyote Point Systems E550si
Coyote Point Systems E650gx
Dell Power Connect 6224
Extreme Networks Summit 1i
HP ProCurve J9020A

TABLE 4: TESTED GIGABIT PHY LINK PARTNERS (CONTINUED)

Link Partner
Intel NetStructure 480T
Polycom SoundPoint IP 670 Phone
Realtek RTL8368S+RTL8214
Realtek RTL8369+RTL8212
Realtek 8111C NIC

Work around

None.

PLAN

This erratum will not be corrected in a future revision.

Module 8: Transmitter common mode voltage drift at cold temperature

DESCRIPTION

Below 0^{o}C, the voltage controlled output of the transmitter can become unstable and lead to distorted signaling. The voltage instability is common on both the TX+ and TX- lines, so the AC data is not affected unless the voltage drifts to the AVDDH level. If the common mode voltage drifts too close to AVDDH, the higher voltages will begin to clip, which can prevent successful Ethernet communication.

END USER IMPLICATIONS

There are two possible ways this issue may be seen:

- The device may exhibit communication issues (i.e., dropped link)
- The device may not link or communicate

Work around

- Operate above 0^{o}C
- Contact your local sales representative for additional information

PLAN

This erratum has been corrected in silicon revision A4. All future orders will be transitioning to A4 devices. Contact your local sales representative for additional information.

APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS80000691D (05-25-17)	Module 8.	Updated module to indicate the erratum has been corrected in silicon revision A4.
	Intro	Added note: "All future orders will be transitioning to silicon revision A4. Contact your local sales representative for additional information."
	Table 2	Added "Affected Silicon Revisions" column for clarity.
	All	Minor grammatical corrections.
DS80000691C (01-13-17)	Module 8.	Added new erratum: • Transmitter common mode voltage drift at cold temperature
DS80000691B (07-26-16)	Module 6., Module 7.	Added new errata: • 1000BASE-T Transmitter Jitter fails to meet IEEE compliance specification • 1000BASE-T Transmitter Distortion fails to meet IEEE compliance specification
DS80000691A (03-16-16)	All	Initial release

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