bq51222 Dual Mode 5-W (WPC v1.2 and PMA) Single Chip Wireless Power Receiver

1 Features

- Robust 5-W Solution with 50% Lower Losses for Improved Thermals
  - Inductorless Receiver for Lowest Height Profile Solution
  - Adjustable Output Voltage (4.5 to 8 V) for Coil and Thermal Optimization
  - Fully Synchronous Rectifier with 96% Efficiency
  - 97% Efficient Post Regulator
  - 79% System Efficiency at 5 W
- WPC v1.2 and PMA Compliant Communication
- Patented Transmitter Pad Detect Function Improves User Experience
- I^2C Communication with Host

2 Applications

- Smart Phones, Tablets, and Headsets
- Wi-Fi Hotspots
- Power Banks
- Other Handheld Devices

3 Description

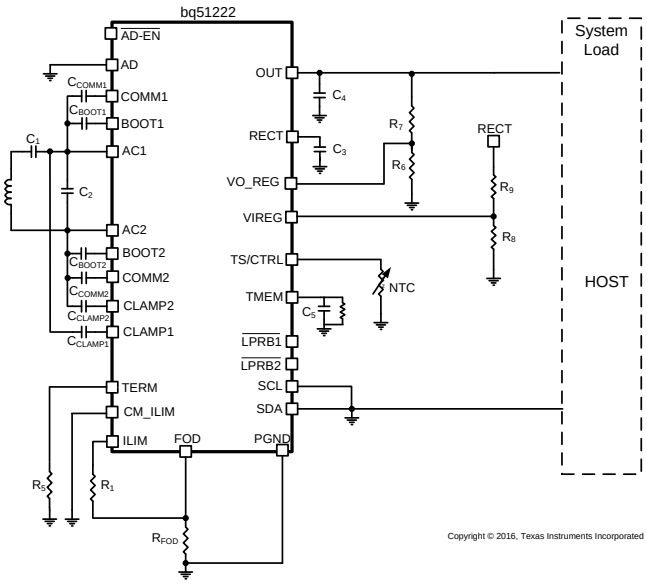
The bq51222 device is a fully contained wireless power receiver capable of operating in both the Wireless Power Consortium (WPC) Qi and Power Matters Alliance (PMA) protocols which allows a wireless power system to work with both inductive charging standards. The bq51222 device provides a single device power conversion (rectification and regulation) as well as the digital control and communication for both standards. It also has autonomous detection of protocol and requires no additional active devices. The bq51222 device complies with the WPC v1.2 and PMA communication protocol. Together with the WPC or a PMA primary-side controller, the bq51222 device enables a complete wireless power transfer system for a wireless power supply solution. The receiver allows for synchronous rectification, regulation and control and communication to all exist in a market-leading form factor, efficiency, and solution size.

Device Information(1)

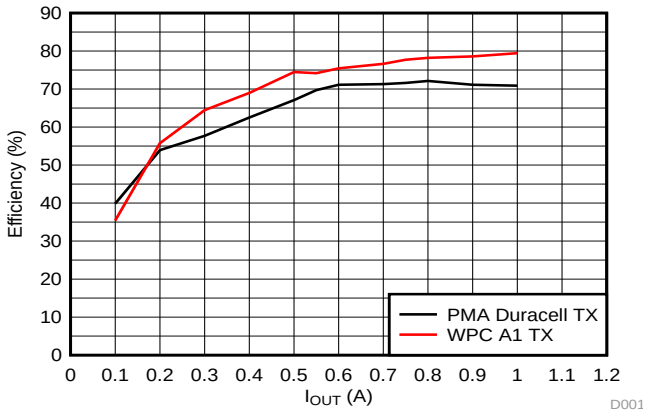
PART NUMBER	PACKAGE	BODY SIZE (MAX)
bq51222	DSBGA (42)	3.586 mm × 2.874 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Dual Mode Efficiency 5-V Out



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Original (July 2016) to Revision A **Page**

- Changed from Product Preview to Production Data ... 1

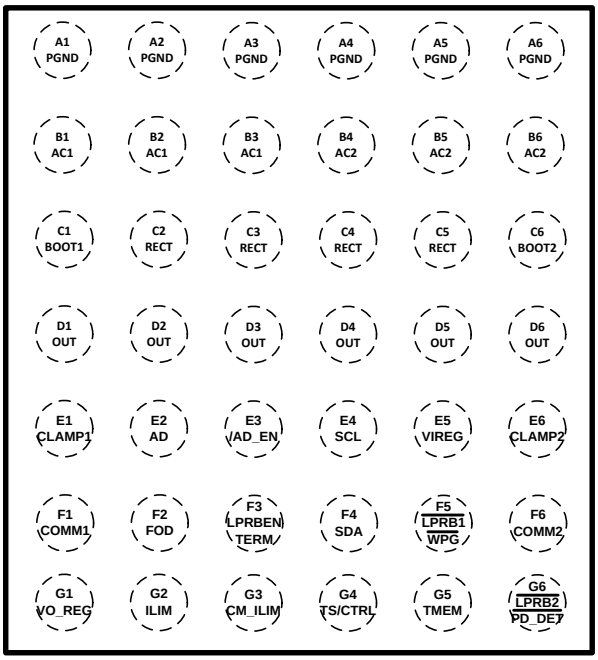
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5 Device Comparison Table

DEVICE	MODE	MORE
bq51221	Dual (WPC v1.1, PMA)	Adjustable output voltage, highest system efficiency, I^2C
bq51222	Dual (WPC v1.2, PMA)	Adjustable output voltage, highest system efficiency, I^2C
bq51021	WPC v1.1	Adjustable output voltage, highest system efficiency, I^2C
bq51020	WPC v1.1	Adjustable output voltage, highest system efficiency, standalone

6 Pin Configuration and Functions

YFP Package
42-Pin DSBGA
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
AC1	B1, B2, B3	I	AC input power from receiver resonant tank
AC2	B4, B5, B6	I	
AD	E2	I	Adapter sense pin
$\overline{\text{AD-EN}}$	E3	O	Push-pull driver for PFET that can pass AD input to the OUT pin; used for adapter mux control
BOOT1	C1	O	Bootstrap capacitors for driving the high-side FETs of the synchronous rectifier
BOOT2	C6	O	
COMM1	F1	O	Open-drain FETs used to communicate with primary by varying reflected impedance
COMM2	F6	O	
CLAMP1	E1	O	Open-drain FETs used to clamp the secondary voltage by providing low impedance across secondary
CLAMP2	E6	O	
CM_ILIM	G3	I	Enables or disables communication current limit; can be pulled high or low to disable or enable communication current limit
FOD	F2	I	Input that is used for scaling the received power message
ILIM	G2	I/O	Output current or overcurrent level programming pin

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Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
$\overline{\text{LPRB 1}}$	F5	O	Open drain – active to help drive RECT voltage high at light load on a PMA TX
$\overline{\text{LPRB 2}}$	G6		
OUT	D1, D2, D3, D4, D5, D6	O	Output pin, used to deliver power to the load
$\overline{\text{PD_DET}}$	G6	O	Open drain output that allows user to sense when receiver is on transmitter
PGND	A1, A2, A3, A4, A5, A6	—	Power and logic ground
RECT	C2, C3, C4, C5	O	Filter capacitor for the internal synchronous rectifier
SCL	E4	I	SCL and SDA are used for I^2C communication
SDA	F4	I	
TERM, LPRBEN	F3	I	Sets termination current as a percentage of I_{ILIM} as TERM pin. When TERM resistor is populated, LPRB pins are enabled with appropriate function
TMEM	G5	O	TMEM allows capacitor to be connected to GND so energy from transmitter ping can be stored to retain memory of state
TS/CTRL	G4	I	Temperature sense. Can be pulled high to send end power transfer (EPT) or end of charge (EOC) to TX
VIREG	E5	I	Rectifier voltage feedback
VO_REG	G1	I	Sets the regulation voltage for output
$\overline{\text{WPG}}$	F5	O	Open-drain output that allows user to sense when power is transferred to load

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Input voltage	AC1, AC2	–0.8	20	V
	RECT, COMM1, COMM2, OUT, $\overline{\text{LPRB1}}$, $\overline{\text{LPRB2}}$, CLAMP1, CLAMP2, $\overline{\text{WPG}}$, $\overline{\text{PD_DET}}$	–0.3	20	
	AD, $\overline{\text{AD-EN}}$	–0.3	30	
	BOOT1, BOOT2	–0.3	20	
	SCL, SDA, TERM, CM_ILIM, FOD, TS/CTRL, ILIM, TMEM, VIREG, VO_REG, LPRBEN	–0.3	7	
Input current	AC1, AC2 (RMS)	2.5		A
Output current	OUT	1.5		A
Output sink current	$\overline{\text{LPRB1}}$, $\overline{\text{LPRB2}}$	15		mA
Output sink current	COMM1, COMM2	1		A
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) All voltages are with respect to the PGND pin, unless otherwise noted.
(2) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (2), 100 pF, 1.5 kΩ	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (3)	±500	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{RECT}	RECT voltage range	4	10	V
I_{OUT}	Output current		1	A
I_{AD-EN}	Sink current		1	mA
I_{COMM}	COMMx sink current		500	mA
T_J	Junction temperature	0	125	ºC

7.4 Thermal Information

THERMAL METRIC (1)		bq51222 YFP (DSBGA) 42 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	49.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance (3)	0.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance (4)	6.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter (5)	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter (6)	6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance (7)	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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7.5 Electrical Characteristics

$I_{LOAD} = I_{OUT}$, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVLO}	Undervoltage lockout	V_{RECT}: 0 to 3 V		2.8	2.9	V
$V_{HYS-UVLO}$	Hysteresis on UVLO	V_{RECT}: 3 to 2 V		393		mV
$V_{RECT-OVP}$	Input overvoltage threshold	V_{RECT}: 5 to 16 V	14.6	15.1	15.6	V
$V_{HYS-OVP}$	Hysteresis on OVP	V_{RECT}: 16 to 5 V		1.5		V
$V_{RECT(REG)}$	Voltage at RECT pin set by communication with primary		V_{OUT} + 0.12		V_{OUT} + 2	V
$V_{RECT(TRACK)}$	V_{RECT} regulation above V_{OUT}	V_{ILIM} = 1.2 V		140		mV
$I_{LOAD-HYS}$	I_{LOAD} hysteresis for dynamic V_{RECT} thresholds as a % of I_{ILIM}	I_{LOAD} falling		4%		
$V_{RECT-DPM}$	Rectifier under voltage protection, restricts I_{OUT} at $V_{RECT-DPM}$		3	3.1	3.2	V
$V_{RECT-REV}$	Rectifier reverse voltage protection with a supply at the output	$V_{RECT-REV} = V_{OUT} – V_{RECT}$, V_{OUT} = 10 V		8.8	9.2	V
$I_{\overline{LPRB1}-dis}$	Current at which $\overline{LPRB1}$ is disabled	I_{OUT} 0 to 200 mA		125		mA
$I_{\overline{LPRB2}-dis}$	Current at which $\overline{LPRB2}$ is disabled	I_{OUT} 0 to 400 mA		322		mA
QUIESCENT CURRENT						
$I_{OUT(standby)}$	Quiescent current at the output when wireless power is disabled	$V_{OUT} \le 5$ V, 0°C ≤ T_J ≤ 85°C		20	35	µA
ILIM SHORT CIRCUIT						
$R_{ILIM-SHORT}$	Highest value of R_{ILIM} resistor considered a fault (short). Monitored for I_{OUT} > 100 mA	R_{ILIM}: 200 to 50 Ω. I_{OUT} latches off, cycle power to reset		215	230	Ω
$t_{DGL-Short}$	Deglitch time transition from ILIM short to I_{OUT} disable			1		ms
I_{LIM_SC}	$I_{LIM-SHORT,OK}$ enables the ILIM short comparator when I_{OUT} is greater than this value	I_{LOAD}: 0 to 200 mA	110	125	140	mA
$I_{LIM-SHORT,OK\ HYSTERESIS}$	Hysteresis for $I_{LIM-SHORT,OK}$ comparator	I_{LOAD}: 200 to 0 mA		20		mA
I_{OUT-CL}	Maximum output current limit	Maximum I_{LOAD} that can be delivered for 1 ms when ILIM is shorted		3.7		A
OUTPUT						
V_{O_REG}	Feedback voltage set point	I_{LOAD} = 1000 mA	0.495	0.5013	0.5075	V
		I_{LOAD} = 1 mA	0.4951	0.5014	0.5076	
K_{ILIM}	Current programming factor for hardware short circuit protection	$R_{ILIM} = K_{ILIM} / I_{ILIM}$, where I_{ILIM} is the hardware current limit I_{OUT} = 850 mA		842		AΩ
I_{OUT_RANGE}	Current limit programming range				1500	mA
I_{COMM}	Output current limit during communication	$I_{OUT} \ge 400$ mA		I_{OUT} – 50		mA
		100 mA ≤ I_{OUT} < 400 mA		I_{OUT} + 50		
		I_{OUT} < 100 mA		None		
$t_{HOLD-OFF}$	Hold off time for the communication current limit during startup			1		s

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Electrical Characteristics (continued)

I_{LOAD} = I_{OUT}, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TS/CTRL						
$V_{TS-Bias}$	TS bias voltage (internal)	$I_{TS-Bias}$ < 100 µA and communication is active (periodically driven, see $t_{TS/CTRL-Meas}$)		1.8		V
$V_{CTRL-HI}$	CTRL pin threshold for a high	$V_{TS/CTRL}$: 50 to 150 mV	90	105	120	mV
$T_{TS/CTRL-Meas}$	Time period of TS/CTRL measurements, when TS is being driven	TS bias voltage is only driven when power packets are sent			1700	ms
V_{TS-HOT}	Voltage at TS pin when device shuts down			0.38		V
THERMAL PROTECTION						
$T_{J(OFF)}$	Thermal shutdown temperature			155		°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			20		°C
OUTPUT LOGIC LEVELS ON $\overline{WPG}$						
V_{OL}	Open drain $\overline{WPG}$ pin	I_{SINK} = 5 mA			550	mV
$I_{OFF,STAT}$	$\overline{WPG}$ leakage current when disabled	V_{WPG} = 20 V			1	µA
COMM PIN						
$R_{DS-ON(COMM)}$	COMM1 and COMM2	V_{RECT} = 2.6 V		1		Ω
f_{COMM}	Signaling frequency on COMMx pin for WPC			2.00		Kb/s
$I_{OFF,COMM}$	COMMx pin leakage current	V_{COMM1} = 20 V, V_{COMM2} = 20 V			1	µA
CLAMP PIN						
$R_{DS-ON(CLAMP)}$	CLAMP1 and CLAMP2			0.5		Ω
ADAPTER ENABLE						
V_{AD-EN}	V_{AD} rising threshold voltage	V_{AD} 0 V to 5 V	3.5	3.6	3.8	V
$V_{AD-EN-HYS}$	V_{AD-EN} hysteresis	V_{AD} 5 V to 0 V		450		mV
I_{AD}	Input leakage current	V_{RECT} = 0 V, V_{AD} = 5 V			50	µA
R_{AD_EN-OUT}	Pullup resistance from $\overline{AD-EN}$ to OUT when adapter mode is disabled and V_{OUT} > V_{AD}	V_{AD} = 0 V, V_{OUT} = 5 V		230	350	Ω
V_{AD_EN-ON}	Voltage difference between V_{AD} and V_{AD-EN} when adapter mode is enabled	V_{AD} = 5 V, 0°C ≤ T_J ≤ 85°C	4	4.5	5	V
		V_{AD} = 9 V, 0°C ≤ T_J ≤ 85°C	3	6	7	V
SYNCHRONOUS RECTIFIER						
$I_{SYNC-EN}$	I_{OUT} at which the synchronous rectifier enters half synchronous mode	I_{OUT}: 200 mA to 0 mA		100		mA
$I_{SYNC-EN-HYST}$	Hysteresis for $I_{OUT,RECT-EN}$ (full-synchronous mode enabled)	I_{OUT} 0 mA to 200 mA		40		mA
$V_{HS-DIODE}$	High-side diode drop when the rectifier is in half synchronous mode	$I_{AC-VRECT}$ = 250 mA, and T_J = 25°C		0.7		V
I^2C						
V_{IL}	Input low threshold level SDA	V(PULLUP) = 1.8 V, SDA			0.4	V
V_{IH}	Input high threshold level SDA	V(PULLUP) = 1.8 V, SDA	1.4			V
V_{IL}	Input low threshold level SCL	V(PULLUP) = 1.8 V, SCL			0.4	V
V_{IH}	Input high threshold level SCL	V(PULLUP) = 1.8 V, SCL	1.4			V
I^2C speed		Typical		100		kHz

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7.6 Typical Characteristics

Temperature = 25°C (unless otherwise noted)

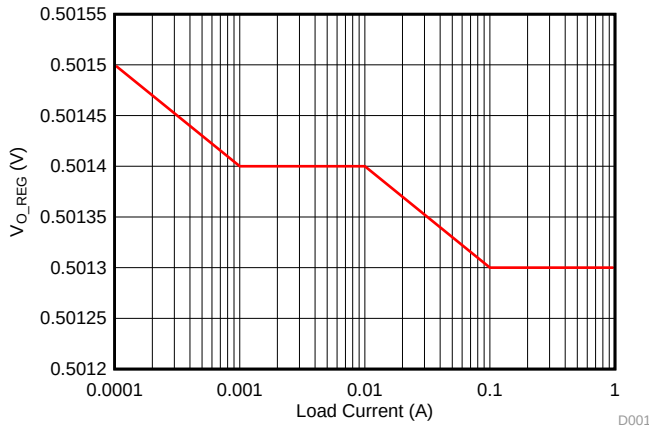


Figure 1. Output Voltage Feedback as a Function of Load

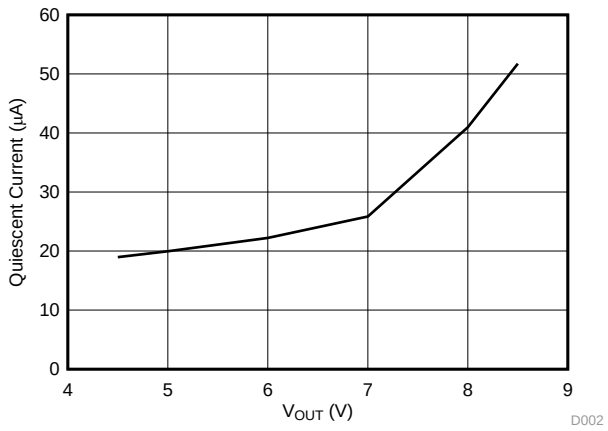


Figure 2. Quiescent Current as a Function of Output Voltage

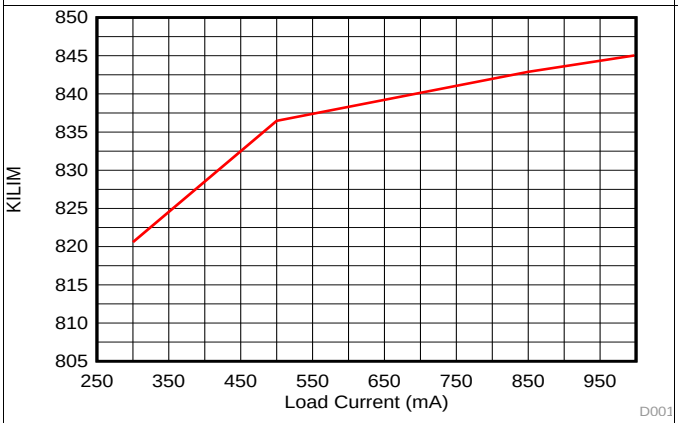


Figure 3. K_{ILIM} as a Function of Load Current

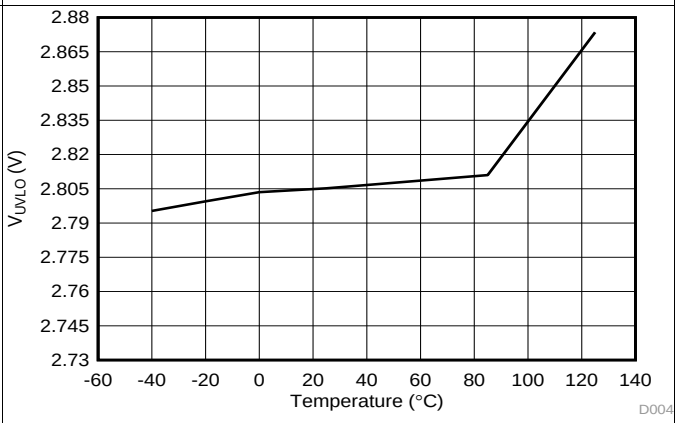
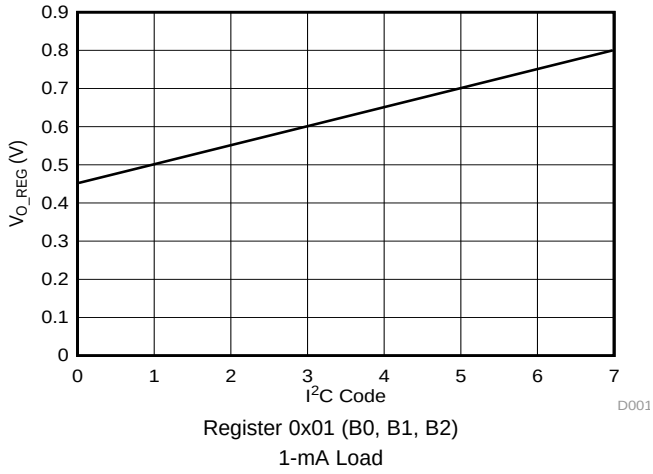
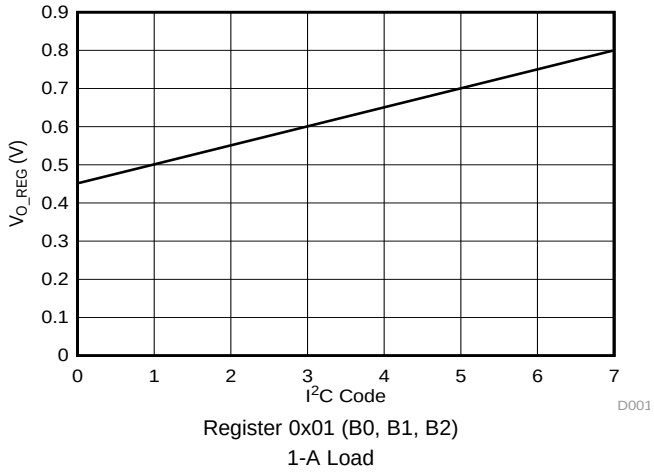


Figure 4. V_{UVLO} as a Function of Junction Temperature



Register 0x01 (B0, B1, B2)
1-mA Load

Figure 5. Register 0x01 control of V_{O_REG}



Register 0x01 (B0, B1, B2)
1-A Load

Figure 6. Register 0x01 control of V_{O_REG}

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8 Detailed Description

8.1 Overview

Both WPC and PMA wireless power systems consist of a charging pad (primary, transmitter) and the secondary-side equipment (receiver). There are coils in the charging pad and secondary equipment, which magnetically couple to each other when the receiver is placed on the transmitter. Power is transferred from the primary to the secondary by transformer action between the coils. The receiver can achieve control over the amount of power transferred by getting the transmitter to change the field strength by changing the frequency, or duty cycle, or voltage rail energizing the primary coil.

The receiver equipment communicates with the primary by modulating the load seen by the primary. This load modulation results in a change in the primary coil current or primary coil voltage, or both, which is measured and demodulated by the transmitter.

In WPC, the system communication is digital — packets that are transferred from the secondary to the primary. Differential bi-phase encoding is used for the packets. The bit rate is 2 kb/s. Various types of communication packets are defined. These include identification and authentication packets, error packets, control packets, power usage packets, and end power transfer packets, among others.

An PMA-compliant receiver communicates based on continuous transmission of signals from the receiver to the transmitter. The PMA specification defines six different communications symbols. These are increment (INC), decrement (DEC), no change (NoCh), end of charge (EOC), MsgBit, and a symbol for future use. Each PMA receiver has a unique PMA RXID, which is a 6-byte unique message that is sent to the PMA TX at startup.

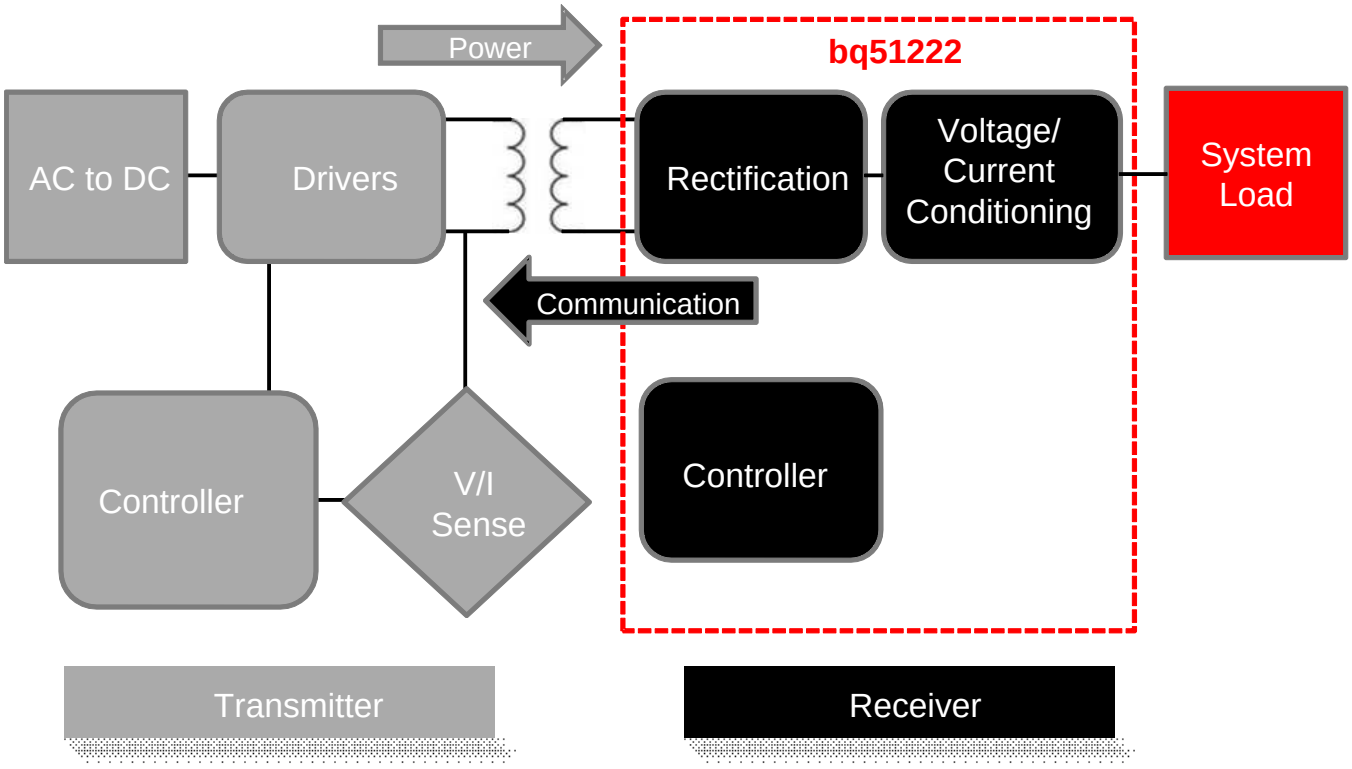


Figure 7. Dual Mode Wireless Power System Indicating the Functional Integration of the bq51222 Family

The bq51222 device integrates fully-compliant WPC v1.2 and PMA communication protocols in order to streamline the dual mode receiver designs (no extra software development required). Other unique algorithms such as *Dynamic Rectifier Control* are integrated to provide best-in-class system efficiency while keeping the smallest solution size of the industry.

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Overview (continued)

As a WPC system, when the receiver shown in Figure 7 is placed on the charging pad, the secondary coil couples to the magnetic flux generated by the coil in the transmitter, which consequently induces a voltage in the secondary coil. The internal synchronous rectifier feeds this voltage to the RECT pin, which in turn feeds the LDO which feeds the output.

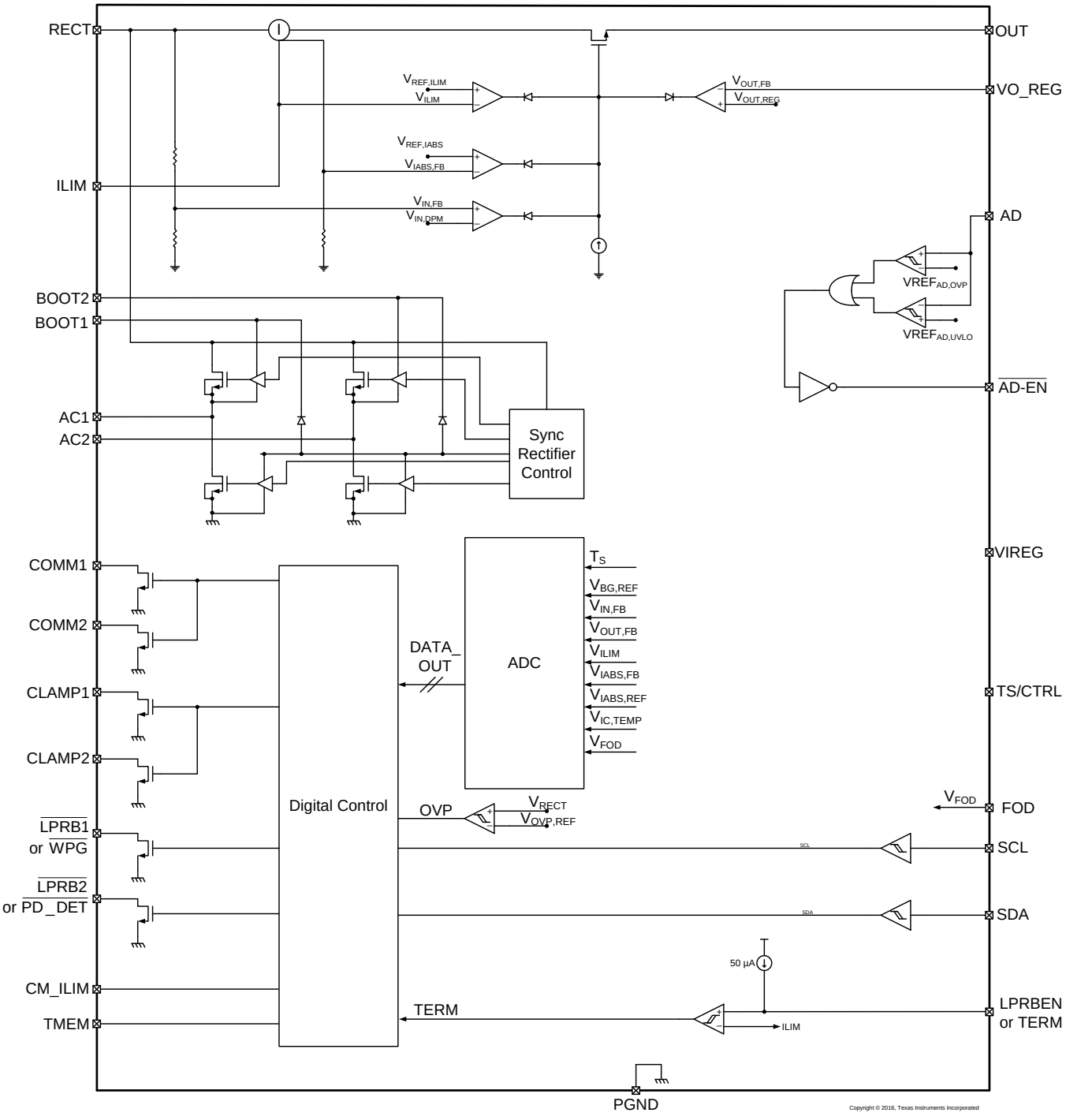
The bq51222 device identifies and authenticates itself to the primary using the COMMx pins, switching on and off the COMM FETs, and hence switching in and out COMM capacitors. If the authentication is successful, the primary remains powered-up. The bq51222 device measures the voltage at the RECT pin, calculates the difference between the actual voltage and the desired voltage $V_{RECT(REG)}$, and sends back error packets to the transmitter. This process goes on until the input voltage settles at $V_{RECT(REG)\ MAX}$. During a load change, the dynamic rectifier algorithm sets the targets specified by targets between $V_{RECT(REG)\ MAX}$ and $V_{RECT(REG)\ MIN}$ shown in Table 1. This algorithm enhances the transient response of the power supply.

After the voltage at the RECT pin is at the desired value, a pass FET is enabled. The voltage control loop ensures that the output voltage is maintained at $V_{OUT(REG)}$, powering the downstream charger. The bq51222 device meanwhile continues to monitor the input voltage, and keeps sending control error packets (CEP) to the primary on average every 250 ms. If a large transient occurs, the feedback to the primary speeds up to 32-ms communication periods to converge on an operating point in less time.

If the receiver shown in Figure 7 is used with a PMA transmitter, the bq51222 device identifies itself to the PMA transmitter using the COMMx pins. If sufficient power is delivered to the bq51222 device to wake up the device, it responds by modulating the power signal according to the PMA communication protocol. Prior to enabling the output, the bq51222 device transmits an RXID message. This is a unique identification message that is controlled through an IEEE sanctioned database and every bq51222 device comes programmed with its own unique RXID that can be read back using I^2C. See I^2C register map in *Register Maps* for details on the location of the RXID. The bq51222 device then monitors the voltage at the RECT pin. If there is a difference between the actual voltage and the desired voltage $V_{RECT(REG)}$, the device sends a PMA DEC or PMA INC signal to the PMA transmitter to control the RECT voltage to be within the desired window. The receiver regulates V_{RECT} to a desired window of operation shown in Figure 15.

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8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Dynamic Rectifier Control

WPC Mode Only

The *Dynamic Rectifier Control* algorithm offers the end system designer optimal transient response for a given maximum output current setting. This is achieved by providing enough voltage headroom across the internal regulator (LDO) at light loads in order to maintain regulation during a load transient. The WPC system has a relatively slow global feedback loop where it can take up to 150 ms to converge on a new rectifier voltage target. Therefore, a transient response is dependent on the loosely coupled transformer's output impedance profile. The Dynamic Rectifier Control allows for a 1.5-V change in rectified voltage before the transient response is observed at the output of the internal regulator (output of the bq51222 device). A 1-A application allows up to a 2-Ω output impedance. The *Dynamic Rectifier Control* behavior is illustrated in Figure 13 where R_{ILIM} is set to 680 Ω.

8.3.2 Dynamic Power Scaling

WPC Mode Only

The *Dynamic Power Scaling* feature allows for the loss characteristics of the bq51222 device to be scaled based on the maximum expected output power in the end application. This effectively optimizes the efficiency for each application. This feature is achieved by scaling the loss of the internal LDO based on a percentage of the maximum output current. Note that the maximum output current is set by the K_{ILIM} term and the R_{ILIM} resistance (where $R_{ILIM} = K_{ILIM} / I_{ILIM}$). The flow diagram in Figure 13 shows how the rectifier is dynamically controlled (*Dynamic Rectifier Control*) based on a fixed percentage of the I_{ILIM} setting. Table 1 summarizes how the rectifier behavior is dynamically adjusted based on two different R_{ILIM} settings. The table is shown for I_{MAX}, which is typically lower than I_{ILIM} (about 20% lower). See *RILIM Calculations* for more details.

Table 1. Dynamic Rectifier Regulation

OUTPUT CURRENT PERCENTAGE	R_{ILIM} = 1400 Ω I_{MAX} = 0.5 A	R_{ILIM} = 700 Ω I_{MAX} = 1.0 A	VRECT
0 to 10%	0 to 0.05 A	0 to 0.1 A	V_{OUT} + 2
10 to 20%	0.05 to 0.1 A	0.1 to 0.2 A	V_{OUT} + 1.68
20 to 40%	0.1 to 0.2 A	0.2 to 0.4 A	V_{OUT} + 0.56
>40%	>0.2 A	>0.4 A	V_{OUT} + 0.12

Dynamic Rectifier Control shows the shift in the dynamic rectifier control behavior based on the two different R_{ILIM} settings. With the rectifier voltage (V_{RECT}) being the input to the internal LDO, this adjustment in the *Dynamic Rectifier Control* thresholds dynamically adjusts the power dissipation across the LDO where:

$$P_{DIS} = (V_{RECT} - V_{OUT}) \cdot I_{OUT} \quad (1)$$

Figure 40 shows how the system efficiency is improved due to the *Dynamic Power Scaling* feature. Note that this feature balances efficiency with optimal system transient response.

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8.3.3 VO_REG and VIREG Calculations

WPC and PMA Modes

The bq51222 device allows the designer to set the output voltage by setting a feedback resistor divider network from the OUT pin to the VO_REG pin as seen in Figure 8. The resistor divider network should be chosen so that the voltage at the VO_REG pin is 0.5 V at the desired output voltage. This applies to the default I^2C code for VO_REG shown in I^2C register 0x01 shown in Table 5 (Bits B0, B1, B2).

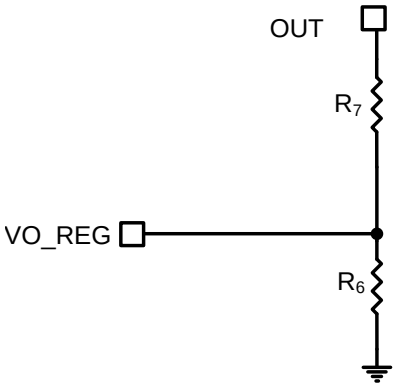


Figure 8. VO_REG Network

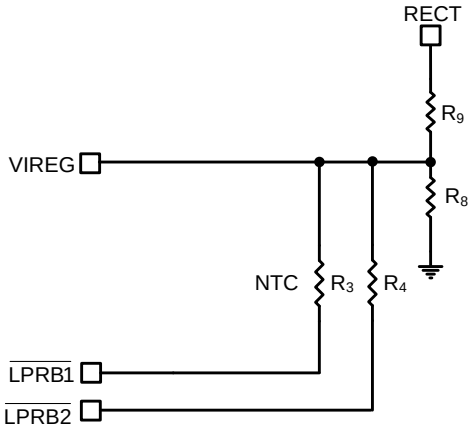


Figure 9. VIREG Network (For PMA)

Choose the desired output voltage V_{OUT} and R_6:

$$K_{VO} = \frac{0.5\ V}{V_{OUT}} \quad (2)$$

$$R_6 = \frac{K_{VO} \times R_7}{1 - K_{VO}} \quad (3)$$

After R_6 and R_7 are chosen, the same divider network is attached to VIREG pin from RECT to GND, as shown in Figure 9. $R_9 = R_7$ and $R_8 = R_6$.

$\overline{\text{LPRB1}}$ and $\overline{\text{LPRB2}}$ are two additional pins that are used to implement a back cover solution and are used for PMA (see Figure 55). In a back cover solution where the system designer cannot depend on the characteristics of the downstream charger in the phone, these pins can be used to boost the rectifier at a lower power (Low Power Rectifier Boost), so that the system is able to survive a load transient from 0 mA to the maximum current by boosting the rectifier during low power output that the system is designed for. See resistor calculations for $\overline{\text{LPRB1}}$ and $\overline{\text{LPRB2}}$: in the bq51222 web page "Tools & software" tab. The Excel file not only provides how to calculate the LPRB resistor values but also assists with other calculations. The Excel file can be accessed at www.ti.com/product/bq51222/toolssoftware.

Table 2. LPRB Condition Table

I_{OUT}	$\overline{\text{LPRB1}}$	$\overline{\text{LPRB2}}$
0 mA < I_{OUT} < 100 mA	ON	ON
100 mA < I_{OUT} < 350 mA	OFF	ON
350 mA < I_{OUT} < Maximum current	OFF	OFF

The $\overline{\text{LPRB1}}$ and $\overline{\text{LPRB2}}$ resistors can be omitted in an embedded solution where the system designer is in control of the voltage at which the downstream charger can regulate the input current to prevent the input from collapsing in a load transient (VIN-DPM). The functionality of $\overline{\text{LPRB1}}$ and $\overline{\text{LPRB2}}$ can be reverted to $\overline{\text{WPG}}$ and $\overline{\text{PD_DET}}$ by not populating the TERM resistor. In this case, the host enables the charge complete on the TS/CTRL pin by pulling this pin high.

For the back cover solution, the TERM resistor is populated and this enables $\overline{\text{LPRB1}}$ and $\overline{\text{LPRB2}}$ functionality. The functionality can be seen in Table 2.

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8.3.4 RILIM Calculations

WPC and PMA Modes

The bq51222 device includes a means of providing hardware overcurrent protection (I_{ILIM}) through an analog current regulation loop. The hardware current limit provides an extra level of safety by clamping the maximum allowable output current (for example, current compliance). The R_{ILIM} resistor size also sets the thresholds for the dynamic rectifier levels providing efficiency tuning per each application's maximum system current. The calculation for the total R_{ILIM} resistance is as follows:

$$R_{ILIM} = K_{ILIM} / I_{ILIM} \quad (4)$$

$$R_1 = R_{ILIM} – R_{FOD} \quad (5)$$

R_{ILIM} allows for the ILIM pin to reach 1.2 V at an output current equal to I_{ILIM}. When choosing R_{ILIM}, two options are possible.

If the user's application requires an output current equal to or greater than the external I_{ILIM} that the circuit is designed for (input current limit on the charger where the receiver device is tied higher than the external I_{ILIM}), ensure that the downstream charger is capable of regulating the voltage of the input into which the receiver device output is tied to by lowering the amount of current being drawn. This ensures that the receiver output does not drop to 0 V. Such behavior is referred to as Dynamic Power Management (VIN-DPM) in TI chargers. Unless such behavior is enabled on the charger, the charger will pull the output of the receiver device to ground when the receiver device enters current regulation. If the user's applications are designed to extract less than the I_{ILIM} (1-A maximum), typical designs should leave a design margin of at least 10%, so that the voltage at ILIM pin reaches 1.2 V when 10% more than maximum current is drawn from the output. Such a design would have input current limit on the charger lower than the external ILIM of the receiver device. In both cases however, the charger must be capable of regulating the current drawn from the device to allow the output voltage to stay at a reasonable value. This same behavior is also necessary during the WPC communication. The following calculations show how such a design is achieved:

$$R_{ILIM} = K_{ILIM} / (1.1 \times I_{ILIM}) \quad (6)$$

$$R_1 = R_{ILIM} – R_{FOD} \quad (7)$$

where I_{LIM} is the hardware current limit.

When referring to the application diagram shown in *Typical Applications*, R_{ILIM} is the sum of the R_1 and R_{FOD} resistance (that is, the total resistance from the ILIM pin to GND). R_{FOD} is chosen according to the application. The tool for calculating R_{FOD} can be obtained by contacting your TI representative. Use R_{FOD} to allow the receiver implementation to comply with WPC v1.2 requirements related to received power accuracy.

8.3.5 Adapter Enable Functionality

WPC and PMA Modes

The bq51222 device can also help manage the multiplexing of adapter power to the output and can shut off the TX when the adapter is plugged in and is above the V_{AD-EN}. After the adapter is plugged in and the output turns off, the RX device sends an EOC to the TX. In this case, the $\overline{AD_EN}$ pins are then pulled to approximately 4 V below AD, which allows the device turn on the back-to-back PMOS connected between AD and OUT (Figure 54).

Both the AD and $\overline{AD\text{-}EN}$ pins are rated at 30 V, while the OUT pin is rated at 20 V. It must also be noted that it is required to connect a back-to-back PMOS between AD and OUT so that voltage is blocked in both directions. Also, when AD mode is enabled, no load can be pulled from the RECT pin as this could cause an internal device overvoltage in the bq51222 device.

8.3.6 Turning Off the Transmitter

WPC and PMA Modes

Both specifications allow the receiver to turn off the transmitter and put the system in a low-power standby mode. There are two different ways to accomplish this with the bq51222 device. In both modes, the EPT charge complete (WPC) or end of charge (PMA) can be sent to the TX by pulling the TS pin high (above 1.4 V). The bq51222 device will then sense this and send the appropriate signal to the TX, thus putting the TX in a low power standby mode.

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8.3.6.1 WPC End Power Transfer (EPT)

The WPC allows for a special command to terminate power transfer from the TX termed EPT packet. The v1.2 specifies the following reasons and their responding data field value in Table 3.

Table 3. End Power Transfer Codes in WPC

REASON	VALUE	CONDITION(1)
Unknown	0x00	AD > 3.6 V
Charge Complete	0x01	TS/CTRL = 1
Internal Fault	0x02	T_J > 150°C or R_{ILIM} < 215 Ω
Over Temperature	0x03	TS < V_{TS-HOT}, or TS/CTRL < 100 mV(2)
Over Voltage	0x04	V_{RECT} target does not converge(3)
Over Current	0x05	Not sent
Battery Failure	0x06	Not sent
Reconfigure	0x07	Not sent
No Response	0x08	Not sent

(1) The *Condition* column corresponds to the case where the bq51222 device will send the WPC EPT command.
(2) The TS < V_{TS-HOT} condition refers to using an external thermistor for temperature control. The TS/CTRL < 100 mV condition refers to driving the TS/CTRL pin from an external GPIO.
(3) If the voltage on the RECT pin does not reach the required value (typically 8 V) within 64 error packets during startup (weak coil coupling), the receiver sends EPT-OV and the transmitter will shut off.

8.3.6.2 PMA EOC

PMA EOC is a state where the bq51222 device disables the output and sends EOC frequency to terminate the power transfer on a PMA transmitter. This can be done by setting the TERM pin resistor so that the voltage on the TERM pin is higher than the ILIM pin at the desired termination current. This TERM resistor method of sending the EOC to the transmitter only works with PMA TX. After the TERM resistor is populated, it also changes the behavior of the LPRBx pins. Check the section on LPRBx resistors for more information. Another way to send an EOC to the PMA TX is to pull the TS pin above 1.4 V through an external pullup.

8.3.7 CM_ILIM

WPC Mode Only

Communication current limit is a feature that allows for error free communication to happen between the RX and TX in the WPC mode. This is done by decoupling the coil from the load transients by limiting the output current during communication with the TX. The communication current limit is set according to Table 4. The communication current limit can be disabled by pulling CM_ILIM pin high (> 1.4 V) or enabled by pulling the CM_ILIM pin low. There is an internal pulldown that enables communication current limit when the CM_ILIM pin is left floating.

Table 4. Communication Current Limit Table

I_{OUT}	COMMUNICATION CURRENT LIMIT
0 mA < I_{OUT} < 100 mA	None
100 mA < I_{OUT} < 400 mA	I_{OUT} + 50 mA
400 mA < I_{OUT} < Max current	I_{OUT} – 50 mA

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When the communication current limit is enabled, the amount of current that the load can draw is limited. If the charger in the system does not have a VIN-DPM feature, the output of the receiver will collapse if communication current limit is enabled. In order to disable Communication Current Limit, pull CM_ILIM pin high.

8.3.8 $\overline{\text{PD_DET}}$ and TMEM

$\overline{\text{PD_DET}}$ is only available in WPC mode. This is an open-drain pin that goes low based on the voltage of the TMEM pin. When the voltage of TMEM is higher than 1.6 V, $\overline{\text{PD_DET}}$ will be low. The voltage on the TMEM pin depends on capturing the energy from the digital ping from the transmitter and storing it on the C_5 capacitor in Figure 10. After the receiver sends an EPT (charge complete), the transmitter shuts down and goes into a low-power mode. However, it will continue to check if the receiver would like to renegotiate a power transfer by periodically performing the digital ping. The energy from the digital ping can be stored on the TMEM pin until the next digital ping refreshes the capacitor. A bleedoff resistor R_{MEM} can be chosen in parallel with C_5 that sets the time constant so that the TMEM pin will fall below 1.6 V once the next ping timer expires. The duration between digital pings is indeterminate and depends on each transmitter manufacturer.

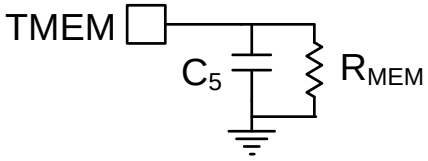


Figure 10. TMEM Configuration

Set capacitor on C_5 = TMEM to 2.2 µF. Resistor R_{MEM} across C_5 can be set by understanding the duration between digital pings (t_{ping}). Set the resistor such that:

$$R_{MEM} = \frac{t_{ping}}{C_5} \tag{8}$$

8.3.9 TS, Both WPC and PMA

The bq51222 device includes a ratio metric external temperature sense function. The temperature sense function has a low ratio metric threshold which represents a hot condition. TI recommends an external temperature sensor in order to provide safe operating conditions for the receiver product. This pin is best used for monitoring the surface that can be exposed to the end user (for example, place the negative temperature coefficient (NTC) resistor closest to the user touch point on the back cover). A resistor in series or parallel can be inserted to adjust the NTC to match the trip point of the device. The implementation in Figure 11 shows the series-parallel resistor implementation for setting the threshold at which V_{TS-HOT} is reached. Once V_{TS-HOT} is reached, the device will send an EPT – overtemperature signal for a WPC transmitter or an EOC signal to a transmitter depending on the mode the device is operating in. An Excel tool to assist with defining the correct resistor values is available on the bq51222 web folder under 'Tools & Software'. The Excel file can be found at www.ti.com/product/bq5122PMA2/toolssoftware.

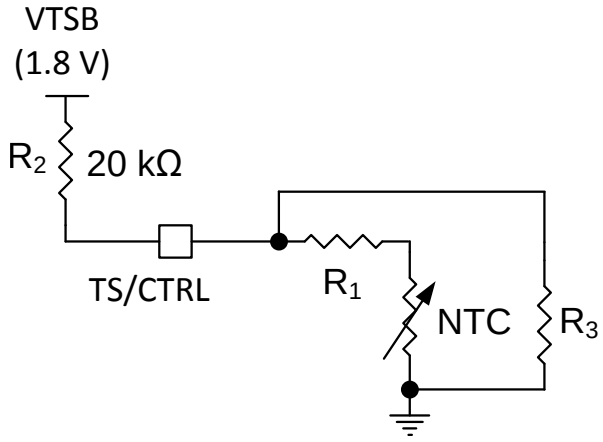


Figure 11. NTC Resistor Setup

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Figure 11 shows a parallel resistor setup that can be used to adjust the trip point of V_{TS-HOT}. After the NTC is chosen and R_{NTCHOT} at V_{TS-HOT} is determined from the data sheet of the NTC, Equation 9 can be used to calculate R_1 and R_3. In many cases depending on the NTC resistor, R_1 or R_3 can be omitted. When calculating V_{TS-HOT}, omit R_1 by setting it to 0 Ω, and omit R_3 by setting it to 10 MΩ.

$$V_{TS-HOT} = 1.8\ V \times \frac{\frac{(R_{NTCHOT} + R_1) \times R_3}{(R_{NTCHOT} + R_1) + R_3}}{\frac{(R_{NTCHOT} + R_1) \times R_3}{((R_{NTCHOT} + R_1) + R_3)} + R_2} \quad (9)$$

8.3.10 I²C Communication

WPC and PMA Modes

The bq51222 device allows for I²C communication with the internal CPU. In case the I²C is not used, ground SCL and SDA. See *Register Maps* for more information.

8.3.11 Input Overvoltage

WPC and PMA Modes

If the input voltage suddenly increases in potential for some condition (for example a change in position of the equipment on the charging pad), the voltage-control loop inside the bq51222 device becomes active, and prevents the output from going beyond $V_{OUT(REG)}$. The receiver then starts sending back error packets every 30 ms until the input voltage comes back to an acceptable level, and then maintains the error communication every 250 ms.

If the input voltage increases in potential beyond $V_{RECT-OVP}$, the device switches off the LDO and informs the primary to bring the voltage back to $V_{RECT(REG)}$. In addition, a proprietary voltage protection circuit is activated by means of C_{CLAMP1} and C_{CLAMP2} that protects the device from voltages beyond the maximum rating of the device.

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8.4 Device Functional Modes

In WPC mode, at startup operation, the bq51222 device must comply with proper handshaking in order to be granted a power contract from the WPC transmitter. The transmitter initiates the handshake by providing an extended digital ping after analog ping detects an object on the transmitter surface. If a receiver is present on the transmitter surface, the receiver then provides the signal strength, configuration, and identification packets to the transmitter (see volume 1 of the WPC specification for details on each packet). These are the first three packets sent to the transmitter. The only exception is if there is a true shutdown condition on the AD, or TS/CTRL pins where the receiver shuts down the transmitter immediately. See Table 3 for details. After the transmitter has successfully received the signal strength, configuration, and identification packets, the receiver is granted a power contract and is then allowed to control the operating point of the power transfer. With the use of the bq51222 device *Dynamic Rectifier Control* algorithm, the receiver will inform the transmitter to adjust the rectifier voltage above 8 V prior to enabling the output supply. This method enhances the transient performance during system startup. For the startup flow diagram details, see Figure 12.

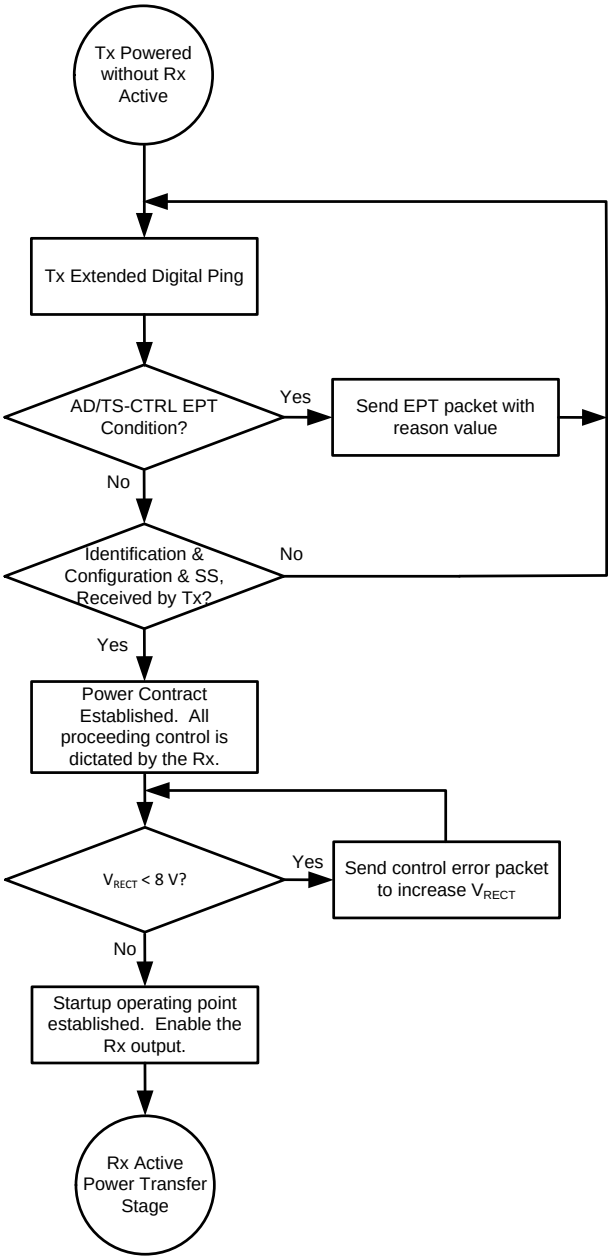


Figure 12. Wireless Power Startup Flow Diagram on WPC TX

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Device Functional Modes (continued)

After the startup procedure has been established, the receiver will enter the active power transfer stage. This is considered the main loop of operation. The *Dynamic Rectifier Control* algorithm determines the rectifier voltage target based on a percentage of the maximum output current level setting (set by K_{ILIM} and the R_{ILIM}). The receiver will send control error packets in order to converge on these targets. As the output current changes, the rectifier voltage target dynamically changes. As a note, the feedback loop of the WPC system is relatively slow, it can take up to 150 ms to converge on a new rectifier voltage target. It should be understood that the instantaneous transient response of the system is open loop and dependent on the receiver coil output impedance at that operating point. The main loop also determines if any conditions in Table 3 are true in order to discontinue power transfer. Figure 13 shows the active power transfer loop.

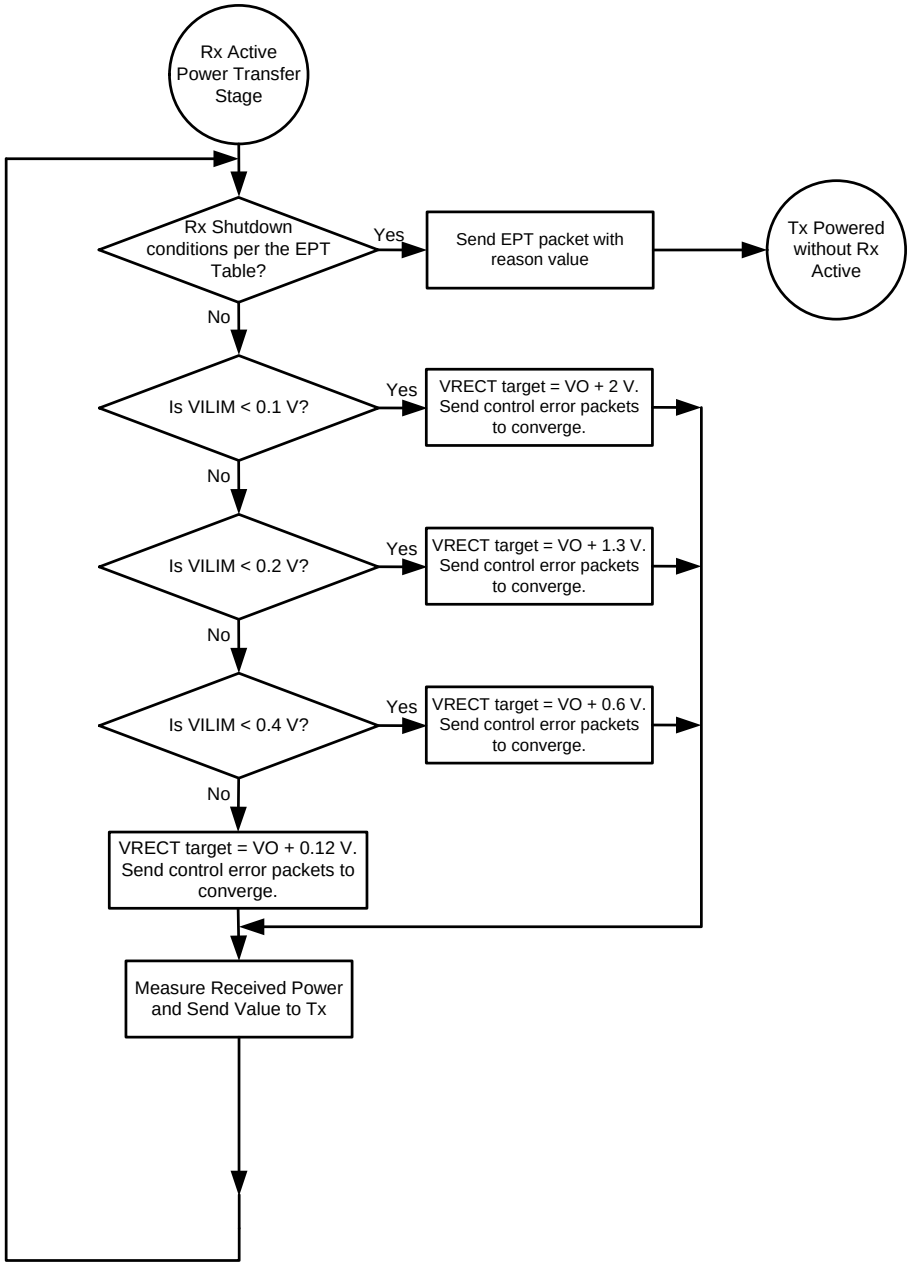


Figure 13. Active Power Transfer Flow Diagram on WPC TX

Device Functional Modes (continued)

In PMA mode, during startup operation, PMA transmitter generates a digital ping in a predefined structure regarding the frequencies and timing. If the power delivered during the digital ping is sufficient to wake up the bq51222 device, it responds by modulating the power signal according to the PMA communication protocol. If the transmitter receives a valid PMA signal from the receiver, it continues to the identification phase, without removing the power signal. The receiver continues to send PMA DEC or PMA INC signals until target V_{RECT} is achieved, and after desired V_{RECT} is achieved, the bq51222 device sends a PMA NoCh signal to indicate that no further change is needed in transmitter frequency. Please note unlike the WPC mode receiver, in PMA mode, the bq51222 device will continue to send the PMA NoCh signal if the target V_{RECT} is within a defined voltage range. This means that the device will regulate the V_{RECT} voltage within an acceptable window. This can be seen in Figure 15.

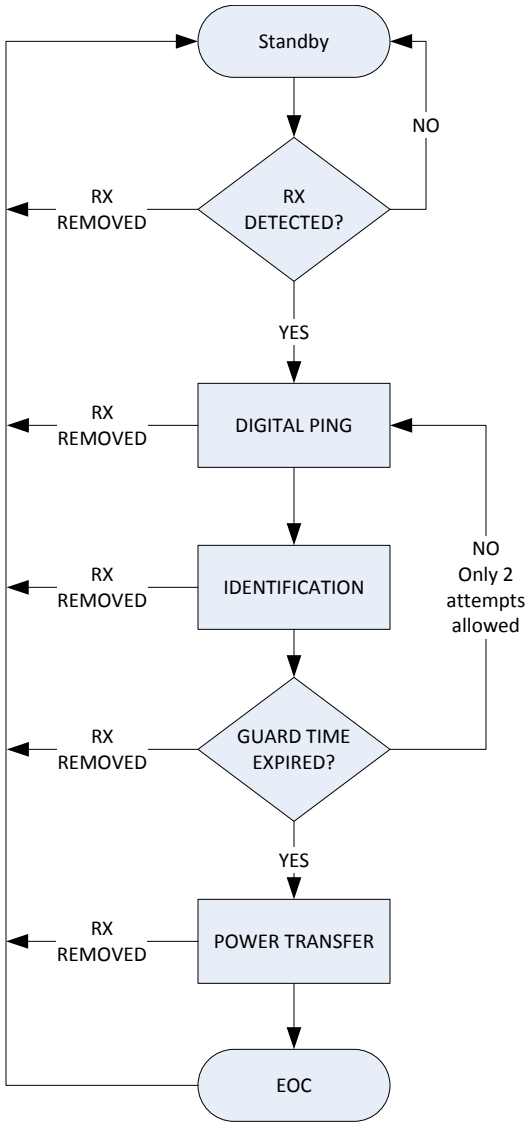


Figure 14. Active Power Transfer Flow Diagram on PMA TX Type 1

Optimized rectification voltage is key to maintaining high efficiency on the bq51222. Figure 15 indicates the control and communication protocol between the receiver and the transmitter. The bq51222 sends an increment signal (INC) for increasing the operating frequency of the transmitter to decrease the transferred power if the rectification voltage is above VREFHI_H. INC signals will occur until the rectification voltage is below VREFHI_L. If the rectification voltage is below VREFLO_L then the bq51222 will send a decrease signal (DEC) to the transmitter which will decrease the frequency resulting in increased power delivery. VREFLO_H is the hysteresis

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Device Functional Modes (continued)

level for terminating the DEC signal. A no change signal (NoCh) is sent when the rectification voltage is between VREFLO_H and VREFHI_L indicating there is no need to increase or decrease the transferred power. Additionally, the Hysteresis zones can be NoCh depending on the direction entered. For example, if the rectification voltage moves through VREFHI_L to enter Hysteresis, the NoCh command is sent. If the same Hysteresis zone is entered through VREFHI_H then the INC will continue to be sent until it reaches VREFHI_L where the NoCh signal will commence. The device will not react to a change in load while the rectification voltage falls within the indicated levels (VREFHI_H > V_{RECT} > VREFLO_L). When a load change occurs sufficient to move V_{RECT} outside this range, the appropriate signal (INC or DEC) will be sent.

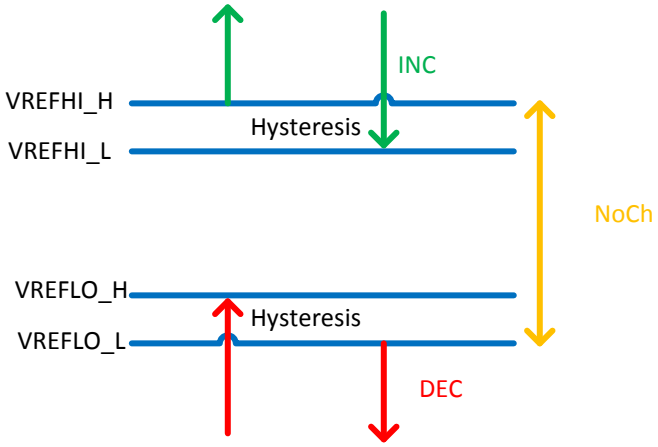


Figure 15. PMA Active Power Control Diagram

8.5 Register Maps

Locations 0x01 and 0x02 can be written to any time. Locations 0xE0 to 0xFF are only functional when V_{RECT} > V_{UVLO}. When V_{RECT} goes below V_{UVLO}, locations 0xE0 to 0xFF are reset.

8.5.1 Wireless Power Supply Current Register 1 (address = 0x01) [reset = 00000001]

Figure 16. Wireless Power Supply Current Register Format

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	V_{OREG2}	V_{OREG1}	V_{OREG0}
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

Table 5. Wireless Power Supply Current Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
B7:B3	Reserved	R/W	00000	Not used
B2	V_{OREG2}	R/W	0	450, 500, 550, 600, 650, 700, 750, or 800 mV Changes V_{O_REG} target
B1	V_{OREG1}	R/W	0	
B0	V_{OREG0}	R/W	1	

8.5.2 Wireless Power Supply Current Register 2 (address = 0x02) [reset = 00000111]

Figure 17. Wireless Power Supply Current Register 2 Format

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	I_{OREG2}	I_{OREG1}	I_{OREG0}
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

Table 6. Wireless Power Supply Current Register 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
B7:B3	Reserved	R/W	00000	Not used
B2	I_{OREG2}	R/W	1	10%, 20%,30%, 40%, 50%, 60%, 90%, and 100% of I_{ILIM} current based on configuration 000, 001, ... 111
B1	I_{OREG1}	R/W	1	
B0	I_{OREG0}	R/W	1	

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8.5.3 I²C Mailbox Register (address = 0xE0) [reset = 10000000]

Figure 18. I²C Mailbox Register Format

7	6	5	4	3	2	1	0
USER_PKT_DONE	USER_PKT_ERR		FOD Mailer	ALIGN Mailer	FOD Scaler	Reserved	Reserved
R	R		R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only

Table 7. I²C Mailbox Register Field Descriptions

Bit	Field	Type	Reset	Description
B7	USER_PKT_DONE	R	1	Set bit to 0 to send proprietary packet with header in 0xE2. CPU checks header to pick relevant payload from 0xF1 to 0xF4 This bit will be set to 1 after the user packet with the header in register 0xE2 is sent.
B6:B5	USER_PKT_ERR	R	00	00 = No error in sending packet 01 = Error: no transmitter present 10 = Illegal header found: packet will not be sent 11 = Error: not defined yet
B4	FOD Mailer	R/W	0	Not used
B3	ALIGN Mailer	R/W	0	Setting this bit to 1 will enable alignment aid mode where the CEP = 0 will be sent until this bit is set to 0 (or CPU reset occurs)
B2	FOD Scaler	R/W	0	Not used,write to 0 if register is written
B1:B0	Reserved	R/W	00	Not used

8.5.4 Wireless Power Supply FOD RAM Register (address = 0xE1) [reset =00000000]

Figure 19. Wireless Power Supply FOD RAM Register Format

7	6	5	4	3	2	1	0
ESR_ENABLE	OFF_ENABLE	Ro_{FOD5}	Ro_{FOD4}	Ro_{FOD3}	Rs_{FOD2}	Rs_{FOD1}	Rs_{FOD0}
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

Table 8. Wireless Power Supply FOD RAM Register Field Descriptions

Bit	Field	Type	Reset	Description(1)	
B7	ESR_ENABLE	R/W	0	Enables I²C based ESR in received power, Enable = 1, Disable = 0	
B6	OFF_ENABLE	R/W	0	Enables I²C based offset power, Enable = 1, Disable = 0	
B5	Ro_{FOD5}	R/W	0	000 – 0 mW 001 – +39 mW 010 – +78 mW 011 – +117 mW 100 – +156 mW	101 – +195 mW 110 – +234 mW 111 – +273 mW The value is added to received power message
B4	Ro_{FOD4}	R/W	0		
B3	Ro_{FOD3}	R/W	0		
B2	Rs_{FOD2}	R/W	0	000 – ESR 001 – ESR 010 – ESR × 2 011 – ESR × 3	100 – ESR x 4 101 – ESR 110 – ESR 111 – ESR x 0.5
B1	Rs_{FOD1}	R/W	0		
B0	Rs_{FOD0}	R/W	0		

(1) A non-zero value will change the I²R calculation resistor and offset in the received power calculation by a factor shown in the table.

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8.5.5 Wireless Power User Header RAM Register (address = 0xE2) [reset = 00000000]

Figure 20. Wireless Power User Header RAM Register Format

7	6	5	4	3	2	1	0
HEADER7	HEADER6	HEADER5	HEADER4	HEADER3	HEADER2	HEADER1	HEADER0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

Table 9. Wireless Power User Header RAM Register Field Descriptions

Bit	Field	Type	Reset	Description(1)
B7:B0	HEADER	R/W	00000000	Proprietary packet 8-bit header

(1) Must write a valid header to enable proprietary package. As soon as mailer (0xE0) is written, payload bytes are sent on the next available communication slot as determined by CPU. Once payload is sent, the mailer (USER_PKT_DONE) is set to 1.

8.5.6 Wireless Power USER V_{RECT} Status RAM Register (address = 0xE3) [reset = 00000000]

This register reads back the V_{RECT} voltage with LSB = 46 mV.

Figure 21. Wireless Power USER V_{RECT} Status RAM Register Format

7	6	5	4	3	2	1	0
V_{RECT7}	V_{RECT6}	V_{RECT5}	V_{RECT4}	V_{RECT3}	V_{RECT2}	V_{RECT1}	V_{RECT0}
R	R	R	R	R	R	R	R

LEGEND: R = Read only

Table 10. Wireless Power USER V_{RECT} Status RAM Register Field Descriptions

Bit	Field	Type	Reset	Description
B7	V_{RECT7}	R	0	V_{RECT} voltage Range – 0 V to 12 V, LSB = 46 mV
B6	V_{RECT6}	R	0	
B5	V_{RECT5}	R	0	
B4	V_{RECT4}	R	0	
B3	V_{RECT3}	R	0	
B2	V_{RECT2}	R	0	
B1	V_{RECT1}	R	0	
B0	V_{RECT0}	R	0	

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8.5.7 Wireless Power VOUT Status RAM Register (address = 0xE4) [reset = 00000000]

This register reads back the V_{OUT} voltage with LSB = 46 mV.

Figure 22. Wireless Power VOUT Status RAM Register Format

7	6	5	4	3	2	1	0
V_{OUT7}	V_{OUT6}	V_{OUT5}	V_{OUT4}	V_{OUT3}	V_{OUT2}	V_{OUT1}	V_{OUT0}
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

Table 11. Wireless Power VOUT Status RAM Register Field Descriptions

Bit	Field	Type	Reset	Description
B7	V_{OUT7}	R/W	0	V_{OUT} voltage LSB = 46 mV
B6	V_{OUT6}	R/W	0	
B5	V_{OUT5}	R/W	0	
B4	V_{OUT4}	R/W	0	
B3	V_{OUT3}	R/W	0	
B2	V_{OUT2}	R/W	0	
B1	V_{OUT1}	R/W	0	
B0	V_{OUT0}	R/W	0	

8.5.8 Wireless Power REC PWR Byte Status RAM Register (address = 0xE8) [reset = 00000000]

This register reads back the received power with LSB = 39 mW.

Figure 23. Wireless Power REC PWR Byte Status RAM Register Format

7	6	5	4	3	2	1	0
RECPWR7	RECPWR6	RECPWR5	RECPWR4	RECPWR3	RECPWR2	RECPWR1	RECPWR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

Table 12. Wireless Power REC PWR Byte Status RAM Register Field Descriptions

Bit	Field	Type	Reset	Description
B7:B0	RECPWR	R/W	00000000	Received Power LSB = 39 mW

8.5.9 Wireless Power Mode Indicator Register (address = 0xEF) [reset = 00000000]

This register reads back the MODE (WPC or PMA) based on the Transmitter.

Figure 24. Wireless Power Mode Indicator Register Format

7	6	5	4	3	2	1	0
Reserved	ALIGN	Reserved	Reserved	Reserved	Reserved	Reserved	MODE
R/W	R	R/W	R/W	R/W	R/W	R/W	R

LEGEND: R/W = Read/Write; R = Read only

Table 13. Wireless Power Mode Indicator Register Field Descriptions

Bit	Field	Type	Reset	Description
B7	Reserved	Read / Write	0	Not Used
B6	ALIGN Status	Read	0	Alignment mode = 1, Normal operation = 0 (Status bit)
B5:B1	Reserved	Read / Write	00000	Not Used
B0	Mode	Read	0	PMA = 1, WPC = 0 (Status bit)

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8.5.10 Wireless Power Prop Packet Payload RAM Byte 0 Register (address = 0xF1) [reset = 00000000]

Figure 25. Wireless Power Prop Packet Payload RAM Byte 0 Register Format

7	6	5	4	3	2	1	0
PL0_7	PL0_6	PL0_5	PL0_4	PL0_3	PL0_2	PL0_1	PL0_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

Table 14. Wireless Power Prop Packet Payload RAM Byte 0 Register Field Descriptions

Bit	Field	Type	Reset	Description
B7:B0	PL0	R/W	00000000	Proprietary Packet Byte 0 content

8.5.11 Wireless Power Prop Packet Payload RAM Byte 1 Register (address = 0xF2) [reset = 00000000]

Figure 26. Wireless Power Prop Packet Payload RAM Byte 1

7	6	5	4	3	2	1	0
PL1_7	PL1_6	PL1_5	PL1_4	PL1_3	PL1_2	PL1_1	PL1_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

Table 15. Wireless Power Prop Packet Payload RAM Byte 1 Field Descriptions

Bit	Field	Type	Reset	Description
B7:B0	PL1	R/W	00000000	Proprietary Packet Byte 1 content

8.5.12 Wireless Power Prop Packet Payload RAM Byte 2 Register (address = 0xF3) [reset = 00000000]

Figure 27. Wireless Power Prop Packet Payload RAM Byte 2 Register Format

7	6	5	4	3	2	1	0
PL2_7	PL2_6	PL2_5	PL2_4	PL2_3	PL2_2	PL2_1	PL2_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

Table 16. Wireless Power Prop Packet Payload RAM Byte 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
B7:B0	PL2	R/W	00000000	Proprietary Packet Byte 2 content

8.5.13 Wireless Power Prop Packet Payload RAM Byte 3 Register (address = 0xF4) [reset = 00000000]

Figure 28. Wireless Power Prop Packet Payload RAM Byte 3 Register Format

7	6	5	4	3	2	1	0
PL3_7	PL3_6	PL3_5	PL3_4	PL3_3	PL3_2	PL3_1	PL3_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

Table 17. Wireless Power Prop Packet Payload RAM Byte 3 Register Field Descriptions

Bit	Field	Type	Reset	Description
B7:B0	PL3	R/W	00000000	Proprietary Packet Byte 3 content

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8.5.14 RXID Readback Register (address = 0xF5 - 0xFA) [reset = see Table 18 note]

Registers 0xF5 to 0xFA store the RXID that can be read back when $V_{RECT} > V_{UVLO}$.

Figure 29. RXID Readback Register Format

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R	R	R	R	R	R	R	R

LEGEND: R = Read only

Table 18. RXID Readback Register Field Descriptions

Bit	Field	Type	Reset(1)	Description
B7:B0	Reserved	R		RXID

(1) Reset value is programmed at TI factory as a unique ID for each device.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

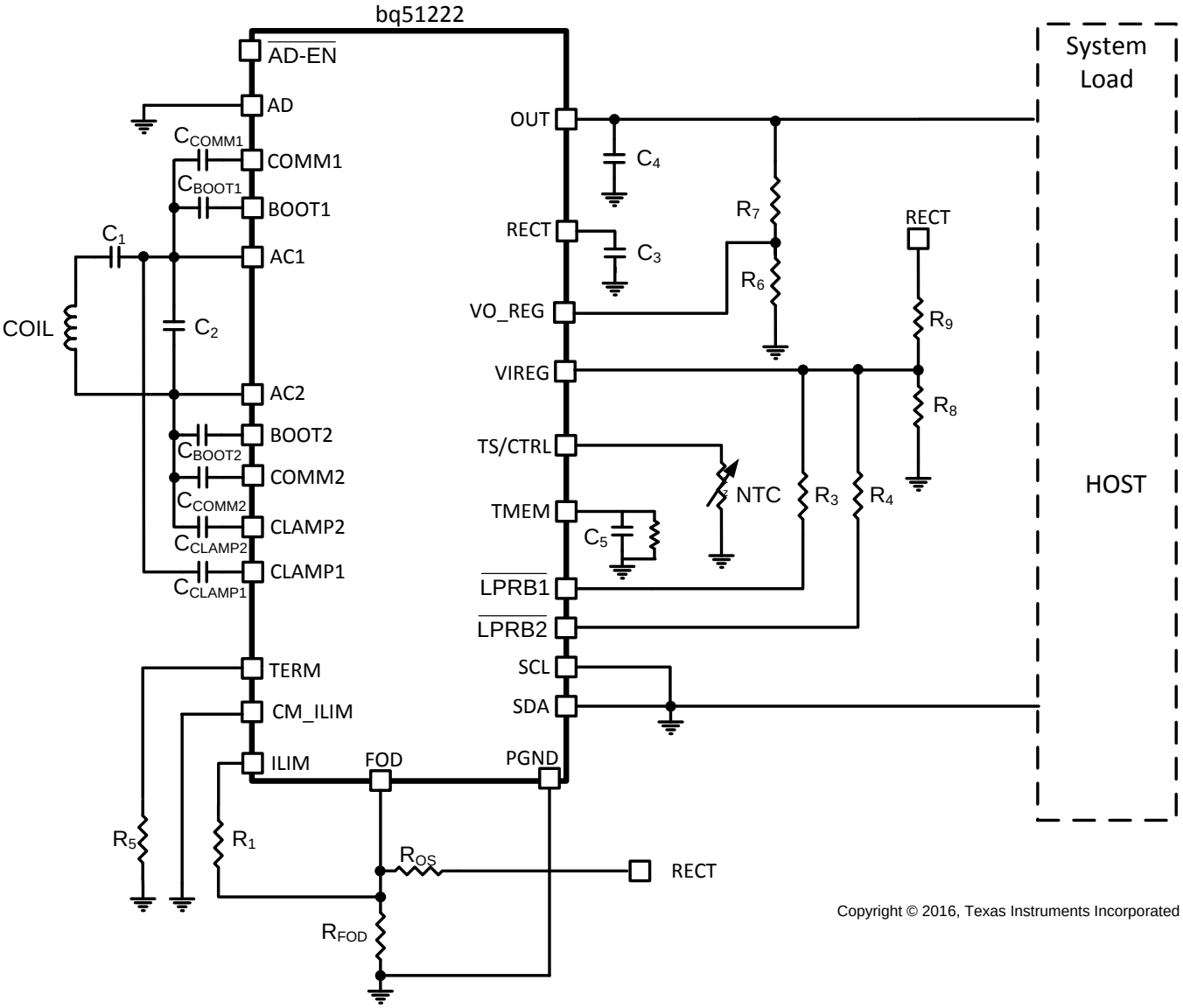
9.1 Application Information

The bq51222 device is a dual mode device which complies with both WPC v1.2 and PMA standards. This allows a system designer to design a system that complies with both wireless power standards. There are several tools available for the design of the system. These tools may be obtained by checking the product page at www.ti.com/product/bq51222. The following sections detail how to design a dual mode RX system.

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9.2 Typical Applications

9.2.1 Dual Mode Design (WPC and PMA Compliant) Power Supply 5-V Output with 1-A Maximum Current



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Figure 30. Dual Mode Schematic using bq51222

Typical Applications (continued)

9.2.1.1 Design Requirements

Table 19. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{OUT}	5 V
I_{OUT} MAXIMUM	1 A
MODE	WPC and PMA

9.2.1.2 Detailed Design Procedure

To start the design procedure, start by determining the following.

- Mode of operation – in this case dual mode (WPC and PMA)
- Output voltage
- Maximum output current

9.2.1.2.1 Output Voltage Set Point

The output voltage of the bq51222 device can be set by adjusting a feedback resistor divider network. The resistor divider network is used to set the voltage gain at the VO_REG pin. The device is intended to operate where the voltage at the VO_REG pin is set to 0.5 V. This value is the default setting and can be changed through I^2C. In Figure 31, R_6 and R_7 are the feedback network for the output voltage sense.

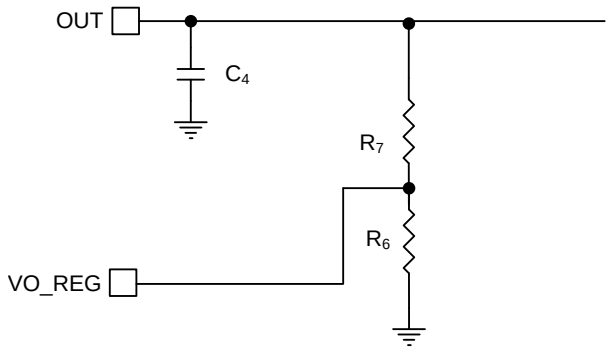


Figure 31. Voltage Gain for Feedback

$$K_{VO} = \frac{0.5\ V}{V_{OUT}} \quad (10)$$

$$R_6 = \frac{K_{VO} \times R_7}{1 - K_{VO}} \quad (11)$$

Choose R_7 to be a standard value. In this case, care should be taken to choose R_6 and R_7 to be fairly large values so as to not dissipate excessive amount of power in the resistors and thereby lower efficiency.

K_{VO} is set to be 0.5 / 5 = 0.1, choose R_7 to be 102 kΩ, and thus R_6 to be 11.3 kΩ.

After R_6 and R_7 are chosen, the same values should be used on R_8 and R_9. This allows the device to regulate the rectifier in the PMA mode to accurately track the output voltage when the output voltage is changed through I^2C.

9.2.1.2.2 Output and Rectifier Capacitors

Set C_4 between 1 µF and 4.7 µF. This example uses 1 µF.

Set C_3 between 4.7 µF and 22 µF. This example uses 20 µF.

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9.2.1.2.2.1 TMEM

Set C_5 to 2.2 µF. In order to determine the bleed off resistor, the WPC transmitters for which the $\overline{PD_DET}$ is being set for needs to be determined. After the ping timing (time between two consecutive digital pings after EPT charge complete is sent) is determined, the bleedoff resistor can be determined. This example uses TI transmitter EVMs as the use case. In this case the time between pings is 5 s. In order to set the time constant using Equation 8, it is set to 5.6 MΩ.

9.2.1.2.3 Maximum Output Current Set Point

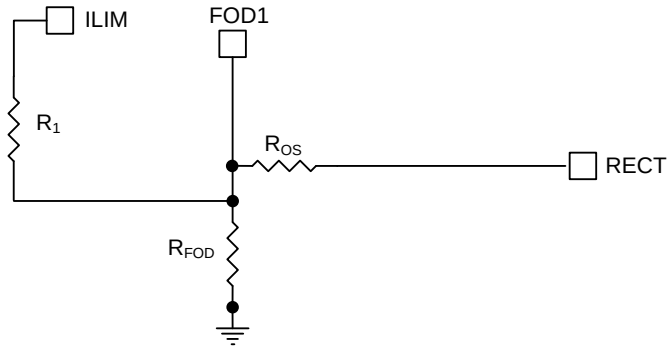


Figure 32. Current Limit Setting for bq51222

The bq51222 device includes a means of providing hardware overcurrent protection by means of an analog current regulation loop. The hardware current limit provides a level of safety by clamping the maximum allowable output current (for example, a current compliance). The R_{ILIM} resistor size also sets the thresholds for the dynamic rectifier levels and thus providing efficiency tuning per each application's maximum system current. The calculation for the total R_{ILIM} resistance is as follows:

$$R_{ILIM} = \frac{K_{ILIM}}{I_{ILIM}} \quad (12)$$

$$R_1 = R_{ILIM} - R_{FOD} \quad (13)$$

The R_{ILIM} will allow for the ILIM pin to reach 1.2 V at an output current equal to I_{ILIM}. When choosing R_{ILIM}, two options are possible.

If the application requires an output current equal to or greater than external ILIM that the circuit is designed for (input current limit on the charger where the RX is delivering power to is higher than the external ILIM), ensure that the downstream charger is capable of regulating the voltage of the input into which the RX device output is tied to by lowering the amount of current being drawn. This will ensure that the RX output does not collapse.

Such behavior is referred to as VIN-DPM in TI chargers. Unless such behavior is enabled on the charger, the charger will pull the output of the RX device to ground when the RX device enters current regulation.

If the applications are designed to extract less than the ILIM (1-A maximum), typical designs should leave a design margin of at least 20% so that the voltage at ILIM pin reaches 1.2 V when 20% more than maximum current of the system is drawn from the output of the RX. Such a design would have input current limit on the charger lower than the external ILIM of the RX device.

In both cases however, the charger must be capable of regulating the current drawn from the device to allow the output voltage to stay at a reasonable value. This same behavior is also necessary during the WPC v1.2 Communication. See *Communication Current Limit* for more details. The following calculations show how such a design is achieved:

$$R_{ILIM} = \frac{K_{ILIM}}{1.2 \times I_{ILIM}} \quad (14)$$

$$R_1 = R_{ILIM} - R_{FOD} \quad (15)$$

When referring to the application diagram shown in Figure 32, R_{ILIM} is the sum of the R_1 and R_{FOD} resistance (that is, the total resistance from the ILIM pin to GND). R_{FOD} is chosen according to the FOD application note that can be obtained by contacting your TI representative. This is used to allow the RX implementation to comply with WPC v1.2 requirements related to received power accuracy.

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Also note that in many applications, the resistor R_{OS} is needed in order to comply with WPC v1.2 requirements. In such a case, the offset on the FOD pin from the voltage on R_{FOD} can cause a shift in the calculation that can reduce the expected current limit. Therefore, it is always a good idea to check the output current limit after FOD calibration is performed according to the FOD section shown below. Unfortunately, because the RECT voltage is not deterministic, and depends on transmitter operation to a certain degree, it is not possible to determine R_1 with R_{OS} present in a deterministic manner.

In this example, set maximum current for the example to be 1000 mA. To set I_{ILIM} = 1.2 A to allow for the 20% margin.

$$R_{ILIM} = \frac{840}{1.2} = 700\ \Omega \tag{16}$$

9.2.1.2.4 TERM Resistor

The TERM resistor is used to set the termination threshold on the RX. The device will send an EPT Charge Complete, or EOC message to the transmitter and thus allow for the system to go into a low standby mode. This is also mandated through PMA specification.

By picking a resistor to ground from the TERM pin the system designer can set the termination threshold. The device will send the EPT/EOC message, when the voltage on the ILIM pin goes below the voltage on the TERM pin. The designer can therefore set a resistor on the TERM pin that will determine the threshold.

$$R_5 = \frac{V_{ILIM_TERM}}{50 \times 10^{-6}} \tag{17}$$

Typically, one can use R_{ILIM} to set R_5 resistor such that at the desired current, on OUT pin, V_{ILIM_TERM} can be reached. However, this can be made indeterministic because of the presence of the R_{os} resistor that is used to comply with WPC v1.2 FOD requirements. Therefore, the system designer is suggested to measure the voltage on the ILIM pin at the output current where he would like to set the termination. This voltage on the ILIM pin is termed as V_{ILIM_TERM}. In the design example, to set 50 mA, measure V_{ILIM_TERM}. After this is done, set the resistor R_5 using the equation Equation 17.

9.2.1.2.5 Setting $\overline{\text{LPRB1}}$ and $\overline{\text{LPRB2}}$ Resistors

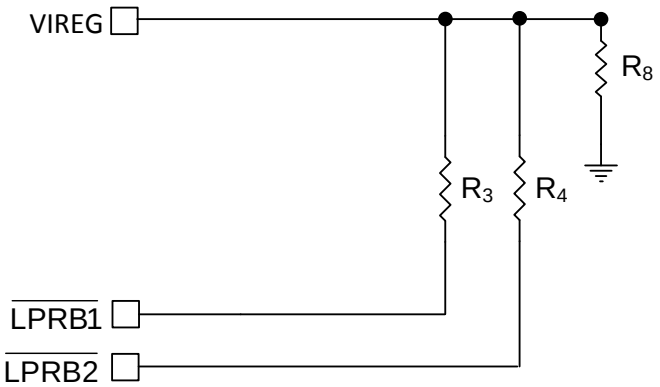


Figure 33. Setting Low Power Rectifier Boost

$\overline{\text{LPRB1}}$ and $\overline{\text{LPRB2}}$ are multifunction pins. Depending on whether the termination resistor is used or not, the $\overline{\text{LPRB}}$ pins will change function. This allows the designer to optimize the PMA design for efficiency or transient performance.

Table 20. LPRB Setup for Different Applications

IMPLEMENTATION	TERM RESISTOR	BALL NUMBER F5	BALL NUMBER G6
Backcover	Populated	$\overline{\text{LPRB1}}$	$\overline{\text{LPRB2}}$
Embedded	Not populated	$\overline{\text{WPG}}$	$\overline{\text{PD_DET}}$

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For more information on how to set the TERM resistor, see *TERM Resistor*.

The $\overline{\text{LPRBx}}$ boosts the rectifier voltage to a higher voltage, and thus it sets the transmitter in PMA mode to operate in frequency or load line that can sustain load step which is part of the PMA certification process. $\overline{\text{LPRB1}}$ is used to boost the rectifier voltage at low power (output current below about 95 mA). $\overline{\text{LPRB2}}$ is used to boost the rectifier voltage when output current is below about 310 mA). Both pins are connected to VIREG through resistors, R_3 and R_4 as shown in *Setting $\overline{\text{LPRB1}}$ and $\overline{\text{LPRB2}}$ Resistors*. These two values depend on the coil and the output voltage choice. Also, the allowable voltage drop also defined by the board manufacturer can allow you to set the voltage in these modes to optimize the efficiency and transient response. To design R_3 and R_4, set a window of V_{RECT} to boost the operating frequency of the TX a 0-mA load and 100 mA

Good starting points are: 7.3 to 7.8 V for 0 to 100 mA and 6.7 to 7.3 V for 100 to 400 mA

Now, find the values of R_3 and R_4 that can provide the chosen window. The lower and upper reference of VIREG is 0.4906 and 0.5318 V

Calculate V_{RECT} as follows using the TI tool provided in the product folder under the "Tools & sofware" tab.

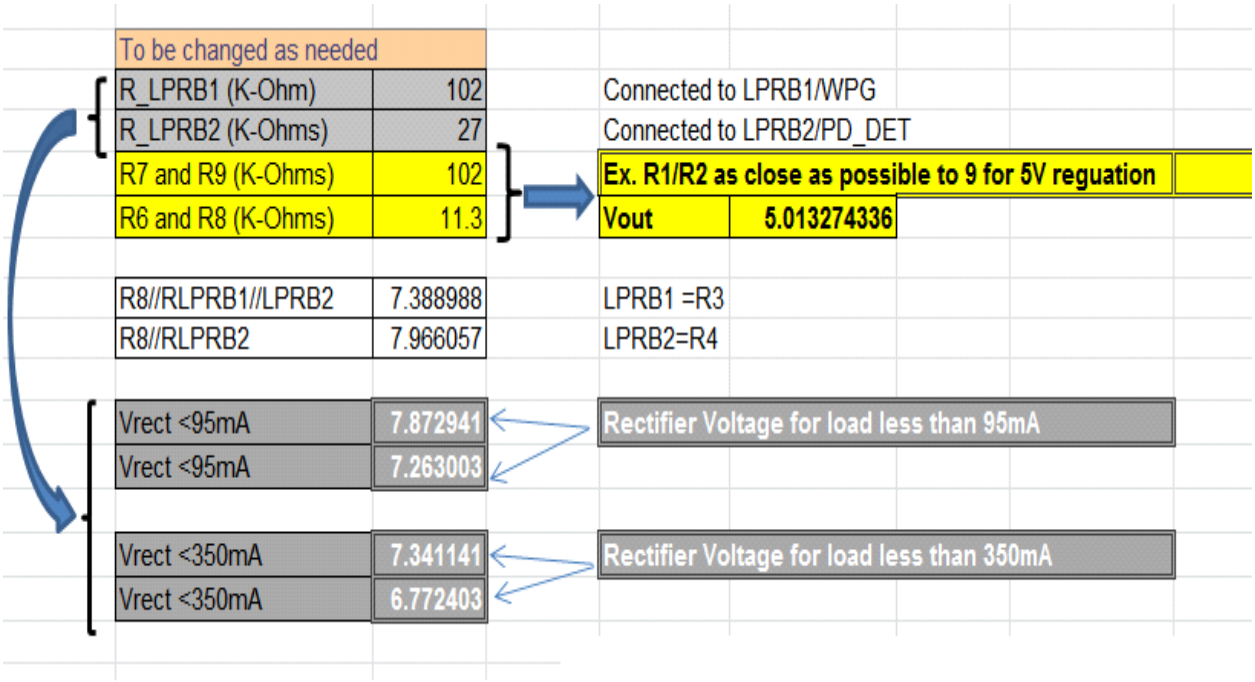


Figure 34. LPRB Resistor Calculations

9.2.1.2.6 I^2C

The I^2C lines are used to communicate with the device. In order to enable the I^2C, they can be pulled up to an internal host bus. When not in use as in Figure 55, tie them to GND. The device address is 0x6C.

9.2.1.2.7 Communication Current Limit

Communication current limit allows the device to communicate with the transmitter in an error free manner by decoupling the coil from load transients on the OUT pin during WPC communication. In some cases this communication current limit feature is not desirable. In this design, the user enables the communication current limit. This is done by tying the CM_ILIM pin to GND. In the case that this is not needed, the CM_ILIM pin can be tied to OUT pin to disable the communication current limit. In this case, take care that the voltage on the CM_ILIM pin does not exceed the maximum rating of the pin.

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9.2.1.2.8 Receiver Coil

The receiver coil design is the most open and interesting part of the system design. The choice of the receiver inductance, shape, and materials all intimately influence the parameters themselves in an intertwined manner. This design can be complicated and involves optimizing many different aspects; refer to the user's guide for the EVM (SLUUAX6).

The typical choice of the inductance of the receiver coil for a dual mode 5-V solution is between 6 to 8 µH.

9.2.1.2.9 Series and Parallel Resonant Capacitors

Resonant capacitors C_1 and C_2 are set according to WPC specification. Although this is a dual mode solution, the PMA does not specify an exact resonance frequency for the resonant capacitors and in fact does not specify that resonant capacitors are indeed needed.

The equations for calculating the values of the resonant capacitors are shown:

$$C_1 = \left[\left(f_S \times 2\pi \right)^2 \times L'_S \right]^{-1}$$

$$C_2 = \left[\left(f_D \times 2\pi \right)^2 \times L_S - \frac{1}{C_1} \right]^{-1} \quad (18)$$

9.2.1.2.10 Communication, Boot and Clamp Capacitors

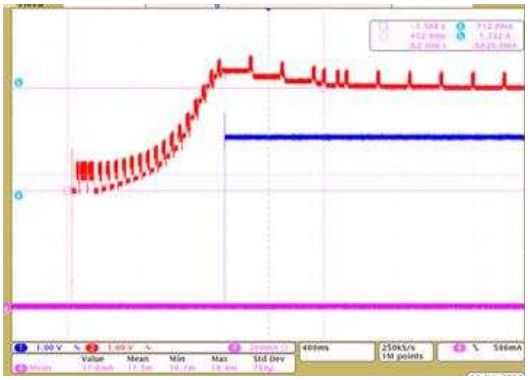
Set C_{COMMx} to a value ranging from C_1 / 8 to C_1 / 3. The higher the value of the communication capacitors, the easier it is to comply with PMA specification. However, higher capacitors do lower the overall efficiency of the system. Make sure these are X7R ceramic material and have a minimum voltage rating of 25 V.

Set C_{BOOTx} to be 15 nF. Make sure these are X7R ceramic material and have a minimum voltage rating of 25 V.

Set C_{CLAMPx} to be 470 nF. Make sure these are X7R ceramic material and have a minimum voltage rating of 25 V.

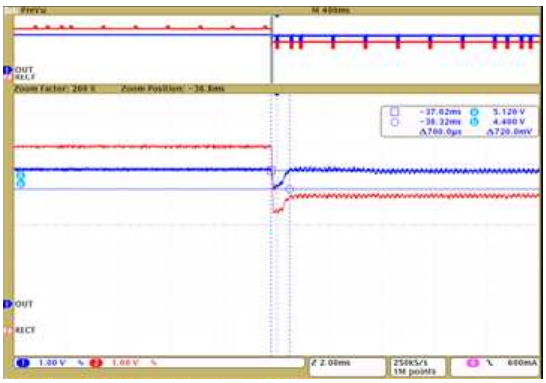
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9.2.1.3 Application Curves



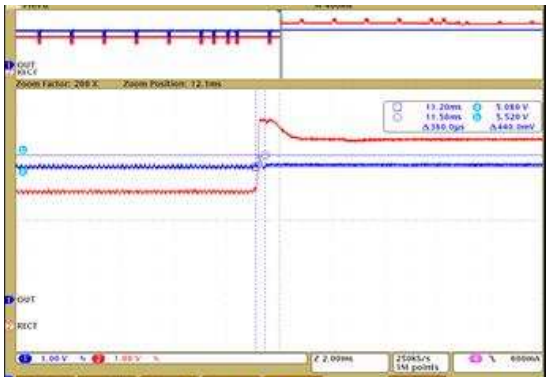
Ch1: V_{OUT}, 1 V Ch3: unused 400 ms/Div
Ch2: V_{RECT}, 1 V Ch4: I_{OUT}, 200 mA

Figure 35. bq51222 No Load Start-up on a WPC TX



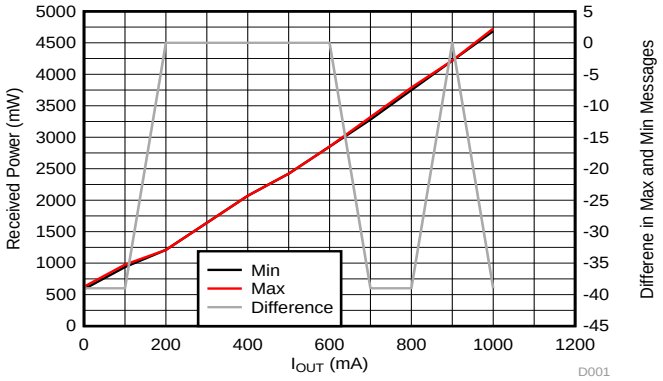
Ch1: V_{OUT}, 1 V Ch3: unused 2 ms/Div
Ch2: V_{RECT}, 1 V Ch4: I_{OUT}, 200 mA

Figure 36. 0-mA to 1000-mA Step on a WPC TX



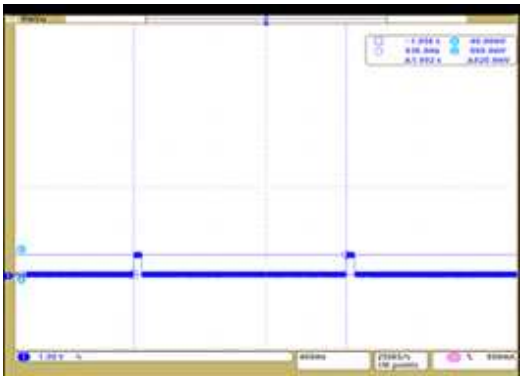
Ch1: V_{OUT}, 1 V Ch3: unused 2 ms/Div
Ch2: V_{RECT}, 1 V Ch4: unused

Figure 37. 1000-mA to 0-mA Load Dump on a WPC TX



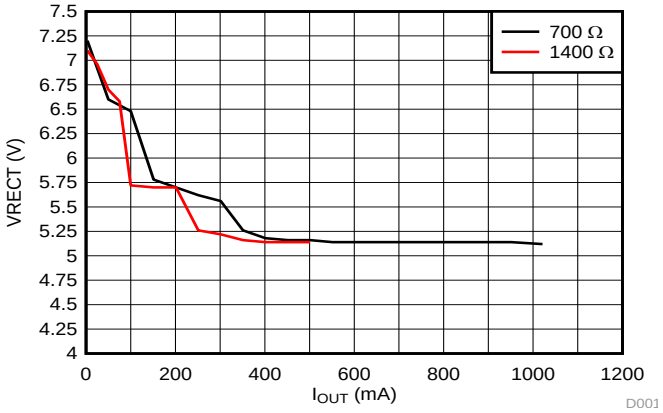
Data taken over approximately 3 minutes

Figure 38. Received Power Variation (mW) vs I_{OUT} (mA) on a WPC TX



Ch1: TS, 1 V Ch3: unused 400 ms/Div
Ch2: unused Ch4: unused

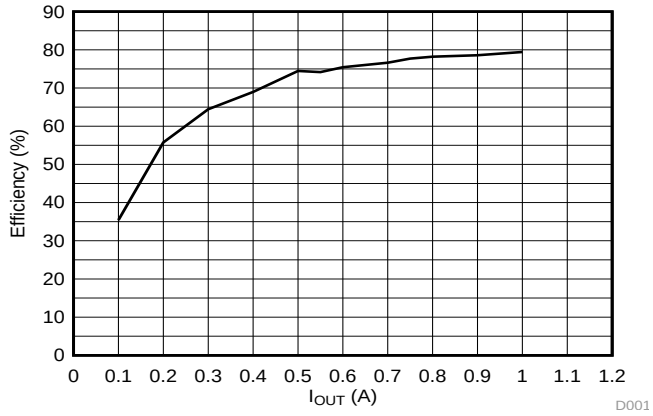
Figure 39. TS Voltage Bias without TS Resistor



R_{ILIM} = 700 Ω
R_{ILIM} = 1400 Ω

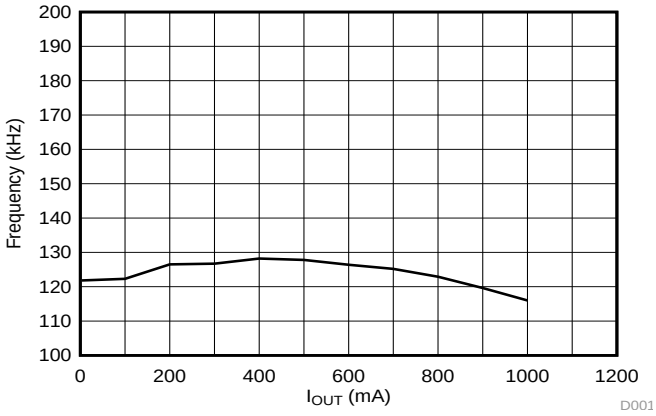
Figure 40. Rectifier Regulation on a WPC TX

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V_{OUT} = 5 V

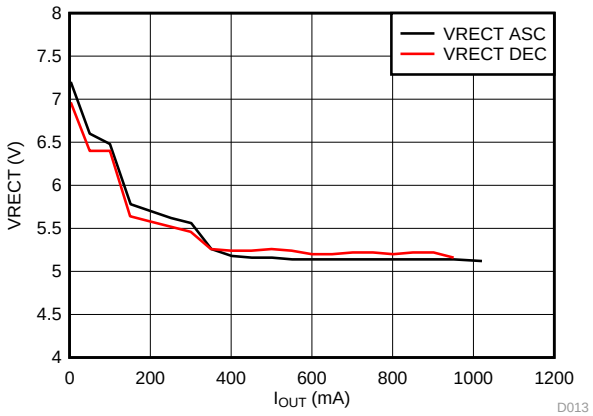
Figure 41. bq51222 WPC Efficiency on a WPC TX



V_{OUT} = 5 V

TX: bq500210EVM-689, RX: bq51222EVM-520

Figure 42. Frequency Range on a WPC TX



R_{ILIM} = 700 Ω

TX: bq500210EVM-689, RX: bq51222EVM-520

Figure 43. Dynamic Regulation on a WPC TX

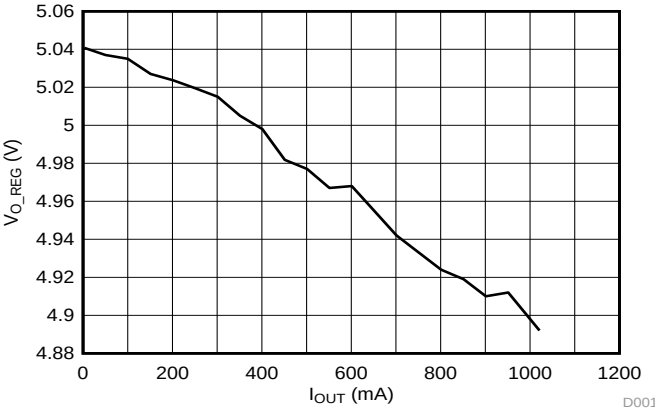


Figure 44. Output Regulation on a WPC TX

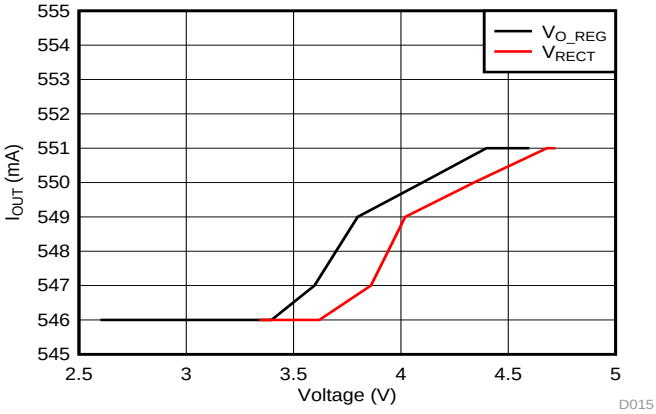
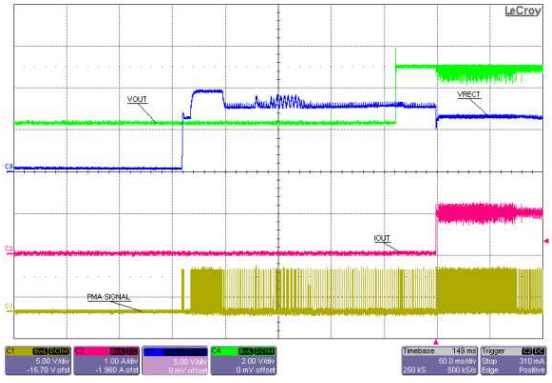


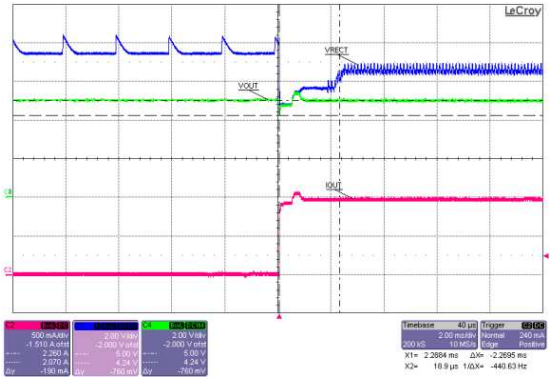
Figure 45. RECT Foldback in Current Limit on a WPC TX



Ch1: PMA communication, 5 V
Ch2: I_{OUT}, 1 A
Ch3: V_{RECT}, 5 V
Ch4: V_{OUT}, 2 V
50 ms/Div

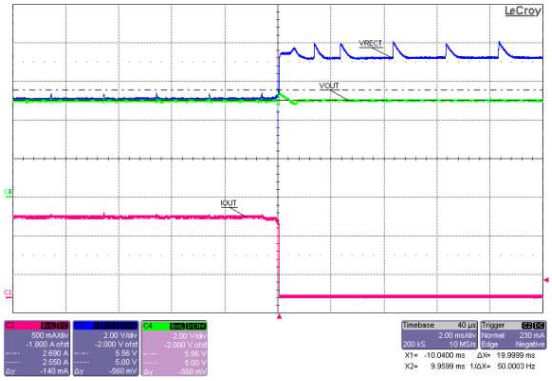
Figure 46. Startup on a PMA TX

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Ch1: unused Ch3: V_{RECT}, 2 V 2 ms/Div
Ch2: I_{OUT}, 500 mA Ch4: V_{OUT}, 2 V

Figure 47. Load Step from 0 mA to 1000 mA on PMA TX



Ch1: unused Ch3: V_{RECT}, 2 V 2 ms/Div
Ch2: I_{OUT}, 500 mA Ch4: V_{OUT}, 2 V

Figure 48. Load Dump from 1000 mA to 0 mA on PMA TX

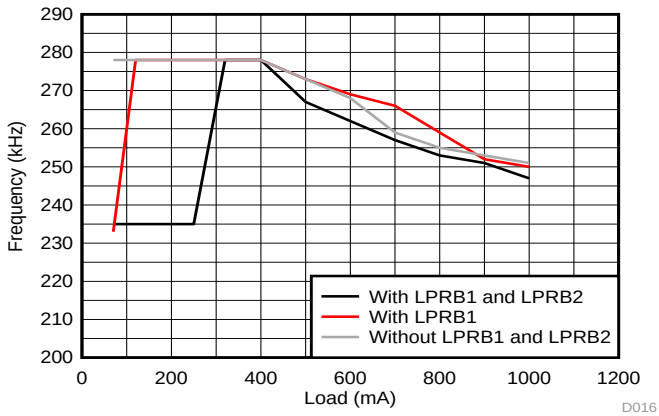
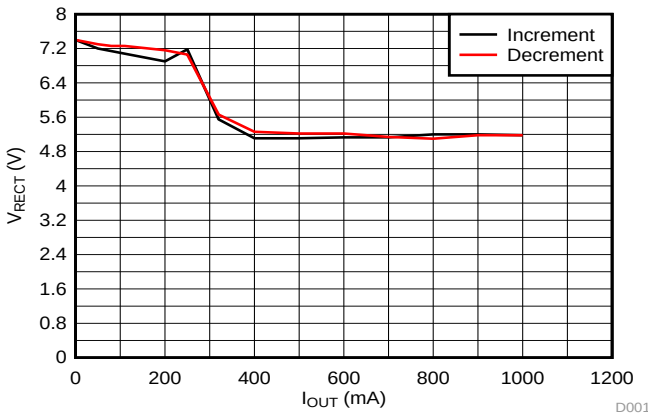
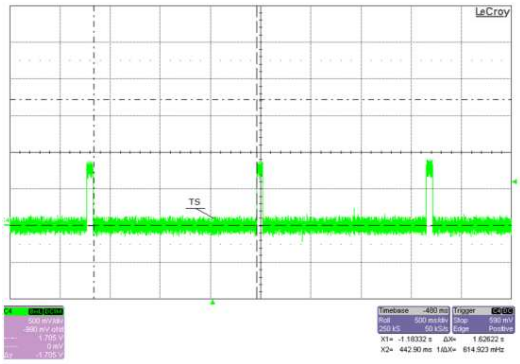


Figure 49. Frequency of Operation on a PMA TX



V_{OUT} = 5 V
TX: Duracell Powermat, RX: bq51222EVM-520

Figure 50. V_{RECT} on a PMA TX



Ch1: unused Ch3: unused 500 ms/Div
Ch2: unused Ch4: TS, 500 mV

Figure 51. TS Measurement on a PMA TX

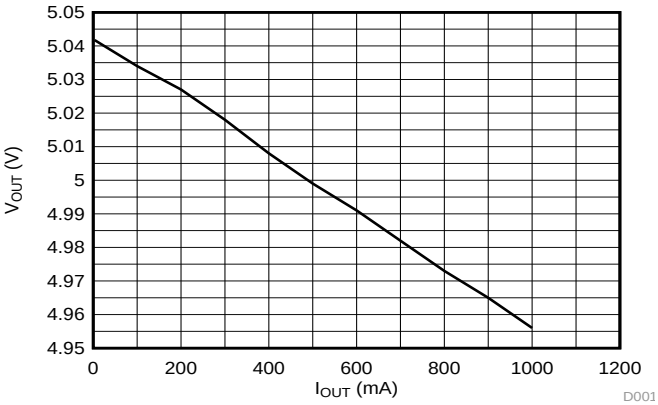
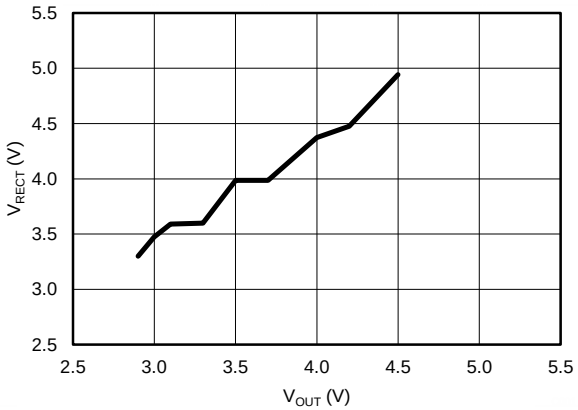


Figure 52. Output Voltage Regulation on a PMA TX

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PMA mode, operating in current limit
I_{ILIM} = 1 A

Figure 53. V_{RECT} Tracks V_{OUT}

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9.2.2 Embedded in System Board

When the bq51222 device is implemented as an embedded device on the system board, LPRBEN (TERM) pin is floated and WPG and PD_DET are set to their function. When LPRBEN has a resistor to ground to enable TERM, PD_DET becomes LPRB1 and WPG becomes LPRB2. This second configuration with TERM enabled is preferred for a back cover implementation. A back cover implementation is one where the receiver device and receiver coil are contained in the back cover of the mobile phone where the receiver is being implemented. With an embedded implementation (one where only the coil is in the mobile device back cover and the receiver device is on the main motherboard for the mobile phone and is controlled by the host controller device in the phone), the expectation is that the host controller (PMIC or Charger) will use the TS/CTRL pin to establish termination and associated EPT or EOC.

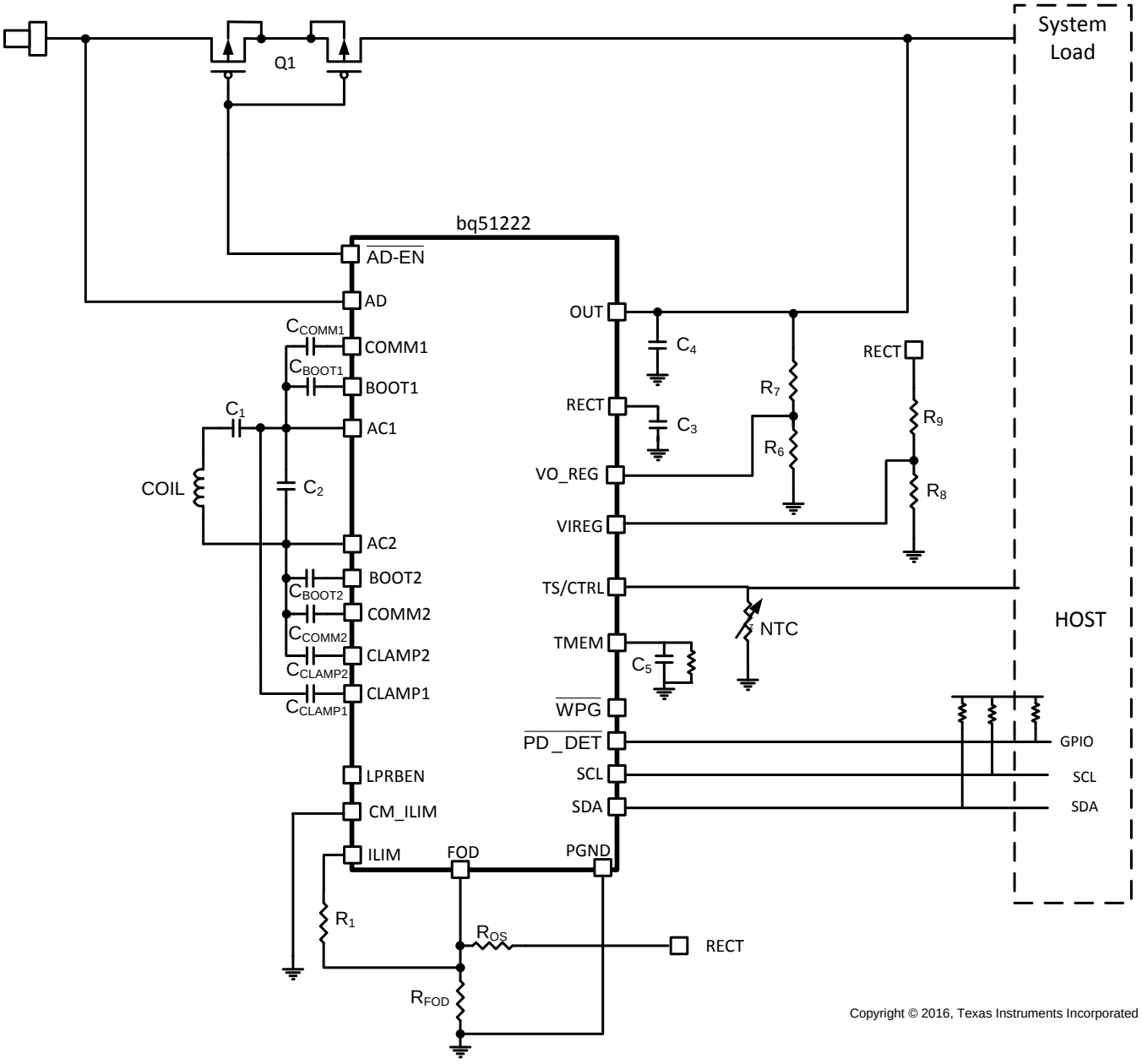


Figure 54. bq51222 Embedded in a System Board

Refer to *Dual Mode Design (WPC and PMA Compliant) Power Supply 5-V Output with 1-A Maximum Current* for all design details.

9.2.3 bq51222 Implemented in Back Cover

When the bq51222 device is implemented as a back cover solution, set TERM resistor to enable PMA term and LPRB1 and LPRB2 functions are automatically enabled. In this implementation, the bq51222 device can autonomously determine if EOC can be established because the termination current has been reached. In this configuration, PD_DET becomes LPRB1 and WPG becomes LPRB2. This allows the RECT voltage to be controlled at different levels so that transient performance from light load to maximum current can be optimized.

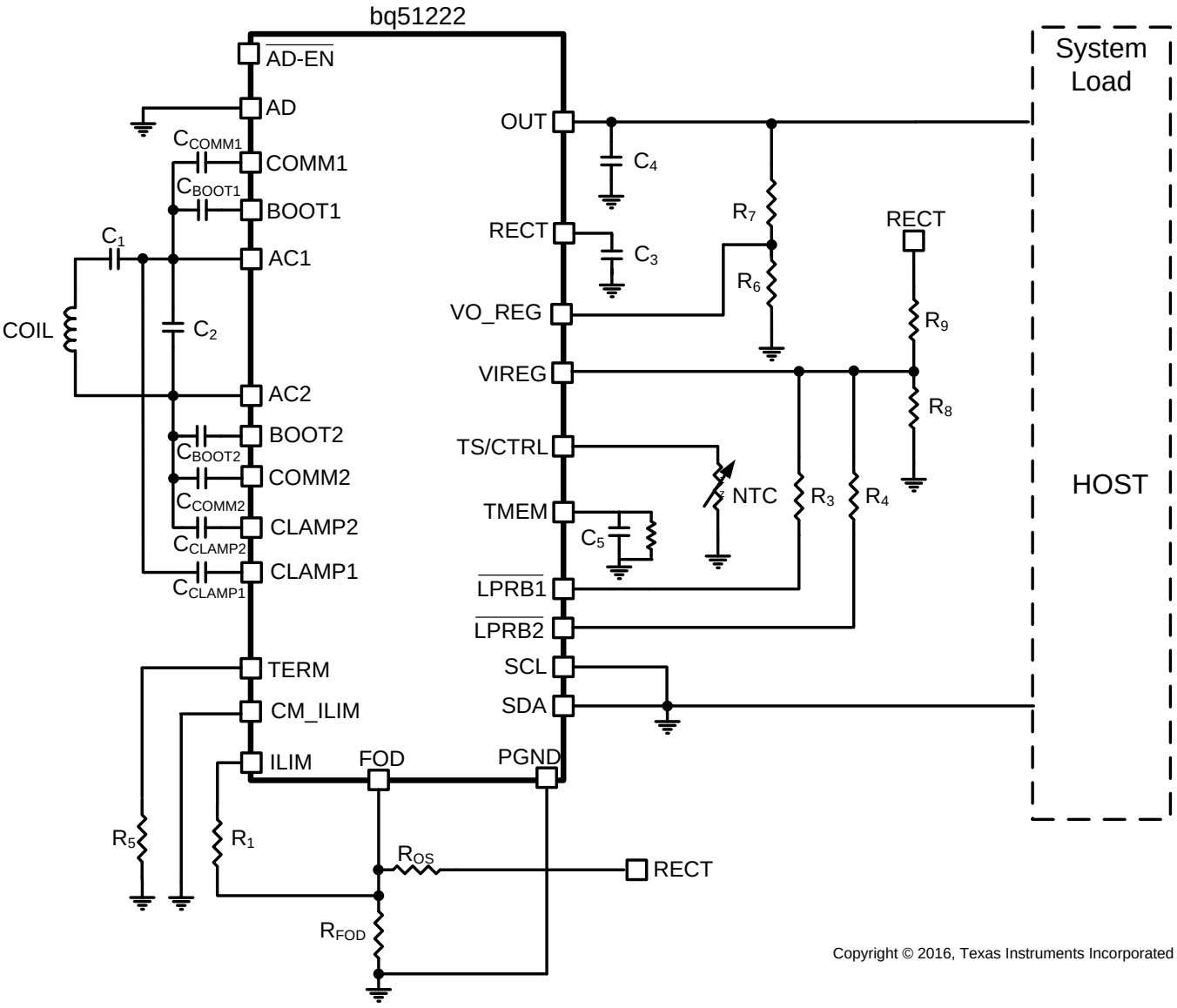


Figure 55. bq51222 Implemented in a Back Cover

Refer to *Dual Mode Design (WPC and PMA Compliant) Power Supply 5-V Output with 1-A Maximum Current* for all design details.

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10 Power Supply Recommendations

These devices are intended to be operated within the ranges shown in the *Recommended Operating Conditions*. Because the system involves a loosely coupled inductor set up, the voltages produced on the receiver are a function of the inductances and the available magnetic field. Ensure that the design in the worst case keeps the voltages within the *Absolute Maximum Ratings*.

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11 Layout

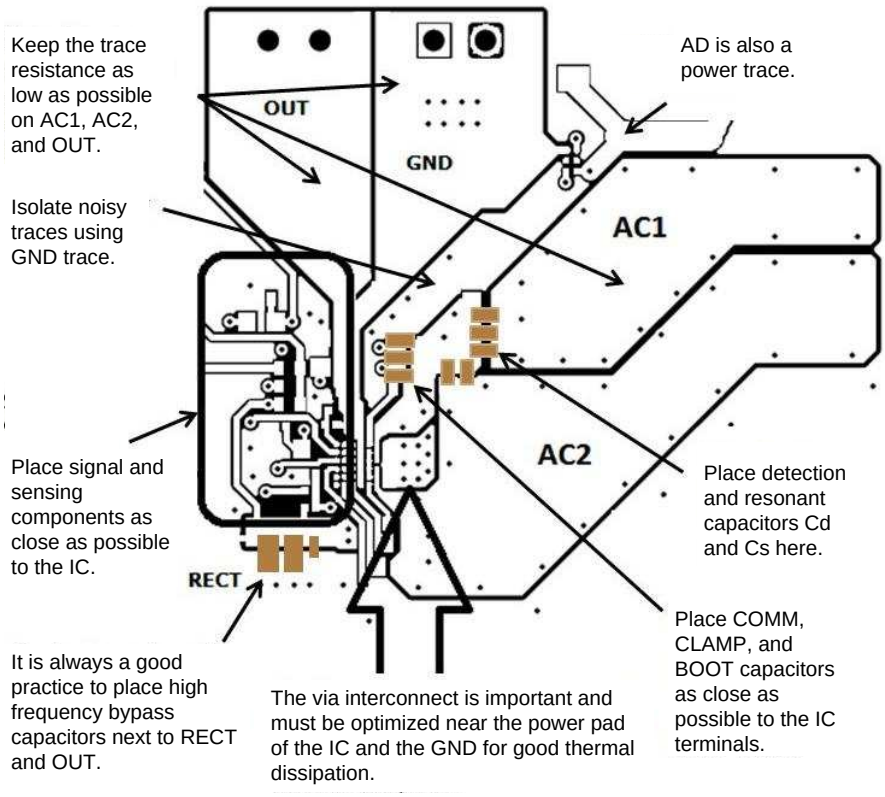
11.1 Layout Guidelines

- Keep the trace resistance as low as possible on AC1, AC2, and OUT.
- Detection and resonant capacitors need to be as close to the device as possible.
- COMM, CLAMP, and BOOT capacitors need to be placed as close to the device as possible.
- Via interconnect on GND net is critical for appropriate signal integrity and proper thermal performance.
- High frequency bypass capacitors need to be placed close to RECT and OUT pins.
- ILIM and FOD resistors are important signal paths and the loops in those paths to GND must be minimized.

  Signal and sensing traces are the most sensitive to noise; the sensing signal amplitudes are usually measured in mV, which is comparable to the noise amplitude. Make sure that these traces are not being interfered by the noisy and power traces. AC1, AC2, BOOT1, BOOT2, COMM1, and COMM2 are the main source of noise in the board. These traces should be shielded from other components in the board. It is usually preferred to have a ground copper area placed underneath these traces to provide additional shielding. Also, make sure they do not interfere with the signal and sensing traces. The PCB should have a ground plane (return) connected directly to the return of all components through vias (two vias per capacitor for power-stage capacitors, one via per capacitor for small-signal components).

  For a 1-A fast charge current application, the current rating for each net is as follows:
  - AC1 = AC2 = 1.2 A
  - OUT = 1 A
  - RECT = 100 mA (RMS)
  - COMMx = 300 mA
  - CLAMPx = 500 mA
  - All others can be rated for 10 mA or less

11.2 Layout Example



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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ51222YFPR	ACTIVE	DSBGA	YFP	42	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	BQ51222	Samples
BQ51222YFPT	ACTIVE	DSBGA	YFP	42	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	BQ51222	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

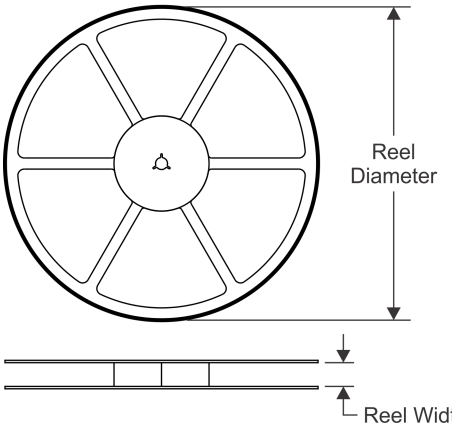
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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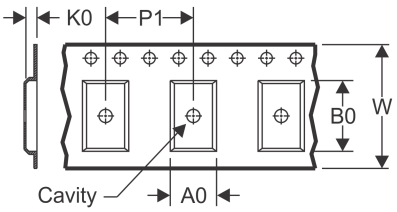
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

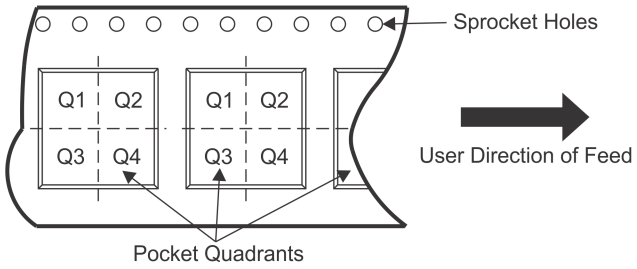


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

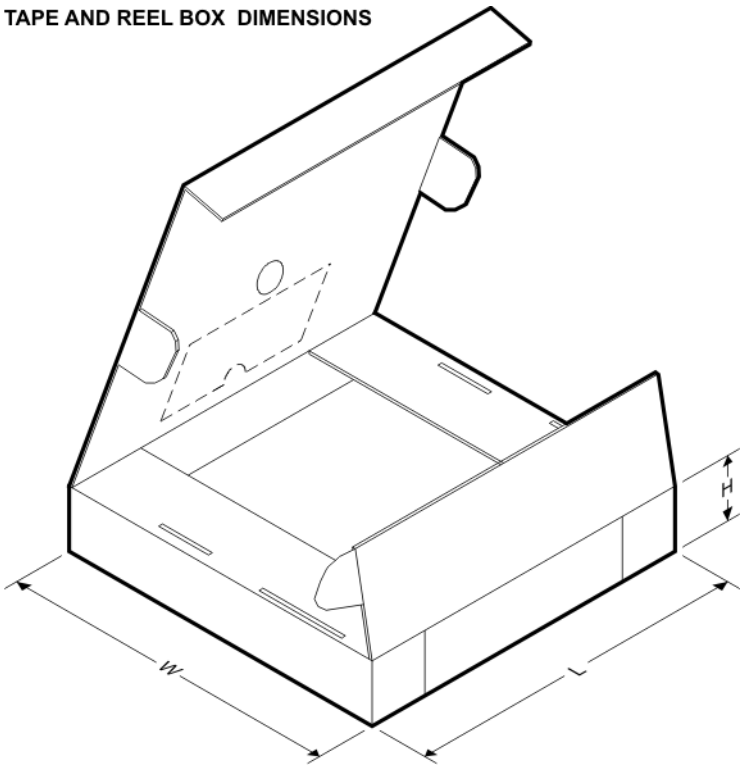
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ51222YFPR	DSBGA	YFP	42	3000	330.0	12.4	2.99	3.71	0.81	8.0	12.0	Q1
BQ51222YFPT	DSBGA	YFP	42	250	330.0	12.4	2.99	3.71	0.81	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

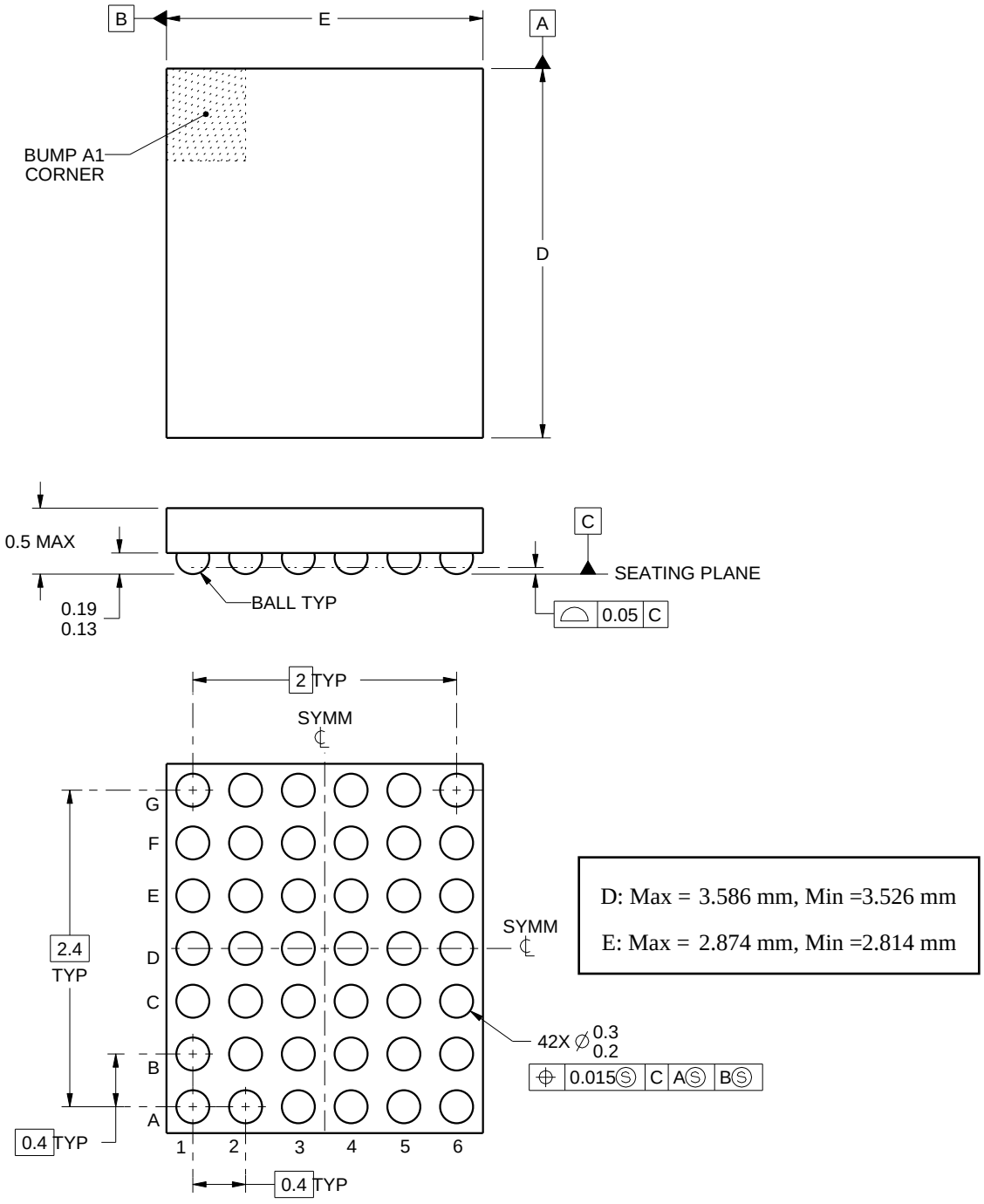
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ51222YFPR	DSBGA	YFP	42	3000	335.0	335.0	25.0
BQ51222YFPT	DSBGA	YFP	42	250	335.0	335.0	25.0

PACKAGE OUTLINE

YFP0042

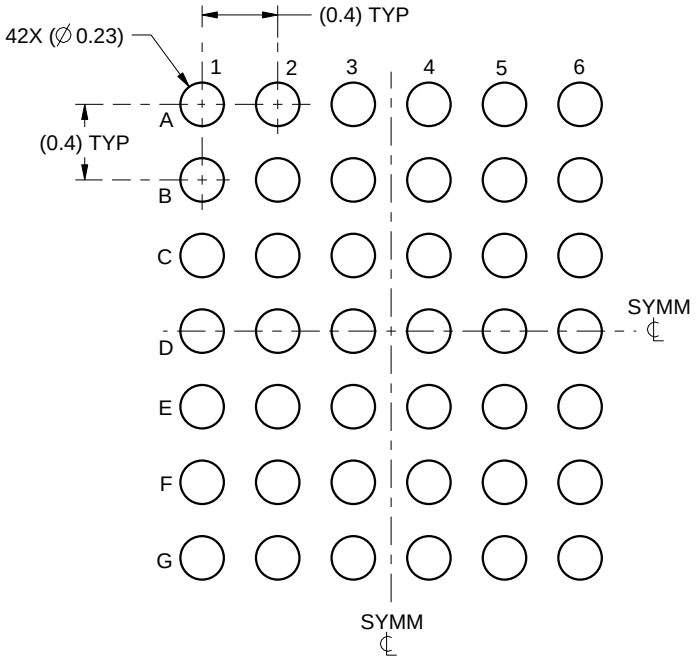
DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

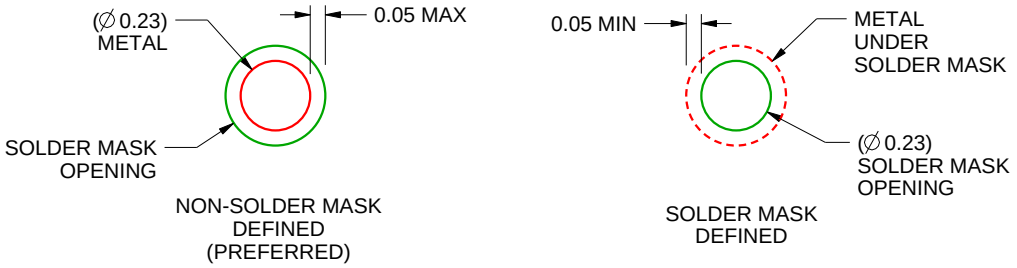


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:25X

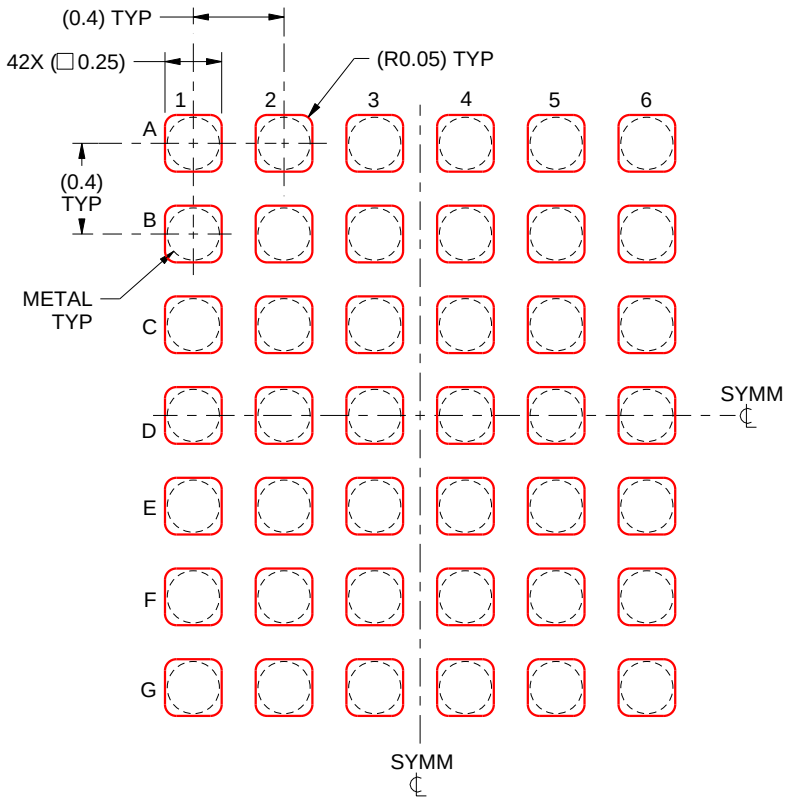


SOLDER MASK DETAILS
NOT TO SCALE

4221555/B 04/2015

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4221555/B 04/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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