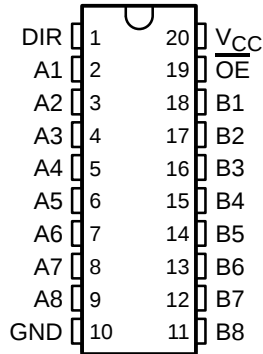


# SN54HC645, SN74HC645 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

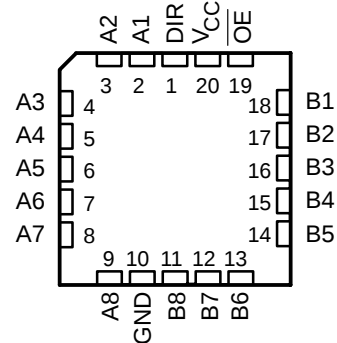
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- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 12$  ns
- $\pm 6$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- True Logic

SN54HC645 . . . J OR W PACKAGE  
SN74HC645 . . . DW, N, OR NS PACKAGE  
(TOP VIEW)



SN54HC645 . . . FK PACKAGE  
(TOP VIEW)



## description/ordering information

These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated.

## ORDERING INFORMATION

| $T_A$          | PACKAGE <sup>†</sup> |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------------------|---------------|-----------------------|------------------|
| –40°C to 85°C  | PDIP – N             | Tube          | SN74HC645N            | SN74HC645N       |
|                | SOIC – DW            | Tube          | SN74HC645DW           | HC645            |
|                |                      | Tape and reel | SN74HC645DWR          |                  |
|                | SOP – NS             | Tape and reel | SN74HC645NSR          | HC645            |
| –55°C to 125°C | CDIP – J             | Tube          | SNJ54HC645J           | SNJ54HC645J      |
|                | CFP – W              | Tube          | SNJ54HC645W           | SNJ54HC645W      |
|                | LCCC – FK            | Tube          | SNJ54HC645FK          | SNJ54HC645FK     |

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE

| INPUTS          |     | OPERATION       |
|-----------------|-----|-----------------|
| $\overline{OE}$ | DIR |                 |
| L               | L   | B data to A bus |
| L               | H   | A data to B bus |
| H               | X   | Isolation       |



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

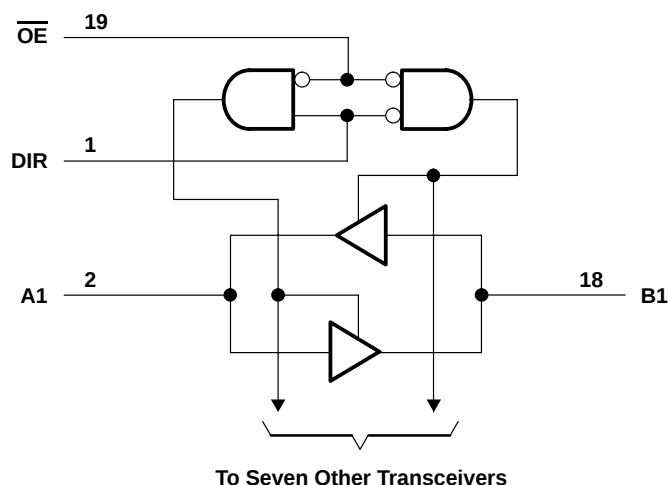
# SN54HC645, SN74HC645

## OCTAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                             |                |
|-----------------------------------------------------------------------------|----------------|
| Supply voltage range, $V_{CC}$                                              | –0.5 V to 7 V  |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)  | $\pm 20$ mA    |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1) | $\pm 20$ mA    |
| Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )                  | $\pm 35$ mA    |
| Continuous current through $V_{CC}$ or GND                                  | $\pm 70$ mA    |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package           | 58°C/W         |
| N package                                                                   | 69°C/W         |
| NS package                                                                  | 60°C/W         |
| Storage temperature range, $T_{stg}$                                        | –65°C to 150°C |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 3)

|                 |                                 |                         | SN54HC645 |                 |     | SN74HC645 |                 |     | UNIT |
|-----------------|---------------------------------|-------------------------|-----------|-----------------|-----|-----------|-----------------|-----|------|
|                 |                                 |                         | MIN       | NOM             | MAX | MIN       | NOM             | MAX |      |
| V <sub>CC</sub> | Supply voltage                  |                         | 2         | 5               | 6   | 2         | 5               | 6   | V    |
| V <sub>IH</sub> | High-level input voltage        | V <sub>CC</sub> = 2 V   | 1.5       |                 |     | 1.5       |                 |     | V    |
|                 |                                 | V <sub>CC</sub> = 4.5 V | 3.15      |                 |     | 3.15      |                 |     |      |
|                 |                                 | V <sub>CC</sub> = 6 V   | 4.2       |                 |     | 4.2       |                 |     |      |
| V <sub>IL</sub> | Low-level input voltage         | V <sub>CC</sub> = 2 V   | 0.5       |                 |     | 0.5       |                 |     | V    |
|                 |                                 | V <sub>CC</sub> = 4.5 V | 1.35      |                 |     | 1.35      |                 |     |      |
|                 |                                 | V <sub>CC</sub> = 6 V   | 1.8       |                 |     | 1.8       |                 |     |      |
| V <sub>I</sub>  | Input voltage                   |                         | 0         | V <sub>CC</sub> |     | 0         | V <sub>CC</sub> |     | V    |
| V <sub>O</sub>  | Output voltage                  |                         | 0         | V <sub>CC</sub> |     | 0         | V <sub>CC</sub> |     | V    |
| Δt/Δv           | Input transition rise/fall time | V <sub>CC</sub> = 2 V   | 1000      |                 |     | 1000      |                 |     | ns   |
|                 |                                 | V <sub>CC</sub> = 4.5 V | 500       |                 |     | 500       |                 |     |      |
|                 |                                 | V <sub>CC</sub> = 6 V   | 400       |                 |     | 400       |                 |     |      |
| T <sub>A</sub>  | Operating free-air temperature  |                         | −55       | 125             |     | −40       | 85              |     | °C   |



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# SN54HC645, SN74HC645 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS            |                                | $V_{CC}$   | $T_A = 25^\circ\text{C}$ |            |           | SN54HC645 |            | SN74HC645 |            | UNIT          |
|-----------|----------------------------|--------------------------------|------------|--------------------------|------------|-----------|-----------|------------|-----------|------------|---------------|
|           |                            |                                |            | MIN                      | TYP        | MAX       | MIN       | MAX        | MIN       | MAX        |               |
| $V_{OH}$  | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OH} = -20\ \mu\text{A}$    | 2 V        | 1.9                      | 1.998      |           | 1.9       |            | 1.9       |            | V             |
|           |                            |                                | 4.5 V      | 4.4                      | 4.499      |           | 4.4       |            | 4.4       |            |               |
|           |                            |                                | 6 V        | 5.9                      | 5.999      |           | 5.9       |            | 5.9       |            |               |
|           |                            | $I_{OH} = -6\ \text{mA}$       | 4.5 V      | 3.98                     | 4.3        |           | 3.7       |            | 3.84      |            |               |
|           |                            | $I_{OH} = -7.8\ \text{mA}$     | 6 V        | 5.48                     | 5.8        |           | 5.2       |            | 5.34      |            |               |
| $V_{OL}$  | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OL} = 20\ \mu\text{A}$     | 2 V        |                          | 0.002      | 0.1       |           | 0.1        |           | 0.1        | V             |
|           |                            |                                | 4.5 V      |                          | 0.001      | 0.1       |           | 0.1        |           | 0.1        |               |
|           |                            |                                | 6 V        |                          | 0.001      | 0.1       |           | 0.1        |           | 0.1        |               |
|           |                            | $I_{OL} = 6\ \text{mA}$        | 4.5 V      |                          | 0.17       | 0.26      |           | 0.4        |           | 0.33       |               |
|           |                            | $I_{OL} = 7.8\ \text{mA}$      | 6 V        |                          | 0.15       | 0.26      |           | 0.4        |           | 0.33       |               |
| $I_I$     | DIR or $\overline{OE}$     | $V_I = V_{CC}$ or 0            | 6 V        |                          | $\pm 0.1$  | $\pm 100$ |           | $\pm 1000$ |           | $\pm 1000$ | nA            |
| $I_{OZ}$  | A or B                     | $V_O = V_{CC}$ or 0            | 6 V        |                          | $\pm 0.01$ | $\pm 0.5$ |           | $\pm 10$   |           | $\pm 5$    | $\mu\text{A}$ |
| $I_{CC}$  |                            | $V_I = V_{CC}$ or 0, $I_O = 0$ | 6 V        |                          |            | 8         |           | 160        |           | 80         | $\mu\text{A}$ |
| $C_i$     | DIR or $\overline{OE}$     |                                | 2 V to 6 V |                          | 3          | 10        |           | 10         |           | 10         | pF            |

## switching characteristics over recommended operating free-air temperature range, $C_L = 50\ \text{pF}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT)    | TO (OUTPUT) | $V_{CC}$ | $T_A = 25^\circ\text{C}$ |     |     | SN54HC645 |     | SN74HC645 |     | UNIT |
|-----------|-----------------|-------------|----------|--------------------------|-----|-----|-----------|-----|-----------|-----|------|
|           |                 |             |          | MIN                      | TYP | MAX | MIN       | MAX | MIN       | MAX |      |
| $t_{pd}$  | A or B          | B or A      | 2 V      |                          | 40  | 105 |           | 160 |           | 130 | ns   |
|           |                 |             | 4.5 V    |                          | 15  | 21  |           | 32  |           | 26  |      |
|           |                 |             | 6 V      |                          | 12  | 18  |           | 27  |           | 22  |      |
| $t_{en}$  | $\overline{OE}$ | A or B      | 2 V      |                          | 125 | 230 |           | 340 |           | 290 | ns   |
|           |                 |             | 4.5 V    |                          | 23  | 46  |           | 68  |           | 58  |      |
|           |                 |             | 6 V      |                          | 20  | 39  |           | 58  |           | 49  |      |
| $t_{dis}$ | $\overline{OE}$ | A or B      | 2 V      |                          | 74  | 200 |           | 300 |           | 250 | ns   |
|           |                 |             | 4.5 V    |                          | 25  | 40  |           | 60  |           | 50  |      |
|           |                 |             | 6 V      |                          | 21  | 34  |           | 51  |           | 43  |      |
| $t_t$     |                 | A or B      | 2 V      |                          | 20  | 60  |           | 90  |           | 75  | ns   |
|           |                 |             | 4.5 V    |                          | 8   | 12  |           | 18  |           | 15  |      |
|           |                 |             | 6 V      |                          | 6   | 10  |           | 15  |           | 13  |      |



# SN54HC645, SN74HC645

## OCTAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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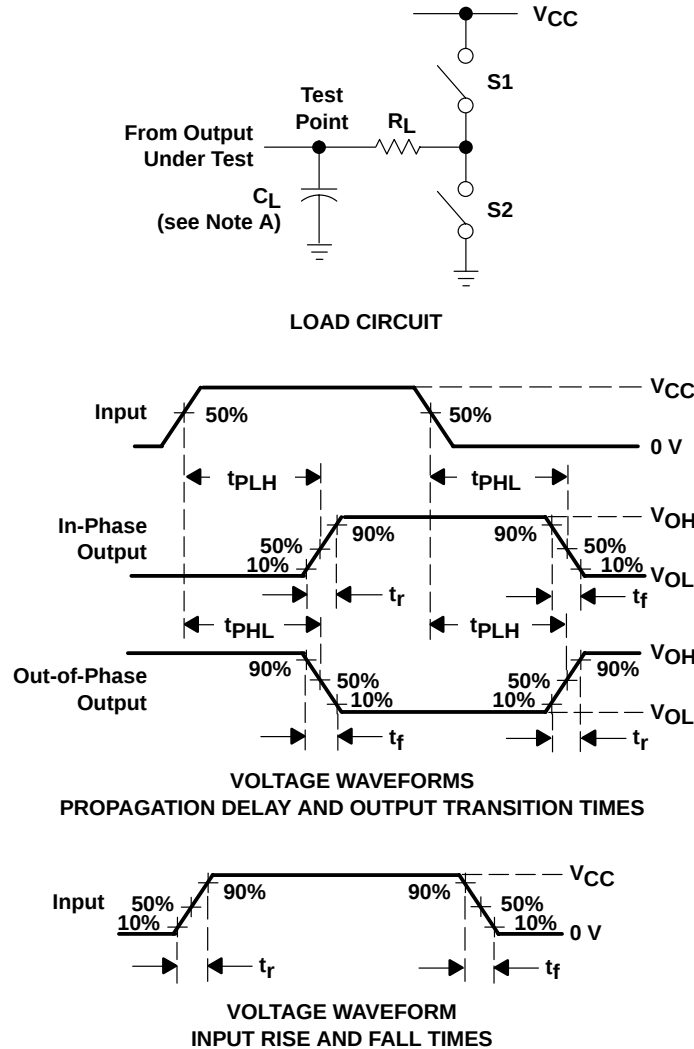
switching characteristics over recommended operating free-air temperature range,  $C_L = 150$  pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CC}$ | $T_A = 25^\circ\text{C}$ |     |     | SN54HC645 |     | SN74HC645 |     | UNIT |
|-----------|-----------------|----------------|----------|--------------------------|-----|-----|-----------|-----|-----------|-----|------|
|           |                 |                |          | MIN                      | TYP | MAX | MIN       | MAX | MIN       | MAX |      |
| $t_{pd}$  | A or B          | B or A         | 2 V      |                          | 54  | 135 |           | 200 |           | 170 | ns   |
|           |                 |                | 4.5 V    |                          | 18  | 27  |           | 40  |           | 34  |      |
|           |                 |                | 6 V      |                          | 15  | 23  |           | 34  |           | 29  |      |
| $t_{en}$  | $\overline{OE}$ | A or B         | 2 V      |                          | 150 | 270 |           | 405 |           | 335 | ns   |
|           |                 |                | 4.5 V    |                          | 31  | 54  |           | 81  |           | 67  |      |
|           |                 |                | 6 V      |                          | 25  | 46  |           | 69  |           | 56  |      |
| $t_t$     |                 | A or B         | 2 V      |                          | 45  | 210 |           | 315 |           | 265 | ns   |
|           |                 |                | 4.5 V    |                          | 17  | 42  |           | 63  |           | 53  |      |
|           |                 |                | 6 V      |                          | 13  | 36  |           | 53  |           | 45  |      |

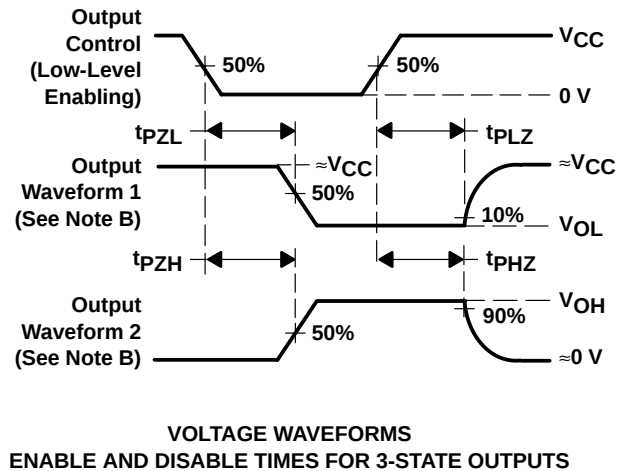
operating characteristics,  $T_A = 25^\circ\text{C}$

| PARAMETER |                                               | TEST CONDITIONS | TYP | UNIT |
|-----------|-----------------------------------------------|-----------------|-----|------|
| $C_{pd}$  | Power dissipation capacitance per transceiver | No load         | 40  | pF   |

## PARAMETER MEASUREMENT INFORMATION



| PARAMETER         | $R_L$        | $C_L$           | S1     | S2     |
|-------------------|--------------|-----------------|--------|--------|
| $t_{en}$          | 1 k $\Omega$ | 50 pF or 150 pF | Open   | Closed |
|                   |              |                 | Closed | Open   |
| $t_{dis}$         | 1 k $\Omega$ | 50 pF           | Open   | Closed |
|                   |              |                 | Closed | Open   |
| $t_{pd}$ or $t_t$ | --           | 50 pF or 150 pF | Open   | Open   |



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN54HC645J       | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | SN54HC645J              | <a href="#">Samples</a> |
| SN74HC645DW      | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | HC645                   | <a href="#">Samples</a> |
| SN74HC645DWR     | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | HC645                   | <a href="#">Samples</a> |
| SN74HC645N       | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | NIPDAU                  | N / A for Pkg Type   | -40 to 85    | SN74HC645N              | <a href="#">Samples</a> |
| SNJ54HC645FK     | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD                        | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | SNJ54HC<br>645FK        | <a href="#">Samples</a> |
| SNJ54HC645J      | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | SNJ54HC645J             | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54HC645, SN74HC645 :**

- Catalog: [SN74HC645](#)
- Military: [SN54HC645](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


|    |                                                           |
|----|-----------------------------------------------------------|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC645DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.0    | 2.7     | 12.0    | 24.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC645DWR | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF<br>TERMINALS<br>** | A                |                  | B                |                  |
|---------------------------|------------------|------------------|------------------|------------------|
|                           | MIN              | MAX              | MIN              | MAX              |
| 20                        | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                        | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                        | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                        | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                        | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                        | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



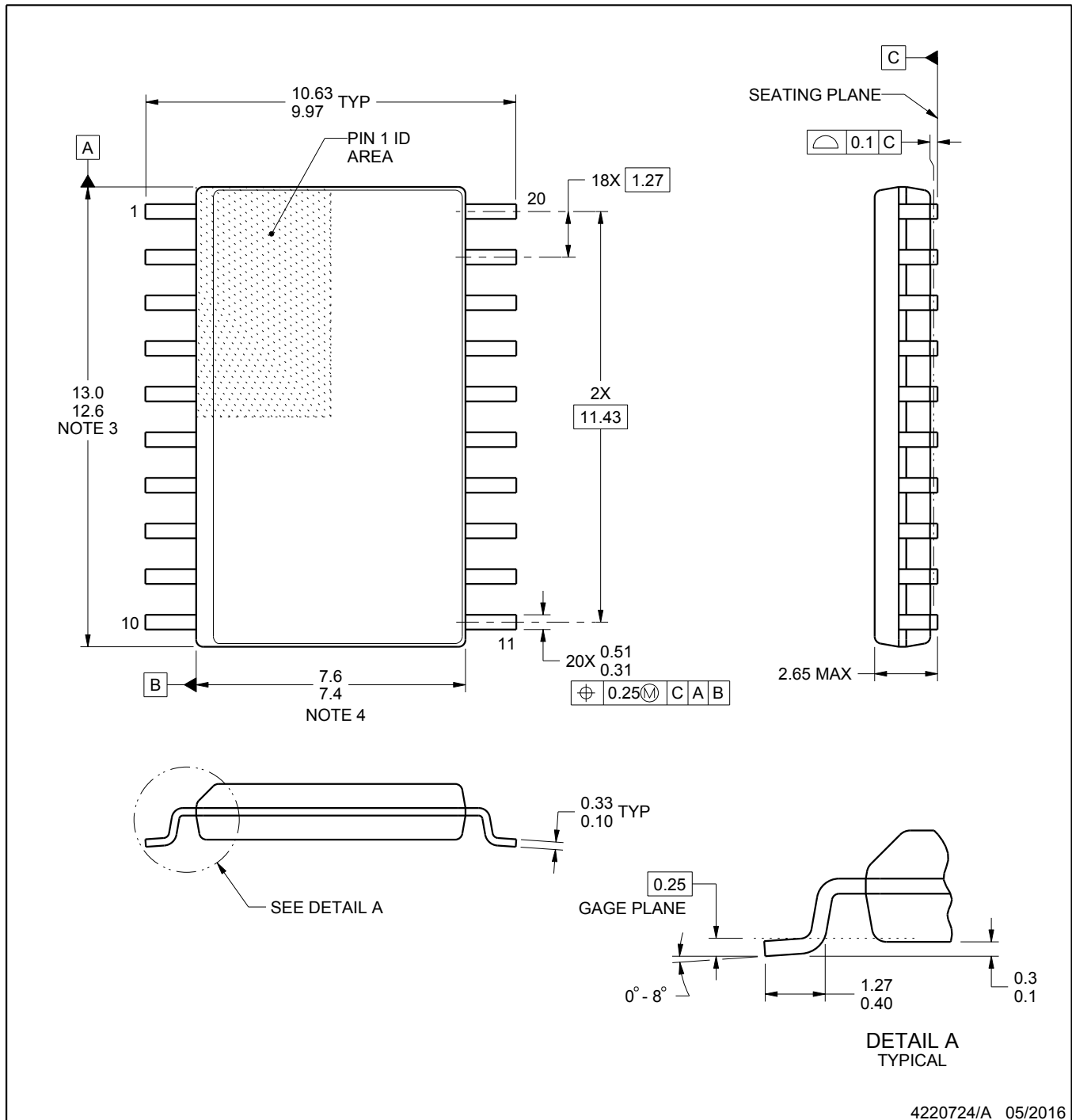
| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

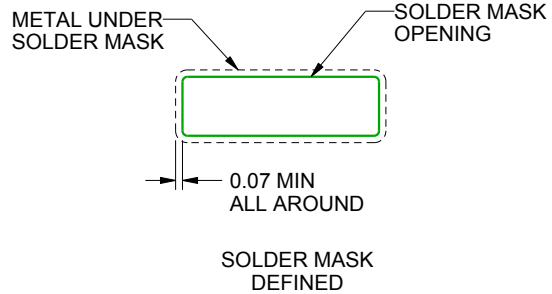
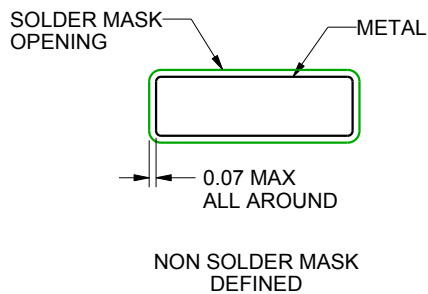
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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