0.25 dB LSB, 7-Bit, Silicon Digital Attenuator, 0.1 GHz to 6.0 GHz

Data Sheet **HMC1119**

FEATURES

- Attenuation range: 0.25 dB LSB steps to 31.75 dB
- Low insertion loss:
  - 1.1 dB at 1.0 GHz
  - 1.3 dB at 2.0 GHz
- Typical step error: less than ±0.1 dB
- Excellent attenuation accuracy: less than ±0.2 dB
- Low phase shift error: 6° phase shift at 1.0 GHz
- Safe state transitions
- High linearity
  - 1 dB compression (P1dB): 31 dBm typical
  - Input third-order intercept (IP3): 54 dBm typical
- RF settling time (0.05 dB final RF output): 250 ns
- Single supply operation: 3.3 V to 5.0 V
- ESD rating: Class 2 (2 kV human body model (HBM))
- 24-lead, 4 mm × 4 mm LFCSP package: 16 mm²

FUNCTIONAL BLOCK DIAGRAM

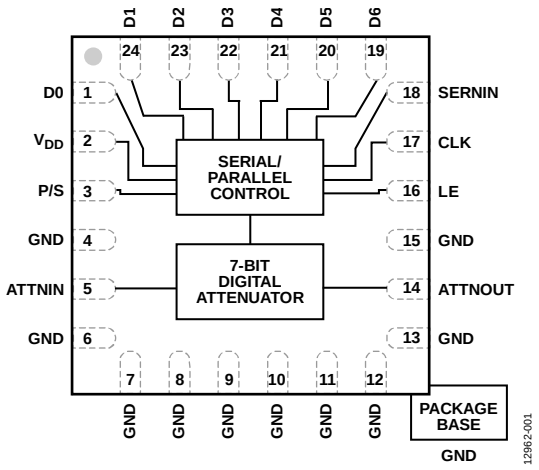

Figure 1.

APPLICATIONS

- Cellular infrastructure
- Microwave radios and very small aperture terminals (VSATs)
- Test equipment and sensors
- IF and RF designs

GENERAL DESCRIPTION

The HMC1119 is a broadband, highly accurate, 7-bit digital attenuator, operating from 0.1 GHz to 6.0 GHz with 31.5 dB attenuation control range in 0.25 dB steps.

The HMC1119 is implemented in a silicon process, offering very fast settling time, low power consumption, and high ESD robustness. The device features safe state transitions and is optimized for excellent step accuracy and high linearity over frequency and temperature range. The RF input and output are internally matched to 50 Ω and do not require any external matching components. The design is bidirectional; therefore, the RF input and output are interchangeable.

The HMC1119 has an on-chip regulator that can support a wide supply operating range from 3.3 V to 5.0 V with no performance change in electrical characteristics. The HMC1119 incorporates a driver that supports serial (3-wire) and parallel controls of the attenuator.

The HMC1119 comes in a RoHS-compliant, compact, 4 mm × 4 mm LFCSP package.

A fully populated evaluation board is available.

Rev. C
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REVISION HISTORY

4/2018—Rev. B to Rev C

Changes to Figure 23 ... 12
Change to PCB Description, Table 7 ... 13
Updated Outline Dimensions ... 15

9/2017—Rev. A to Rev. B

Changed CP-24-16 to HCP-24-3 ... Throughout
Updated Outline Dimensions ... 15
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8/2017—Rev. 0 to Rev. A

Added Timing Specifications Section ... 4
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Moved Parallel Control Interface Section, Direct Parallel Mode Section, Latched Parallel Mode Section, Power-Up Sequence Section, and Power-Up States Section ... 12
Updated Outline Dimensions ... 15

9/2016—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{DD} = 3.3 V to 5.0 V, T_A = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		0.1		6.0	GHz
INSERTION LOSS	0.1 GHz to 1.0 GHz		1.1	1.8	dB
	0.1 GHz to 2.0 GHz		1.3	2.0	dB
	0.1 GHz to 4.0 GHz		1.6	2.3	dB
	0.1 GHz to 6.0 GHz		2.0	2.8	dB
ATTENUATION	0.2 GHz to 6.0 GHz				
Range	Delta between minimum and maximum attenuation states		31.75		dB
Accuracy	Referenced to insertion loss; all attenuation states	−(0.05 + 4% of attenuation setting)		+(0.05 + 4% of attenuation setting)	dB
Step Error	All attenuation states		±0.1		dB
Overshoot	Between all attenuation states		≤0.1		dB
RETURN LOSS	All attenuation states				
ATTNIN, ATTNOUT	1.0 GHz		23		dBm
	2.0 GHz		22		dBm
	4.0 GHz		19		dBm
	6.0 GHz		17		dBm
RELATIVE PHASE	1.0 GHz		6		Degrees
	2.0 GHz		18		Degrees
	4.0 GHz		38		Degrees
	6.0 GHz		58		Degrees
SWITCHING CHARACTERISTICS					
t_{RISE}, t_{FALL}	10%/90% RF output		60		ns
t_{ON}, t_{OFF}	50% CTL to 10%/90% RF output		150		ns
Settling Time	50% CTL to 0.05 dB final RF output		250		ns
	50% CTL to 0.10 dB final RF output		200		ns
INPUT LINEARITY	All attenuation states, 0.2 GHz to 6 GHz				
0.1 dB Compression (P0.1dB)			30		dBm
1 dB Compression (P1dB)			31		dBm
Input Third-Order Intercept (IP3)	Two-tone input power = 16 dBm/tone, Δf = 1 MHz		54		dBm
SUPPLY CURRENT (I_{DD})	V_{DD} = 3.3 V		0.3		mA
	V_{DD} = 5.0 V		0.6		mA
CONTROL VOLTAGE THRESHOLD	<1 µA typical				
Low	V_{DD} = 3.3 V	0		0.5	V
	V_{DD} = 5.0 V	0		0.8	V
High	V_{DD} = 3.3 V	2.0		3.3	V
	V_{DD} = 5.0 V	3.5		5.0	V
RECOMMENDED OPERATING CONDITIONS					
Supply Voltage Range (V_{DD})		3.0		5.4	V
Digital Control Voltage Range	For P/S, CLK, SERNIN, LE, D0 to D6 pins	0		V_{DD}	V
RF Input Power	All attenuation states, T_{CASE} = 85°C			24	dBm
Case Temperature (T_{CASE})		−40		+85	°C

TIMING SPECIFICATIONS

See Figure 23 and Figure 24 for the timing diagrams.

Table 2.

Parameter	Description	Min	Typ	Max	Unit
t_{SCK}	Minimum serial period, see Figure 23	70			ns
t_{CS}	Control setup time, see Figure 23	15			ns
t_{CH}	Control hold time, see Figure 23		20		ns
t_{LN}	LE setup time, see Figure 23	15			ns
t_{LEW}	Minimum LE pulse width, see Figure 24		10		ns
t_{LES}	Minimum LE pulse spacing, see Figure 23		630		ns
t_{CKN}	Serial clock hold time from LE, see Figure 23		0		ns
t_{PH}	Hold time, see Figure 24		10		ns
t_{PS}	Setup time, see Figure 24		2		ns

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
RF Input Power (T_{CASE} = 85°C)	25 dBm
Digital Control Inputs (P/S, CLK, SERNIN, LE, D0 to D6)	−0.3 V to V_{DD} + 0.5 V
Supply Voltage (V_{DD})	−0.3 V to +5.5 V
Continuous Power Dissipation (P_{DISS})	0.31 W
Thermal Resistance (at Maximum Power Dissipation)	156°C/W
Temperature	
Channel Temperature	135°C
Storage	−65°C to +150°C
Maximum Reflow Temperature	260°C (MSL3 Rating)
ESD Sensitivity (HBM)	2 kV (Class 2)

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

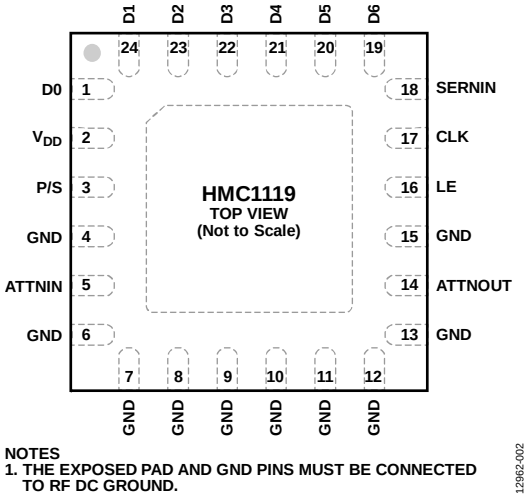

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 19 to 24	D0, D6 to D1	Parallel Control Voltage Inputs. These pins attain the required attenuation (see Table 6). There is no internal pull-up or pull-down on these pins; therefore, these pins must always be kept at a valid logic level (V_{IH} or V_{IL}) and must not be left floating.
2	V_{DD}	Supply Voltage Pin.
3	P/S	Parallel/Serial Control Input. There is no internal pull-up or pull-down on this pin; therefore, this pin must always be kept at a valid logic level (V_{IH} or V_{IL}) and must not be left floating. For parallel mode, set Pin 3 to low; for serial mode, set Pin 3 to high.
4, 6 to 13, 15	GND	Ground. The package bottom has an exposed metal pad that must connect to the printed circuit board (PCB) RF/dc ground. See Figure 4 for the GND interface schematic.
5	ATTNIN	Attenuator Input. This pin is dc-coupled and matched to 50 Ω. A blocking capacitor is required. Select the value of the capacitor based on the lowest frequency of operation. See Figure 5.
14	ATTNOUT	Attenuator Output. This pin is dc-coupled and matched to 50 Ω.A blocking capacitor is required. Select the value of the capacitor based on the lowest frequency of operation. See Figure 5.
16	LE	Serial/Parallel Interface Latch Enable Input. There is no internal pull-up or pull-down on this pin; therefore, this pin must always be kept at a valid logic level (V_{IH} or V_{IL}) and must not be left floating. See the Theory of Operation section for more information.
17	CLK	Serial Interface Clock Input. There is no internal pull-up or pull-down on this pin; therefore, this pin must always be kept at a valid logic level (V_{IH} or V_{IL}) and must not be left floating. See the Theory of Operation section for more information.
18	SERNIN	Serial interface Data Input. There is no internal pull-up or pull-down on this pin; therefore, this pin must always be kept at a valid logic level (V_{IH} or V_{IL}) and must not be left floating. See the Theory of Operation section for more information.
	EPAD	Exposed Pad. The exposed pad must be connected to RF/dc ground.

INTERFACE SCHEMATICS

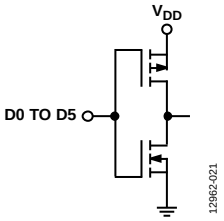

Figure 3. D0 to D6 Interface

Figure 4. GND Interface

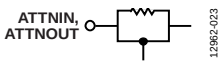

Figure 5. ATTIN and ATTOUT Interface

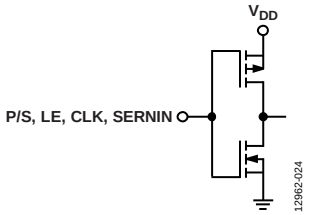

Figure 6. P/S, LE, CLK, and SERNIN Interface

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, STATE ERROR, STEP ERROR, AND RELATIVE PHASE

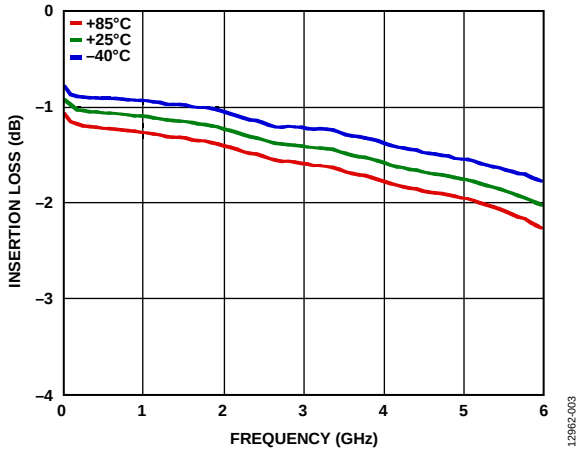

Figure 7. Insertion Loss vs. Frequency at Various Temperatures

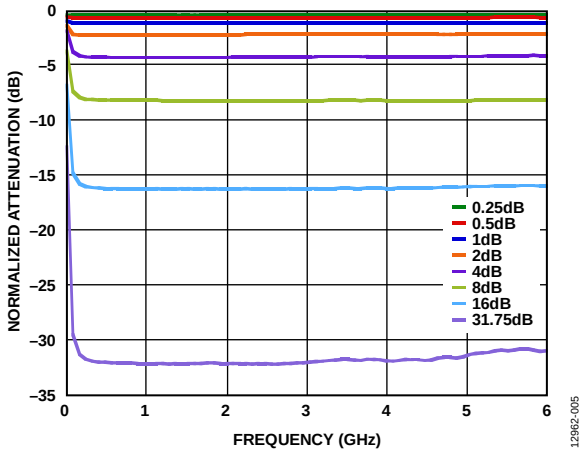

Figure 10. Normalized Attenuation (Major States Only)

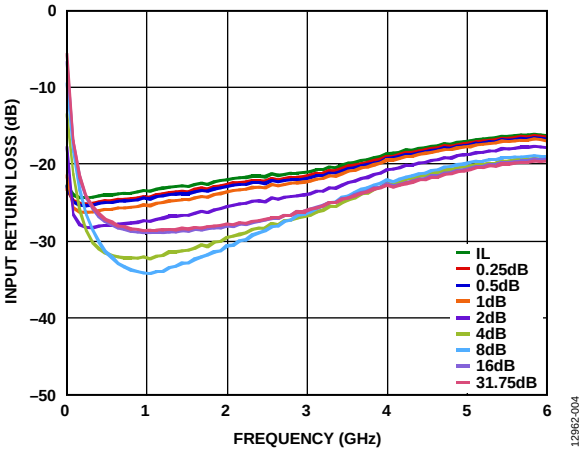

Figure 8. Input Return Loss (Major States Only)

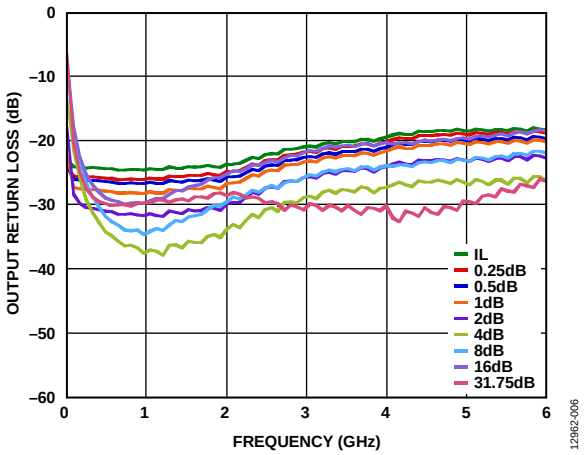

Figure 11. Output Return Loss (Major States Only)

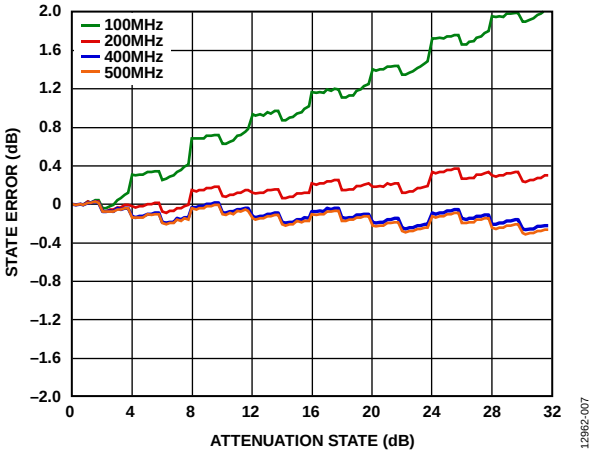

Figure 9. State Error vs. Attentuation State, 0.1 GHz to 0.5 GHz

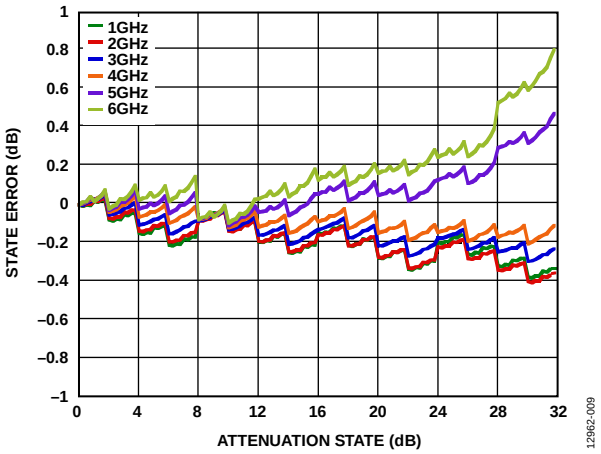

Figure 12. State Error vs. Attentuation State, 1 GHz to 6 GHz

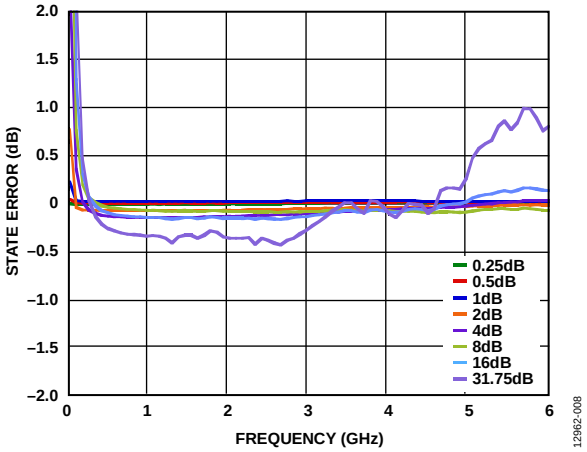

Figure 13. State Error vs. Frequency, Major States Only

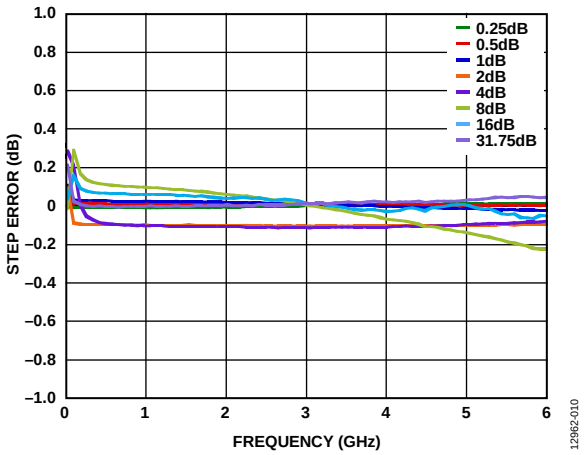

Figure 15. Step Error vs. Frequency, Major States Only

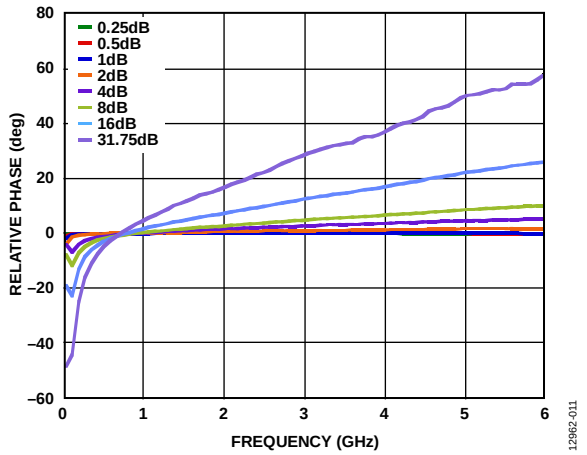

Figure 14. Relative Phase vs. Frequency, Major States Only

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

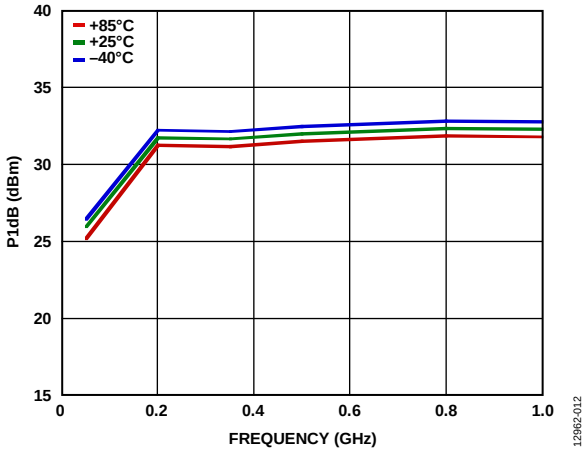

Figure 16. P1dB vs. Frequency at Various Temperatures, Minimum Attenutation State, 0.05 GHz to 1 GHz

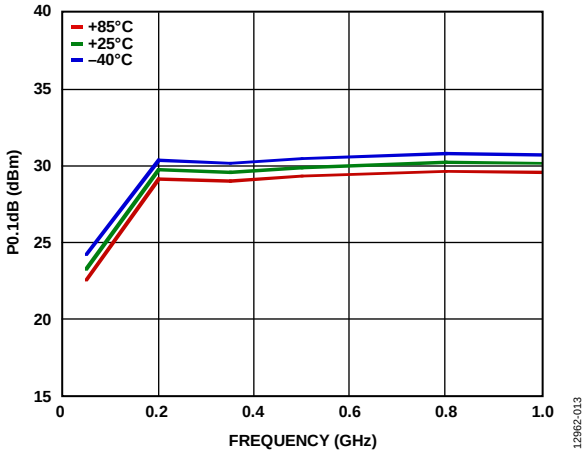

Figure 17. P0.1dB vs. Frequency at Various Temperatures, Minimum Attenutation State, 0.05 GHz to 1 GHz

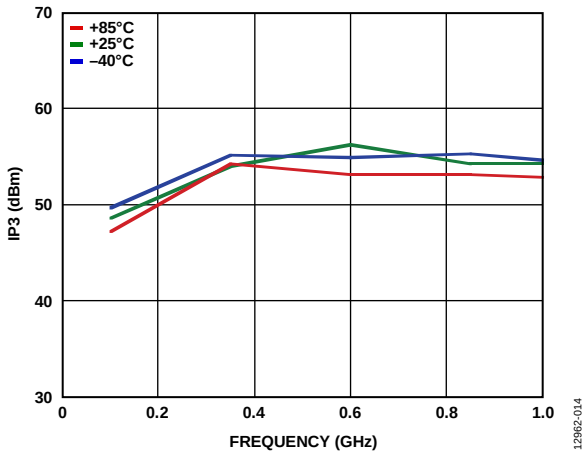

Figure 18. IP3 vs. Frequency at Various Temperatures, Minimum Attenutation State, 0.1 GHz to 1 GHz

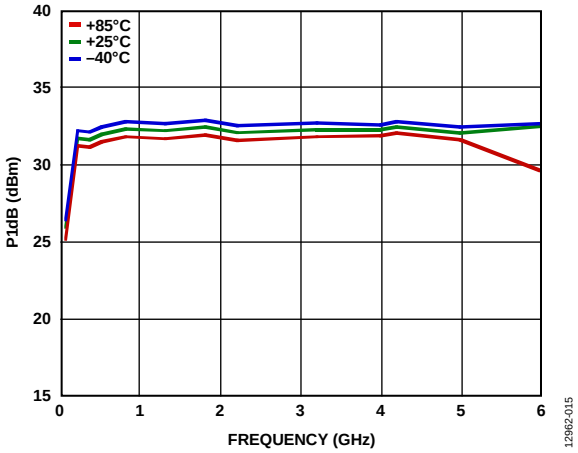

Figure 19. P1dB vs. Frequency at Various Temperatures, Minimum Attenutation State, 0.05 GHz to 6 GHz

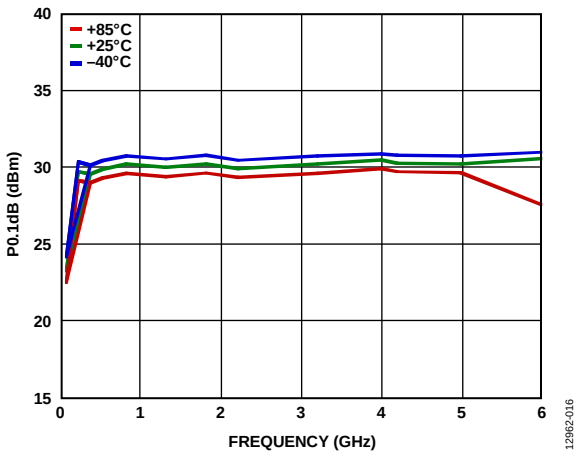

Figure 20. P0.1dB vs. Frequency at Various Temperatures, Minimum Attenutation State, 0.05 GHz to 6 GHz

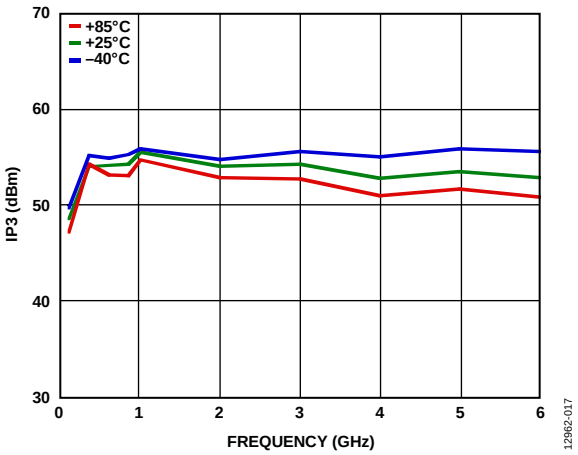

Figure 21. IP3 vs. Frequency at Various Temperatures, Minimum Attenutation State, 0.1 GHz to 6 GHz

THEORY OF OPERATION

The HMC1119 incorporates a 7-bit fixed attenuator array that offers an attenuation range of 0.25 dB to 31.75 dB, with 0.25 dB steps. An integrated driver provides both serial and parallel mode control of the attenuator array (see Figure 22).

The HMC1119 can be in either serial or parallel mode control by setting the P/S pin to high or low, respectively (see Table 5). The 7-bit data, loaded in either serial or parallel mode, then latches with the control signal, LE, to determine the attenuator value.

Table 5. Mode Selection Table[1]

P/S Pin State	Control Mode
Low	Parallel
High	Serial

[1] The P/S pin must always be kept at a valid logic level (V_{IH} or V_{IL}) and must not be left floating.

SERIAL CONTROL INTERFACE

The HMC1119 utilizes a 3-wire serial to parallel (SPI) configuration, as shown in the serial mode timing diagram (see Figure 23): serial data input (SERNIN), clock (CLK), and latch enable (LE). The serial control interface activates when the P/S pin is set to high.

In serial mode, the 7-bit SERNIN data is clocked MSB first on rising CLK edges into the shift register; then, LE must be toggled high to latch the new attenuation state into the device. The LE must be set low to clock a set of 7-bit data into the shift register because CLK is masked to prevent the attenuator value from changing if LE is kept high.

In serial mode operation, both the serial control inputs (LE, CLK, SERNIN) and the parallel control inputs (D0 to D6) must always be kept at a valid logic level (V_{IH} or V_{IL}) and must not be left floating. It is recommended to connect the parallel control inputs to ground and to use pull-down resistors on all serial control input lines if the device driving these input lines goes high impedance during hibernation.

RF INPUT OUTPUT

The attenuator in the HMC1119 is bidirectional; the ATTNIN and ATTNOUT pins are interchangeable as the RF input and output ports. The attenuator is internally matched to 50 Ω at both input and output; therefore, no external matching components are required. The RF pins are dc-coupled; therefore, dc blocking capacitors are required on RF lines.

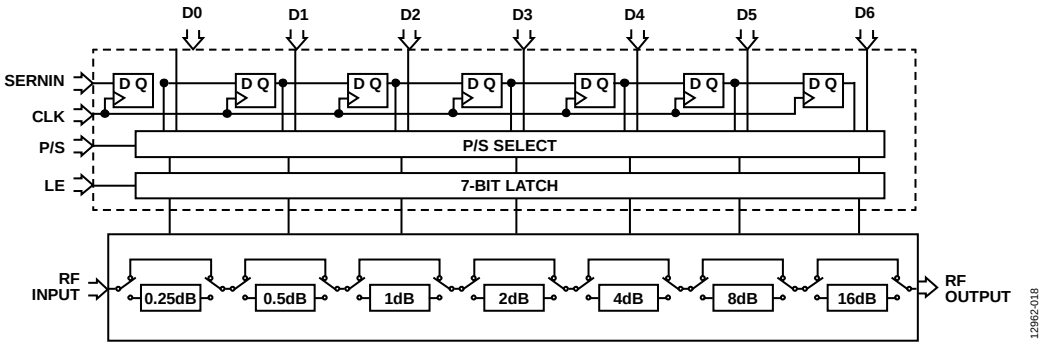

Figure 22. Attenuator Array Functional Block Diagram

Table 6. Truth Table

Digital Control Input[1]							
D6	D5	D4	D3	D2	D1	D0	Attenuation State (dB)
Low	Low	Low	Low	Low	Low	Low	0 (reference)
Low	Low	Low	Low	Low	Low	High	0.25
Low	Low	Low	Low	Low	High	Low	0.5
Low	Low	Low	Low	High	Low	Low	1.0
Low	Low	Low	High	Low	Low	Low	2.0
Low	Low	High	Low	Low	Low	Low	4.0
Low	High	Low	Low	Low	Low	Low	8.0
High	Low	Low	Low	Low	Low	Low	16.0
High	High	High	High	High	High	High	31.75

[1] Any combination of the control voltage input states shown in Table 6 provides an attenuation equal to the sum of the bits selected.

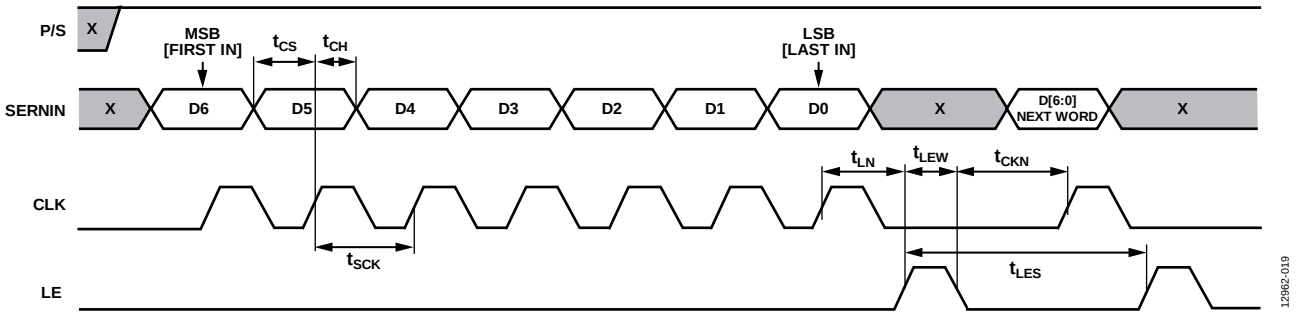

Figure 23. Serial Control Timing Diagram

PARALLEL CONTROL INTERFACE

The parallel control interface has seven digital control input lines (D6 to D0) to set the attenuation value. D6 is the most significant bit (MSB) that selects the 16 dB attenuator stage, and D0 is the least significant bit (LSB) that selects the 0.25 dB attenuator stage (see Figure 22).

In parallel mode operation, both the serial control inputs (LE, CLK, SERNIN) and the parallel control inputs (D0 to D6) must always be kept at a valid logic level (V_{IH} or V_{IL}) and must not be left floating. It is recommended to connect the serial control inputs to ground and to use pull-down resistors on all parallel control input lines if the device driving these input lines goes high impedance during hibernation.

Setting P/S to low enables parallel mode. There are two modes of parallel operation: direct parallel mode and latched parallel mode.

Direct Parallel Mode

For direct parallel mode, the latch enable (LE) pin must be kept high. Change the attenuation state using the control voltage inputs (D0 to D6) directly. This mode is ideal for manual control of the attenuator and using hardware, switches, or a jumper.

Latched Parallel Mode

The latch enable (LE) pin must be low when changing the control voltage inputs (D0 to D6) to set the attenuation state. When the desired state is set, LE must be toggled high to transfer the 7-bit data to the bypass switches of the attenuator array, then toggled low to latch the change into the device (see Figure 24).

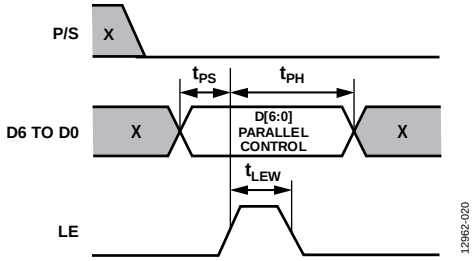

Figure 24. Latched Parallel Mode Timing Diagram

POWER-UP SEQUENCE

The ideal power-up sequence is as follows:

1. Power up GND.
2. Power up V_{DD}.
3. Power up the digital control inputs (the relative order of the digital control inputs is not important).
4. Power up the RF input.

For latched parallel mode operation, LE must be toggled. The relative order of the digital inputs is not important as long as the inputs are powered up after GND and V_{DD}.

Power-Up States

The logic state of the device is at maximum attenuation when, at power up, LE is set to low. The attenuator latches in the desired power-up state approximately 200 ms after power up.

APPLICATIONS INFORMATION

EVALUATION PRINTED CIRCUIT BOARD

The schematic of the evaluation board, EV2HMC1119LP4M, is shown in Figure 25. The PCB is four-layer material with a copper thickness of 0.7 mils on each layer. Each copper layer is separated with a dielectric material. The top dielectric material is 10-mil RO4350 with a typical dielectric constant of 3.48. The middle and bottom dielectric materials are FR-4 material, used for mechanical strength and to meet the overall board thickness of approximately 62 mils, which allows SMA connectors to be slipped in at board edges.

All RF and dc traces are routed on the top copper layer. The RF transmission lines are designed using coplanar waveguide model (CPWG) with a width of 18 mils, spacing of 17 mils, and dielectric thickness of 10 mils to maintain 50 Ω characteristic impedance. The inner and bottom layers are solid ground planes. For optimal electrical and thermal performance, an ample number of vias are populated around the transmission lines and under the package exposed pad. The evaluation board layout serves as a recommendation for the optimal performance on both electrical and thermal aspects.

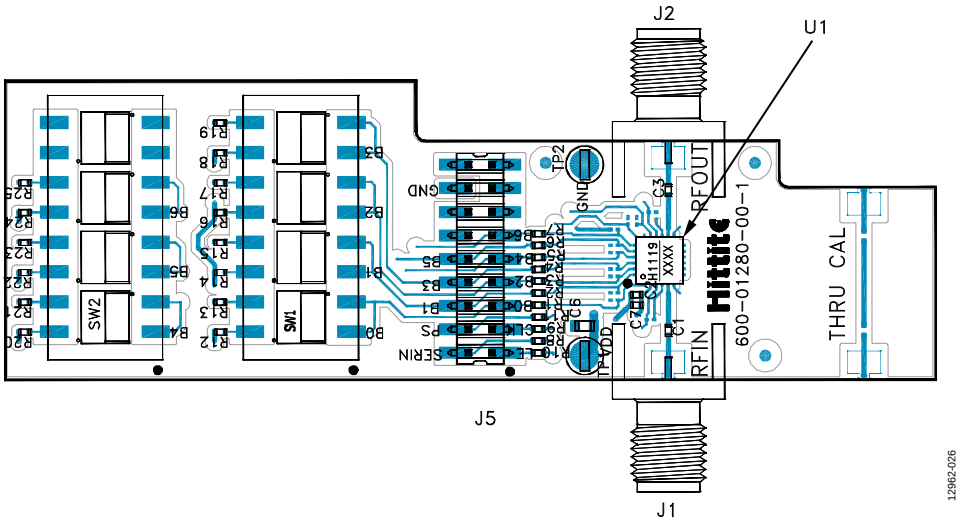

Figure 25. EV2HMC1119LP4M Evaluation PCB

Table 7. Bill of Materials

Item	Value[1]	Description	Manufacturer[2]
J1, J2		PCB mount SMA connector	
J3		18-pin dc connector	
TP1, TP2		Through hole mount test point	
C1, C3	100 pF	Capacitor, 0402 package	
C6	10 µF	Capacitor, 0603 package	
C7	1000 pF	Capacitor, 0402 package	
R1 to R11	0 Ω	Resistor, 0402 package	
R12 to R25	100 kΩ	Resistor, 0402 package	
SW1, SW2		SPDT four-position DIP switch	
U1		HMC1119 digital attenuator	Analog Devices, Inc.
PCB[3]		600-01280-00-1 evaluation PCB	EV2HMC1119LP4M[4] from Analog Devices

[1] Blank cells in the Value column indicate that there is no specific value recommendation for the listed component.
[2] Blank cells in the Manufacturer column indicate that there is no specific manufacturer recommendation for the listed component.
[3] Circuit board material is Arlon 25FR.
[4] Reference this number when ordering the full evaluation PCB. See the Ordering Guide section.

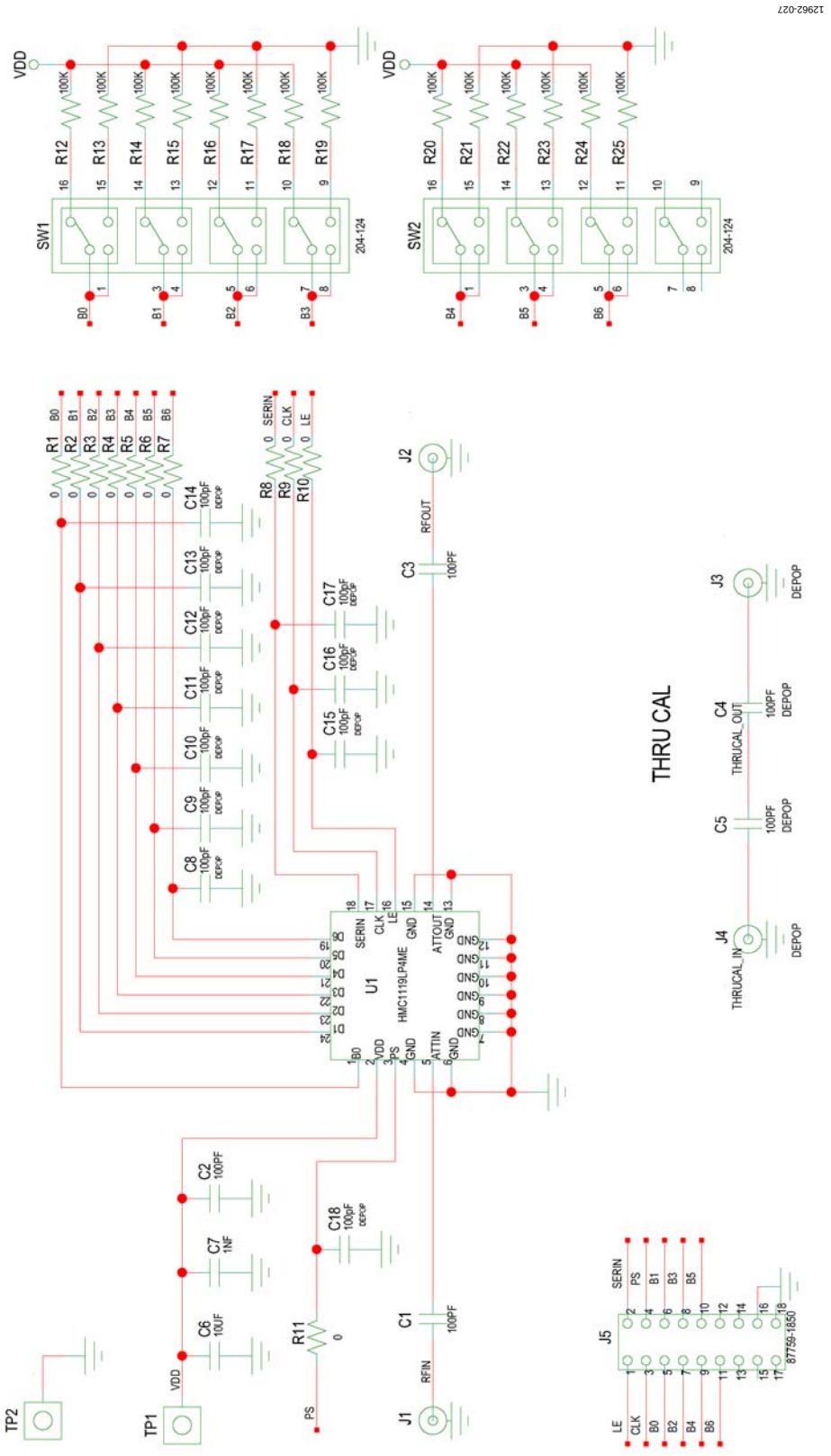

Figure 26. Applications Circuit

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS

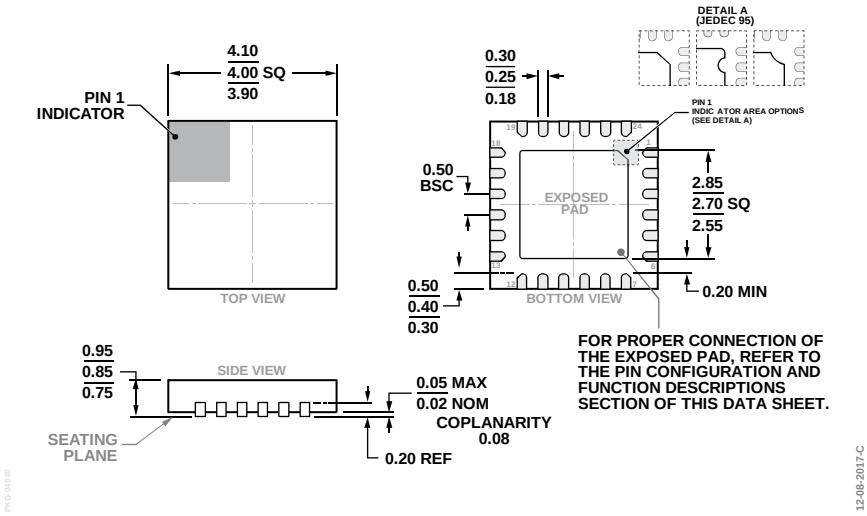

Figure 27. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.85 mm Package Height
(HCP-24-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description	Package Option
HMC1119LP4ME	−40°C to +85°C	MSL3	24-Lead Lead Frame Chip Scale Package [LFCSP]	HCP-24-3
HMC1119LP4METR	−40°C to +85°C	MSL3	24-Lead Lead Frame Chip Scale Package [LFCSP]	HCP-24-3
EV2HMC1119LP4M			Evaluation Board	

[1] All models are RoHS compliant.
[2] See the Absolute Maximum Ratings section.

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D12962-0-4/18(C)