NC7WZ38

TinyLogic UHS Dual 2-Input NAND Gate (Open Drain Output)

ON Semiconductor®

www.onsemi.com

Description

The NC7WZ38 is a dual 2−Input NAND Gate with open drain output stage from ON Semiconductor's Ultra High Speed Series of TinyLogic. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.65 V to 5.5 V V_{CC} range. The inputs and output are high impedance when V_{CC} is 0 V. Inputs tolerate voltages up to 5.5 V independent of V_{CC} operating voltage. The open drain output stage will tolerate voltages up to 5.5 V independent of V_{CC} when in the high impedance state.

Features

- Space Saving US8 Surface Mount Package
- MicroPak™ Pb−Free Leadless Package
- Open Drain Output Stage for OR Tied Applications
- Ultra High Speed: t_{PD} 2.2 ns Typ. into 50 pF at 5 V V_{CC}
- High Output Sink Drive: ±24 mA at 3 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V to 5.5 V
- Matches the Performance of LCX when Operated at 3.3 V V_{CC}
- Power Down High Impedance Inputs / Output
- Overvoltage Tolerant Inputs Facilitate 5 V to 3 V Translation
- Patented Noise / EMI Reduction Circuitry Implemented
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

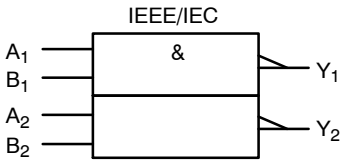
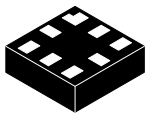


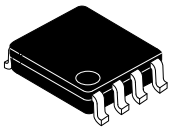
Figure 1. Logic Symbol

MARKING DIAGRAMS

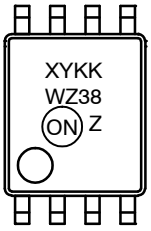


UQFN8
1.6X1.6, 0.5P
CASE 523AY





US8
CASE 846AN



U5, WZ38 = Specific Device Code
KK = 2−Digit Lot Run Traceability Code
XY = 2−Digit Date Code Format
Z = Assembly Plant Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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Connection Diagram

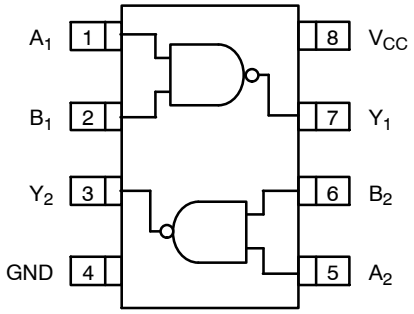


Figure 2. Connection Diagram (Top View)

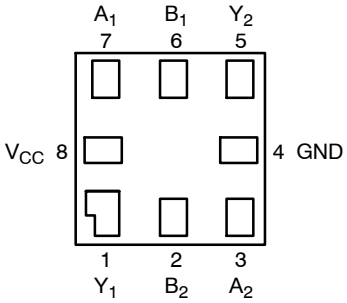
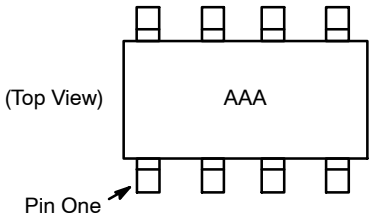


Figure 4. Pad Assignments for MicroPak (Top Thru View)



AAA represents Product Code Top Mark – see ordering code

NOTE: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Figure 3. Pin One Orientation Diagram

PIN DESCRIPTIONS

Pin Names	Description
A_n, B_n	Inputs
Y_n	Output

FUNCTION TABLE ($Y = \overline{AB}$)

Inputs		Output
A	**B**	**Y**
L	L	*H
L	H	*H
H	L	*H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level
*H = HIGH Impedance Output State (Open Drain)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		−0.5	6.5	V
V_{IN}	DC Input Voltage		−0.5	6.5	V
V_{OUT}	DC Output Voltage		−0.5	6.5	V
I_{IK}	DC Input Diode Current	V_{IN} < −0.5 V	−	−50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < −0.5 V	−	−50	mA
I_{OUT}	DC Output Current		−	±50	mA
I_{CC} / I_{GND}	DC V_{CC} / GND Current		−	±100	mA
T_{STG}	Storage Temperature		−65	+150	°C
T_J	Junction Temperature under Bias		−	150	°C
T_L	Junction Lead Temperature (Soldering, 10 Seconds)		−	260	°C
P_D	Power Dissipation @ +85°C		−	250	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage Operating		1.65	5.5	V
	Supply Voltage Data Retention		1.5	5.5	
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		−40	+85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 1.8 V ±0.15 V, 2.5 V ±0.2 V	0	20	ns/V
		V_{CC} = 3.3 V ±0.3 V	0	10	
		V_{CC} = 5.0 V ±0.5 V	0	5	
θ_{JA}	Thermal Resistance		−	250	°C/W

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTICAL CHARACTERISTICS

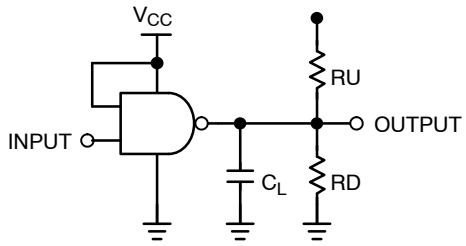
Symbol	Parameter	V_{CC} (V)	Conditions		T_A = +25°C			T_A = −40 to +85°C		Unit
					Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage	1.65 to 1.95			0.65 V_{CC}	–	–	0.65 V_{CC}	–	V
		2.3 to 5.5			0.7 V_{CC}	–	–	0.7 V_{CC}	–	
V_{IL}	LOW Level Input Voltage	1.65 to 1.95			–	–	0.35 V_{CC}	–	0.35 V_{CC}	V
		2.3 to 5.5			–	–	0.3 V_{CC}	–	0.3 V_{CC}	
I_{LKG}	HIGH Level Output Leakage	5.5	V_{IN} = V_{IL} V_{OUT} = V_{CC} or GND		–	–	±5	–	±10	μA
V_{OL}	LOW Level Output Voltage	1.65	V_{IN} = V_{IH}	I_{OL} = 100 μA	–	0.0	0.1	–	0.1	V
		2.3			–	0.0	0.1	–	0.1	
		3.0			–	0.0	0.1	–	0.1	
		4.5			–	0.0	0.1	–	0.1	
		1.65		I_{OL} = 4 mA	–	0.08	0.24	–	0.24	
		2.3		I_{OL} = 8 mA	–	0.10	0.3	–	0.3	
		3.0		I_{OL} = 16 mA	–	0.15	0.4	–	0.4	
		3.0		I_{OL} = 24 mA	–	0.22	0.55	–	0.55	
		4.5		I_{OL} = 32 mA	–	0.22	0.55	–	0.55	
I_{IN}	Input Leakage Current	5.5	V_{IN} = 5.5 V, GND		–	–	±0.1	–	±1	μA
I_{OFF}	Power Off Leakage Current	0.0	V_{IN} or V_{OUT} = 5.5 V		–	–	1	–	10	μA
I_{CC}	Quiescent Supply Current	1.65 to 5.5	V_{IN} = 5.5 V, GND		–	–	1	–	10	μA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C			T_A = −40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PZL}	Propagation Delay (Figure 5, 7)	1.8 ±0.15	C_L = 50 pF, RU = 500 Ω, RD = 500 Ω, V_I = 2 x V_{CC}	–	5.2	9.2	–	9.6	ns
		2.5 ±0.2		–	3.5	5.7	–	6.1	
		3.3 ±0.3		–	2.8	4.1	–	4.5	
		5.0 ±0.5		–	2.2	3.4	–	3.6	
t_{PLZ}	Propagation Delay (Figure 5, 7)	1.8 ±0.15	C_L = 50 pF, RU = 500 Ω, RD = 500 Ω, V_I = 2 x V_{CC}	–	4.6	9.2	–	9.6	ns
		2.5 ±0.2		–	3.2	5.7	–	6.1	
		3.3 ±0.3		–	2.4	4.1	–	4.5	
		5.0 ±0.5		–	1.6	3.4	–	3.6	
C_{IN}	Input Capacitance	0		–	2.5	–	–	–	pF
C_{OUT}	Output Capacitance	0		–	4.2	–	–	–	pF
C_{PD}	Power Dissipation Capacitance (Figure 6)	3.3	(Note 2)	–	7	–	–	–	pF
		5.0		–	9	–	–	–	

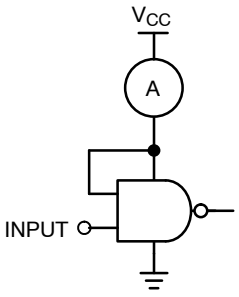
2. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (see Figure 6) C_{PD} is related to I_{CCD} dynamic operating current by the expression: I_{CCD} = (C_{PD}) (V_{CC}) (f_{IN}) + (I_{CC}static).

AC Loading and Waveforms



C_L includes load and stray capacitance
Input PRR = 1.0 MHz, t_W = 500 ns

Figure 5. AC Test Circuit



Input = AC Waveform; t_r = t_f = 1.8 ns;
PRR = 10 MHz; Duty Cycle = 50%.

Figure 6. I_{CCD} Test Circuit

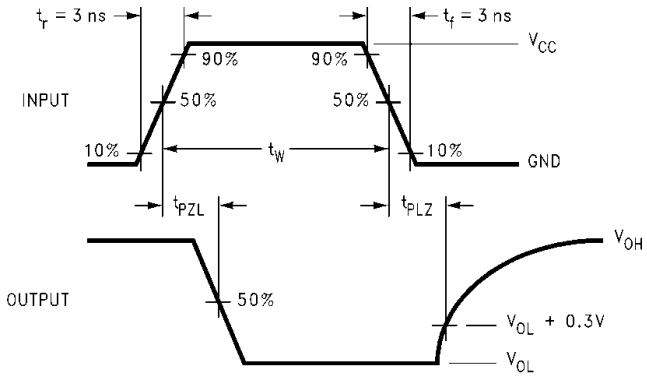


Figure 7. AC Waveforms

ORDERING INFORMATION

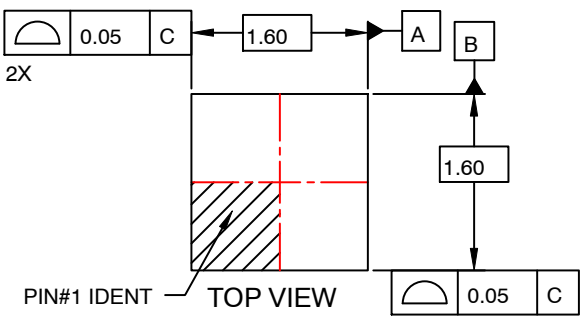
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NC7WZ38L8X	U5	8−Lead MicroPak, 1.6 mm Wide (Pb−Free)	5000 / Tape & Reel

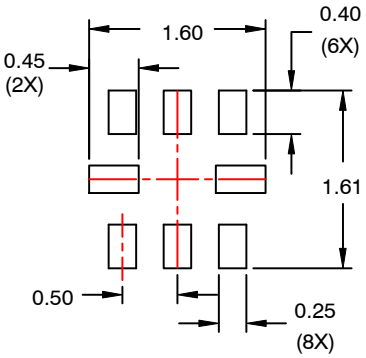
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
3. Pb−Free package per JEDEC J−STD−020B.

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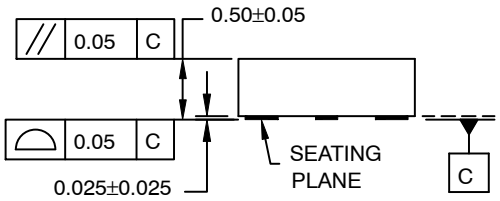
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RECOMMENDED
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SIDE VIEW

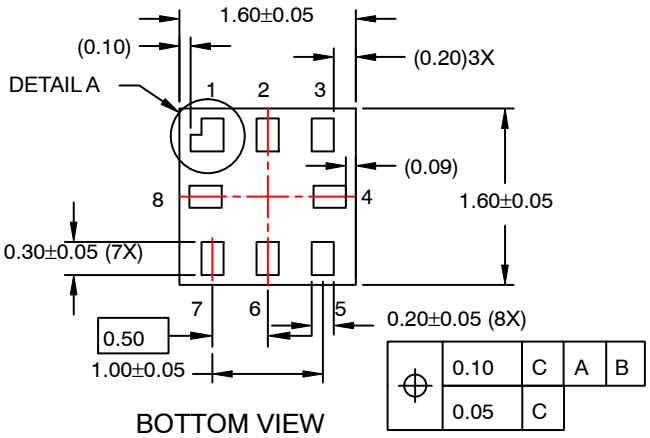
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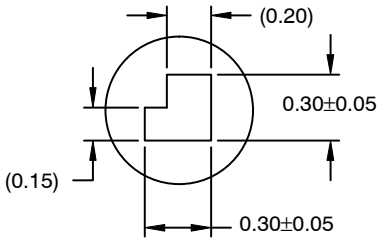
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BOTTOM VIEW



DETAIL A
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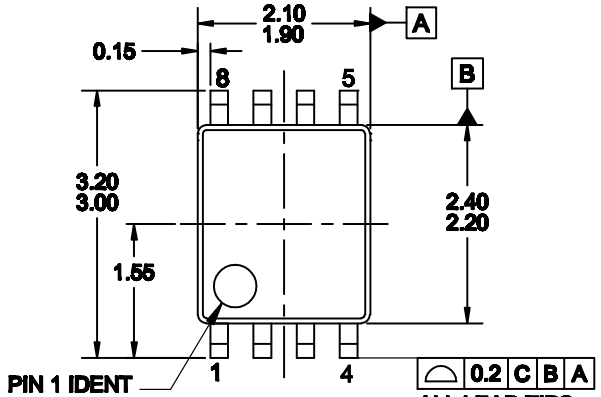
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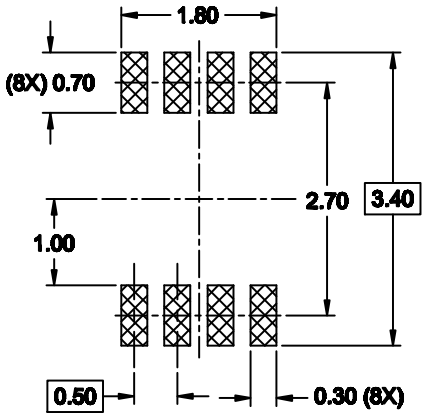
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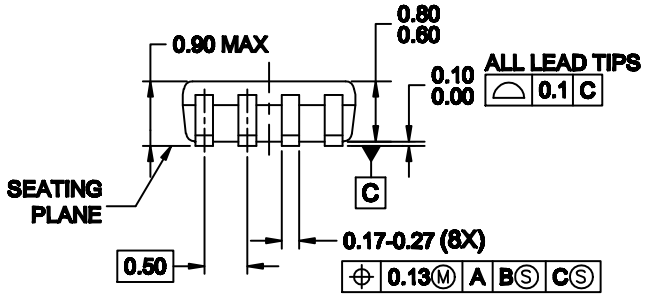
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TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW

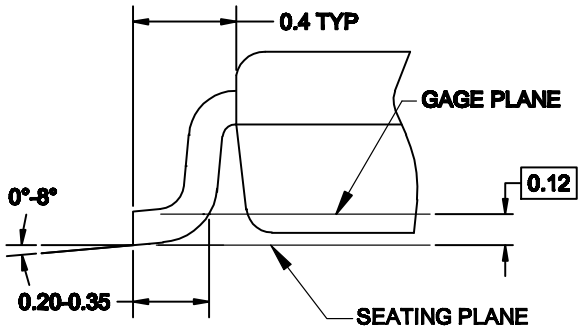
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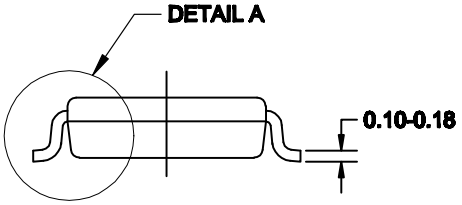
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DETAIL A



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