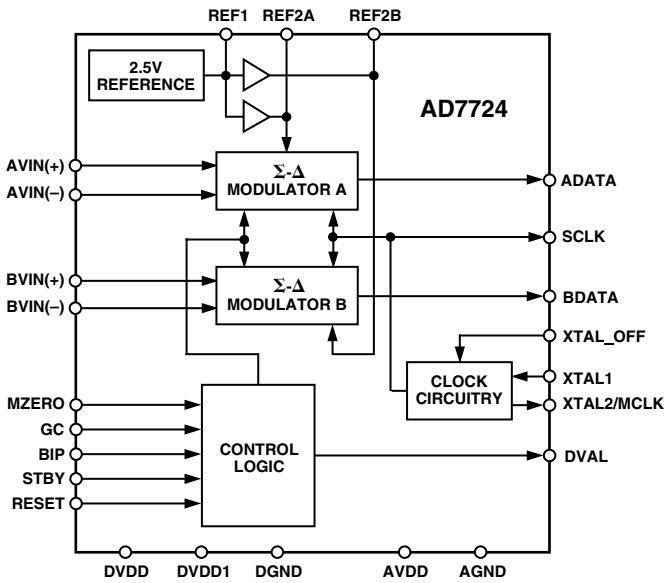
Dual CMOS Σ-Δ Modulators

AD7724

FEATURES

- 13 MHz Master Clock Frequency
- 0 V to +2.5 V or ±1.25 V Input Range
- Single Bit Output Stream
- 90 dB Dynamic Range
- Power Supplies
  - AVDD, DVDD: 5 V ± 5%
  - DVDD1: 3 V ± 5%
- Logic Outputs 3 V/5 V Compatible
- On-Chip 2.5 V Voltage Reference
- 48-Lead LQFP

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

This device consists of two seventh order sigma-delta modulators. Each modulator converts its analog input signal into a high speed 1-bit data stream. The part operates from a 5 V power supply and accepts a differential input range of 0 V to +2.5 V or ±1.25 V centered about a common-mode bias. The analog inputs are continuously sampled by the analog modulators, eliminating the need for external sample-and-hold circuitry. The input information is contained in the output stream as a density of ones. The original information can be digitally reconstructed with an appropriate digital filter.

The part provides an accurate on-chip 2.5 V reference for each modulator. A reference input/output function is provided to allow either the internal reference or an external system reference to be used as the reference source for the modulator.

The device is offered in a 48-lead LQFP package and designed to operate from –40°C to +85°C.

REV. B

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AD7724–SPECIFICATIONS[1] (AVDD = 5 V ± 5%; DVDD = 5 V ± 5%, DVDD1 = 3 V ± 5%; AGND = DGND = 0 V, f_{MCLK} = 13 MHz ac-coupled sine wave, REF2A = REF2B = 2.5 V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	A Version	Unit	Test Conditions/Comments
STATIC PERFORMANCE			When Tested with Ideal FIR Filter as in Figure 1
Integral Nonlinearity	±0.003	% FSR typ	
Offset Error	±0.24	% FSR typ	
Gain Error[2]	±0.6	% FSR typ	
Offset Error Drift	±37.69	µV/°C typ	
Gain Error Drift			REF2 Is an Ideal Reference, REF1 = AGND
Unipolar Mode	±37.69	µV/°C typ	
Bipolar Mode	±18.85	µV/°C typ	
ANALOG INPUTS			
Signal Input Span (VIN(+) – VIN(–))			
Bipolar Mode	$\pm V_{REF2}/2$	V max	BIP = V_{IH}
Unipolar Mode	0 to V_{REF2}	V max	BIP = V_{IL}
Maximum Input Voltage	AVDD	V	
Minimum Input Voltage	0	V	
Input Sampling Capacitance	2	pF typ	
Input Sampling Rate	2 f_{MCLK}	MHz	
Differential Input Impedance	$10^9/(8\ f_{MCLK})$	kΩ typ	
REFERENCE INPUTS			
REF1 Output Voltage	2.32 to 2.68	V min/max	
REF1 Output Voltage Drift	60	ppm/°C typ	
REF1 Output Impedance	4	kΩ typ	
Reference Buffer Offset Voltage	±12	mV max	Offset Between REF1 and REF2
Using Internal Reference			
REF2 Output Voltage	2.32 to 2.68	V min/max	
REF2 Output Voltage Drift	60	ppm/°C typ	
Using External Reference			REF1 = AGND
REF2 Input Impedance	$10^9/(16\ f_{MCLK})$	kΩ typ	
External Reference Voltage Range	2.32 to 2.68	V min/max	Applied to REF1 or REF2
DYNAMIC SPECIFICATIONS[3]			When Tested with Ideal FIR Filter as in Figure 1
Bipolar Mode			BIP = V_{IH}, V_{CM} = 2.5 V, VIN(+) = VIN(–) = 1.25 V p-p or VIN(–) = 1.25 V, VIN(+) = 0 V to 2.5 V
Signal-to-(Noise + Distortion)	90	dB typ	Input BW = 0 kHz–94.25 kHz
	86	dB min	
Total Harmonic Distortion	–90	dB max	Input BW = 0 kHz–94.25 kHz
Spurious Free Dynamic Range	–90	dB max	Input BW = 0 kHz–94.25 kHz
Unipolar Mode			BIP = V_{IL}, VIN(–) = 0 V, VIN(+) = 0 V to 2.5 V
Signal-to-(Noise + Distortion)	88	dB typ	Input BW = 0 kHz–94.25 kHz
Total Harmonic Distortion	–90	dB typ	Input BW = 0 kHz–101.556 kHz
Spurious Free Dynamic Range	–90	dB typ	Input BW = 0 kHz–101.556 kHz
Intermodulation Distortion	–93	dB typ	
AC CMRR	96	dB typ	VIN(+) = VIN(–) = 2.5 V p-p, V_{CM} = 1.25 V to 3.75 V, 20 kHz
CLOCK			
Square Wave[4]			
MCLK Duty Ratio	45 to 55	% max	For Specified Operation
V_{MCLKH}, MCLK High Voltage	4	V min	MCLK Uses CMOS Logic
V_{MCLKL}, MCLK Low Voltage	0.4	V max	
Sine Wave			
XTAL1 Voltage Swing	0.4	V p-p min	XTAL_OFF Tied Low
	4	V p-p max	
LOGIC INPUTS			
V_{IH}, Input High Voltage	2.4	V min	
V_{IL}, Input Low Voltage	0.8	V max	
I_{INH}, Input Current	10	µA max	
C_{IN}, Input Capacitance	10	pF max	

Parameter	A Version	Unit	Test Conditions/Comments
LOGIC OUTPUTS			
V_{OH}, Output High Voltage	DVDD1 – 0.2	V min	$\|I_{OUT}\| \leq 200\ \mu A$
V_{OL}, Output Low Voltage	0.4	V max	$\|I_{OUT}\| \leq 1.6$ mA
POWER SUPPLIES			
AVDD/DVDD	4.75/5.25	V min/V max	
DVDD1	2.85/5.25	V min/V max	
I_{DD} (Total for AVDD, DVDD)			Digital Inputs Equal to 0 V or DVDD
Active Mode	60	mA max	
Standby Mode	20	μA max	

NOTES
[1]Operating temperature range is as follows: A Version: –40°C to +85°C.
[2]Gain Error excludes reference error. The modulator gain is calibrated wrt the voltage on the REF2 pin.
[3]Measurement Bandwidth = 0.5 × f_{MCLK}; Input Level = –0.05 dB.
[4]When a square wave clock is used, the dynamic specifications will degrade by 1 dB typically.

Specifications subject to change without notice.

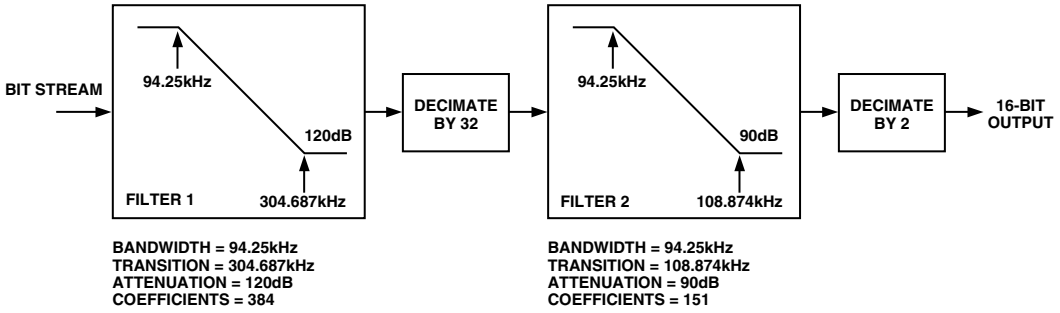


Figure 1. Digital Filter (Consists of Two FIR Filters). This Filter is Implemented on the AD7722.

TIMING CHARACTERISTICS[1, 2]

(AVDD = 5 V ± 5%; DVDD = 5 V ± 5%; DVDD1 = 3 V ± 5%; AGND = DGND = 0 V, REF2A = REF2B = 2.5 V, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} (A Version)	Unit	Conditions/Comments
f_{MCLK}	100	kHz min	Master Clock Frequency
	15	MHz max	13 MHz for Specified Performance
t_{DELAY}	14	ns max	MCLK to SCLK Delay
t_1	67	ns min	Master Clock Period
t_2	$0.45 \times t_{MCLK}$	ns min	Master Clock Input High Time
t_3	$0.45 \times t_{MCLK}$	ns min	Master Clock Input Low Time
t_4	15	ns min	Data Hold Time After SCLK Rising Edge
t_5	10	ns min	RESET Pulsewidth
t_6	10	ns min	RESET Low Time Before MCLK Rising
t_7	$20 \times t_{MCLK}$	ns max	DVAL High Delay After RESET Low
t_8	3	ns max	Data Access Time After SCLK Falling Edge
t_9	t_3–t_8	ns max	Data Valid Time Before SCLK Rising Edge

NOTES
[1]Sample tested at 25°C to ensure compliance.
[2]Guaranteed by design.

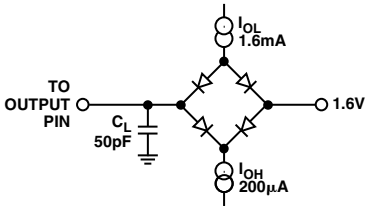


Figure 2. Load Circuit for Access Time and Bus Relinquish Time

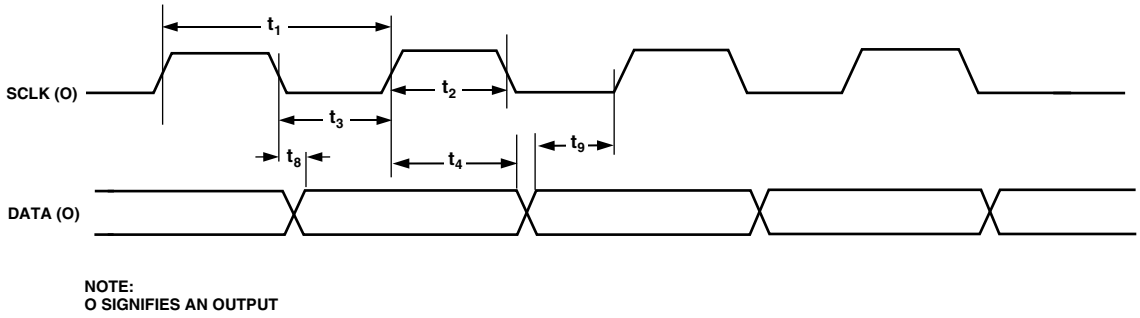


Figure 3. Data Timing

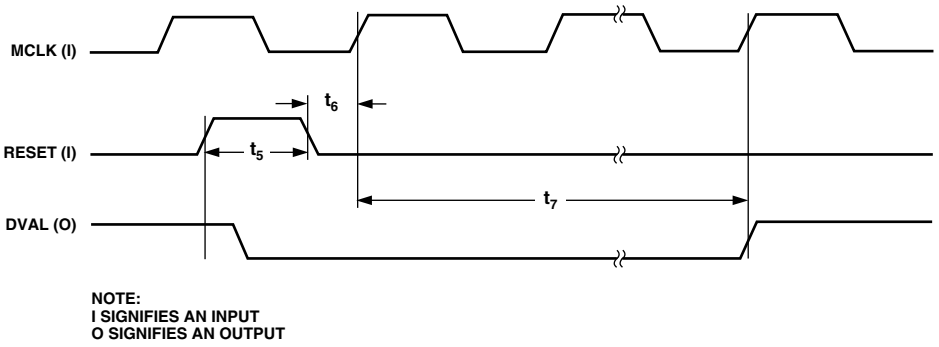


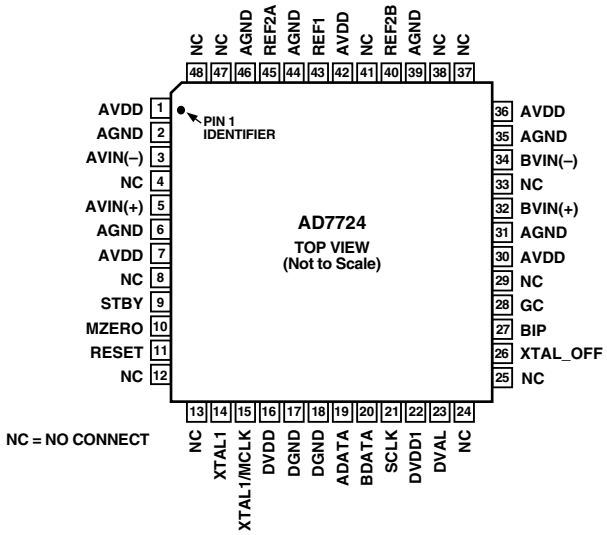
Figure 4. RESET Timing

ABSOLUTE MAXIMUM RATINGS *
(T_A = 25°C unless otherwise noted)

DVDD to DGND ..... –0.3 V to +7 V
AVDD to AGND ..... –0.3 V to +7 V
AVDD to DVDD ..... –1 V to +1 V
AGND to DGND ..... –0.3 V to +0.3 V
Digital Inputs to DGND ..... –0.3 V to DVDD + 0.3 V
Digital Outputs to DGND ..... –0.3 V to DVDD + 0.3 V
VIN(+), VIN(–) to AGND ..... –0.3 V to AVDD + 0.3 V
REF1 to AGND ..... –0.3 V to AVDD + 0.3 V
REF2 to AGND ..... –0.3 V to AVDD + 0.3 V
REFIN to AGND ..... –0.3 V to AVDD + 0.3 V
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... 150°C
θ_{JA} Thermal Impedance ..... 75°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... 215°C
Infrared (15 sec) ..... 220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7724AST	–40°C to +85°C	48-Lead Plastic Thin Quad Flatpack (LQFP)	ST-48

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7724 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN FUNCTION DESCRIPTIONS

Mnemonic	Description
AVDD	Analog Positive Supply Voltage, 5 V ± 5%.
AGND	Ground reference point for analog circuitry.
AVIN(–), AVIN(+)	Analog Input to Modulator A. In unipolar operation, the analog input range on AVIN(+) is AVIN(–) to (AVIN(–) + VREF); for bipolar operation, the analog input range on AVIN(+) is (AVIN(–) ± VREF/2). The absolute analog input range must lie between 0 and AVDD. The input range is continuously sampled and processed by the analog modulator.
STBY	Standby, Logic Input. When STBY is high, the device is placed in a low power mode. When STBY is low, the device is powered up.
MZERO	Digital Control Input. When MZERO is high, the modulator inputs are internally grounded i.e. tied to AGND in unipolar mode and REF2 in bipolar mode. MZERO allows on-chip offsets to be calibrated out. MZERO is low for normal operation.
RESET	Reset Logic Input. RESET is an asynchronous input. When RESET is taken high, the sigma-delta modulator is reset by shorting the integrator capacitors in the modulator. DVAL goes low for 20 MCLK cycles while the modulator is being reset.
XTAL1	Input to Crystal Oscillator Amplifier. This pin can also be used to gain up a small input square or sine wave with XTAL_OFF tied low (see Figure 32 on page 12). When a clock source is applied to XTAL1, SCLK will be inverted and the XTAL1_CLK to SCLK delay will be typically 14 ns longer than t_{DELAY}.
XTAL2/MCLK	Clock Input. An external clock source can be applied directly to this pin with XTAL_OFF tied high. In this case, XTAL1 should be tied to AGND. Alternatively, a parallel resonant fundamental frequency crystal, in parallel with a 1 MΩ resistor, can be connected between XTAL1 and XTAL2 with XTAL_OFF tied low. External capacitors are then required from the XTAL1 and XTAL2 pins to ground. Consult the crystal manufacturer's recommendation for the load capacitors. A sine wave can also be used to provide the clock. A sine wave with a voltage swing between 0.4 V p-p and 4 V p-p is needed. XTAL_OFF is tied low and a 1 MΩ resistor is needed between XTAL1 and XTAL2. A 22 pF capacitor is connected in parallel with this resistor. The sine wave is ac coupled to XTAL1 using a 120 pF capacitor. The use of a sine wave to generate the clock eliminates the need for a square wave clock source which introduces noise.
DVDD	Digital Supply Voltage, 5 V ± 5%.
DGND	Ground reference for the digital circuitry.
ADATA	Modulator A Bit Stream. The digital bit stream from the sigma-delta modulator is output at ADATA.
BDATA	Modulator B Bit Stream. The digital bit stream from the sigma-delta modulator is output at BDATA.
SCLK	Serial Clock, Logic Output. The bit stream from modulator A and modulator B is valid on the rising edge of ASCLK.
DVDD1	Digital Supply Voltage for the digital outputs. DVDD1 can have a value of 5 V ± 5% or 3 V ± 5% so that the logic outputs can be 3 V or 5 V compatible.
DVAL	Data Valid Logic Output. A logic high on DVAL indicates that the data bit stream from the AD7724 is an accurate digital representation of the analog voltage at the input to the sigma-delta modulator. The DVAL pin is set low for 20 MCLK cycles if the analog input is overranged.
XTAL_OFF	Oscillator Enable Input. A logic high disables the crystal oscillator amplifier to allow use of an external clock source. XTAL_OFF is set to a logic low when an external crystal is used between XTAL1 and XTAL2.
BIP	Analog Input Range Select, Logic Input. A logic low on this input selects unipolar mode. A logic high selects bipolar mode.
GC	Digital Control Input. When GC is high, the gain error of the modulator can be calibrated.
BVIN(–), BVIN(+)	Analog Input to Modulator B. In unipolar operation, the analog input range on BVIN(+) is BVIN(–) to (BVIN(–) + VREF); for bipolar operation, the analog input range on BVIN(+) is (BVIN(–) ± VREF/2). The absolute analog input range must lie between 0 and AVDD. The input range is continuously sampled and processed by the analog modulator.
REF2B	Reference Input/Output to Sigma-Delta Modulator B. REF2B connects to the output of an external buffer amplifier used to drive sigma-delta modulator B. When REF2B is used as an input, REF1 must be connected to AGND.
REF1	Reference Input/Output. REF1 connects through 3 kΩ to the output of the internal 2.5 V reference and to the input of two buffer amplifiers that drive Σ-Δ modulator A and Σ-Δ modulator B. The pin can be overdriven with an external 2.5 V reference.
REF2A	Reference Input/Output to Sigma-Delta Modulator A. REF2A connects to the output of an external buffer amplifier used to drive sigma-delta modulator A. When REF2A is used as an input, REF1 must be connected to AGND.

TERMINOLOGY (IDEAL FIR FILTER USED WITH AD7724 [FIGURE 1])

Integral Nonlinearity

This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale (not to be confused with bipolar zero), a point 0.5 LSB below the first code transition (100 . . . 00 to 100 . . . 01 in bipolar mode and 000 . . . 00 to 000 . . . 01 in unipolar mode) and full scale, a point 0.5 LSB above the last code transition (011 . . . 10 to 011 . . . 11 in bipolar mode and 111 . . . 10 to 111 . . . 11 in unipolar mode). The error is expressed in LSBs.

Common-Mode Rejection Ratio

The ability of a device to reject the effect of a voltage applied to both input terminals simultaneously—often through variation of a ground level—is specified as a common–mode rejection ratio. CMRR is the ratio of gain for the differential signal to the gain for the common-mode signal.

Unipolar Offset Error

Unipolar offset error is the deviation of the first code transition from the ideal VIN(+) voltage which is (VIN(–) + 0.5 LSB) when operating in the unipolar mode.

Bipolar Offset Error

This is the deviation of the midscale transition (111 . . . 11 to 000 . . . 00) from the ideal VIN(+) voltage which is (VIN(–) –0.5 LSB) when operating in the bipolar mode.

Gain Error

The first code transition should occur at an analog value 1/2 LSB above minus full scale. The last code transition should occur for an analog value 1 1/2 LSB below the nominal full-scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Signal-to-(Noise + Distortion)

Signal-to-(Noise + Distortion) is the measured signal-to-noise plus distortion ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise plus distortion is the rms sum of all of the nonfundamental signals and harmonics up to half the Output Data Rate ($f_O/2$), excluding dc. Signal-to-(Noise + Distortion) is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical Signal-to-(Noise + Distortion) ratio for a sine wave input is given by

$$\textit{Signal-to-(Noise + Distortion)} = (6.02\ N + 1.76)\ dB$$

where N is the number of bits.

Total Harmonic Distortion

THD is the ratio of the rms sum of harmonics to the rms value of the fundamental. THD is defined as

$$THD = 20 \log \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonic.

Spurious Free Dynamic Range

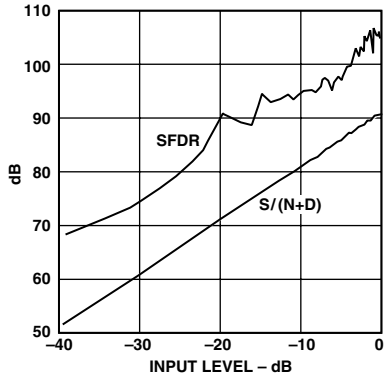
Spurious free dynamic range is the difference, in dB, between the peak spurious or harmonic component in the ADC output spectrum (up to $f_O/2$ and excluding dc) and the rms value of the fundamental. Normally, the value of this specification will be determined by the largest harmonic in the output spectrum of the FFT. For input signals whose second harmonics occur in the stop band region of the digital filter, a spur in the noise floor limits the SFDR.

Intermodulation Distortion

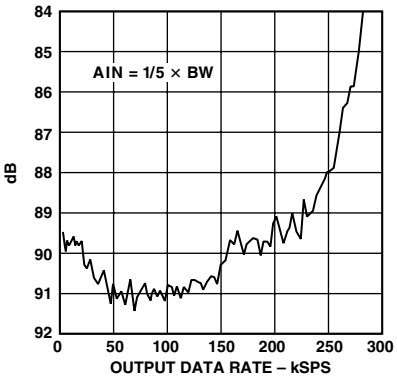
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

AD7724–Typical Performance Characteristics

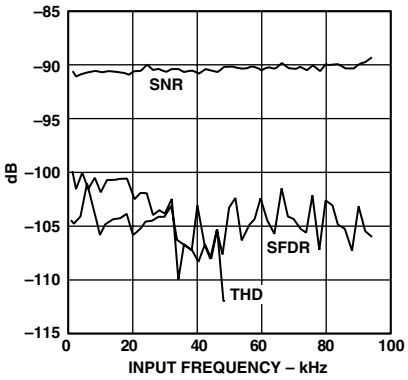
(AVDD = DVDD = 5.0 V, T_A = 25°C; CLKIN = 13 MHz ac-coupled sine wave, AIN = 20 kHz, Bipolar Mode; V_{IN}(+) = 0 V to 2.5 V, V_{IN}(–) = 1.25 V unless otherwise noted)



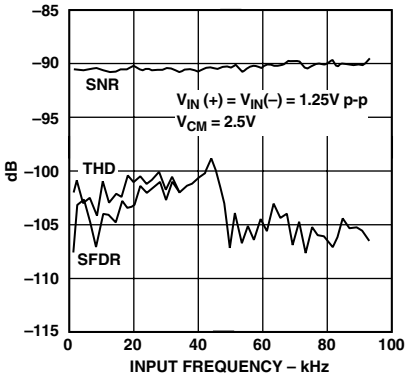
TPC 1. S/(N+D) and SFDR vs. Analog Input Level



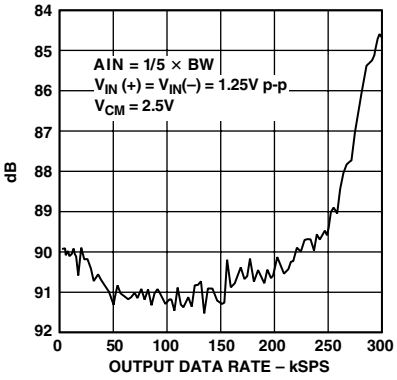
TPC 2. S/(N+D) vs. Output Sample Rate



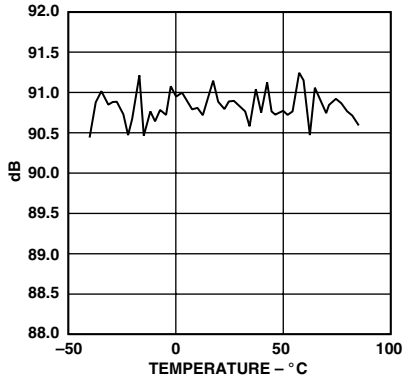
TPC 3. SNR, THD, and SFDR vs. Input Frequency



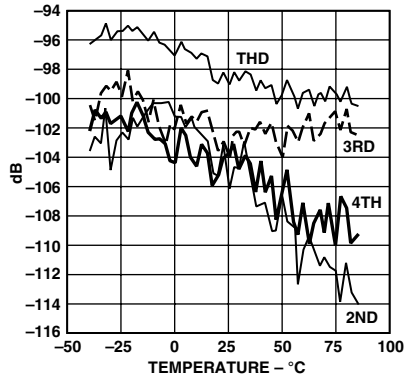
TPC 4. SNR, THD, and SFDR vs. Input Frequency



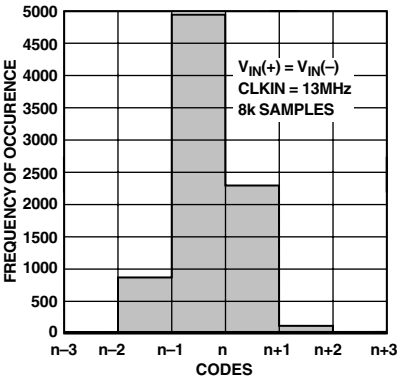
TPC 5. S/(N+D) vs. Output Sample Rate



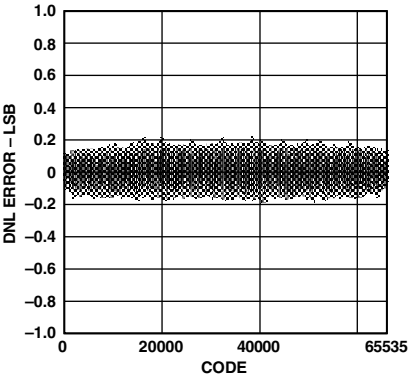
TPC 6. SNR vs. Temperature



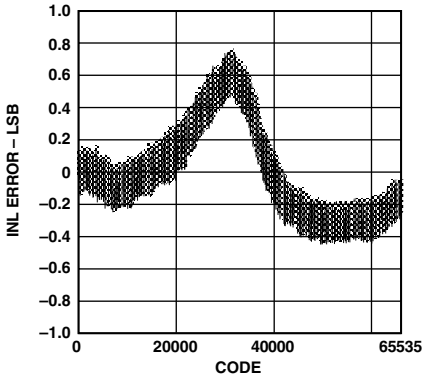
TPC 7. THD vs. Temperature



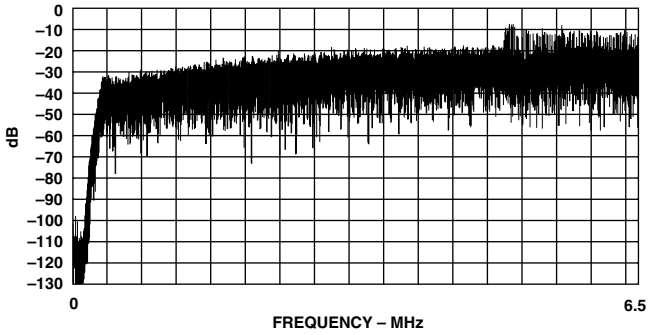
TPC 8. Histogram of Output Codes with DC Input



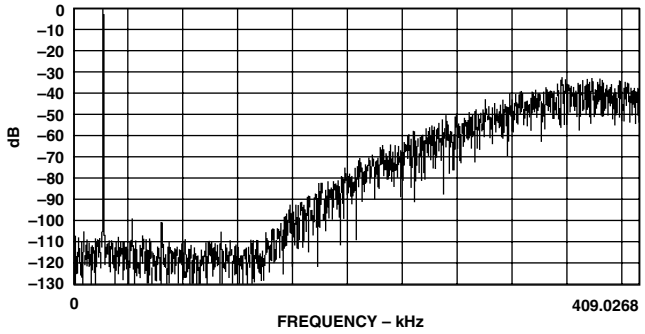
TPC 9. Differential Nonlinearity



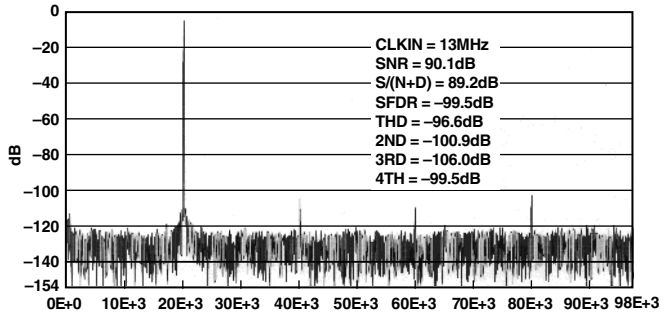
TPC 10. Integral Nonlinearity Error



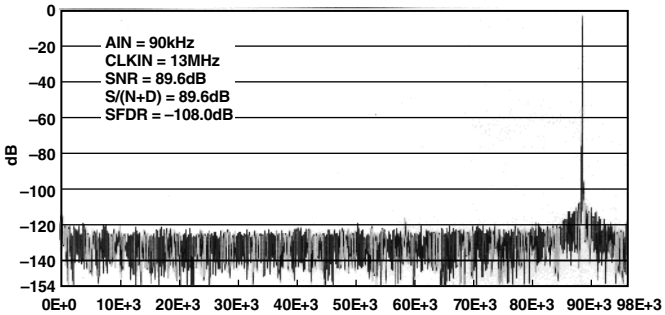
TPC 11. Modulator Output (0 Hz to MCLK/2)



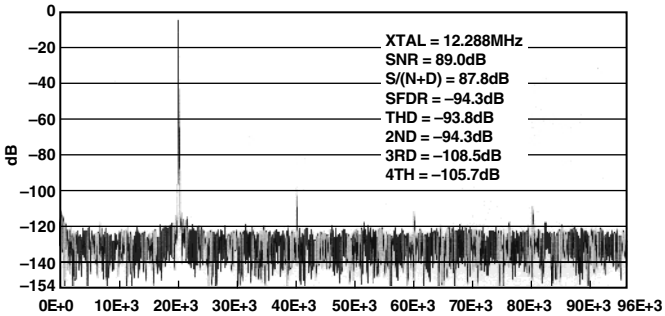
TPC 14. Modulator Output (0 to 409.0268 kHz)



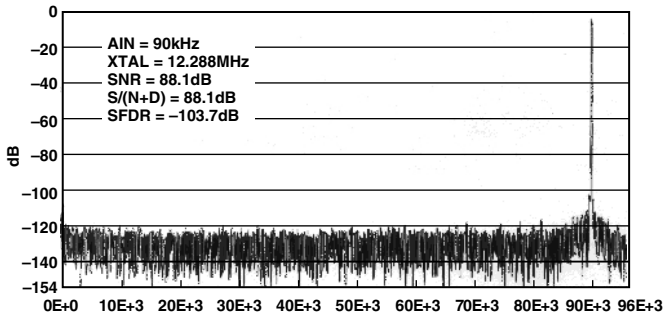
TPC 12. 16K Point FFT



TPC 15. 16K Point FFT



TPC 13. 16K Point FFT



TPC 16. 16K Point FFT

CIRCUIT DESCRIPTION

The AD7724 employs a sigma-delta conversion technique to convert the analog input into a digital pulse train. The analog input is continuously sampled by a switched capacitor modulator at twice the rate of the clock input frequency (2 f_{MCLK}). The digital data that represents the analog input is in the ones' density of the bit stream at the output of the sigma-delta modulator. The modulator outputs the bit stream at a data rate equal to f_{MCLK}.

Due to the high oversampling rate, which spreads the quantization noise from 0 to $f_{MCLK}/2$, the noise energy contained in the band of interest is reduced (Figure 5a). To reduce the quantization noise further, a high order modulator is employed to shape the noise spectrum, so that most of the noise energy is shifted out of the band of interest (Figure 5b).

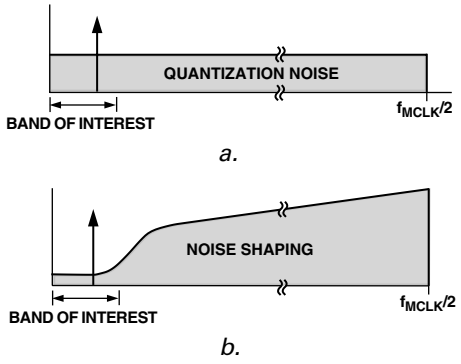


Figure 5. Sigma-Delta ADC

USING THE AD7724

ADC Differential Inputs

The AD7724 uses differential inputs to provide common-mode noise rejection (i.e., the converted result will correspond to the differential voltage between the two inputs). The absolute voltage on both inputs must lie between AGND and AVDD.

In the unipolar mode, the full scale-input range (VIN(+) – VIN(–)) is 0 V to V_{REF}. In the bipolar mode configuration, the full-scale analog input range is $\pm V_{REF}/2$. The bipolar mode allows complementary input signals. Alternatively, VIN(–) can be connected to a dc bias voltage to allow a single-ended input on VIN(+) equal to $V_{BIAS} \pm V_{REF}/2$.

Differential Inputs

The analog input to the modulator is a switched capacitor design. The analog input is converted into charge by highly linear sampling capacitors. A simplified equivalent circuit diagram of the analog input is shown in Figure 6. A signal source driving the analog input must be able to provide the charge onto the sampling capacitors every half MCLK cycle and settle to the required accuracy within the next half cycle.

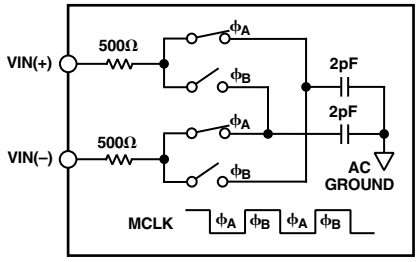


Figure 6. Analog Input Equivalent Circuit

Since the AD7724 samples the differential voltage across its analog inputs, low noise performance is attained with an input circuit that provides low differential mode noise at each input. The amplifiers used to drive the analog inputs play a critical role in attaining the high performance available from the AD7724.

When a capacitive load is switched onto the output of an op amp, the amplitude will momentarily drop. The op amp will try to correct the situation and, in the process, hits its slew rate limit. This nonlinear response, which can cause excessive ringing, can lead to distortion. To remedy the situation, a low-pass RC filter can be connected between the amplifier and the input to the AD7724 as shown in Figure 7. The external capacitor at each input aids in supplying the current spikes created during the sampling process. The resistor in the diagram, as well as creating a pole for the antialiasing, isolates the op amp from the transient nature of the load.

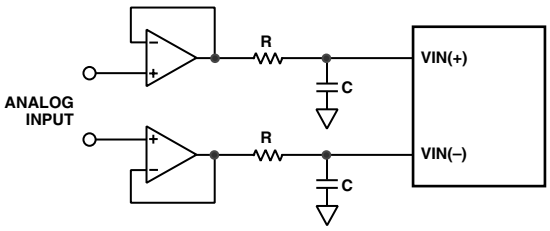


Figure 7. Simple RC Antialiasing Circuit

The differential input impedance of the AD7724 switched capacitor input varies as a function of the MCLK frequency, given by the equation:

$$Z_{IN} = 10^9/\left(8\,f_{MCLK}\right)k\Omega$$

Even though the voltage on the input sampling capacitors may not have enough time to settle to the accuracy indicated by the resolution of the AD7724, as long as the sampling capacitor charging follows the exponential curve of RC circuits, only the gain accuracy suffers if the input capacitor is switched away too early.

An alternative circuit configuration for driving the differential inputs to the AD7724 is shown in Figure 8.

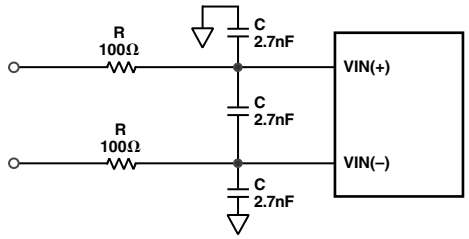


Figure 8. Differential Input with Antialiasing

A capacitor between the two input pins sources or sinks charge to allow most of the charge needed by one input to be effectively supplied by the other input. This minimizes undesirable charge transfer from the analog inputs to and from ground. The series resistor isolates the operational amplifier from the current spikes created during the sampling process and provides a pole for antialiasing. The 3 dB cutoff frequency of the antialias filter is given by Equation 1, and the attenuation of the filter is given by Equation 2.

$$f_{3\,dB} = 1/\left(2\,\pi R_{EXT} C_{EXT}\right) \quad (1)$$

$$Attenuation = 20\ log\left(1/\sqrt{1+\left(f/f_{3\,dB}\right)^2}\right) \quad (2)$$

The choice of the filter cutoff frequency will depend on the amount of roll-off that is acceptable in the passband of the digital filter and the required attenuation at the first image frequency.

The capacitors used for the input antialiasing circuit must have low dielectric absorption to avoid distortion. Film capacitors such as polypropylene or polycarbonate are suitable. If ceramic capacitors are used, they must have NPO dielectric.

Applying the Reference

The reference circuitry used in the AD7724 includes an on-chip 2.5 V bandgap reference and a reference buffer circuit. The block diagram of the reference circuit is shown in Figure 9. The internal reference voltage is connected to REF1 via a 3 kΩ resistor and is internally buffered to drive the analog modulator's switched capacitor DAC (REF2). When using the internal reference, connect 110 nF between REF1 and AGND. If the internal reference is required to bias external circuits, use an external precision op amp to buffer REF1.

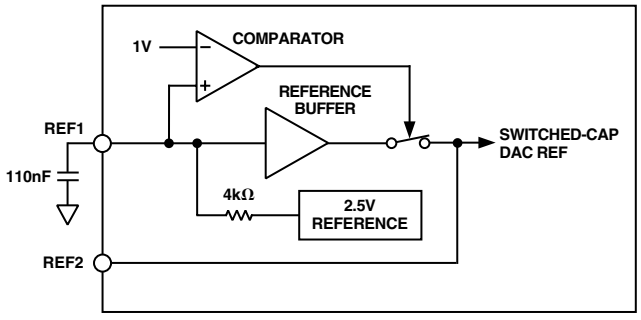


Figure 9. Reference Circuit Block Diagram

The AD7724 can operate with its internal reference, or an external reference can be applied in two ways. An external reference can be connected to REF1, overdriving the internal reference. However, an error will be introduced due to the offset of the internal buffer amplifier. For lowest system gain errors when using an external reference, REF1 is grounded (disabling the internal buffer) and the external reference is connected to REF2.

In all cases, since the REF2 voltage connects to the analog modulator, a 110 nF capacitor must connect directly from REF2 to AGND. The external capacitor provides the charge required for the dynamic load presented at the REF2 pin (Figure 10).

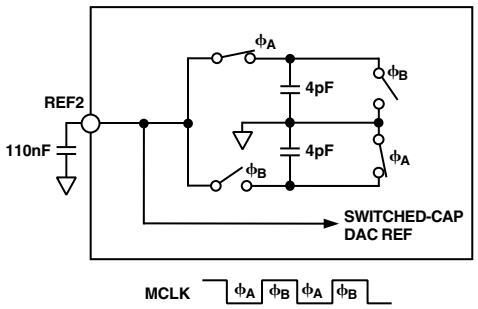


Figure 10. REF2 Equivalent Circuit

The AD780 is ideal to use as an external reference with the AD7724. Figure 11 shows a suggested connection diagram.

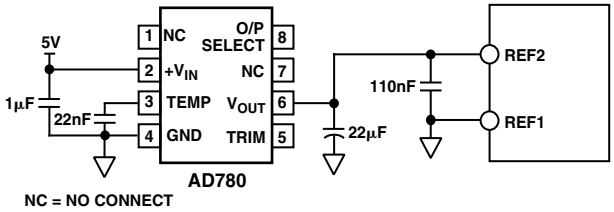


Figure 11. External Reference Circuit Connection

Input Circuits

Figures 12 and 13 show two simple circuits for bipolar mode operation. Both circuits accept a single-ended bipolar signal source and create the necessary differential signals at the input to the ADC.

The circuit in Figure 12 creates a 0 V to 2.5 V signal at the VIN(+) pins to form a differential signal around an initial bias voltage of 1.25 V. For single-ended applications, best THD performance is obtained with VIN(–) set to 1.25 V rather than 2.5 V. The input to the AD7724 can also be driven differentially with a complementary input as shown in Figure 13.

In this case, the input common-mode voltage is set to 2.5 V. The 2.5 V p-p full-scale differential input is obtained with a 1.25 V p-p signal at each input in antiphase. This configuration minimizes the required output swing from the amplifier circuit and is useful for single supply applications.

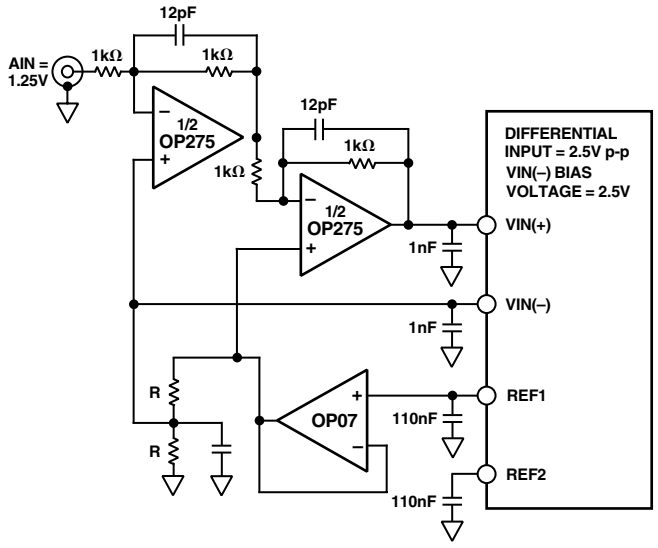


Figure 12. Single-Ended Analog Input for Bipolar Mode Operation

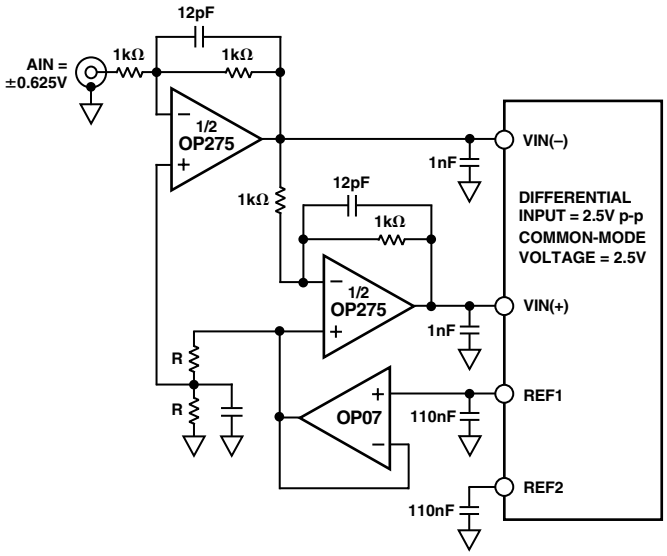


Figure 13. Single-Ended-to-Differential Analog Input Circuit for Bipolar Mode Operation

The 1 nF capacitors at each input store charge to aid the amplifier settling as the input is continuously switched. A resistor in series with the drive amplifier output and the 1 nF input capacitor may also be used to create an antialias filter.

Clock Generation

The AD7724 contains an oscillator circuit to allow a crystal or an external clock signal to generate the master clock for the ADC. The connection diagram for use with the crystal is shown in Figure 14. Consult the crystal manufacturer's recommendation for the load capacitors.

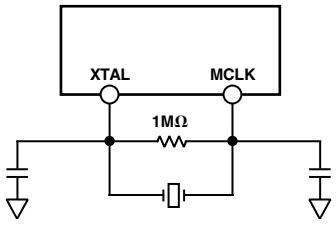


Figure 14. Crystal Oscillator Connection

An external clock must be free of ringing and have a minimum rise time of 5 ns. Degradation in performance can result as high edge rates increase coupling that can generate noise in the sampling process. The connection diagram for an external clock source (Figure 15) shows a series damping resistor connected between the clock output and the clock input to the AD7724. The optimum resistor will depend on the board layout and the impedance of the trace connecting to the clock input.

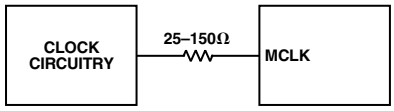


Figure 15. External Clock Oscillator Connection

A low phase clock should be used to generate the ADC sampling clock because sampling clock jitter effectively modulates the input signal and raises the noise floor. The sampling clock generator should be isolated from noisy digital circuits, grounded and heavily decoupled to the analog ground plane.

A sine wave can also be used to provide the clock (Figure 16.) A sine wave with a voltage swing between 0.4 V p-p and 4 V p-p is needed. XTAL_OFF is tied low and a 1 MΩ resistor is needed between XTAL1 and XTAL2. A 22 pF capacitor is connected in parallel with this resistor. The sine wave is ac coupled to XTAL1 using a 120 pF capacitor. The use of a sine wave to generate the clock eliminates the need for a square wave clock source which introduces noise.

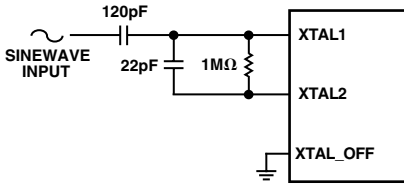


Figure 16. Using a Sine Wave Input as a Clock Source

The sampling clock generator should be referenced to the analog ground plane in a split ground system. However, this is not always possible because of system constraints. In many cases, the sampling clock must be derived from a higher frequency multipurpose system clock that is generated on the digital ground plane. If the clock signal is passed between its origin on a digital plane to the AD7724 on the analog ground plane, the ground noise between the two planes adds directly to the clock and will produce excess jitter. The jitter can cause unwanted degradation in the signal-to-noise ratio and also produce unwanted harmonics.

This can be somewhat remedied by transmitting the sampling signal as a differential one, using either a small RF transformer or a high-speed differential driver and receiver such as PECL. In either case, the original master system clock should be generated from a low phase noise crystal oscillator.

Offset and Gain Calibration

The analog inputs of the AD7724 can be configured to measure offset and gain errors. Pins MZERO and GC are used to configure the part. Before calibrating the device, the part should be reset so that the modulator is in a known state at calibration. When MZERO is taken high, the analog inputs are tied to AGND in unipolar mode and VREF in bipolar mode. After taking MZERO high, 1000 MCLK cycles should be allowed for the circuitry to settle before the bit stream is read from the device. The ideal ones density is 50% when bipolar operation is selected and 37.5% when unipolar mode is selected.

When GC is taken high, VIN(–) is tied to ground while VIN(+) is tied to VREF. Again, 1000 MCLK cycles should be allowed for the circuitry to settle before the bit stream is read. The ideal ones density is 62.5%.

The calibration results apply only for the particular analog input mode (unipolar/bipolar) selected when performing the calibration cycle. On changing to a different analog input mode, a new calibration must be performed.

Before calibrating, ensure that the supplies have settled and that the voltage on the analog input pins is between the supply voltages.

Standby

The part can be put into a low power standby mode by taking STBY high. During standby, the clock to the modulators is turned off and bias is removed from all analog circuits.

Reset

The RESET pin is used to reset the modulators to a known state. When RESET is taken high, the integrator capacitors of the modulator are shorted and DVAL goes low and remains low until 20 MCLK cycles after RESET is deasserted. However, an additional 1000 MCLK cycles should be allowed before reading the modulator bit stream as the modulator circuitry needs to settle after the reset.

DVAL

The DVAL pin is used to indicate that an overrange input signal has resulted in invalid data at the modulator output. As with all single-bit DAC high-order sigma-delta modulators, large overloads on the inputs can cause the modulator to go unstable. The modulator is designed to be stable with signals within the input bandwidth that exceed full-scale by 100%. When instability is detected by internal circuits, the modulator is reset to a stable state and DVAL is held low for 20 clock cycles.

Grounding and Layout

Since the analog inputs are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent common-mode rejection of the part will remove common-mode noise on these inputs. The analog and digital supplies to the AD7724 are independent and separately pinned out to minimize coupling between analog and digital sections of the device.

The printed circuit board that houses the AD7724 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should be joined in only one place. If the AD7724 is the only device requiring an AGND-to-DGND connection, the ground planes should be connected at the AGND and DGND pins of the AD7724. If the AD7724 is in a system where multiple devices require AGND-to-DGND connections, the connection should still be made at one point only, a star ground point that should be established as close as possible to the AD7724.

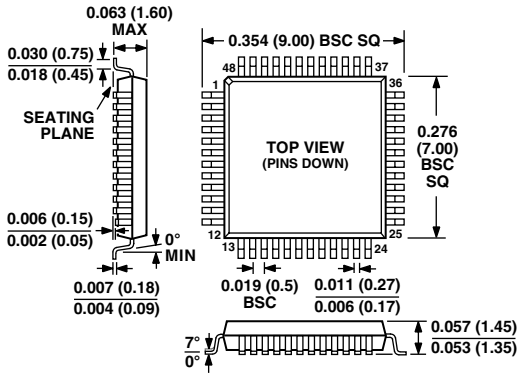
Avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7724 to avoid noise coupling. The power supply lines to the AD7724 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best, but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the other side.

Good decoupling is important when using high resolution ADCs. All analog and digital supplies should be decoupled to AGND and DGND respectively, with 100 nF ceramic capacitors in parallel with 10 µF tantalum capacitors. To achieve the best from these decoupling capacitors, they should be placed as close as possible to the device, ideally right up against the device. In systems where a common supply voltage is used to drive both the AVDD and DVDD of the AD7724, it is recommended that the system's AVDD supply be used. This supply should have the recommended analog supply decoupling between the AVDD pins of the AD7724 and AGND and the recommended digital supply decoupling between the DVDD pins and DGND.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Lead Plastic Thin Quad Flatpack (ST-48)



Revision History

Location	Page
Data Sheet changed from REV. A to REV. B.	
Additions to TIMING CHARACTERISTICS	4
Edits to Figure 3	4
Edits to PIN FUNCTION DESCRIPTIONS	6

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