RT600

Errata sheet RT600

Rev. 1.1 — May 27, 2020 **Errata sheet**

Document information

Info	Content
Keywords	MIMXRT685SFFOB, MIMXRT685SFVKB, MIMXRT685SFAWBR, MIMXRT633SFVKB, MIMXRT633SFAWBR
Abstract	RT600 errata

Revision history

Rev	Date	Description
1.1	20200508	Added FlexSPI DLL lock status timing issue and addressed part marking.
1.0	20200213	Initial version.

Contact information

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1. Product identification

The MIMXRT6xxSFAWBR WLCSP114 production samples has the following top-side package marking:

- First line: MRT6xxSF
- Second line: AW[R]R
- Third line: xxxxxx xx
- Fourth line: xxxxyyww
  - yyww: Date code with yy = year and ww = week

  Fifth line: xxx-yyy
- Sixth line: NXP

The MIMXRT6xxSFVKB VFBGA176 production samples has the following top-side package marking:

- First line: MRT6xxSFV
- Second line: K[R] xxxxxx
- Third line: xxyyww
- Fourth line: xxxxx
  - yyww: Date code with yy = year and ww = week

The MIMXRT685SFFOB FOWLP249 production samples has the following top-side package marking:

- First line: MRT6xxSFFOB
- Second line: xxxxxx
- Third line: xxxxxx
- Fourth line: xxxxxyyww
  - yyww: Date code with yy = year and ww = week

Table 1. Device revision table

Revision identifier	Revision description [R]
B	Initial device revision

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
FlexSPI	FlexSPI DLL lock status bit not accurate due to timing issue.	B	Section 3.1 “FlexSPI.1: FlexSPI DLL lock status bit not accurate due to timing issue”

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Product version(s)	Detailed description
n/a	n/a	n/a	n/a

Table 4. Errata notes

Errata notes	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

3. Functional problems detail

3.1 FlexSPI.1: FlexSPI DLL lock status bit not accurate due to timing issue

Introduction

Based on the sample clock source selection, the DLL control register (DLLxCR) can be used to set the delay line chain which allows a fixed number of delay cells or auto-adjusted to lock on a certain phase delay to the reference clock.

Problem

After configuring the DLL and setting the lock status bit, data may not be in sync if a read/write is performed immediately from a FLEXSPI based external flash due to timing issues.

Work-around

Add a delay time (100 NOP) again after the DLL lock status is set.

4. AC/DC deviations detail

5. Errata notes detail

No known errata.

6. Legal information

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