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Single-Channel: 6N138M, 6N139M
Dual-Channel: HCPL2730M, HCPL2731M
8-Pin DIP Low Input Current High Gain Split Darlington Optocouplers

Features

- Low Current – 0.5 mA
- Superior CTR – 2000%
- Superior CMR – 10 kV/μs
- CTR Guaranteed 0 to 70°C
- Dual Channel – HCPL2730M, HCPL2731M
- Safety and Regulatory Approvals
  - UL1577, 5,000 VAC_{RMS} for 1 Minute
  - DIN EN/IEC60747-5-5

Applications

- Digital Logic Ground Isolation
- Telephone Ring Detector
- EIA-RS-232C Line Receiver
- High Common Mode Noise Line Receiver
- μP Bus Isolation
- Current Loop Receiver

Description

The single-channel, 6N138M, 6N139M and dual-channel HCPL2730M, HCPL2731M optocouplers consist of an AlGaAs LED optically coupled to a high gain split darlington photodetector.

The split darlington configuration separating the input photodiode and the first stage gain from the output transistor permits lower output saturation voltage and higher speed operation than possible with conventional darlington phototransistor optocoupler. In the dual channel devices, HCPL2730M and HCPL2731M, an integrated emitter-base resistor provides superior stability over temperature.

The combination of a very low input current of 0.5 mA and a high current transfer ratio of 2000% makes this family particularly useful for input interface to MOS, CMOS, LSTTL and EIA RS232C, while output compatibility is ensured to CMOS as well as high fan-out TTL requirements. An internal noise shield provides exceptional common mode rejection of 10 kV/μs.

Related Resources

- www.fairchildsemi.com/products/optoelectronics/
- www.fairchildsemi.com/pf/HC/HCPL0700.html
- www.fairchildsemi.com/pf/HC/HCPL0730.html
- www.fairchildsemi.com/pf/HC/HCPL0731.html

Schematics

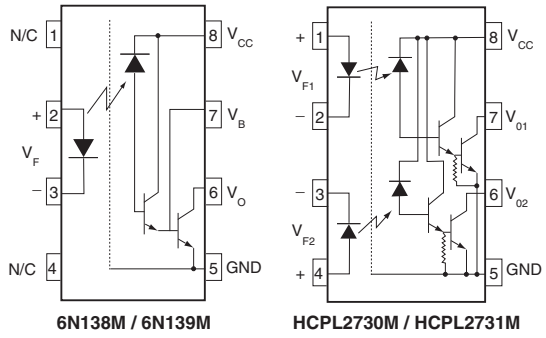


Figure 1. Schematics

Package Outlines

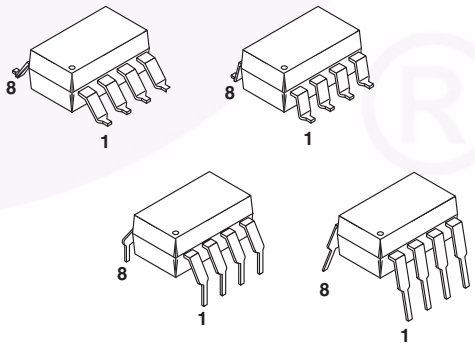


Figure 2. Package Options

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Safety and Insulation Ratings

As per DIN EN/IEC 60747-5-5, this optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

Parameter		Characteristics
Installation Classifications per DIN VDE 0110/1.89 Table 1, For Rated Mains Voltage	< 150 V_{RMS}	I–IV
	< 300 V_{RMS}	I–IV
	< 450 V_{RMS}	I–III
	< 600 V_{RMS}	I–III
	< 1,000 V_{RMS} (Option T, TS)	I-III
Climatic Classification		40/100/21
Pollution Degree (DIN VDE 0110/1.89)		2
Comparative Tracking Index		175

Symbol	Parameter	Value	Unit
V_{PR}	Input-to-Output Test Voltage, Method A, V_{IORM} x 1.6 = V_{PR}, Type and Sample Test with t_m = 10 s, Partial Discharge < 5 pC	2,262	V_{peak}
	Input-to-Output Test Voltage, Method B, V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 s, Partial Discharge < 5 pC	2,651	V_{peak}
V_{IORM}	Maximum Working Insulation Voltage	1,414	V_{peak}
V_{IOTM}	Highest Allowable Over-Voltage	6,000	V_{peak}
	External Creepage	≥ 8.0	mm
	External Clearance	≥ 7.4	mm
	External Clearance (for Option TV, 0.4" Lead Spacing)	≥ 10.16	mm
DTI	Distance Through Insulation (Insulation Thickness)	≥ 0.5	mm
T_S	Case Temperature(1)	150	°C
$I_{S,INPUT}$	Input Current(1)	200	mA
$P_{S,OUTPUT}$	Output Power (Duty Factor ≤ 2.7%)(1)	300	mW
R_{IO}	Insulation Resistance at T_S, V_{IO} = 500 V(1)	> 10^9	Ω

Note:

1. Safety limit value - maximum values allowed in the event of a failure.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A = 25°C unless otherwise specified.

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	-40 to +125	°C
T_{OPR}	Operating Temperature	-40 to +100	°C
T_J	Junction Temperature	-40 to +125	°C
T_{SOL}	Lead Solder Temperature	260 for 10 sec	°C

Symbol	Parameter	Device	Value	Unit
EMITTER				
I_F (avg)	DC/Average Forward Input Current Per Channel	All	20	mA
I_F (pk)	Peak Forward Input Current Per Channel (50% duty cycle, 1 ms P.W.)	All	40	mA
I_F (trans)	Peak Transient Input Current Per Channel (≤ 1 µs P.W., 300 pps)	All	1	A
V_R	Reverse Input Voltage Per Channel	All	5	V
P_D	Input Power Dissipation Per Channel(2)	All	35	mW
DETECTOR				
I_O (avg)	Average Output Current Per Channel	All	60	mA
V_{ER}	Emitter-Base Reverse Voltage	6N138M, 6N139M	0.5	V
V_{CC}, V_O	Supply Voltage, Output Voltage	6N138M, HCPL2730M	-0.5 to 7.0	V
		6N139M, HCPL2731M	-0.5 to 18.0	
P_O	Output Power Dissipation Per Channel	All	100	mW

Note:

2. No derating required for devices operated within the T_{OPR} specification (6N138M and 6N139M only).

Electrical Characteristics

Individual Component Characteristics

(V_{CC} = 5.0 V, T_A = 0°C to 70°C unless otherwise specified. Typical value is measured at T_A = 25°C.)

Symbol	Parameter	Device	Test Conditions	Min.	Typ.	Max.	Unit
EMITTER							
V_F	Input Forward Voltage	All	I_F = 1.6 mA, T_A = 25°C		1.30	1.70	V
			I_F = 1.6 mA			1.75	
BV_R	Input Reverse Breakdown Voltage	All	I_R = 10 µA, T_A = 25°C	5.0	19.0		V
$\Delta V_F / \Delta T_A$	Temperature Coefficient of Forward Voltage	All	I_F = 1.6 mA		-1.94		mV/°C
DETECTOR							
I_{CCL}	Logic Low Supply Current	6N138M, 6N139M	I_F = 1.6 mA, V_O = Open, V_{CC} = 18 V		0.4	1.5	mA
		HCPL2730M	V_{CC} = 7 V; $I_{F1} = I_{F2}$ = 1.6 mA, $V_{O1} = V_{O2}$ = Open		1.25	3	
		HCPL2731M	V_{CC} = 18 V; $I_{F1} = I_{F2}$ = 1.6 mA, $V_{O1} = V_{O2}$ = Open				
I_{CCH}	Logic High Supply Current	6N138M, 6N139M	I_F = 0 mA, V_O = Open, V_{CC} = 18 V		0.0003	10	µA
		HCPL2730M	V_{CC} = 7 V; $I_{F1} = I_{F2}$ = 0 mA, $V_{O1} = V_{O2}$ = Open		0.0003	20	
		HCPL2731M	V_{CC} = 18 V; $I_{F1} = I_{F2}$ = 0 mA, $V_{O1} = V_{O2}$ = Open				

Transfer Characteristics

Symbol	Parameter	Device	Test Conditions	Min.	Typ.	Max.	Unit
COUPLED							
CTR	Current Transfer Ratio[3][4]	6N138M	I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V	300	1600		%
		HCPL2730M			2400		
		6N139M	I_F = 0.5 mA, V_O = 0.4 V, V_{CC} = 4.5 V	400	2000		
		HCPL2731M			3500		
		6N139M	I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V	500	1600		
		HCPL2731M			2400		
I_{OH}	Logic High Output Current	6N138M	I_F = 0 mA, $V_O = V_{CC}$ = 7 V		0.001	250	µA
		HCPL2730M					
		6N139M	I_F = 0 mA, $V_O = V_{CC}$ = 18 V		0.0036	100	
		HCPL2731M					
V_{OL}	Logic Low Output Voltage[4]	6N138M	I_F = 1.6 mA, I_O = 4.8 mA, V_{CC} = 4.5 V		0.06	0.4	V
		HCPL2730M			0.05		
		6N139M	I_F = 0.5 mA, I_O = 2 mA, V_{CC} = 4.5 V		0.05	0.4	
		6N139M	I_F = 1.6 mA, I_O = 8 mA, V_{CC} = 4.5 V		0.093	0.4	
		HCPL2731M			0.08		
		6N139M	I_F = 5 mA, I_O = 15 mA, V_{CC} = 4.5 V		0.13	0.4	
		HCPL2731M			0.12		
		6N139M	I_F = 12 mA, I_O = 24 mA, V_{CC} = 4.5 V		0.18	0.4	
		HCPL2731M			0.17		

Notes:

3. Current Transfer Ratio is defined as a ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
4. Pin 7 open. (6N138M and 6N139M only)

Electrical Characteristics (Continued)

(V_{CC} = 5.0 V, T_A = 0°C to 70°C unless otherwise specified. Typical value is measured at T_A = 25°C.)

Switching Characteristics

Symbol	Parameter	Device	Test Conditions	Min.	Typ.	Max.	Unit
t_{PHL}	Propagation Delay Time to Logic LOW(4) (Fig. 15)	6N139M	R_L = 270 Ω, I_F = 12 mA		0.2	2	µs
		HCPL2730M, HCPL2731M	R_L = 270 Ω, I_F = 12 mA		0.5	3	
		6N138M	R_L = 2.2 kΩ, I_F = 1.6 mA		1.0	15	
		HCPL2730M, HCPL2731M	R_L = 2.2 kΩ, I_F = 1.6 mA		2.5	25	
		6N139M	R_L = 4.7 kΩ, I_F = 0.5 mA		2.5	30	
		HCPL2731M	R_L = 4.7 kΩ, I_F = 0.5 mA		8.4	120	
t_{PLH}	Propagation Delay Time to Logic HIGH(4) (Fig. 15)	6N139M	R_L = 270 Ω, I_F = 12 mA		1.3	10	µs
		HCPL2730M, HCPL2731M	R_L = 270 Ω, I_F = 12 mA		1.0	15	
		6N138M, HCPL2730M, HCPL2731M	R_L = 2.2 kΩ, I_F = 1.6 mA		7.3	50	
		6N139M, HCPL2731M	R_L = 4.7 kΩ, I_F = 0.5 mA		13.6	90	
$\|CM_H\|$	Common Mode Transient Immunity at Logic High(5) (Fig. 16)	All	I_F = 0 mA, $\|V_{CM}\|$ = 10 V_{P-P}, R_L = 2.2 kΩ, T_A = 25°C	1,000	10,000		V/µs
$\|CM_L\|$	Common Mode Transient Immunity at Logic Low(5) (Fig. 16)	All	I_F = 1.6 mA, $\|V_{CM}\|$ = 10 V_{P-P}, R_L = 2.2 kΩ, T_A = 25°C	1,000	10,000		V/µs

Note:

5. Common mode transient immunity in logic HIGH level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse signal V_{CM}, to assure that the output will remain in a logic HIGH state (i.e., V_O > 2.0 V). Common mode transient immunity in logic LOW level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a logic LOW state (i.e., V_O < 0.8 V).

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Electrical Characteristics (Continued)

Isolation Characteristics (T_A = 25°C unless otherwise specified.)

Symbol	Parameter	Device	Test Conditions	Min.	Typ.	Max.	Unit
V_{ISO}	Withstand Insulation Test Voltage[6][7]	All	RH ≤ 50%, T_A = 25°C, I_{I-O} ≤ 10 μA, t = 1 min, f = 50 Hz	5,000			VAC_{RMS}
R_{I-O}	Resistance (Input to Output)[6]	All	V_{I-O} = 500 V_{DC}		10^{11}		Ω
C_{I-O}	Capacitance (Input to Output)[6][8]	All	f = 1 MHz, V_{I-O} = 0 V		1		pF
I_{I-I}	Input-Input Insulation Leakage Current[9]	HCPL2730M, HCPL2731M	RH ≤ 45%, V_{I-I} = 500 V_{DC}, t = 5 sec		0.005		μA
R_{I-I}	Input-Input Resistance[9]	HCPL2730M, HCPL2731M	V_{I-I} = 500 V_{DC}		10^{11}		Ω
C_{I-I}	Input-Input Capacitance[9]	HCPL2730M, HCPL2731M	f = 1 MHz		0.03		pF

Notes:

6. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
7. 5000 VAC_{RMS} for 1 minute duration is equivalent to 6000 VAC_{RMS} for 1 second duration.
8. For dual channel devices, C_{I-O} is measured by shorting pins 1 and 2 or pins 3 and 4 together and pins 5 through 8 shorted together.
9. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

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Electrical Characteristics (Continued)

T_A = 25°C unless otherwise specified

Current Limiting Resistor Calculations:

$$R_1 \text{ (Non-Invert)} = \frac{V_{CC1} - V_{DF} - V_{OL1}}{I_F}$$

$$R_1 \text{ (Invert)} = \frac{V_{CC1} - V_{OH1} - V_{DF}}{I_F}$$

$$R_2 = \frac{V_{CC2} - V_{OLX} \text{ (@ } I_L - I_2)}{I_L}$$

Where:

V_{CC1} = Input Supply Voltage

V_{CC2} = Output Supply Voltage

V_{DF} = Diode Forward Voltage

V_{OL1} = Logic "0" Voltage of Driver

V_{OH1} = Logic "1" Voltage of Driver

I_F = Diode Forward Current

V_{OLX} = Saturation Voltage of Output Transistor

I_L = Load Current Through Resistor R_2

I_2 = Input Current of Output Gate

INPUT CONFIGURATION		R_1 (Ω)	R_2 (Ω) @ OUTPUT CONFIGURATION						
			CMOS @ 5 V	CMOS @ 10 V	74XX	74LXX	74SXX	74LSXX	74HXX
CMOS @ 5 V	NON-INV.	2000	1000	2200	750	1000	1000	1000	560
	INV.	510							
CMOS @ 10 V	NON-INV.	5100							
	INV.	4700							
74XX	NON-INV.	2200							
	INV.	180							
74LXX	NON-INV.	1800							
	INV.	100							
74SXX	NON-INV.	2000							
	INV.	360							
74LSXX	NON-INV.	2000							
	INV.	180							
74HXX	NON-INV.	2000							
	INV.	180							

Fig. 3 Resistor Values for Logic Interface

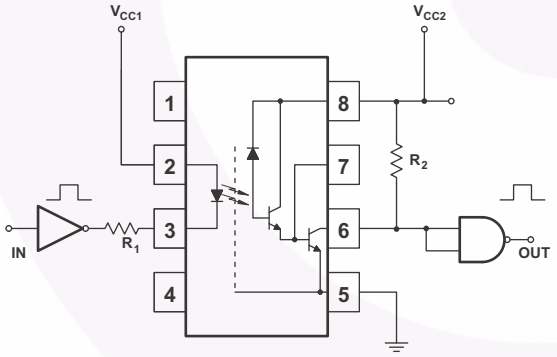


Fig. 4 Non-Inverting Logic Interface

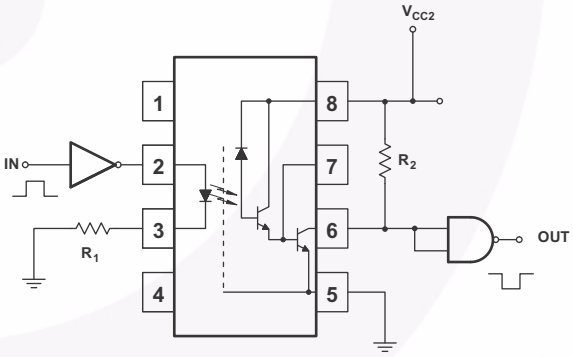


Fig. 5 Inverting Logic Interface

Typical Performance Curves

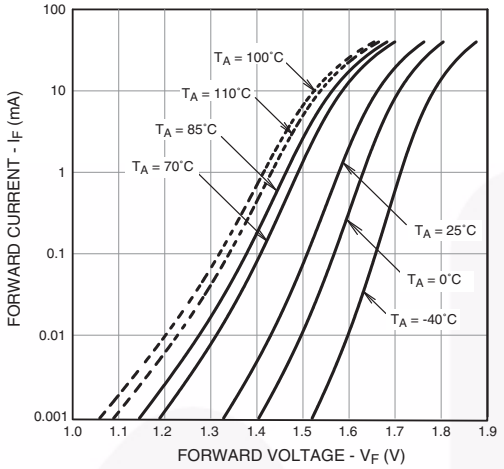


Fig. 6 LED Forward Current vs. Forward Voltage

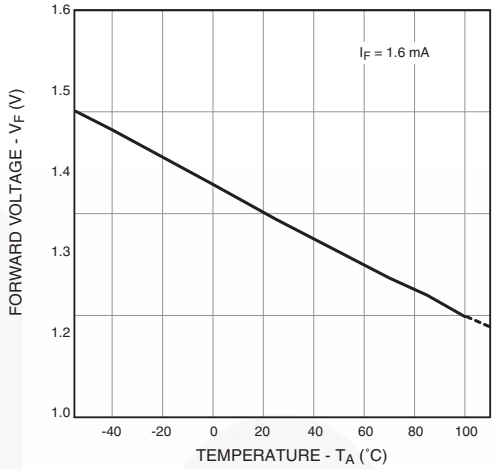


Fig. 7 LED Forward Voltage vs. Temperature

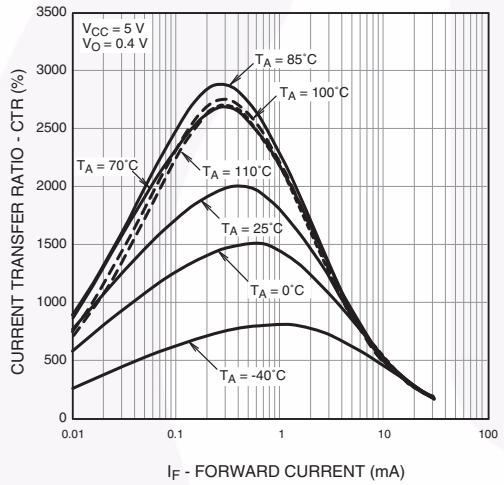


Fig. 8 Current Transfer Ratio vs. Forward Current (6N138M / 6N139M Only)

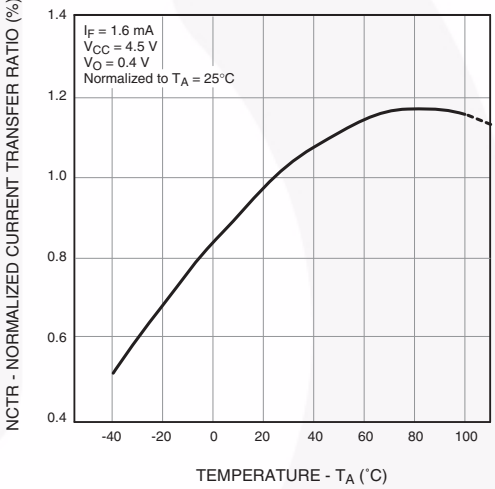


Fig. 9 Normalized Current Transfer Ratio vs. Ambient Temperature (6N138M / 6N139M Only)

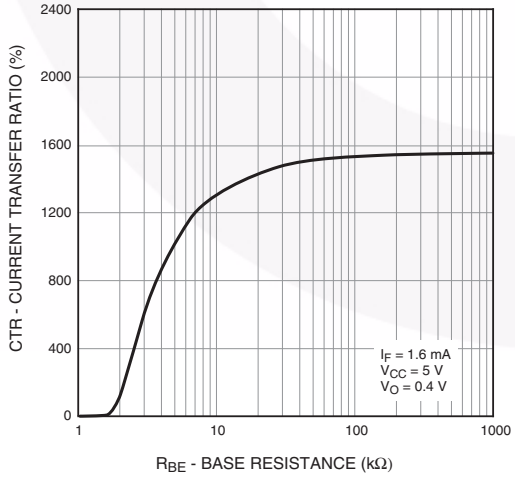


Fig. 10 Current Transfer Ratio vs. Base-Emitter Resistance (6N138M / 6N139M Only)

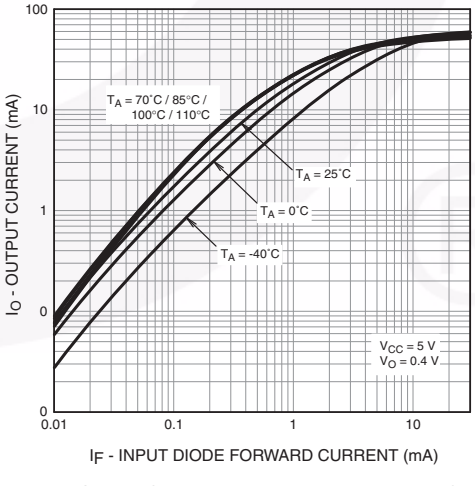


Fig. 11 Output Current vs. Input Diode Forward Current (6N138M / 6N139M Only)

Typical Performance Curves (Continued)

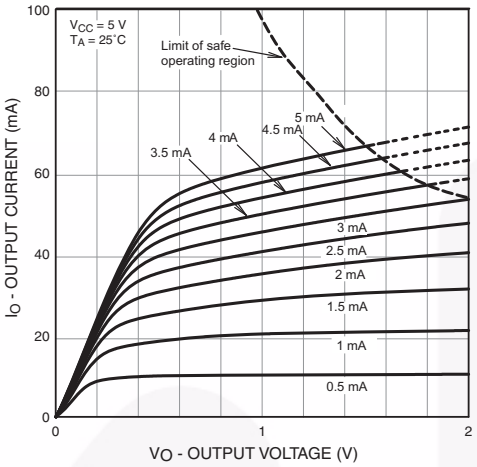


Fig. 12 Output Current vs Output Voltage (6N138M / 6N139M Only)

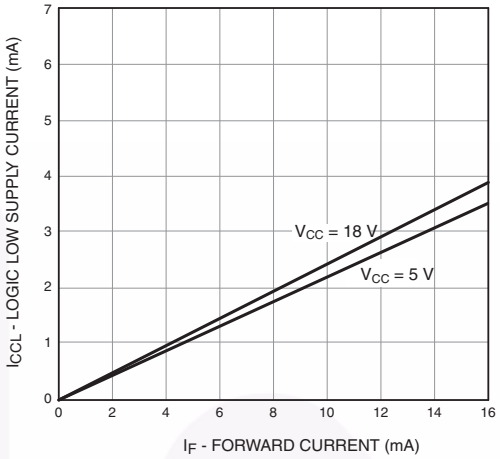


Fig. 13 Logic Low Supply Current vs. Input Diode Forward Current (6N138M / 6N139M Only)

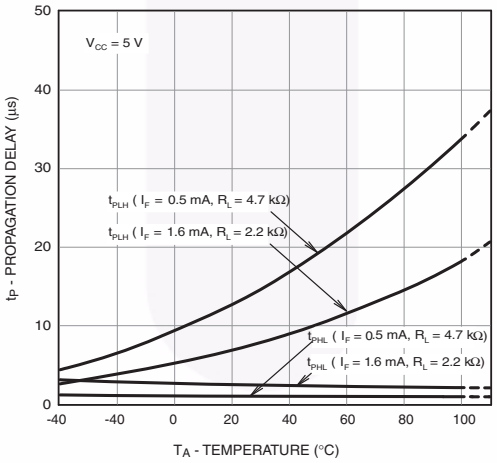


Fig. 14 Propagation Delay vs. Temperature (6N138M / 6N139M Only)

Test Circuits

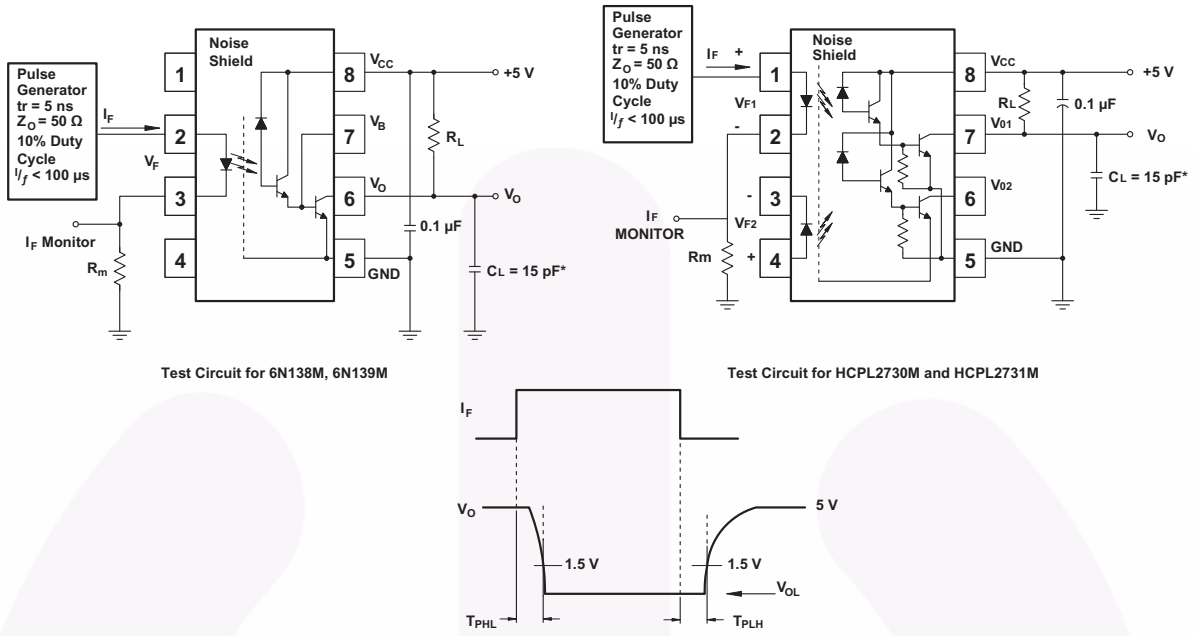


Fig. 15 Switching Time Test Circuit

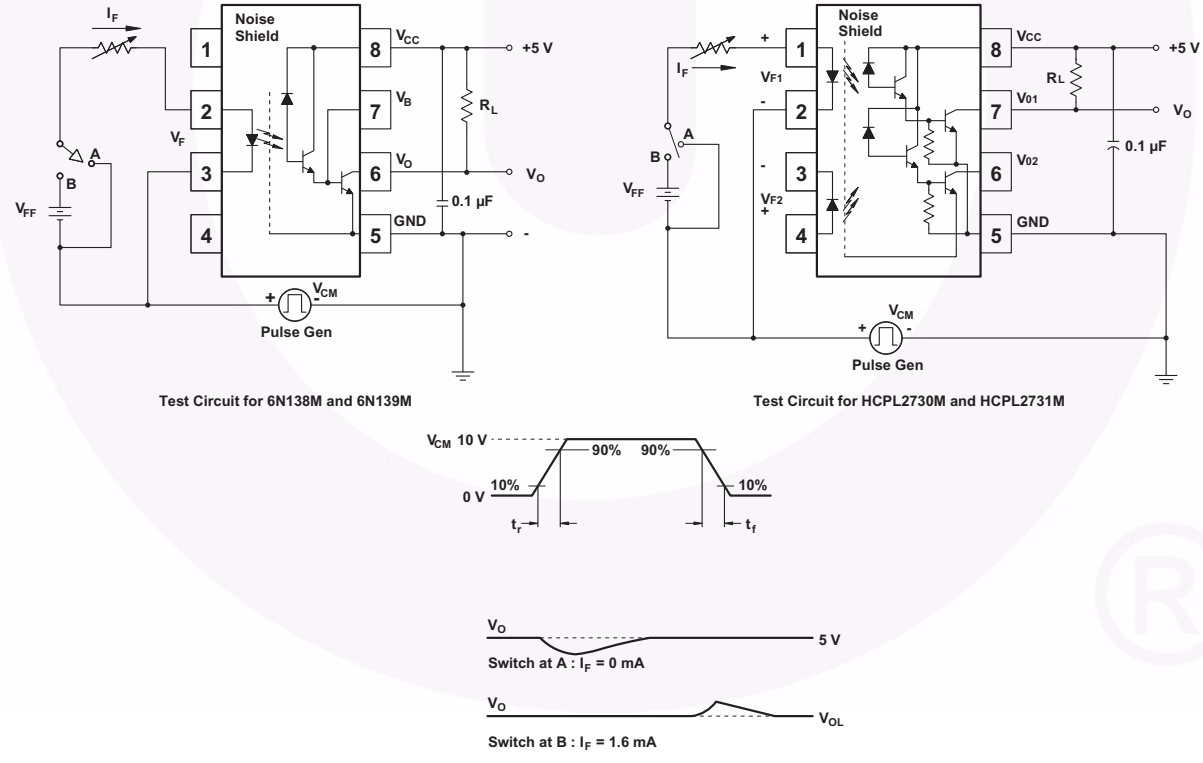
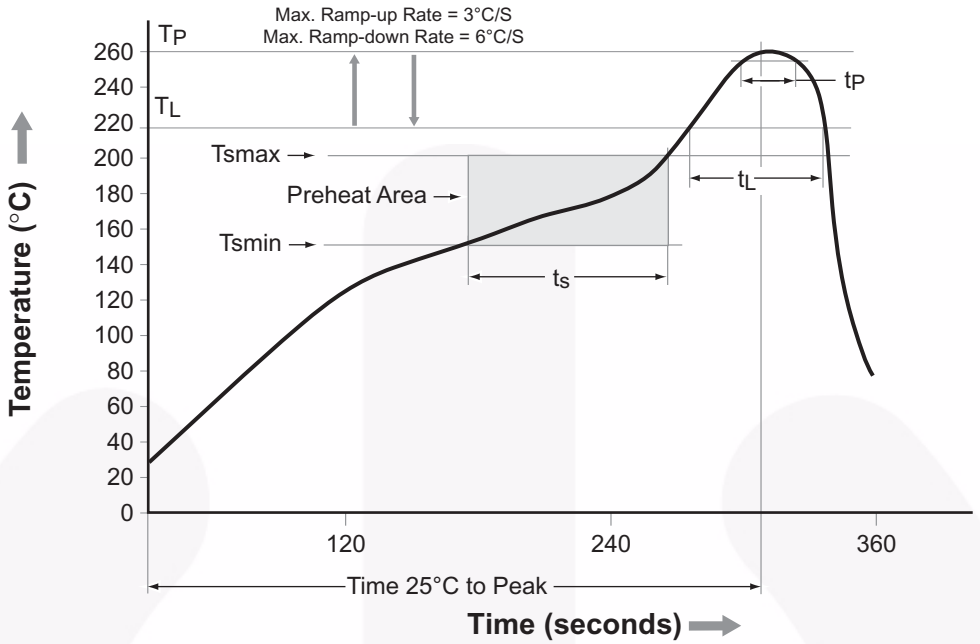


Fig. 16 Common Mode Immunity Test Circuit

Reflow Profile



Profile Freature	Pb-Free Assembly Profile
Temperature Min. (Tsmin)	150°C
Temperature Max. (Tsmax)	200°C
Time (t_S) from (Tsmin to Tsmax)	60–120 seconds
Ramp-up Rate (t_L to t_P)	3°C/second max.
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60–150 seconds
Peak Body Package Temperature	260°C +0°C / –5°C
Time (t_P) within 5°C of 260°C	30 seconds
Ramp-down Rate (T_P to T_L)	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

Ordering Information

Part Number	Package	Packing Method
6N138M	DIP 8-Pin	Tube (50 units per tube)
6N138SM	SMT 8-Pin (Lead Bend)	Tube (50 units per tube)
6N138SDM	SMT 8-Pin (Lead Bend)	Tape and Reel (1,000 units per reel)
6N138VM	DIP 8-Pin, DIN EN/IEC 60747-5-5 Option	Tube (50 units per tube)
6N138SVM	SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-5 Option	Tube (50 units per tube)
6N138SDVM	SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-5 Option	Tape and Reel (1,000 units per reel)
6N138TVM	DIP 8-Pin, 0.4” Lead Spacing, DIN EN/IEC 60747-5-5 Option	Tube (50 units per tube)
6N138TSVM	SMT 8-Pin, 0.4” Lead Spacing, DIN EN/IEC 60747-5-5 Option	Tube (50 units per tube)
6N138TSR2VM	SMT 8-Pin, 0.4” Lead Spacing, DIN EN/IEC 60747-5-5 Option	Tape and Reel (1,000 units per reel)

Note:
The product orderable part number system listed in this table also applies to the 6N139M, HCPL2730M and HCPL2731M product families.

Marking Information

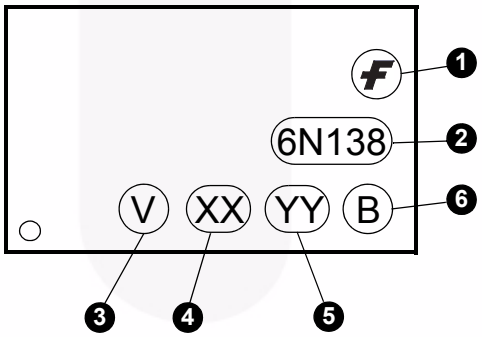
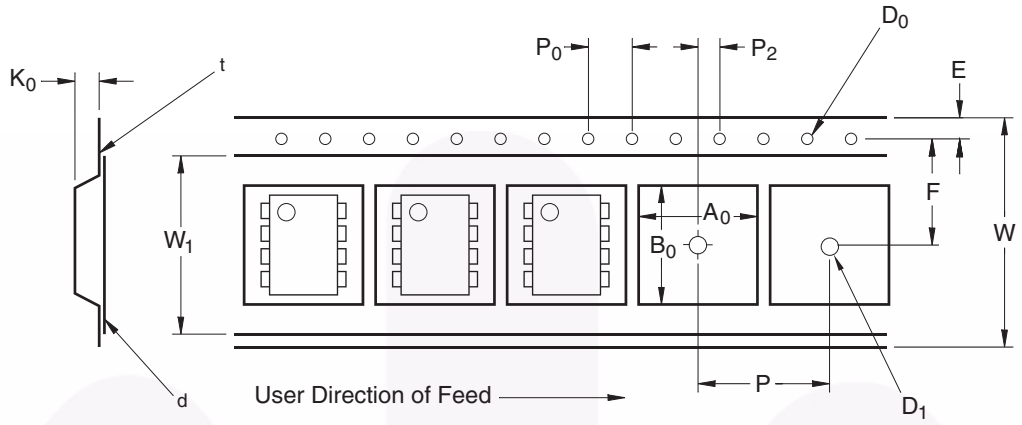


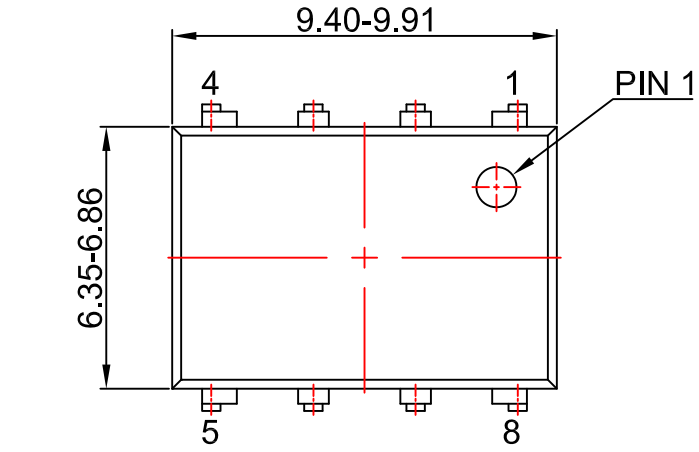
Figure 17. Top Mark

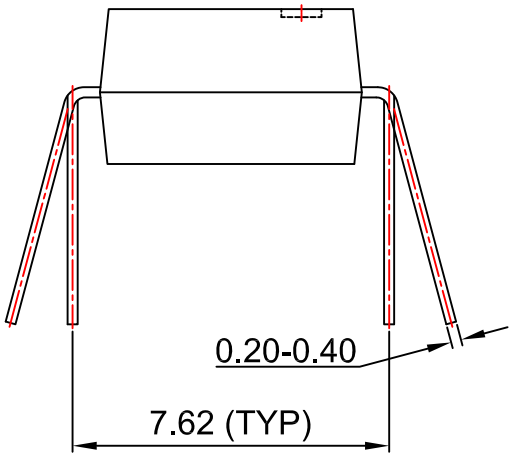
Definitions	
1	Fairchild Logo
2	Device Number
3	DIN EN/IEC60747-5-5 Option (only appears on component ordered with this option)
4	Two Digit Year Code, e.g., ‘16’
5	Two Digit Work Week Ranging from ‘01’ to ‘53’
6	Assembly Package Code

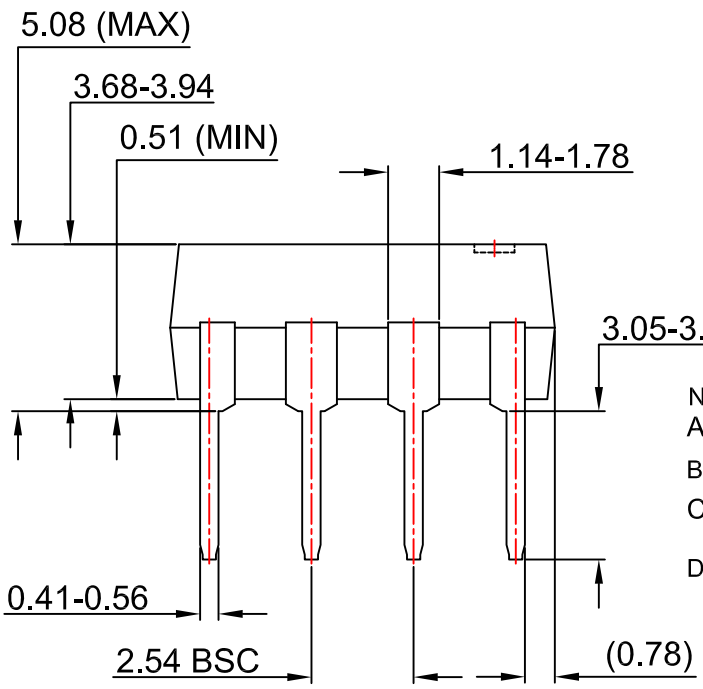
Carrier Tape Specifications (Option SD)



Symbol	Description	Dimension in mm
W	Tape Width	16.0 ± 0.3
t	Tape Thickness	0.30 ± 0.05
P_0	Sprocket Hole Pitch	4.0 ± 0.1
D_0	Sprocket Hole Diameter	1.55 ± 0.05
E	Sprocket Hole Location	1.75 ± 0.10
F	Pocket Location	7.5 ± 0.1
P_2		2.0 ± 0.1
P	Pocket Pitch	12.0 ± 0.1
A_0	Pocket Dimensions	10.30 ±0.20
B_0		10.30 ±0.20
K_0		4.90 ±0.20
W_1	Cover Tape Width	13.2 ± 0.2
d	Cover Tape Thickness	0.1 max
	Max. Component Rotation or Tilt	10°
R	Min. Bending Radius	30







NOTES:

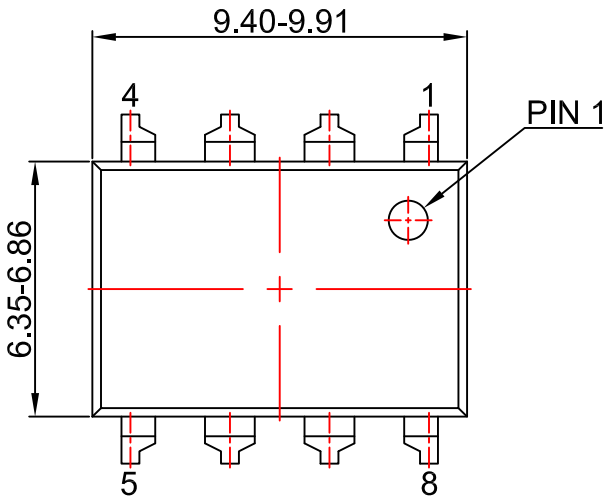
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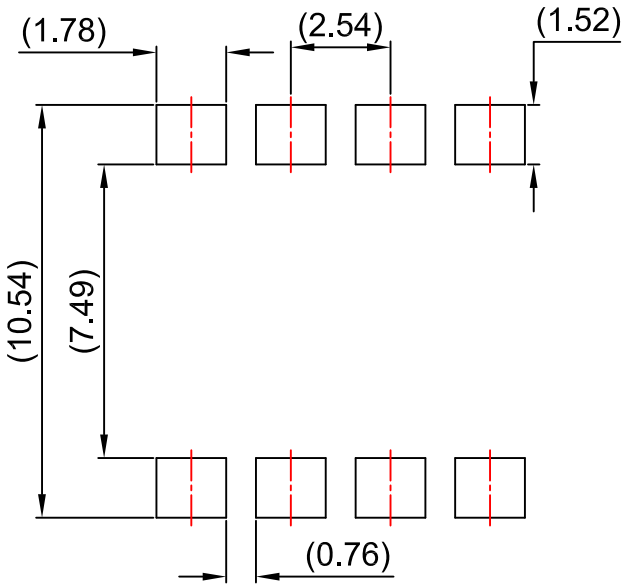
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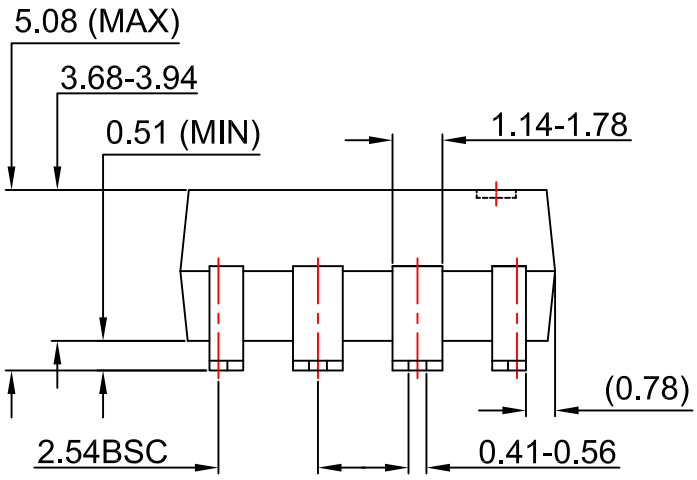
D) DRAWING FILENAME AND REVSION: MKT-N08GREV7

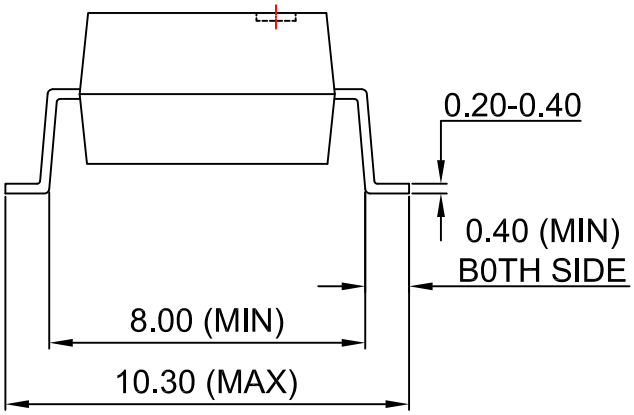
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LAND PATTERN RECOMMENDATION





NOTES:

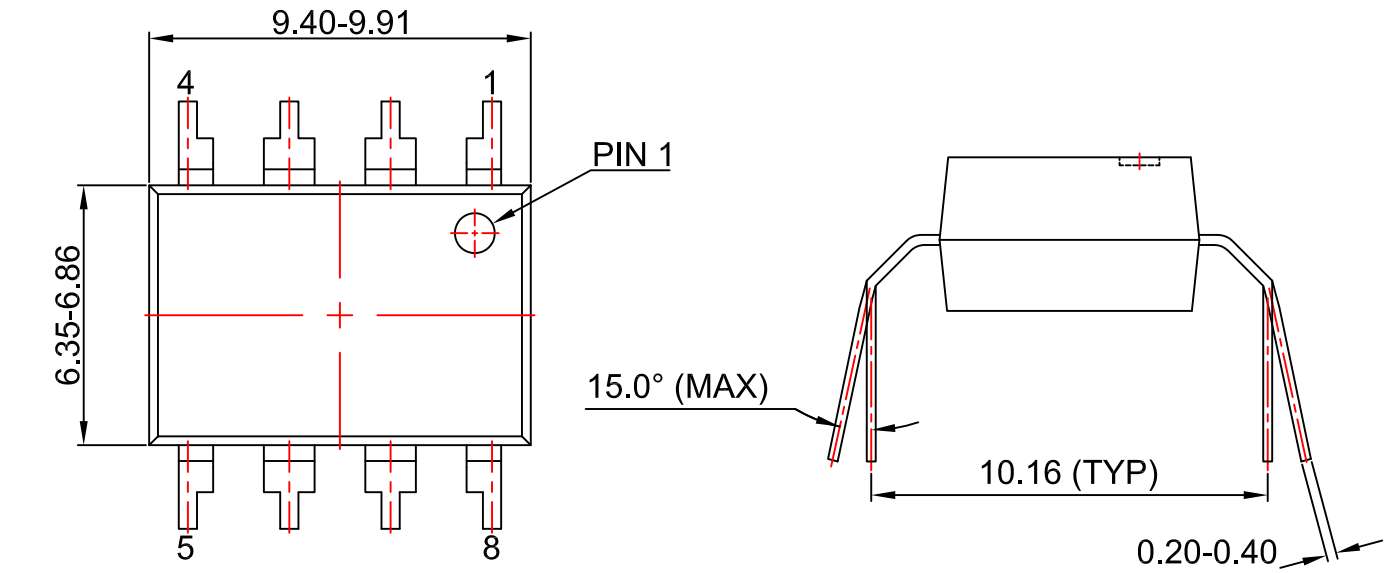
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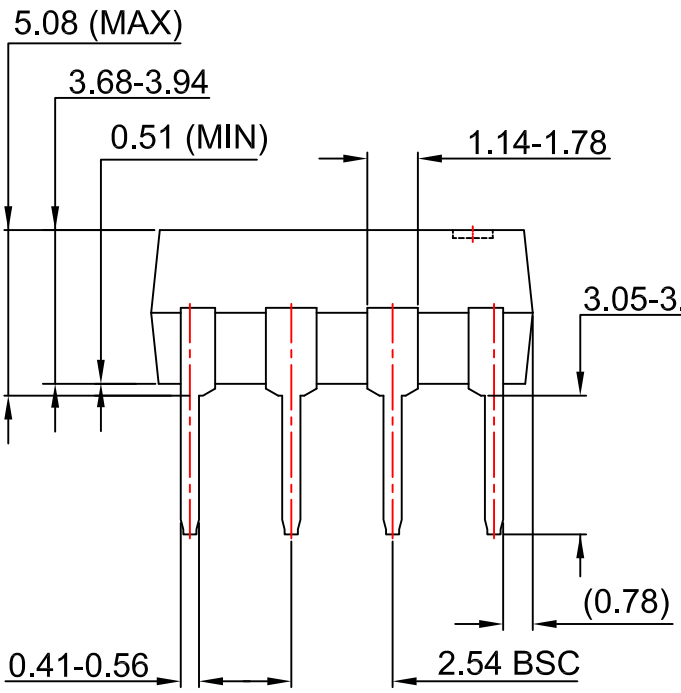
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C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION

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