*Click **here** for production status of specific part numbers.*

MAX22192

Octal Industrial Digital Input with Diagnostics and Digital Isolation

General Description

The MAX22192 is an IEC 61131-2 compliant industrial digital input device with integrated digital isolation. The MAX22192 translates eight, 24V current-sinking, industrial inputs to an isolated serialized SPI-compatible output that interfaces with 1.71V to 5.5V logic voltage. A current-setting resistor allows the MAX22192 to be configured for Type 1, Type 2, or Type 3 inputs. For proximity switches, the field-wiring is verified using the wire break feature. When wire break is enabled, the $\overline{\text{LFAULT}}$ output is asserted and a register flag set if the input current drops below the wire break threshold for more than 20ms. Additional diagnostics that assert $\overline{\text{LFAULT}}$ include: overtemperature protection, low 24V field supply, 24V field supply missing, and CRC communication error.

For robust operation in industrial environments, each input includes a programmable glitch filter. The filter delay on each channel can be independently programmed to one of eight values between 50µs and 20ms, or filter bypass.

The MAX22192 has an isolated 4-pin SPI interface, and in addition uses isolated $\overline{\text{LLATCH}}$ input for synchronizing input data across multiple devices in parallel, and isolated $\overline{\text{LFAULT}}$ output for instantly alerting the host of any diagnostic issues. The digital signals with a name starting with L are logic-side signals, and the digital signals with a name starting with F are field-side signals.

The MAX22192 field-side accepts a single 7V to 65V supply to the V_{DD24F} pin. When powered by the field supply, the MAX22192 generates a 3.3V output on the V_{DD3F} pin from an integrated LDO regulator, which can provide up to 25mA of current for external loads in addition to powering the MAX22192. Alternatively, the MAX22192 can be powered from a 3.0V to 5.5V supply connected to the V_{DD3F} pin. The logic-side of the MAX22192 is powered from a single 1.71V to 5.5V supply to the V_{DDL} pin to interface with 1.8V, 3.3V, or 5V logic levels.

The MAX22192 has an isolation rating of $600V_{RMS}$ for 60 seconds and is available in a 70-pin GQFN package with 2.3mm clearance and creepage. The package material has a minimum comparative tracking index (CTI) of 600V, which gives it a group I rating in creepage tables.

Benefits and Features

- High Integration Reduces BOM Count and Board Space
  - Eight Input Channels with Serializer
  - Integrated Isolation of $600V_{RMS}$ for 60s (V_{ISO})
  - Operates Directly from Field Supply (7V to 65V)
  - Compatible with 1.8V, 3.3V or 5V Logic
  - 6mm x 10mm GQFN Package
- Reduced Power and Heat Dissipation
  - Accurate Input-Current Limiters
  - Energyless Field-Side LED Drivers
- Fault Tolerant with Built-In Diagnostics
  - Input Protection to ±40V with Low-Input Leakage Current
  - Wire-Break Detection
  - Integrated Field-Supply Voltage Monitors
  - Integrated Overtemperature Monitors
  - 5-Bit CRC Code Generation for Error Detection
- Configurability Enables a Wide Range of Applications
  - Configurable IEC 61131-2 Type 1, 2, 3 Inputs
  - Configurable Input Current-Limiting from 0.5mA to 3.4mA
  - Selectable Input Glitch Filter
  - Capable of Daisy-Chaining Other Field-Side Devices Sharing Isolated SPI
- Robust Design
  - ±8kV Contact ESD and ±15kV Air-Gap ESD Using Minimum 1kΩ Resistor
  - ±1kV Surge Tolerant Using Minimum 1kΩ Resistor
  - -40°C to +125°C Ambient Operating Temperature

Applications

- Programmable Logic Controllers
- Industrial Automation
- Process Automation

Safety Regulatory Approvals

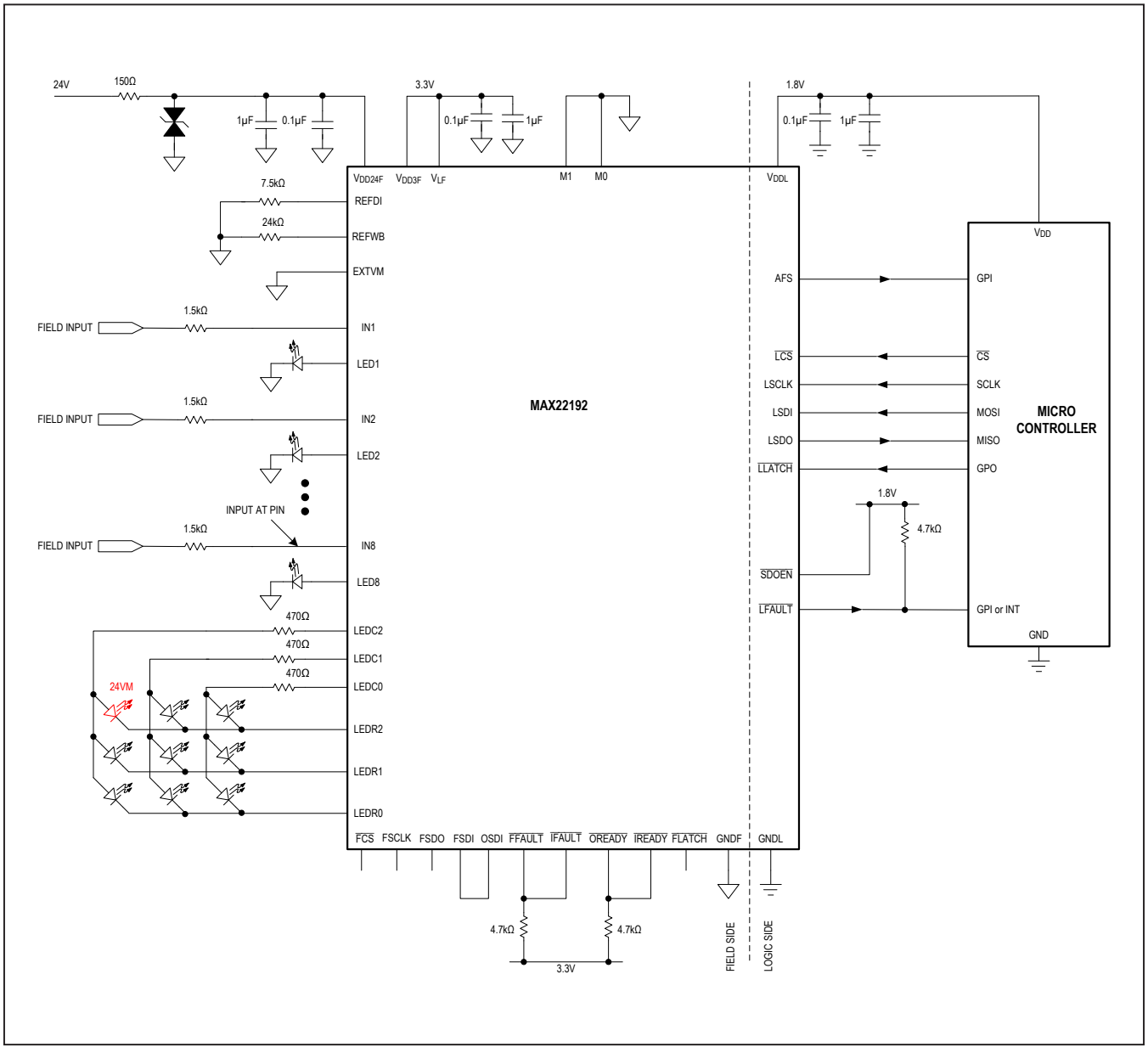
- UL According to UL1577
- cUL According to CSA Bulletin 5A

***Ordering Information** and **Typical Operating Circuits** appear at end of data sheet.*

19-100406; Rev 2; 3/19

maxim integrated™

Isolated Octal Digital Input



Absolute Maximum Ratings

V_{DD3F}, V_{LF} to GNDF .....-0.3V to +6V
V_{DD24F} to GNDF .....-0.3V to +70V
FSCLK, $\overline{FCS}$, OSDI, FSDO to GNDF .....-0.3V to (V_{LF} + 0.3V)
$\overline{FLATCH}$ to GNDF .....-0.3V to (V_{LF} + 0.3V)
FSDI, $\overline{IFAULT}$, $\overline{IREADY}$ to GNDF .....-0.3V to +6V
$\overline{OREADY}$, $\overline{FFAULT}$ to GNDF .....-0.3V to +6V
LEDC_, LEDR_ to GNDF ..... -0.3V to (V_{DD3F} + 0.3V)
REFWB, REFDI to GNDF ..... -0.3V to (V_{DD3F} + 0.3V)
M1, M0, EXTVM to GNDF.....-0.3V to +6V
IN1 – IN8 to GNDF.....-40V to +40V
LED1 – LED8 to GNDF.....-0.3V to +6V
V_{DDL} to GNDL.....-0.3V to +6V
LSCLK, $\overline{LCS}$, LSDI, $\overline{LLATCH}$, $\overline{SDOEN}$ to GNDL ....-0.3V to +6V
$\overline{LFAULT}$ to GNDL.....-0.3V to +6V
LSDO, AFS to GNDL.....-0.3V to (V_{DDL} + 0.3V)
Maximum Current for All Digital Output Pins.....20mA
Continuous Power Dissipation (70-GQFN)
Multilayer Board T_A = +70°C.....2286mW
Derate above +70°C.....28.6mW/°C
Operating Temperature Range..... -40°C to +125°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 70 GQFN	
Package Code	R70610M+1
Outline Number	**21-100252**
Land Pattern Number	**90-100111**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	35°C/W
Junction to Case (θ_{JC})	2.9°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

DC Electrical Characteristics

V_{LF} - V_{GNDF} = +3.0V to +5.5V, V_{DD3F} - V_{GNDF} = +3.0V to +5.5V, V_{DD24F} - V_{GNDF} = +7V to +65V, V_{DDL} - V_{GNDL} = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{LF} - V_{GNDF} = +3.3V, V_{DD3F} - V_{GNDF} = +3.3V, V_{DD24F} - V_{GNDF} = +24V, V_{DDL} - V_{GNDL} = +3.3V, $V_{IN\_}$ = +24V, C_L = 15pF and T_A = +25°C. (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
Supply Voltage	V_{DD24F}	Normal operation		7		65	V
	V_{DD3F}	Powered from an external supply, V_{DD24F} unconnected		3.0		5.5	
Field Logic Supply Voltage	V_{LF}	Referenced to GNDF		3.0		5.5	V
Logic Supply Voltage	V_{DDL}	Referenced to GNDL		1.71		5.5	V
Field Supply Current of V_{DD24F}	I_{DD24F}	V_{DD24F} = 24V	IN1 to IN8 = 0V, LED1 to LED8 = GNDF, SPI static, REFDI = 7.5kΩ, REFWB = 24kΩ		0.6	1.2	mA
Field Supply Current Powered From V_{DD3F}	I_{DD3F}	V_{DD3F} = 3.3V, V_{DD24F} unconnected	IN1 to IN8 = 0V, LED1 to LED8 = GNDF, SPI static, REFDI = 7.5kΩ, REFWB = 24kΩ		0.6	1.2	mA
Field Logic Supply Current	I_{LF}	V_{LF} - V_{GNDF} = 5.5V	$\overline{LCS}$ = V_{DDL}, All logic pins static			2	mA
Logic Supply Current	I_{DDL}	V_{DDL} - V_{GNDL} = 5.5V	$\overline{LCS}$ = V_{DDL}, All logic pins static		1.5	2	mA
V_{DD3F} Undervoltage-Lockout Threshold	V_{UVLO}	V_{DD3F} Rising		2.4		2.9	V
V_{DD3F} Undervoltage-Lockout Threshold Hysteresis	V_{UVHYST}				0.07		V
V_{DD24F} Undervoltage-Lockout Threshold	$V_{UVLO24F}$	V_{DD24F} Rising		6		6.8	V
V_{DD24F} Undervoltage-Lockout Threshold Hysteresis	$V_{UVHYST24F}$				0.5		V
V_{LF} Undervoltage-Lockout Threshold	$V_{UVLOVLF}$	V_{LF} Rising		0.9		1.66	V
V_{LF} Undervoltage-Lockout Threshold Hysteresis	$V_{UVHYSTVLF}$				0.07		V
V_{DDL} Undervoltage-Lockout Threshold	V_{UVLOVL}	V_{DDL} Rising		1.5	1.6	1.66	V
V_{DDL} Undervoltage-Lockout Threshold Hysteresis	$V_{UVHYSTVL}$				45		mV
Regulator Output Voltage	V_{DD3F}	I_{LOAD} = 1mA		3.0	3.3	3.6	V
Line Regulation	$dV_{DD3FLINE}$	I_{LOAD} = 1mA, V_{DD24F} = 12V to 24V			0		mV
Load Regulation	$dV_{DD3FLOAD}$	I_{LOAD} = 1mA to 10mA, V_{DD24F} = 24V			4		mV

DC Electrical Characteristics (continued)

V_{LF} - V_{GNDF} = +3.0V to +5.5V, V_{DD3F} - V_{GNDF} = +3.0V to +5.5V, V_{DD24F} - V_{GNDF} = +7V to +65V, V_{DDL} - V_{GNDL} = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{LF} - V_{GNDF} = +3.3V, V_{DD3F} - V_{GNDF} = +3.3V, V_{DD24F} - V_{GNDF} = +24V, V_{DDL} - V_{GNDL} = +3.3V, $V_{IN\_}$ = +24V, C_L = 15pF and T_A = +25°C. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Regulator Current Capability	I_{DD3F_CC}				25	mA
Short-Circuit Current Limit	I_{DD24F_SC}	V_{DD24F} current when V_{DD3F} shorted to GNDF, V_{DD24F} = 12V	28		50	mA
Field-Side $\overline{\text{OREADY}}$ Threshold	$V_{\overline{\text{OREADY}}}$	V_{DD3F} Rising, V_{DD24F} Floating	2.4		2.9	V
Field-Side $\overline{\text{OREADY}}$ Threshold Hysteresis	$V_{\overline{\text{OREADY}}\_HYST}$			0.07		V
Field-Side $\overline{\text{OREADY}}$ Delay	$t_{D\_\overline{\text{OREADY}}}$	V_{DD3F} valid to $\overline{\text{OREADY}}$ low		1		ms
Logic-Side AFS Delay	t_{D_AFS}	$\overline{\text{IREADY}}$ low to AFS high		100		µs
		$\overline{\text{IREADY}}$ high to AFS low		100		
SUPPLY ALARMS						
V_{DD24F} UV Alarm On/Off	$V_{ALRMOFFUV}$	V_{DD24F} Rising, Undervoltage			17	V
V_{DD24F} UV Alarm Off/On	$V_{ALRMONUV}$	V_{DD24F} Falling, Undervoltage	15			V
Glitch Filter for V_{DD24F} UV				3		µs
V_{DD24F} VM Alarm On/Off	$V_{ALRMOFFVM}$	V_{DD24F} Rising, Missing Voltage			13.9	V
V_{DD24F} VM Alarm Off/On	$V_{ALRMONVM}$	V_{DD24F} Falling, Missing Voltage	12.1			V
Glitch Filter for V_{DD24F} VM				3		µs
EXTVM Threshold UV On/Off	$V_{EXTOFFUV}$	EXTVM Voltage Rising, Undervoltage	0.96	1	1.04	V
EXTVM Threshold UV Off/On	$V_{EXTONUV}$	EXTVM Voltage Falling, Undervoltage	0.93	0.97	1.01	V
EXTVM Threshold VM On/Off	$V_{EXTOFFVM}$	EXTVM Voltage Rising, Missing Voltage	0.77	0.81	0.84	V
EXTVM Threshold VM Off/On	$V_{EXTONVM}$	EXTVM Voltage Falling, Missing Voltage	0.74	0.79	0.82	V
EXTVM Selection Threshold	$EXTVM_{SEL}$			0.3		V
EXTVM Selectable V_{DD24F} Threshold	$EXTVM_{VDD24F}$		10		30	V
EXTVM Leakage Current	I_{L_EXTVM}		-1		+1	µA
TEMPERATURE ALARMS						
Overtemperature Alarm 1	T_{ALRM1}	ALRMT1 bit set in FAULT1 register		115		°C
Overtemperature Alarm 2	T_{ALRM2}	ALRMT2 bit set in FAULT1 register		140		°C
Overtemperature Alarm Hysteresis	T_{ALRM_HYS}			10		°C
Thermal-Shutdown Threshold	T_{SHDN}	OTSHDN bit set in FAULT2 register		165		°C
Thermal-Shutdown Hysteresis	T_{SHDN_HYS}			10		°C

DC Electrical Characteristics (continued)

V_{LF} - V_{GNDF} = +3.0V to +5.5V, V_{DD3F} - V_{GNDF} = +3.0V to +5.5V, V_{DD24F} - V_{GNDF} = +7V to +65V, V_{DDL} - V_{GNDL} = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{LF} - V_{GNDF} = +3.3V, V_{DD3F} - V_{GNDF} = +3.3V, V_{DD24F} - V_{GNDF} = +24V, V_{DDL} - V_{GNDL} = +3.3V, $V_{IN\_}$ = +24V, C_L = 15pF and T_A = +25°C. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
WIRE-BREAK ALARMS						
REFWB Wire-Break Voltage	V_{REFWB}	R_{REFWB} = 5.2kΩ to 50kΩ		0.61		V
REFWB Wire-Break Resistor	R_{REFWB}	Nominal value	5.2		50	kΩ
Wire-Break Current Range	I_{REFWB}	R_{REFWB} = 5.2kΩ	400	470	510	µA
		R_{REFWB} = 50kΩ	40	47	60	
PCB FAULT ALARMS						
REFWB Pin Short Threshold	I_{REFWBS}	RFWBS bit set in FAULT2 register		550		µA
REFWB Pin Open Threshold	I_{REFWBO}	RFWBO bit set in FAULT2 register		6.6		µA
REFDI Pin Short Threshold	I_{REFDIS}	RFDIS bit set in FAULT2 register		550		µA
REFDI Pin Open Threshold	I_{REFDIO}	RFDIO bit set in FAULT2 register		6.6		µA
IC INPUTS (TYPES 1, 2, 3)						
Input Threshold Low-to-High	V_{THP+}	IN1 to IN8			6	V
Input Threshold High-to-Low	V_{THP-}	IN1 to IN8	4.4			V
Input Threshold Hysteresis	$V_{INPHYST}$	IN1 to IN8		0.8		V
LED On-State Current	I_{LEDON}	R_{REFDI} = 7.5kΩ, V_{LED} = 3V	1.5			mA
LED On-State Voltage	V_{LEDON}				3	V
DI Leakage, Current Sources Disabled	I_{DI_LEAK}	IN1 to IN8 = 36V		73		µA
		IN1 to IN8 = 24V		42		
FIELD INPUTS						
REFDI Pin Voltage	V_{REFDI}	R_{REFDI} from 5.2kΩ to 36kΩ		0.61		V
REFDI Current-Limit Resistor	R_{REFDI}	Nominal value	5.2		36	kΩ
Current-Limit Setting	I_{INLIM}	R_{REFDI} = 5.2kΩ		3.39		mA
		R_{REFDI} = 7.5kΩ		2.35		
		R_{REFDI} = 36kΩ		0.48		
TYPE 1 and 3: External Series Resistor R_{IN} = 1.5kΩ, R_{REFDI} = 7.5kΩ, Wire-Break Detection Off, unless otherwise noted						
Input Current Limit	I_{INLIM}	28V > $V_{IN\_}$ at the pin > 5V, LED on, R_{REFDI} = 7.5kΩ (Note 2)	2.10	2.35	2.60	mA
Field Input Threshold Low-to-High	V_{INF+}	R_{REFDI} = 7.5kΩ, R_{IN} = 1.5kΩ external series resistor			9.9	V
Field Input Threshold High-to-Low	V_{INF-}	R_{REFDI} = 7.5kΩ, R_{IN} = 1.5kΩ external series resistor	7.4			V
Field Input Threshold Hysteresis	$V_{INFHYST}$	R_{REFDI} = 7.5kΩ, R_{IN} = 1.5kΩ external series resistor		0.9		V

DC Electrical Characteristics (continued)

V_{LF} - V_{GNDF} = +3.0V to +5.5V, V_{DD3F} - V_{GNDF} = +3.0V to +5.5V, V_{DD24F} - V_{GNDF} = +7V to +65V, V_{DDL} - V_{GNDL} = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{LF} - V_{GNDF} = +3.3V, V_{DD3F} - V_{GNDF} = +3.3V, V_{DD24F} - V_{GNDF} = +24V, V_{DDL} - V_{GNDL} = +3.3V, $V_{IN\_}$ = +24V, C_L = 15pF and T_A = +25°C. (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TYPE 2: External Series Resistor R_{IN} = 1kΩ, R_{REFDI} = 5.2kΩ, Wire-Break Detection Off, unless otherwise noted							
Input Current Limit	I_{INLIM}	28V > $V_{IN\_}$ at the pin > 5V, LED on, R_{REFDI} = 5.2kΩ (Note 2)		3.05	3.39	3.71	mA
Field Input Threshold Low-to-High	V_{INF+}	R_{REFDI} = 5.2kΩ, R_{IN} = 1kΩ external series resistor				9.9	V
Field Input Threshold High-to-Low	V_{INF-}	R_{REFDI} = 5.2kΩ, R_{IN} = 1kΩ external series resistor		7.4			V
Field Input Threshold Hysteresis	$V_{INFHYST}$	R_{REFDI} = 5.2kΩ, R_{IN} = 1kΩ external series resistor			0.9		V
FILTER DELAY							
Input Filter Delay (See DELAY[2:0] bits in FLT_ Registers)	t_{BOUNCE}	FBP = 1: bypass filtering			2		µs
		FBP = 0, DELAY = 0			0.05		ms
		FBP = 0, DELAY = 1			0.1		
		FBP = 0, DELAY = 2			0.4		
		FBP = 0, DELAY = 3			0.8		
		FBP = 0, DELAY = 4			1.6		
		FBP = 0, DELAY = 5			3.2		
		FBP = 0, DELAY = 6			12.8		
		FBP = 0, DELAY = 7			20		
Wire-Break Filter Delay	t_{WBD}				20		ms
LOGIC INTERFACE (FIELD-SIDE AND LOGIC-SIDE)							
Input High Voltage	V_{IH}	$\overline{LCS}$, LSCLK, LSDI, $\overline{LLATCH}$, $\overline{SDOEN}$, relative to GNDL	2.25V ≤ V_{DDL} ≤ 5.5V	0.7 x V_{DDL}			V
			1.71V ≤ V_{DDL} < 2.25V	0.75 x V_{DDL}			
		M1, M0, FSDI, $\overline{IFAULT}$, $\overline{IREADY}$, $\overline{FCS}$, FSCLK, FSDO, $\overline{FLATCH}$ relative to GNDF		0.7 x V_{LF}			
Input Low Voltage	V_{IL}	$\overline{LCS}$, LSCLK, LSDI, $\overline{LLATCH}$, $\overline{SDOEN}$, relative to GNDL	2.25V ≤ V_{DDL} ≤ 5.5V			0.8	V
			1.71V ≤ V_{DDL} < 2.25V			0.7	
		M1, M0, FSDI, $\overline{IFAULT}$, $\overline{IREADY}$, $\overline{FCS}$, FSCLK, FSDO, $\overline{FLATCH}$ relative to GNDF				0.3 x V_{LF}	
Output High Voltage (Note 3)	V_{OH}	$\overline{FCS}$, FSCLK, FSDO, OSDI, $\overline{FLATCH}$, relative to GNDF, 4mA source		V_{LF} - 0.4			V
		AFS, LSDO, relative to GNDL, 4mA source		V_{DDL} - 0.4			

DC Electrical Characteristics (continued)

V_{LF} - V_{GNDF} = +3.0V to +5.5V, V_{DD3F} - V_{GNDF} = +3.0V to +5.5V, V_{DD24F} - V_{GNDF} = +7V to +65V, V_{DDL} - V_{GNDL} = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{LF} - V_{GNDF} = +3.3V, V_{DD3F} - V_{GNDF} = +3.3V, V_{DD24F} - V_{GNDF} = +24V, V_{DDL} - V_{GNDL} = +3.3V, $V_{IN\_}$ = +24V, C_L = 15pF and T_A = +25°C. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Low Voltage (Note 3)	V_{OL}	$\overline{FCS}$, FSCLK, FSDO, OSDI, $\overline{FLATCH}$, $\overline{FFAULT}$, $\overline{OREADY}$, relative to GNDF, 4mA source			0.4	V
		AFS, LSDO, $\overline{LFAULT}$, relative to GNDL, 4mA source			0.4	
Input Pullup Resistance	R_{PU}	$\overline{FCS}$, $\overline{FLATCH}$, relative to GNDF		195		kΩ
Input Pulldown Resistance	R_{PD}	FSCLK, FSDI, M1, M0, relative to GNDF		195		
Input Pullup Current (Note 3)	I_{PU}	$\overline{IREADY}$ pullup to V_{LF}, $\overline{LCS}$, $\overline{LLATCH}$, $\overline{SDOEN}$ pullup to V_{DDL}	-10	-5	-1.5	µA
Input Pulldown Current (Note 3)	I_{PD}	FSDO, $\overline{IFAULT}$ pulldown to GNDF, LSCLK, LSDI pulldown to GNDL	1.5	5	10	µA
Output High-Impedance Leakage Current (Note 3)	I_{OL}	$\overline{FFAULT}$, $\overline{OREADY}$, relative to GNDF, LSDO, $\overline{LFAULT}$, relative to GNDL	-1		+1	µA
LED/GPO DRIVER (LEDR_, LEDC_)						
Output High Voltage	V_{OH_LED}	LED on, I_{LED} = 5mA	V_{LF} - 0.3			V
Output Low Voltage	V_{OL_LED}	LED on, I_{LED} = 5mA			0.3	V
LED Driver Scan Rate	f_{LED}			1		kHz

Dynamic Electrical Characteristics

V_{LF} - V_{GNDF} = +3.0V to +5.5V, V_{DD3F} - V_{GNDF} = +3.0V to +5.5V, V_{DD24F} - V_{GNDF} = +7V to +65V, V_{DDL} - V_{GNDL} = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{LF} - V_{GNDF} = +3.3V, V_{DD3F} - V_{GNDF} = +3.3V, V_{DD24F} - V_{GNDF} = +24V, V_{DDL} - V_{GNDL} = +3.3V, $V_{IN\_}$ = +24V, C_L = 15pF and T_A = +25°C. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FIELD INPUT SAMPLING						
Field Input Sampling Rate	f_{IN}	Input Filter Bypass Mode		1000		kHz
		Input Filter Delay Mode		200		
Minimum Detectable Field Input Pulse Width	t_{PW}	No External Capacitors on Pins IN1 to IN8 (Note 2)		3		µs
$\overline{LLATCH}$ Delay	$t_{\overline{LLATCH}}$	Assertion of $\overline{LLATCH}$ or $\overline{LCS}$ until input data is frozen		75		ns
$\overline{LFAULT}$ Minimum Pulse Width	$t_{PW\_\overline{LFAULT}}$	$\overline{LFAULT}$ low, pullup 4mA	0.8			µs
DIGITAL ISOLATION						
Common-Mode Transient Immunity	CMTI	I_ = GND_ (Note 4)		50		kV/µs

Dynamic Electrical Characteristics (continued)

V_{LF} - V_{GNDF} = +3.0V to +5.5V, V_{DD3F} - V_{GNDF} = +3.0V to +5.5V, V_{DD24F} - V_{GNDF} = +7V to +65V, V_{DDL} - V_{GNDL} = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{LF} - V_{GNDF} = +3.3V, V_{DD3F} - V_{GNDF} = +3.3V, V_{DD24F} - V_{GNDF} = +24V, V_{DDL} - V_{GNDL} = +3.3V, $V_{IN\_}$ = +24V, C_L = 15pF and T_A = +25°C. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI CHARACTERISTICS						
LSCLK Data Rate	DR_{MAX}				5	MHz
LSCLK Pulse Width-High	t_{LSCLKH}	See Figure 1	20			ns
LSCLK Pulse Width-Low	t_{LSCLKL}	See Figure 1	20			ns
LSCLK Clock Period	t_{LSCLK}	See Figure 1	120			ns
$\overline{LCS}$ Pulse Width	$t_{\overline{LCS}PW}$	See Figure 1	20			ns
LSDI-to-LSCLK Setup Time	t_{LSDISU}	See Figure 1	5			ns
LSDI-to-LSCLK Hold Time	t_{LSDIH}	See Figure 1	15			ns
$\overline{LCS}$-Fall-to-LSCLK Rise Time	t_{LSCLK_SU}	See Figure 1	80			ns
LSCLK-Rise-to-$\overline{LCS}$ Rise Time	$t_{\overline{LCS}H}$	Rising edge of LSCLK to rising edge of $\overline{LCS}$ (Figure 1)	40			ns
LSDO Enable Time	$t_{\overline{LCS}\_LSDO\_VALID}$	$\overline{LCS}$ falling to LSDO valid (Figure 1)			70	ns
LSDO Disable Time	$t_{\overline{LCS}\_LSDO\_TRI}$	$\overline{LCS}$ rising to LSDO High-Z (Figure 1)			70	ns
Output Data Propagation Delay	t_{DO}	LSCLK falling to LSDO valid (Figure 1)		43	60	ns
LSDO Rise Time	t_R	LSDO 10% to 90% rising		4		ns
LSDO Fall Time	t_F	LSDO 90% to 10% falling		4		ns

Note 1: All units are production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

Note 2: External resistor REFDI is selected to set any desired current limit between 0.48mA and 3.39mA (typical values). The current limit accuracy of ±11% is guaranteed for values greater or equal to 2mA.

Note 3: All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to their respective ground (GNDF and GNDL), unless otherwise noted.

Note 4: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDF and GNDL.

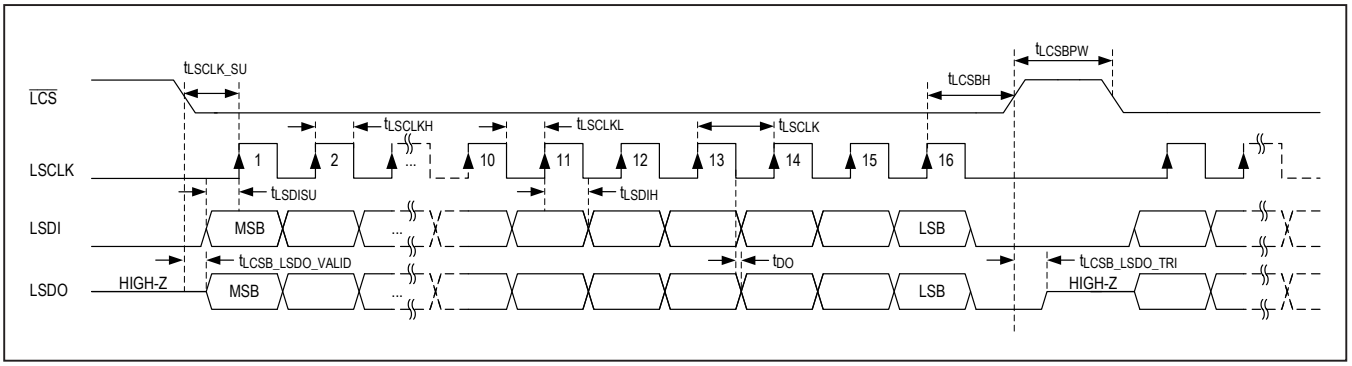


Figure 1. SPI Timing Diagram

Insulation Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Maximum Withstand Isolation Voltage	V_{ISO}	f_{SW} = 60Hz, duration = 60s (Note 5, 6)	600	V_{RMS}
Insulation Resistance	R_{IO}	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^{9}	
Barrier Capacitance Field-Side to Logic-Side	CIO	f_{SW} = 1MHz (Note 7)	2	pF
Minimum Creepage Distance	CPG		2.3	mm
Minimum Clearance Distance	CLR		2.3	mm
Internal Clearance		Distance through insulation	0.015	mm
Comparative Tracking Index	CTI	Material Group I (IEC 60112)	> 600	
Climate Category			40/125/21	
Pollution Degree (Table 1 of DIN VDE 0110)			2	

Note 5: V_{ISO} is defined by the IEC 60747-5-5 standard.
Note 6: Product is qualified at V_{ISO} for 60s and 100% production tested at 120% of V_{ISO} for 1s.
Note 7: Capacitance is measured with all logic pins on field-side and logic-side tied together.

ESD Protection

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
ESD		Human Body Model, All Field-Side Pins Referenced to GNDF, All Logic-Side Pins Referenced to GNDL	±2	kV

ESD and EMC Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Surge	Line-to-Line	IEC 61000-4-5, 1.2/50µs pulse, minimum 1kΩ resistor in series with IN1 - IN8, with respect to GNDF	±2	kV
	Line-to-GNDF	IEC 61000-4-5, 1.2/50µs pulse, minimum 1kΩ resistor in series with IN1 - IN8, with respect to GNDF	±1	
ESD	Contact	IEC 61000-4-2, minimum 1kΩ resistor in series with IN1- IN8, with respect to GNDF	±8	kV
	Air-Gap	IEC 61000-4-2, minimum 1kΩ resistor in series with IN1- IN8, with respect to GNDF	±15	

Safety Regulatory Approvals

UL
The MAX22192 are certified under UL1577. For more details, refer to File E351759.
Rated up to 600V_{RMS} isolation voltage for single protection.
CUL (EQUIVALENT TO CSA NOTICE 5A)
The MAX22192 are certified up to 600V_{RMS} for single protection. For more details, refer to File 351759.

Safety Limits

Damage to the IC can result in a low-resistance path to ground or to the supply and, without current limiting, the MAX22192 could dissipate an excessive amount of power. Excessive power dissipation can damage the die and result in damage to the isolation barrier, potentially causing downstream issues. Table 1 shows the safety limits for the MAX22192.

The maximum safety temperature (T_S) for the device is the 150°C maximum junction temperature specified in the *Absolute Maximum Ratings*. The power dissipation (P_D) and junction-to-ambient thermal impedance (θ_{JA}) determine the junction temperature. Thermal impedance values (θ_{JA} and θ_{JC}) are available in the *Package Information* section of the data sheet. The power dissipation (P_D) can be calculated as:

$$P_D = \sum(V_{IN\_} \times I_{IN\_}) + V_{DD24F} \times I_{DD24F} + V_{LF} \times I_{LF} + V_{DDL} \times I_{DDL}$$

Calculate the junction temperature (T_J) as:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Figure 2 and Figure 3 show the thermal derating curve for safety limiting the power and the current of the device. Ensure that the junction temperature does not exceed 150°C.

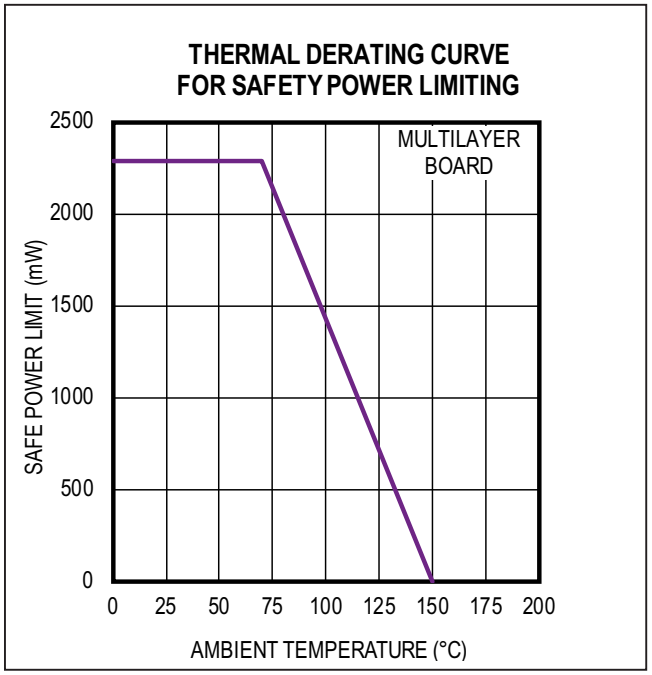


Figure 2. Thermal Derating Curve for Safety Power Limiting

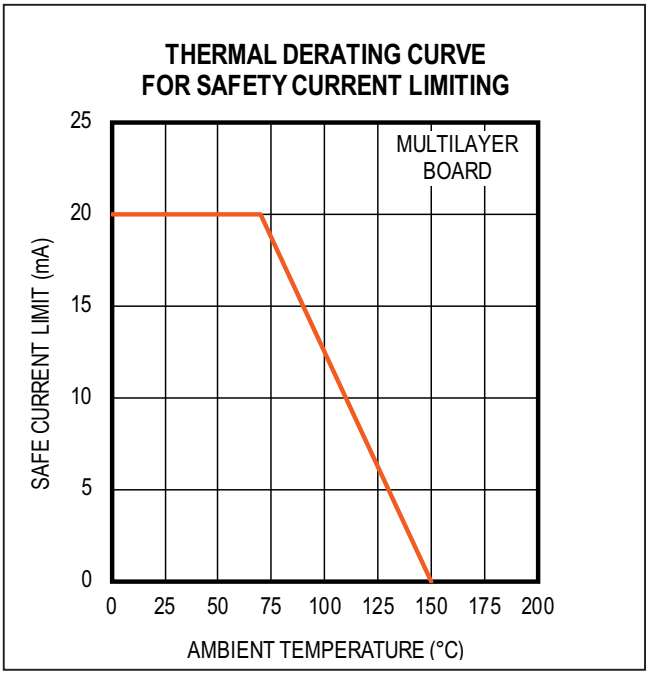


Figure 3. Thermal Derating Curve for Safety Current Limiting

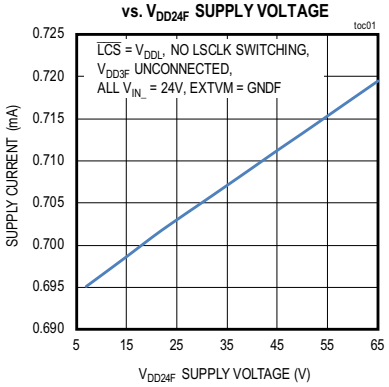
Table 1. Safety Limiting Values for the MAX22192

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNIT
Safety Current on Any Pin	I_S	T_J = 150°C, T_A = 25°C, Multilayer Board	20	mA
Total Safety Power Dissipation	P_S	T_J = 150°C, T_A = 25°C, Multilayer Board	2286	mW
Maximum Safety Temperature	T_S		150	°C

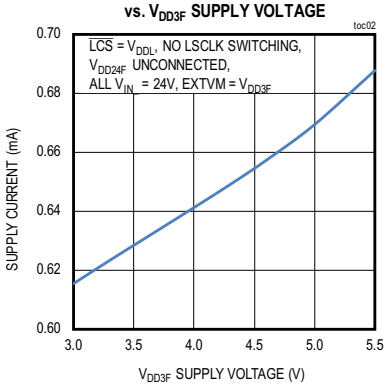
Typical Operating Characteristics

V_{DD24F} = +24V, V_{DD3F} = V_{LF} = +3.3V, V_{DDL} = +3.3V, T_A = +25°C, R_{REFDI} = 7.5kΩ, R_{REFWB} = 24kΩ, R_{IN} = 1.5kΩ, unless otherwise noted.

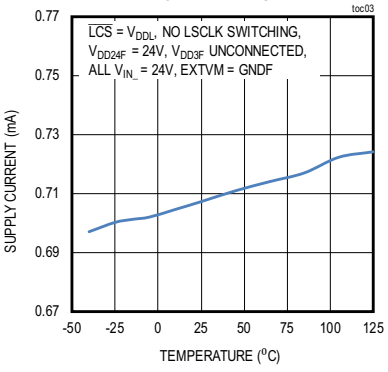
V_{DD24F} SUPPLY CURRENT vs. V_{DD24F} SUPPLY VOLTAGE



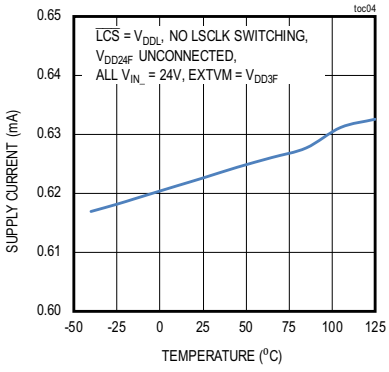
V_{DD3F} SUPPLY CURRENT vs. V_{DD3F} SUPPLY VOLTAGE



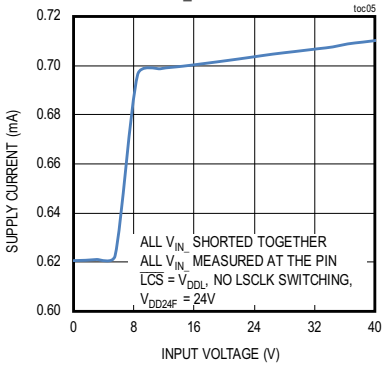
V_{DD24F} SUPPLY CURRENT vs. TEMPERATURE



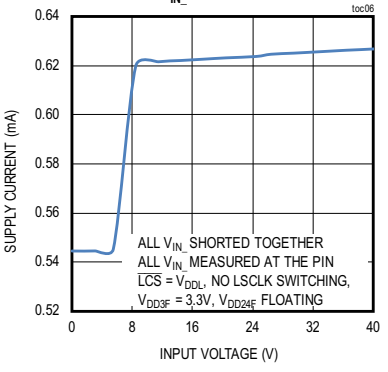
V_{DD3F} SUPPLY CURRENT vs. TEMPERATURE



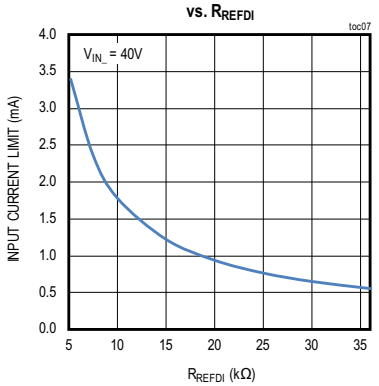
V_{DD24F} SUPPLY CURRENT vs. VIN_ INPUT VOLTAGE



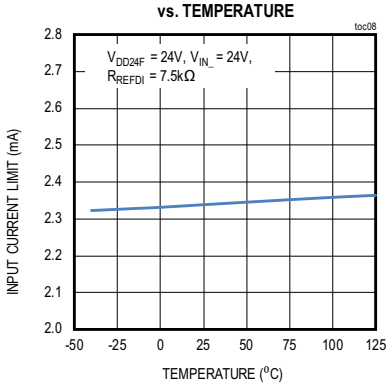
V_{DD3F} SUPPLY CURRENT vs. $V_{IN\_}$ INPUT VOLTAGE



INPUT CURRENT LIMIT I_{INLIM} vs. R_{REFDI}



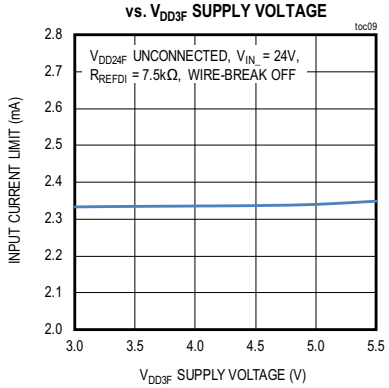
INPUT CURRENT LIMIT I_{INLIM} vs. TEMPERATURE



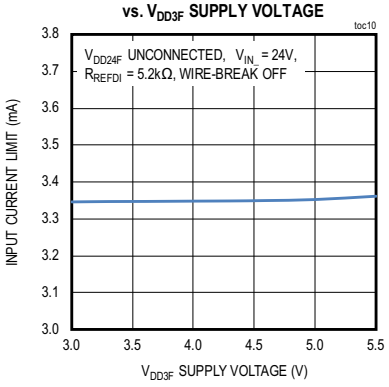
Typical Operating Characteristics (continued)

V_{DD24F} = +24V, V_{DD3F} = V_{LF} = +3.3V, V_{DDL} = +3.3V, T_A = +25°C, R_{REFDI} = 7.5kΩ, R_{REFWB} = 24kΩ, R_{IN} = 1.5kΩ, unless otherwise noted.

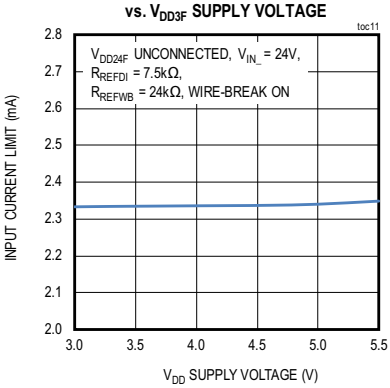
INPUT CURRENT LIMIT I_{INLIM} vs. V_{DD3F} SUPPLY VOLTAGE



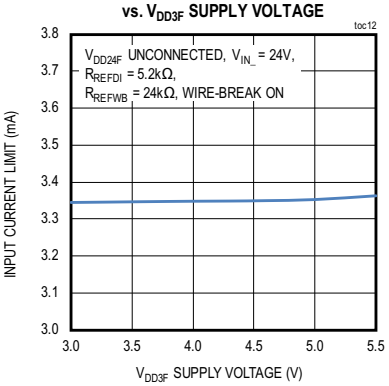
INPUT CURRENT LIMIT I_{INLIM} vs. V_{DD3F} SUPPLY VOLTAGE



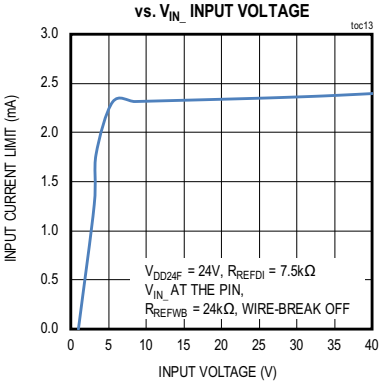
INPUT CURRENT LIMIT I_{INLIM} vs. V_{DD3F} SUPPLY VOLTAGE



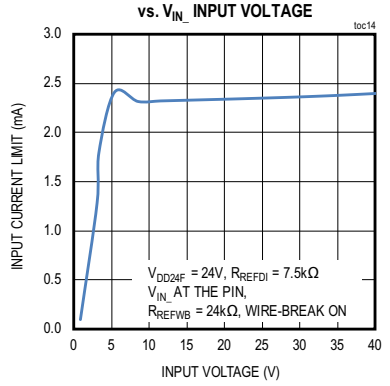
INPUT CURRENT LIMIT I_{INLIM} vs. V_{DD3F} SUPPLY VOLTAGE



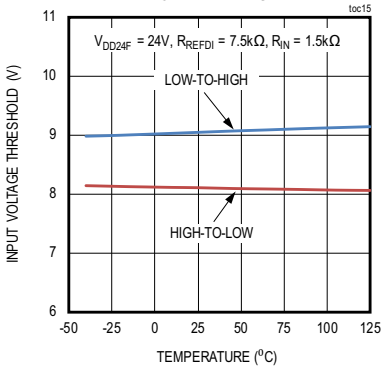
INPUT CURRENT LIMIT I_{INLIM} vs. $V_{IN\_}$ INPUT VOLTAGE



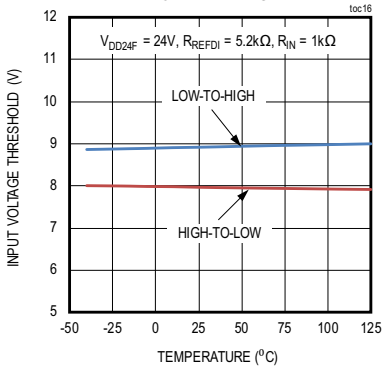
INPUT CURRENT LIMIT I_{INLIM} vs. $V_{IN\_}$ INPUT VOLTAGE



INPUT VOLTAGE THRESHOLD vs. TEMPERATURE



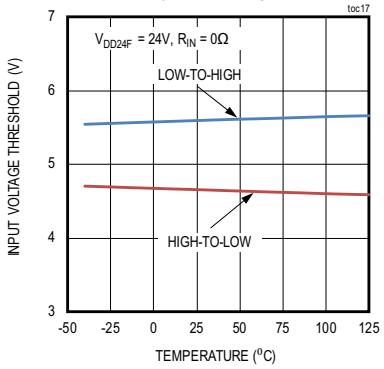
INPUT VOLTAGE THRESHOLD vs. TEMPERATURE



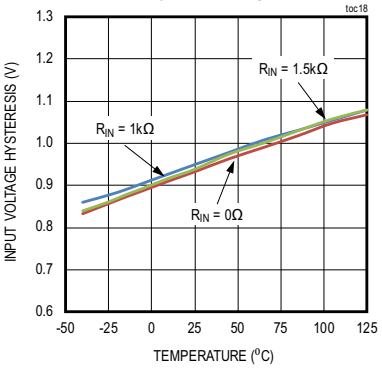
Typical Operating Characteristics (continued)

V_{DD24F} = +24V, V_{DD3F} = V_{LF} = +3.3V, V_{DDL} = +3.3V, T_A = +25°C, R_{REFDI} = 7.5kΩ, R_{REFWB} = 24kΩ, R_{IN} = 1.5kΩ, unless otherwise noted.

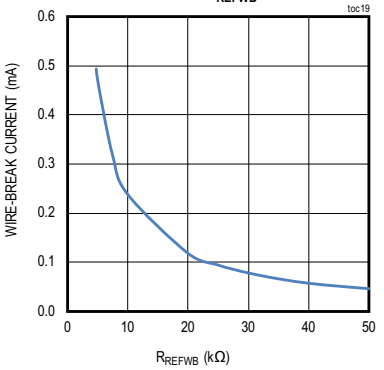
INPUT VOLTAGE THRESHOLD vs. TEMPERATURE



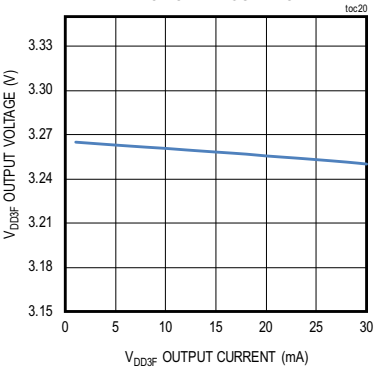
INPUT VOLTAGE HYSTERESIS vs. TEMPERATURE



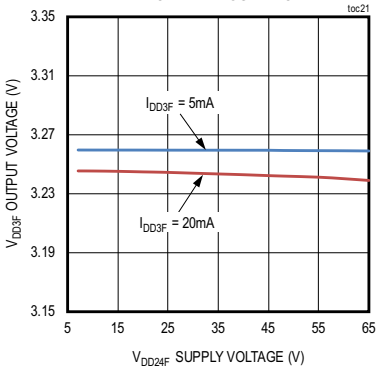
WIRE-BREAK CURRENT THRESHOLD vs. R_{REFWB}



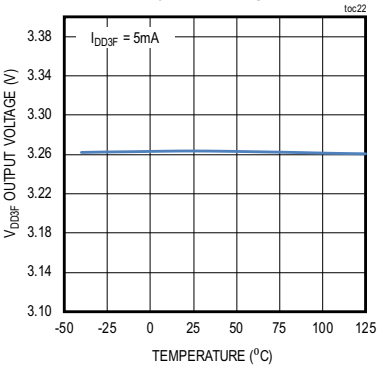
LDO LOAD REGULATION



LDO LINE REGULATION



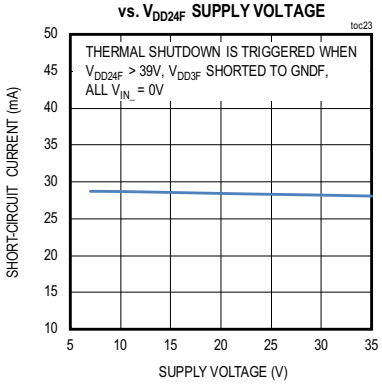
LDO OUTPUT VOLTAGE vs. TEMPERATURE



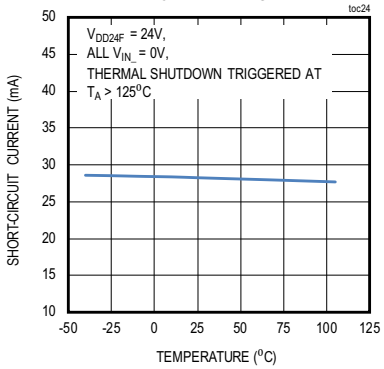
Typical Operating Characteristics (continued)

V_{DD24F} = +24V, V_{DD3F} = V_{LF} = +3.3V, V_{DDL} = +3.3V, T_A = +25°C, R_{REFDI} = 7.5kΩ, R_{REFWB} = 24kΩ, R_{IN} = 1.5kΩ, unless otherwise noted.

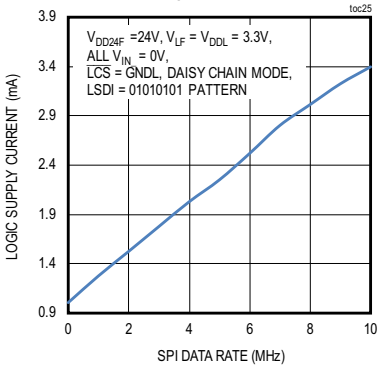
LDO SHORT-CIRCUIT CURRENT vs. V_{DD24F} SUPPLY VOLTAGE



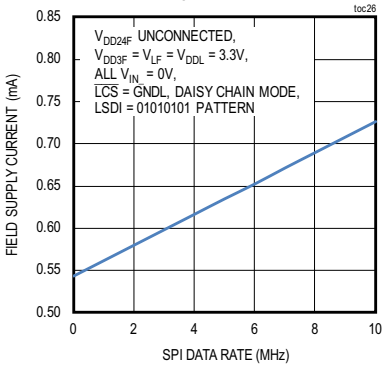
LDO SHORT-CIRCUIT CURRENT vs. TEMPERATURE



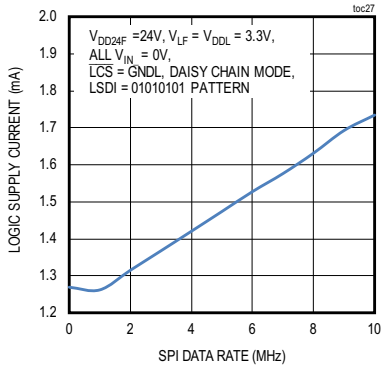
LOGIC SUPPLY V_{LF} CURRENT vs. DATA RATE



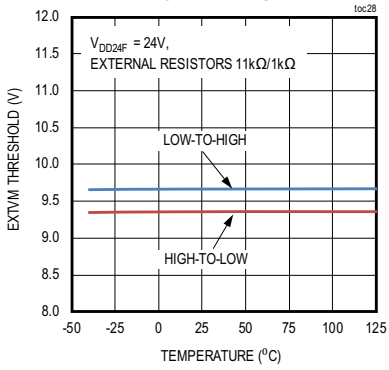
V_{DD3F} SUPPLY CURRENT vs. DATA RATE



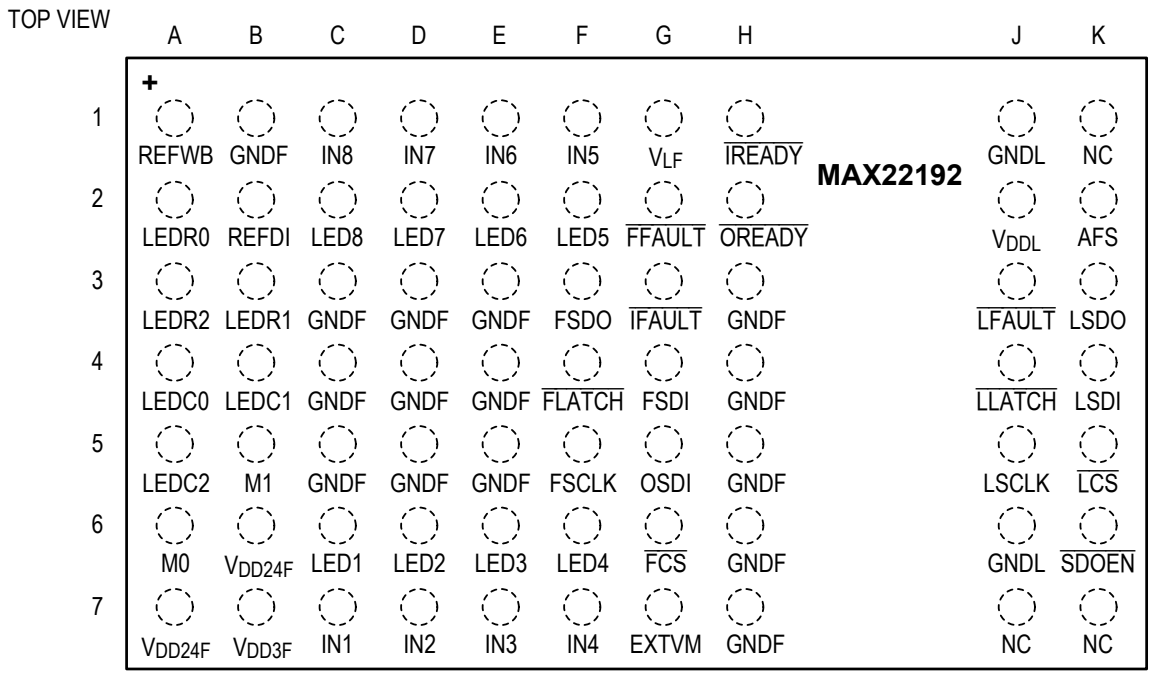
LOGIC SUPPLY V_{DDL} CURRENT vs. DATA RATE



EXTVM THRESHOLD VOLTAGE vs. TEMPERATURE



Pin Configurations



GQFN
(6mm x 10mm)

Pin Description

PIN	NAME	FUNCTION	REFERENCE
POWER SUPPLY			
J2	V_{DDL}	Logic-Side Power Supply. Bypass with 0.1µF ceramic capacitor as close as possible to the pin. Set logic level for all logic-side signals.	GNDL
J1, J6	GNDL	Power and Signal Ground for Logic-Side	-
A7, B6	V_{DD24F}	24V Field Supply. Bypass with 0.1µF capacitor in parallel with 1µF capacitor to GNDF. If powering the MAX22192 from V_{DD3F}, leave V_{DD24F} unconnected.	GNDF
B7	V_{DD3F}	3.3V Field-Side Output. Internal LDO output when powered from V_{DD24F}, or 3.0V–5.5V supply input when V_{DD24F} is unconnected. Bypass to GNDF with 0.1µF capacitor in parallel with 1µF capacitor.	GNDF
G1	V_{LF}	Field-Side Logic Interface Supply. Bypass with 0.1µF ceramic capacitor as close as possible to the pin. Set logic level for all field-side digital signals.	GNDF
B1, C3-C5, D3-D5, E3-E5, H3-H7	GNDF	Power and Signal Ground for Field-Side	-

Pin Description (continued)

PIN	NAME	FUNCTION	REFERENCE
LOGIC-SIDE DIGITAL PINS			
K5	$\overline{LCS}$	Logic-Side Chip-Select Input. Input to $\overline{CS}$ Isolation Channel. Has a weak internal pullup to V_{DDL}. Drive $\overline{LCS}$ low to enable LSDO and assert $\overline{FCS}$ low, which latches input states and enable the field-side SPI interface.	GNDL
J5	LSCLK	Logic-Side Serial Clock Input to SCLK Isolation Channel. Has a weak internal pulldown.	GNDL
K4	LSDI	Logic-Side Serial Data Input to SDI Isolation Channel. Has a weak internal pulldown. Data is clocked into LSDI on the rising edge of LSCLK. OSDI is the output of SDI channel on the field-side.	GNDL
K3	LSDO	Logic-Side Serial Data Output. Becomes High-Z when $\overline{LCS}$ and $\overline{SDOEN}$ are both high. LSDO is enabled when either $\overline{LCS}$ or $\overline{SDOEN}$ is low. Data is updated on the falling edge of LSCLK.	GNDL
J4	$\overline{LLATCH}$	Logic-Side Input to $\overline{LATCH}$ Isolation Channel. Has a weak internal pullup to V_{DDL}. Drive $\overline{LLATCH}$ low to assert $\overline{FLATCH}$ low, which latches all eight input states.	GNDL
J3	$\overline{LFAULT}$	Logic-Side Open-Drain Output of $\overline{FAULT}$ Isolation Channel. $\overline{LFAULT}$ goes low to indicate fault conditions on the field-side. Connect a pullup resistor to V_{DDL}.	GNDL
K6	$\overline{SDOEN}$	LSDO Enable. Has a weak internal pullup to V_{DDL}. Drive $\overline{SDOEN}$ low to enable LSDO when sharing the isolation with other field-side SPI devices in the independent slave configuration; drive $\overline{SDOEN}$ high and allow $\overline{LCS}$ to enable LSDO in the standalone or daisy-chain configuration.	GNDL
K2	AFS	Field-Side Active. AFS is high to indicate field-side is operating normally and $\overline{IREADY}$ is low. When field-side is not powered, AFS is set low and all logic-side outputs are in a default state ($\overline{LFAULT}$ is low and LSDO is low when enabled). A nominal 100µs delay is added between the detection of field-side power and the assertion of AFS to ensure power supply is settled and a minimum pulse width for AFS.	GNDL
K1, J7, K7	NC	Not Connected. Leave it unconnected, or connect to GNDL	-
FIELD-SIDE DIGITAL PINS			
G6	$\overline{FCS}$	Output of $\overline{CS}$ Isolation Channel and Field-Side Chip-Select Input. All digital input states are latched and field-side SPI interface is active when $\overline{FCS}$ is low. Connect the $\overline{CS}$ of other field-side SPI devices to $\overline{FCS}$ when sharing the MAX22192 isolation in the daisy-chain configuration.	GNDF
F5	FSCLK	Output of SCLK Isolation Channel and Field-Side Serial Clock Input. Connect the SCLK of other field-side SPI devices to FSCLK when sharing the MAX22192 isolation.	GNDF
G5	OSDI	Output of SDI Isolation Channel. In the standalone SPI or independent slave configuration, connect OSDI to FSDI. In the daisy-chain configuration, connect OSDI to the SDI of the first field-side SPI device. The MAX22192 is the last device in the chain. Refer to Figure 12 for details.	GNDF

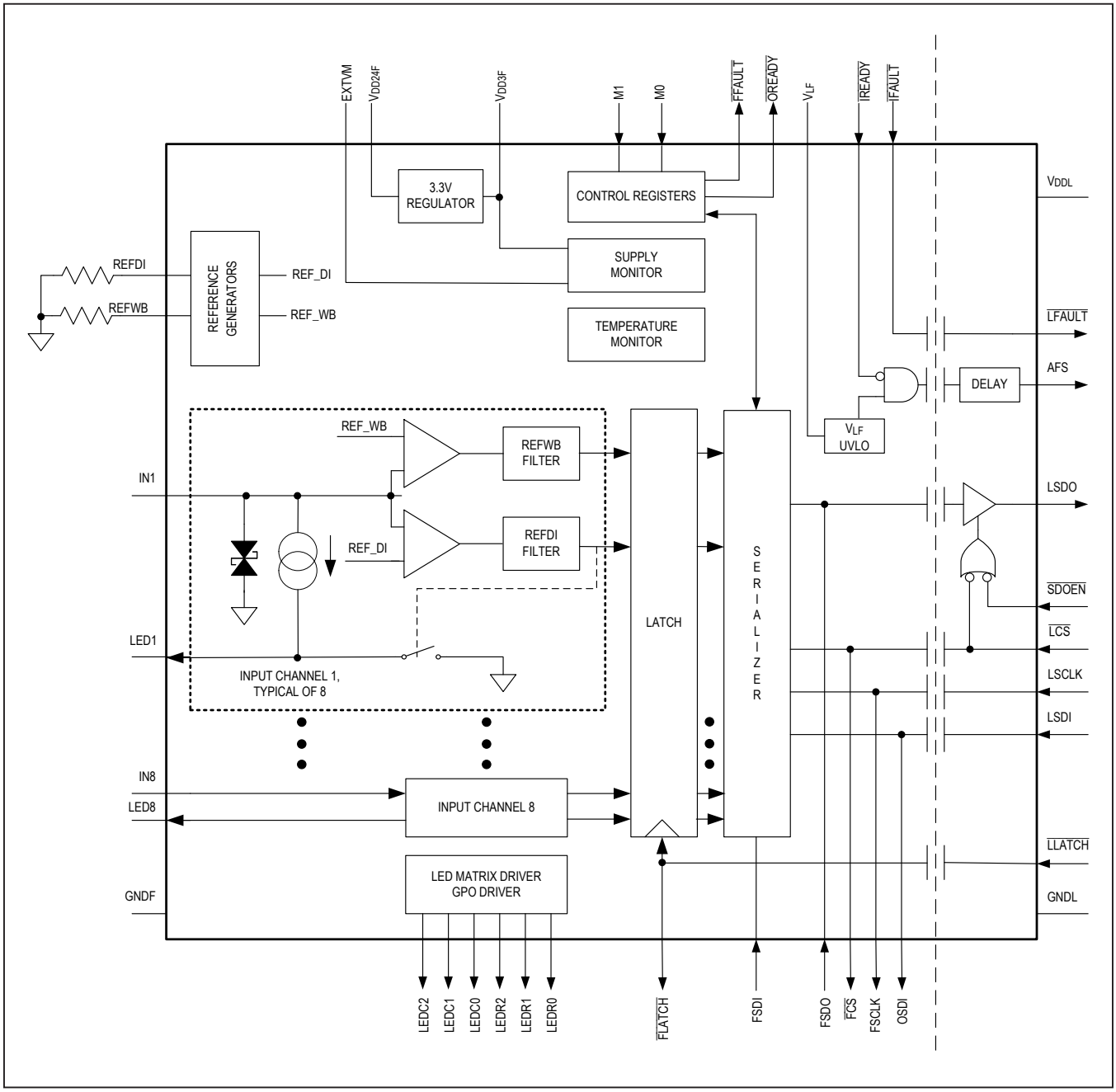
Pin Description (continued)

PIN	NAME	FUNCTION	REFERENCE
G4	FSDI	Field-Side Serial Data Input. Has a weak internal pulldown. Data is clocked into FSDI on the rising edge of FSCLK. In the standalone SPI or independent slave configuration, connect OSDI to FSDI. In the daisy-chain configuration, connect FSDI to the SDO of the next to last field-side SPI device. The MAX22192 is the last device in the chain. Refer to Figure 12 for details.	GNDF
F3	FSDO	Field-Side Serial Data Output and Input to SDO Isolation Channel. Data is updated on the falling edge of FSCLK. When $\overline{FCS}$ is high, FSDO is high-impedance. In the SPI independent slave configuration, connect the SDO of other field-side SPI devices to FSDO. In the daisy-chain configuration, the MAX22192 is the last device in the chain since FSDO is internally connected to the isolation. Refer to Figure 12 for details.	GNDF
F4	$\overline{FLATCH}$	Output of $\overline{LATCH}$ Isolation Channel and Field-Side $\overline{LATCH}$ Input. $\overline{FLATCH}$ and $\overline{FCS}$ control the data latch at the input of the field-side serializer. The latch is transparent when both $\overline{FCS}$ and $\overline{FLATCH}$ are high. The input data is frozen on the falling edge of either $\overline{FLATCH}$ or $\overline{FCS}$. Connect $\overline{FLATCH}$ to the $\overline{LATCH}$ input of other field-side SPI devices when sharing the MAX22192 isolation.	GNDF
G2	$\overline{FFAULT}$	Field-Side Open-Drain Active-Low Fault Indicator. Connect a pullup resistor to V_{LF}. Connect $\overline{FFAULT}$ to $\overline{IFAULT}$ to isolate $\overline{FAULT}$ signal. $\overline{FFAULT}$ goes low to indicate that one or more of the flags in the FAULT registers have been set. The faults include: supply monitors, temperature monitors, CRC error, wire-break detection, and short or open at REFDI or REFWB pins.	GNDF
G3	$\overline{IFAULT}$	Field-Side Input to $\overline{FAULT}$ Isolation Channel. Has a weak internal pulldown. Connect $\overline{FFAULT}$ and $\overline{FAULT}$ of other field-side SPI devices to $\overline{IFAULT}$ when sharing the MAX22192 isolation.	GNDF
H2	$\overline{OREADY}$	Field-Side Open-Drain Active-Low Ready Indicator. $\overline{OREADY}$ goes low indicating the field-side is powered up and ready for operation. Connect $\overline{OREADY}$ to $\overline{IREADY}$ to isolate $\overline{READY}$ signal. Connect a pullup resistor to V_{LF}.	GNDF
H1	$\overline{IREADY}$	Field-Side Ready Input to $\overline{READY}$ Isolation Channel. Has a weak internal pullup. Assert $\overline{IREADY}$ low when field-side is ready for operation. When $\overline{IREADY}$ is high, AFS is low and logic-side outputs are in their default state ($\overline{LFAULT}$ is low and LSDO is low when enabled). When $\overline{IREADY}$ is low, AFS is high and all isolation channels operate normally. Connect $\overline{OREADY}$ and $\overline{READY}$ of other field-side SPI devices to $\overline{IREADY}$ when sharing the MAX22192 isolation.	GNDF
B5	M1	SPI Control Mode. See Table 3 for details.	GNDF
A6	M0		

Pin Description (continued)

PIN	NAME	FUNCTION	REFERENCE
FIELD INPUT PINS			
C7, D7, E7, F7, F1, E1, D1, C1	IN1 - IN8	Field Digital Inputs. For Type 1 and Type 3 inputs, place a 1.5kΩ pulse withstanding resistor between the field input and IN_ pin. For Type 2 inputs, place a 1kΩ pulse withstanding resistor between field input and IN_ pin.	GNDF
C6, D6, E6, F6, F2, E2, D2, C2	LED1 - LED8	Energyless LED Driver Outputs. Connect to GNDF if LEDs are not used.	GNDF
A2, B3, A3	LEDR0 - LEDR2	Open-Drain Auxiliary LED Matrix Row 0–2 Output, or Push-Pull GPO Output. Connect to LED cathode when configured as LED output. Connect a resistor in series with the LED between LEDR_ and LEDC_. Refer to the *GPO Register* and *LED Register* for details.	GNDF
A4, B4, A5	LEDC0 - LEDC2	Open-Drain Auxiliary LED Matrix Column 0–2 Output, or Push-Pull GPO Output. Connect to LED anode when configured as LED output. Connect a resistor in series with the LED between LEDR_ and LEDC_. Refer to the *GPO Register* and *LED Register* for details.	GNDF
B2	REFDI	Digital Input Current-Limit Reference Resistor. For Type 1 and Type 3 inputs, place a 7.5kΩ resistor from REFDI to GNDF. For Type 2 inputs, place a 5.2kΩ resistor from REFDI to GNDF.	GNDF
A1	REFWB	Wire-Break Current-Limit Reference Resistor. Connect a 5.2kΩ–50kΩ resistor from REFWB to GNDF to set the wire-break threshold. See the *Wire-Break Detection* section for details.	GNDF
G7	EXTVM	External V_{DD24F} Supply Monitoring Input. Connect EXTVM to GNDF to use internal thresholds for both V_{DD24F} undervoltage and voltage missing monitoring. Connect EXTVM to external resistive divider to set the external thresholds for both V_{DD24F} undervoltage and voltage missing monitoring. Connect EXTVM to V_{DD3F} to disable V_{DD24F} voltage monitoring, while 24VM and 24VL faults are always off. This is useful when the device is powered by V_{DD3F}.	GNDF

Functional Block Diagram



Detailed Description

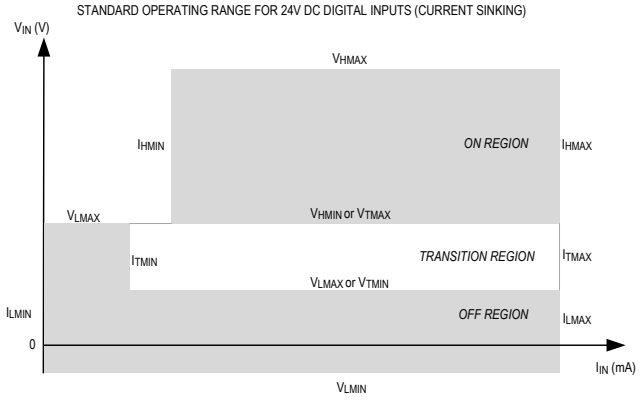
The MAX22192 senses the state (on, high or off, low) of eight digital inputs. The voltages at the IN1 to IN8 input pins are compared against internal references to determine whether the sensor is ON (logic 1) or OFF (logic 0). All eight inputs are simultaneously latched by the assertion of either $\overline{LLATCH}$ or $\overline{LCS}$, and the data made available in a serialized format using the isolated SPI interface. Placing a 7.5kΩ current-setting resistor between REFDI and GNDF, and a 1.5kΩ resistor between each field input and the corresponding IN_ input pin ensures that the current at the ON and OFF trip points, as well as the voltage at the trip points, satisfy the requirements of IEC 61131-2 for Type 1 and Type 3 inputs. The current sunk by each input pin rises linearly with input voltage until the level set by the current limiter is reached; any voltage increase beyond this point does not increase the input current. Limiting the input current ensures compliance with IEC 61131-2 while significantly reducing power dissipation compared to traditional resistive inputs.

The current-setting resistor R_{REFDI} can be calculated using this equation:

$$R_{REFDI} = 17.63V / I_{INLIM}$$

Input Filters

Each input (IN1–IN8) has a programmable filter and input data can be filtered to reduce noise, or it can be read directly for more rapid response. Bit FBP in the corresponding FLT_ register is used to bypass the filter or to enable the filter. One of eight filter delays (50µs, 100µs, 400µs, 800µs, 1.6ms, 3.2ms, 12.8ms, 20ms) can be independently selected for each channel. Noise rejection is accomplished through a nonrollover up-down counter where the state of the field input controls the counting direction (up or down). The filter uses an up-down counter fed by a 200kHz clock. If the input is high, it counts up; if the input is low, it counts down. The filter output is updated when the counter hits the upper or lower limit, with the upper limit depending on the selected filter delay and the lower limit being zero regardless of the filter delay. The low-to-high transition of the filter occurs when the counter reaches the upper limit. The high-to-low transition occurs when the counter reaches the lower limit. There is no rollover; counting simply stops when the upper or lower limit is hit. The filter delay is the time it takes to reach the upper/lower limit in response to a step input when the counter starts from the lower/upper limit.



TYPE OF LIMIT	TYPE 1 LIMITS						TYPE 2 LIMITS						TYPE 3 LIMITS					
	OFF REGION		TRANSITION		ON REGION		OFF REGION		TRANSITION		ON REGION		OFF REGION		TRANSITION		ON REGION	
	V_L (V)	I_L (mA)	V_T (V)	I_T (mA)	V_H (V)	I_H (mA)	V_L (V)	I_L (mA)	V_T (V)	I_T (mA)	V_H (V)	I_H (mA)	V_L (V)	I_L (mA)	V_T (V)	I_T (mA)	V_H (V)	I_H (mA)
MAX	15/5	15	15	15	30	15	11/5	30	11	30	30	30	11/5	15	11	15	30	15
MIN	-3	ND	5	0.5	15	2	-3	ND	5	2	11	6	-3	ND	5	1.5	11	2

ND = NOT DEFINED

Figure 4. Switching Characteristics for IEC 61131-2 Type 1, 2, and 3 24V_{DC} Digital Inputs

If the input is not a step function, but is bouncing, as shown in Figure 5, the output changes state after a total delay of:

Total Delay = Filter Delay + 2 x (Total Time at the Old State)

In the example in Figure 5, the filter has a nominal delay of 1.6ms, and the input returns high for two 0.2ms periods after the first transition from high to low. These transitions back to the high state extend the time before the output of the filter switches. Total Delay = 1.6ms + 2 × (0.2ms + 0.2ms) = 2.4ms.

Wire-Break Detection

Each input (IN1–IN8) includes a second threshold comparator that can be individually enabled to verify the integrity of field wiring. The comparator senses the presence of the small input current produced by a two-wire proximity sensor in its open state, or the current from an open switch with a diagnostic resistor placed across it. The wire break current threshold is set by placing a resistor between REFWB and GNDF, and is adjustable from 50µA to 470µA. If this current is missing, due to an open-wire or a wire shorted to GNDF, the comparator trips, and after filtering, sets a corresponding sticky bit in the WB register. Bits in this register remain set until the register is read, which automatically clears all bits in the register. All wire-break detectors include a fixed 20ms filter, and like the input data, the input to the WB register is frozen when either $\overline{LCS}$ or $\overline{LLATCH}$ is held low. The eight wire-break flags are ORed together to produce the WBG flag in the FAULT1 register. This flag remains set until all flags in the WB register have been cleared.

The wire-break threshold resistor R_{REFWB} can be calculated using this equation:

$$R_{REFWB} = 2.44V \div I_{WB}$$

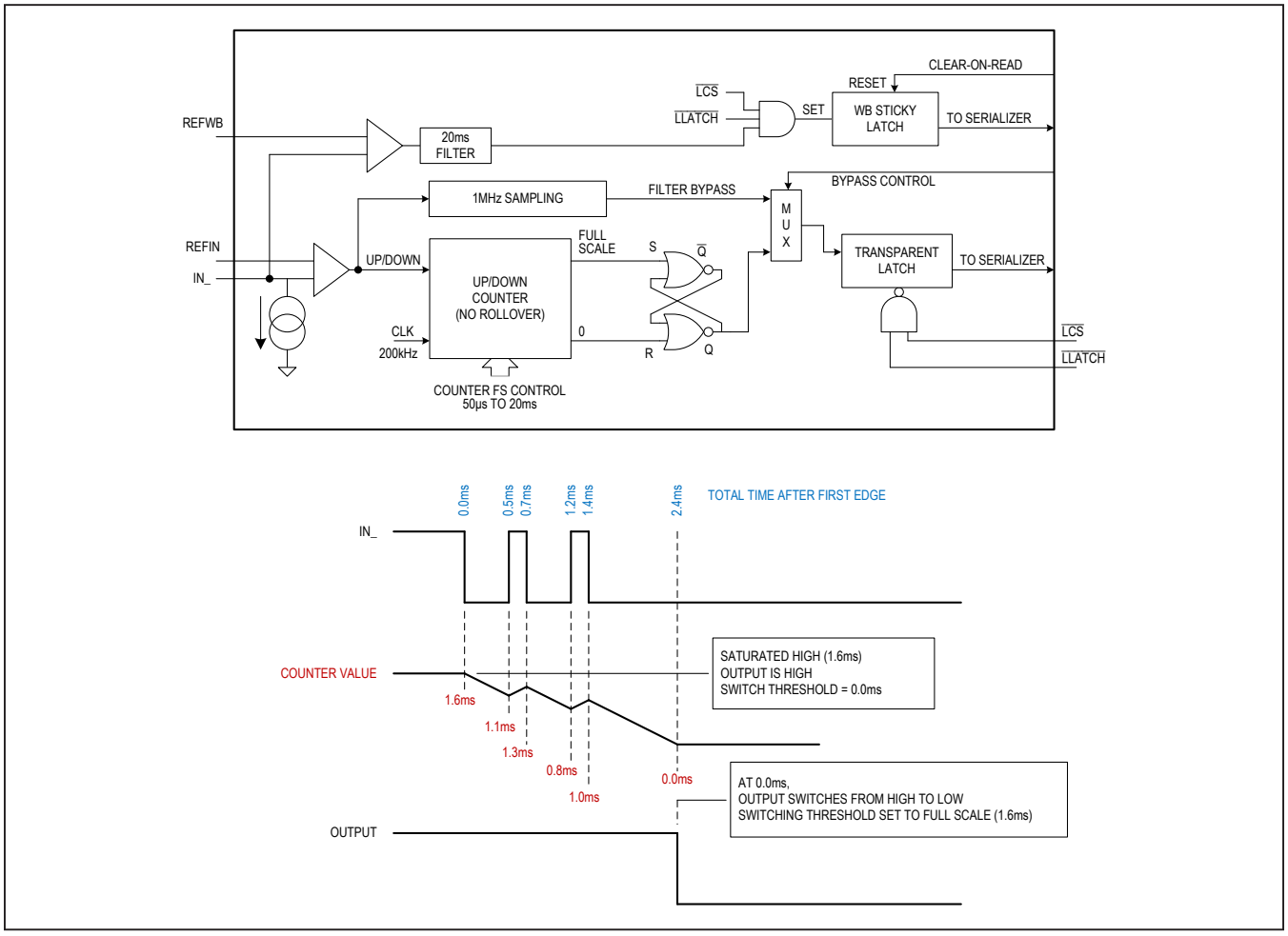


Figure 5. MAX22192 Digital Filter

Type 2 Sensor Inputs

The additional input current (6mA min) and associated power dissipation of the Type 2 input requires the use of two MAX22192 inputs in parallel. The current of each channel is set to a nominal 3.39mA (6.78mA total) by placing a 5.2kΩ resistor from REFDI to GNDF. The proper voltage drop across the input resistor is maintained by reducing the resistance from 1.5kΩ to 1kΩ for each MAX22192 channel. For proper surge protection, it is important that each MAX22192 input has its own resistor. Any two MAX22192 channels can be used; they need not be contiguous (Figure 6). Either channel can be read to determine the input state. The additional power dissipation from this Type 2 configuration can reduce the maximum ambient operating temperature, especially when all the inputs are high, the MAX22192 is powered by V_{DD24F} more than 30V, or V_{DD3F} has additional load.

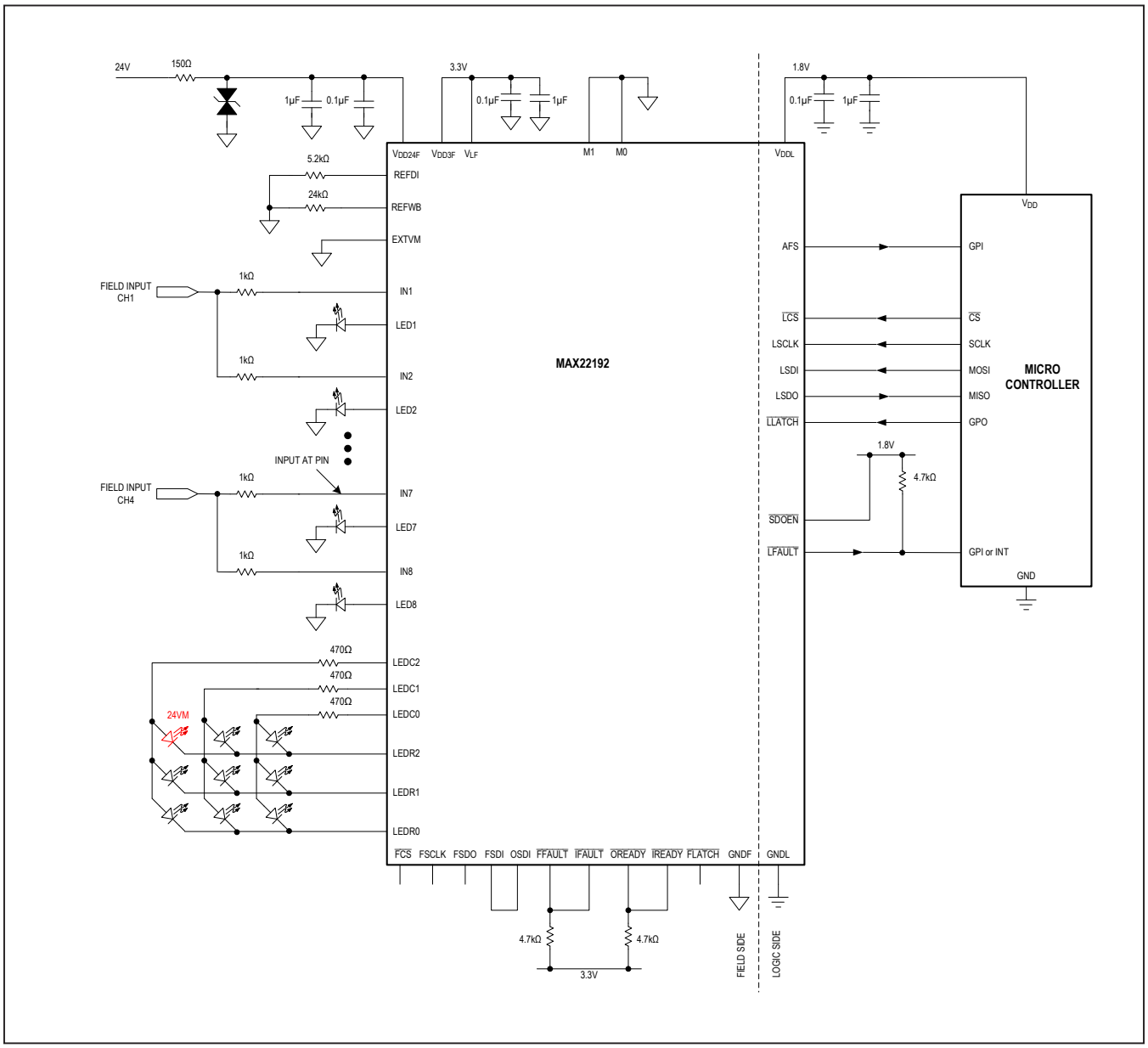


Figure 6. Implementing a 4-Channel Type 2 Digital Input with MAX22192

Energyless LED Drivers

When IN_ is determined to be ON, its input current is diverted to the LED_ pin and flows from that pin to GNDF. Placing an LED between LED_ and GNDF provides an indication of the input state without increasing overall power dissipation. If the indicator LEDs are not used, connect LED_ to GNDF.

Programmable Auxiliary LEDs

LEDR_ and LEDC_ pins can be configured as LED drivers for a 3 × 3 LED crossbar matrix by setting the DIR bit low in the GPO register. LEDR_ pins are open-drain pulldown drivers to be connected to LED's cathode, and LEDC_ pins are open-drain pullup drivers to be connected to LED's anode (see Figure 7). This offers a pin-optimized configuration for driving nine LEDs. One LED, located at row 2 column 2 (R2C2), is dedicated to the status of the V_{DD24F} supply. It is on when V_{DD24F} supply voltage is above the 24VM voltage missing threshold. The remaining eight LEDs are typically configured to indicate the wire break status of eight channels, but can also be used for other purposes. Each LED's On or Off status is controlled by setting the corresponding bit in the LED register. LEDs in the On state are driven with a 33% duty cycle, 1kHz square wave powered by V_{DD3F} supply. Each LED's on-current is set by a current-limiting resistor in series with each LEDC_ output (Figure 7). Current from each resistor flows through only one LED at a time.

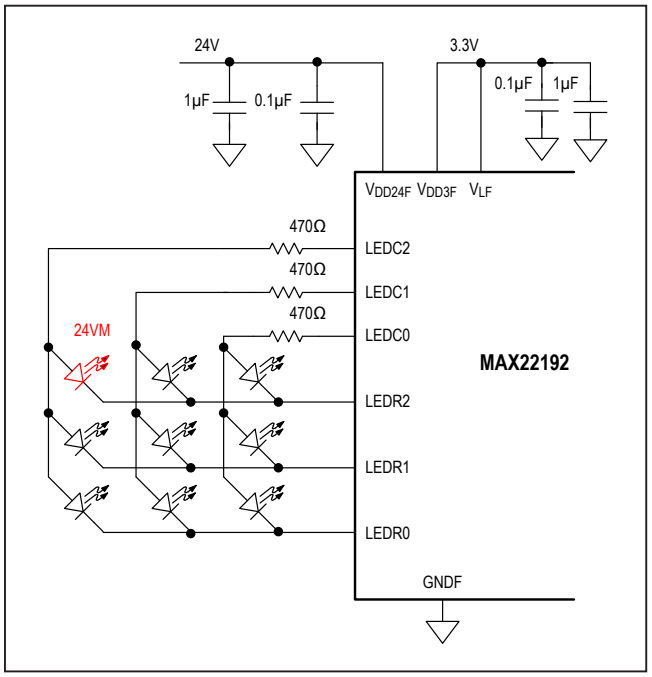


Figure 7. MAX22192 LED Matrix (LEDR_, LEDC_)

When powering the MAX22192 directly from the V_{DD24F} field supply, the V_{DD3F} is powered from V_{DD24F} using an internal LDO. Care should be taken not to exceed the maximum power dissipation ratings (see the *Absolute Maximum Ratings* section). Since the LEDs draw current ultimately from V_{DD24F} supply, each LED in the On state generates approximately the same amount of power dissipation as an input channel in the On state. This is not a concern when the LEDs are used as wire-break indicators, because for each LED that is on, at least one input is in wire-break and guaranteed to be off.

LEDR_ and LEDC_ as GPOs

The LEDR_ and LEDC_ pins used for the LED driver matrix can also be configured as push-pull GPO pins. It provides further flexibility and allows general purpose steady-state signals to be created without multiplexing. Set the DIR bit in the GPO register to high to configure the pins as direct drive outputs and disable the LED matrix drivers. The output state of each pin is configured by the corresponding bits (bits [5:0]) in the GPO register, 0 as output low and 1 as output high (see the *Register Detailed Description* section).

Fault Detection and Monitoring

$\overline{FFAULT}$ is an open-drain output that can be wire ORed with other open-drain field-side outputs and used to notify the host processor of a fault. When enabled, $\overline{FFAULT}$ goes low to indicate that one or more of the flags in the FAULT1 register have been set. These faults include: V_{DD24F} low voltage alarm (24VL), V_{DD24F} voltage missing alarm (24VM), overtemperature alarm 1 (ALRMT1), overtemperature alarm 2 (ALRMT2), CRC error detected on the previous SPI frame (CRC), power-on-reset event (POR), wire-break group error detected (WBG), and sources from the FAULT2 register. The $\overline{FFAULT}$ pin can be configured to be asserted by one or more fault flags if the corresponding fault bits are enabled in the FAULT1EN or FAULT2EN registers. The enabled bits do not affect the flags in the FAULT1 register, they only affect the $\overline{FFAULT}$ pin. Flags ALRMT1, ALRMT2, 24VL, and 24VM in the FAULT1 register are latched; they remain set until read even if the fault goes away. WBG is equivalent to the ORed output of the individual wire-break flags (WB[7:0]), which are latched until cleared by reading the WB register. CRC is not latched, but remains set until an uncorrupted SPI frame is received.

The STK bit in the GPO register configures the $\overline{FFAULT}$ pin to be sticky or to clear when the fault is removed. For example: if a low voltage condition on V_{DD24F} is detected, the 24VL bit in the FAULT1 register is set and $\overline{FFAULT}$ asserts low provided bit 24VLE in the FAULT1EN register is set. If V_{DD24F} then returns to normal levels, the 24VL bit in the FAULT1 register remains set until read; however the state of $\overline{FFAULT}$ pin depends on configuration bit STK in the GPO register. If STK is low, the $\overline{FFAULT}$ pin is not sticky and clears when the fault goes away even though the 24VL bit remains set. If STK is high, then the $\overline{FFAULT}$ pin reflects the state of the bit in the FAULT1 register and remains set until the bit is cleared by reading the FAULT1 register. The minimum pulse width for the $\overline{FFAULT}$ pin asserting low is 1µs typical. This ensures adequate time for the assertion of $\overline{FFAULT}$ to be recognized by the host even if the fault was present for a shorter time.

The power-on default for the FAULT1EN register is to enable CRC and POR. The $\overline{FFAULT}$ pin is in the nonsticky mode.

The MAX22192 provides an isolated $\overline{LFAULT}$ pin on the logic-side. The $\overline{FFAULT}$ signal can be isolated by connecting the $\overline{FFAULT}$ pin to the $\overline{IFAULT}$ pin on the field-side, which is the input of the $\overline{FAULT}$ isolation channel. The $\overline{FAULT}$ isolation channel can be shared by multiple field-side devices by wiring OR with other open-drain $\overline{FAULT}$ outputs, and connecting all field-side $\overline{FAULT}$ signals to $\overline{IFAULT}$ pin.

Clearing Bits in the FAULT1 Register

24VL and 24VM sticky (or latched) bits in the FAULT1 register can be read and cleared either through a direct read of the FAULT1 register, or through a SPI Mode 0 or Mode 2 read or write command if bit 24VF in the CFG register is equal to 0. SPI Modes 0 and 2 transactions read and clear bits 24VL and 24VM (Table 5). This valid SPI transaction also clears the CRC bit. Note that the CRC bit is only active in Modes 0 and 2 since the CRC code is only generated in these two modes. The WBG bit in the FAULT1 register is the real-time ORed value of bits WB[7:0] in the WB register and the WBG bit is not cleared by reading the FAULT1 register. Reading the bits in the WB register clears the WB register and for convenience also clears the WBG bit in the FAULT1 register.

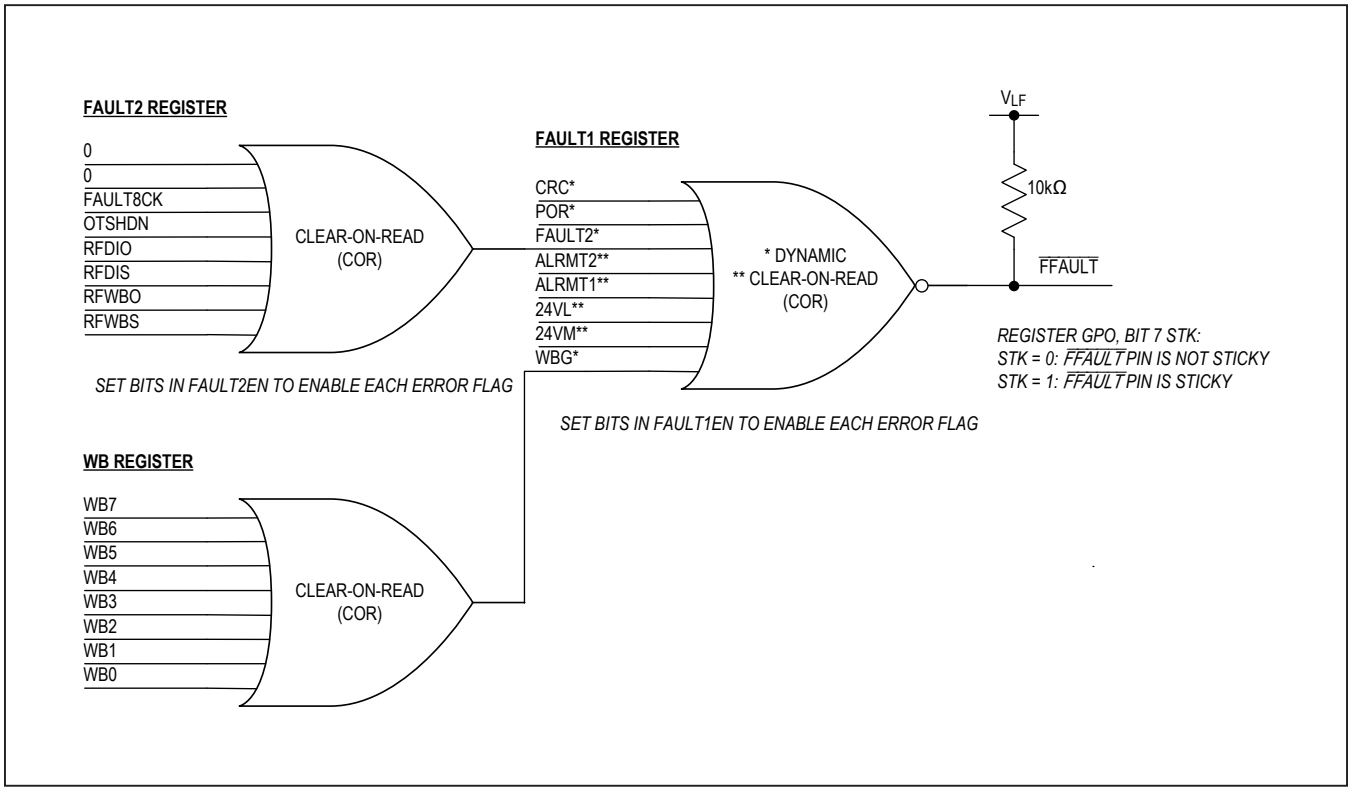


Figure 8. $\overline{FFAULT}$/$\overline{LFAULT}$ Output Sources

External V_{DD24F} Voltage Monitor

The EXTVM input controls the V_{DD24F} field supply voltage monitoring thresholds for both the V_{DD24F} low voltage alarm (24VL) and the V_{DD24F} voltage missing alarm (24VM). When the EXTVM is connected to V_{DD3F}, the V_{DD24F} voltage monitoring on both 24VL and 24VM are turned off, and the 24VL and 24VM bits in the FAULT1 register are always low. This is useful when the MAX22192 is being powered directly from a 3.3V supply on V_{DD3F} and V_{DD24F} is unconnected. When EXTVM is connected to GNDF, the voltage on V_{DD24F} must be above the internal low voltage and voltage missing thresholds to clear the 24VL and 24VM alarms. To use the user-defined V_{DD24F} voltage monitoring thresholds, use an external resistive divider to apply an analog voltage directly to EXTVM. The voltage at EXTVM must be greater than the 24VL threshold of 1V (V_{24VL}) nominal, and the 24VM threshold of 0.81V (V_{24VM}) nominal to clear the faults. Figure 9 shows an example of the V_{DD24F} being monitored with the use of external resistive divider to set user-defined 24VL and 24VM thresholds, V_{DD24_VL} and V_{DD24_VM}.

$$V_{DD24\_VL} = V_{24VL} \times (1 + R2 / R1)$$

$$V_{DD24\_VM} = V_{24VM} \times (1 + R2 / R1)$$

Short/Open Detection at REFDI and REFWB

Short or open detection at the REFDI and REFWB pins is implemented by monitoring the current at REFDI and REFWB pin. When more than 550µA of current is detected at the REFDI pin, meaning a short at REFDI, all input channels are disabled, but the REFDI buffer is still on to keep the detection. When less than a 6.6µA current is detected, meaning an open at REFDI, the 2mA minimum input current is not guaranteed. When open or short at the REFDI pin is detected, the RFDIO or RFDIS bit in the FAULT2 register is set (Table 2).

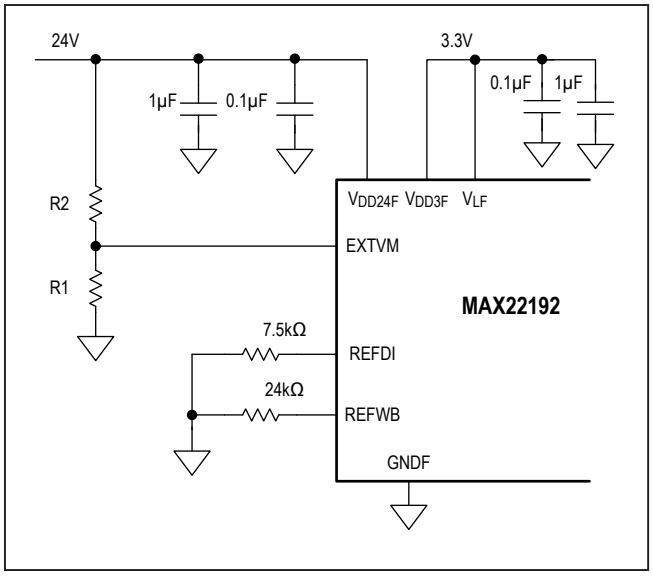


Figure 9. External V_{DD24F} Thresholds Set by EXTVM and External Resistor Divider

When more than 550µA current is detected at the REFWB pin, meaning a short at the REFWB pin, the wire-break faults are always on even though the input wires are correctly connected. When less than 6.6µA current is detected, meaning an open at REFWB, the wire-break faults are always off even though the input wires are not connected. When open or a short at the REFWB pin is detected, the RFWBO or RFWBS bit in the FAULT2 register is set (Table 2). Note the RFWBO bit is set when the wire-break function of all channels are off, or after power-on-reset (see the *Register Detailed Description* section).

Thermal Consideration

The MAX22192 operates at an ambient temperature of 125°C on a properly designed PCB. Operating at higher voltages, with heavy output loads or driving LEDs while input channels are on increases power dissipation and reduces the maximum allowable operating temperature. See the *Package Information* and *Absolute Maximum Ratings* sections for safety operation temperature and maximum power dissipation.

The MAX22192 is in thermal shutdown when the thermal shutdown temperature threshold (165°C typical) is exceeded. During thermal shutdown, the internal voltage regulator, input channels, REFDI and REFWB circuitry, and field-side SPI communication are all turned off, except that register values are retained. A thermal shutdown event can be read back from the FAULT2 register once the device is out of thermal shutdown (Table 2).

Powering the MAX22192 with the V_{DD3F} Pin

The MAX22192 can alternatively be powered using a 3.0V–5.5V supply connected to the V_{DD3F} pin. In this case, a 24V supply is no longer needed and the V_{DD24F} pin must be left unconnected. This configuration has lower power consumption and heat dissipation since the on-chip LDO voltage regulator is disabled (the V_{DD24F} undervoltage lockout is below the threshold and automatically disables the LDO). See Figure 10 for details.

In this configuration, connect the EXTVM pin to V_{DD3F} to disable the V_{DD24F} voltage monitoring function. Otherwise, the device always indicates a “24V FAULT” due to bits 24VL and 24VM in the FAULT1 register, and the $\overline{FFAULT}$ pin is always active (low) if the bits are enabled in the FAULT1EN register. To overcome this, set bits 24VLE and 24VME in the FAULT1EN register to 0.

Table 2. Thermal Shutdown and Open/Short at REFDI and REFWB

	BIT IN FAULT2 REGISTER	BEHAVIOR	INTERNAL BLOCKS
SHORT at REFDI	RFDIS	Input channels are disabled	All input channels disabled, REFDI buffer on
OPEN at REFDI	RFDIO	2mA minimum current limit is not guaranteed	-
SHORT at REFWB	RFWBS	Wire-break faults are always on	-
OPEN at REFWB*	RFWBO	Wire-break faults are always off	-
THERMAL SHUTDOWN	OTSHDN	Device shutdown	Internal LDO disabled, all input channels disabled, REFDI buffer off, field-side SPI off, SPI configuration maintained

**RFWBO is set after power-on-reset or when wire-break detection on all channels are turned off.*

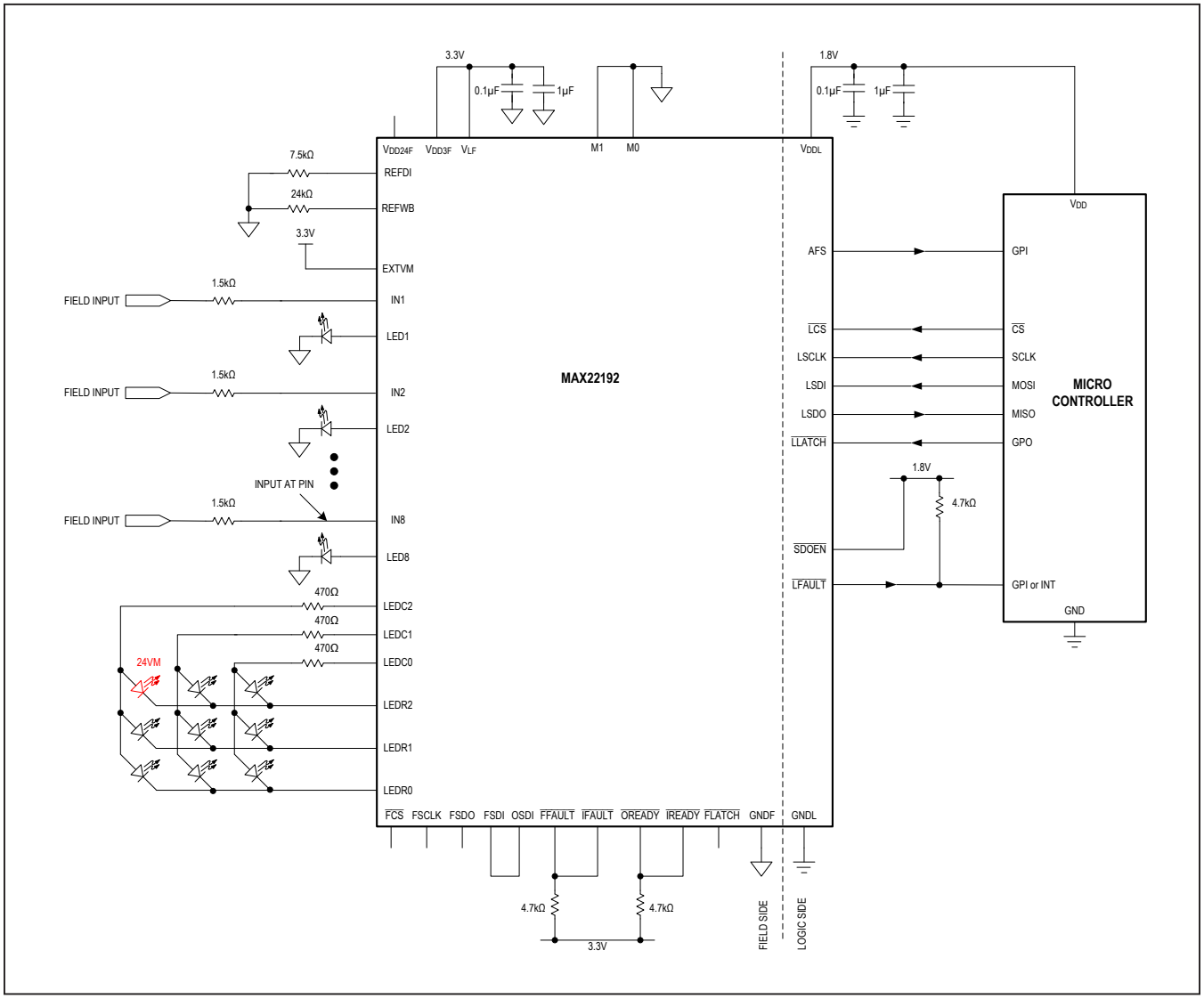


Figure 10. MAX22192 Field-Side Powered by V_{DD3F}, V_{DD24F} Unconnected, EXTVM Disabled

Digital Isolation

The MAX22192 provides galvanic isolation for digital signals that are transmitted between two ground domains, GNDF and GNDL. The device withstands up to $600V_{RMS}$ for up to 60 seconds in the 70-pin GQFN package, which has 2.3mm of creepage and clearance. The package material has a minimum comparative tracking index (CTI) of 600V, giving it a Group I rating in creepage tables.

The MAX22192 offers low-power operation, high electromagnetic interference (EMI) immunity, and stable temperature performance through Maxim's proprietary process technology. The device isolates different ground domains and blocks high-voltage/high-current transients from sensitive or human interface circuitry.

The logic supply voltages V_{LF} and V_{DDL} determine the logic levels on the field-side and logic-side, respectively. The V_{LF} can be set independetly to any voltage from 3.0V to 5.5V, and the V_{DDL} can be set from 1.71V to 5.5V.

Isolation Channels

The MAX22192 provides six isolation channels including $\overline{CS}$, SCLK, SDI, SDO, $\overline{FAULT}$, and $\overline{LATCH}$. The $\overline{LCS}$, LSCLK, LSDI, LSDO, $\overline{LFAULT}$ and $\overline{LLATCH}$ are logic-side signals, referenced to GNDL. These signals are isolated from field-side and usually interface with microcontrollers or FPGAs. The $\overline{FCS}$, FSCLK, FSDI, OSDI, FSDO, $\overline{FFAULT}$, $\overline{IFAULT}$, $\overline{OREADY}$, and $\overline{IREADY}$ are field-side signals, referenced to GNDF. They can be connected with other field-side SPI and control signals when sharing the MAX22192 isolation channels.

The $\overline{LCS}$ and LSCLK are the logic-side isolation inputs, and the $\overline{FCS}$ and FSCLK are their corresponding field-side isolation outputs. The $\overline{CS}$ and SCLK signals from other field-side devices can be connected to $\overline{FCS}$ and FSCLK when sharing the isolation in the daisy-chain or independent slave mode. The $\overline{CS}$ signals from other field-side devices should have their own external isolation channels in the independent slave mode. The OSDI is the field-side output of the SDI isolation channel, and the LSDI is the corresponding logic-side input. Connect the OSDI to FSDI in the standalone or independent slave mode. The SDI signals from other field-side devices can be connected to OSDI when sharing the isolation in the independent slave mode. In the daisy-chain mode, connect the OSDI to the SDI of the first field-side device in the chain, and connect FSDI to the SDO of the next to last field-side device in the chain. The MAX22192 is the last device in the chain. The FSDO is the field-side input of the SDO isolation channel, and the LSDO is the corresponding logic-side output. The SDO signals from other field-side devices can be connected to FSDO when sharing the isolation in the independent slave mode. Refer to the *Typical Operating Circuits* for details.

The $\overline{FFAULT}$ is the field-side active-low open-drain $\overline{FAULT}$ indicator. Connect the $\overline{FFAULT}$ output to the $\overline{IFAULT}$ input to isolate the $\overline{FAULT}$ signal, and $\overline{LFAULT}$ is the logic-side open-drain output. When sharing the isolation with other field-side devices, connect the open-drain $\overline{FAULT}$ signals from other devices to $\overline{IFAULT}$. Both $\overline{FFAULT}$ and $\overline{LFAULT}$ pins require a pullup resistor.

The $\overline{OREADY}$ is the field-side active-low $\overline{READY}$ indicator. $\overline{OREADY}$ goes low indicating the field-side is powered up and ready for operation. Connect the $\overline{OREADY}$ output to the $\overline{IREADY}$ input to isolate the $\overline{READY}$ signal, and AFS is the logic-side output. When $\overline{IREADY}$ is high, AFS is low and logic-side outputs are in their default state, indicating the field-side is not ready for operation. When $\overline{IREADY}$ is low, AFS is high and the MAX22192 operates normally. The $\overline{READY}$ isolation channel can be shared by other field-side devices by connecting other open-drain $\overline{READY}$ signals to $\overline{IREADY}$. Refer to the *Typical Operating Circuits* for details.

When sharing the $\overline{READY}$ isolation channel with other open-drain active-low $\overline{READY}$ signals such as that of MAX22190, the $\overline{OREADY}$ signal and the $\overline{READY}$ signal from the MAX22190s are connected together to the $\overline{IREADY}$ pin. The $\overline{IREADY}$ is pulled low when one of the $\overline{OREADY}$ or $\overline{READY}$ signal from the MAX22190s is low and ready for operation. Care must be taken on the software to determine if all of the devices are ready. Alternatively, an OR gate can be used between $\overline{OREADY}$ and other $\overline{READY}$ signals to guarantee the $\overline{IREADY}$ signal is only pulled low when all the $\overline{READY}$ signals are low.

The logic-side $\overline{SDOEN}$ signal is an output enable control for LSDO. It is useful when the MAX22192 isolation channels are shared by other field-side devices in the independent slave mode by enabling the LSDO when $\overline{LCS}$ is not asserted. When the MAX22192 is operating in standalone or daisy-chain mode, $\overline{LCS}$ low enables all field-side devices' SPI interface as well as the LSDO output. When the MAX22192 is operating in the independent slave mode, the MAX22192 uses $\overline{LCS}$ to enable its own SPI, while other field-side devices have their own dedicated $\overline{CS}$ isolation channel, external to the MAX22192. The independent slave mode requires LSDO to be enabled any time one of the $\overline{CS}$ signals is asserted, which can be accomplished by asserting $\overline{SDOEN}$ low. In the case that there is no need for LSDO to be high-impedance, $\overline{SDOEN}$ can be permanently connected to GNDL. Refer to the *Typical Operating Circuits* for details.

SPI Interface

The MAX22192 has an SPI compatible interface used to read input data, read diagnostic data, and configure all the registers. Each configuration register can be read back to ensure proper configuration. The interface can be operated in one of four modes as controlled by the strapping inputs M0 and M1 (Table 3). Asserting $\overline{LCS}$ low latches the state of all inputs and enables the SPI interface. For all modes, data at the LSDI input is sampled on the rising edge of LSCLK and data at LSDO is updated on the falling edge of LSCLK. The MSB ($\overline{R}$/W bit) is always the first bit of the SPI frame. Transitions of LSCLK while $\overline{LCS}$ is deasserted (high) are ignored. LSCLK must idle low when $\overline{LCS}$ is asserted.

Table 3. SPI Interface Modes

MODE	M1: M0	FRAME LENGTH	CRC	DAISY CHAIN
0	0 0	24-bit	Yes	No
1	0 1	16-bit	No	No
2	1 0	24-bit	Yes	Yes
3	1 1	16-bit	No	Yes

SPI Protocol

The serial output of the device adheres to the SPI protocol, running with CPHA = 0 and CPOL = 0. In all modes, the first 8-bits clocked out of LSDO after $\overline{LCS}$ is asserted are data bits showing the status of inputs IN8–IN1; this allows for rapid and convenient retrieval of the primary data. For write operations in SPI Modes 0 and 1, the next 8-bits clocked out of LSDO are the status bits of the WB (wire-break) register. This is true even if wire-break detection is not enabled, in which case all bits are 0. For reads in SPI Modes 0 and 1, the second 8-bits are the data from the specified register. See Figure 11 for an SPI communication example.

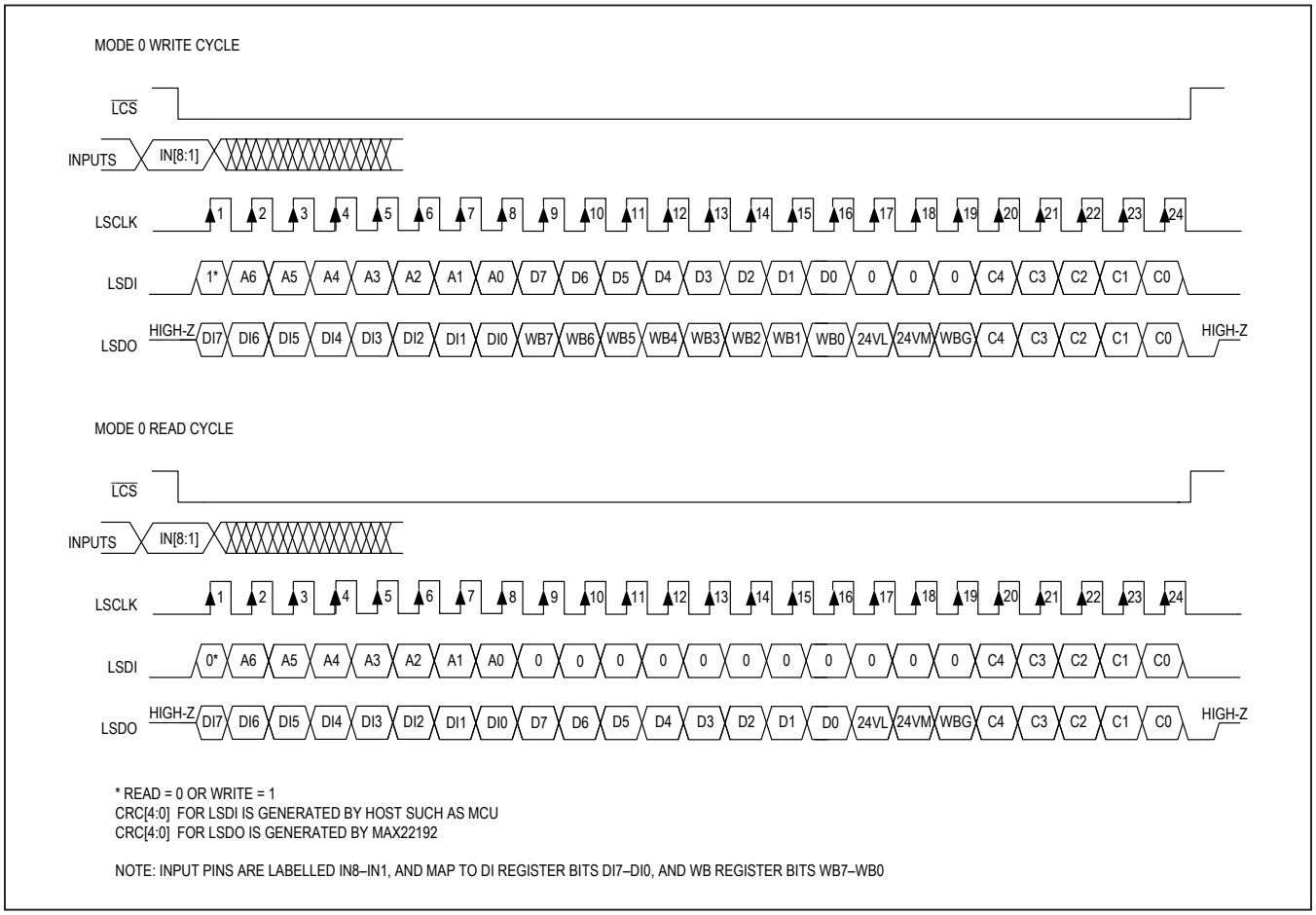


Figure 11. SPI Communication Example (Mode 0)

SPI Modes 2 and 3 are more complex, since the content of the second byte is determined by the previous instruction. For non-daisy-chain compatible modes (SPI Modes 0 and 1), the read instruction is decoded on-the-fly as the SPI frame is clocked in. The instruction is immediately executed and data from the specified register is clocked out in the same SPI frame. This is convenient and quick, but not compatible with daisy-chaining. When daisy-chaining, each unit does not know which portion of the bit stream it should decode until $\overline{LCS}$ is deasserted (the frame is finished). To accommodate this, all daisy-chainable read instructions require two SPI frames. The first frame contains the read instruction and register address, and the second frame returns the register data as the second byte of the frame. This is true regardless of the instruction being clocked in during the second frame.

$\overline{LLATCH}$ is used to simultaneously capture the input states of the MAX22192s and companion Octal Digital Input device MAX22190s, which are not controlled by the same $\overline{LCS}$. This could be MAX22192 and MAX22190s in the same module, or MAX22192s in different modules.

Clock Count for Multiples of 8

For each SPI cycle (between $\overline{LCS}$ going low and going high), the device counts the number of LSCLK pulses. If it is not a multiple of 8, the SPI input data is discarded and bit FAULT8CK is set in the FAULT2 register.

CRC generation

In SPI Interface Modes 0 and 2, five CRC bits can be used to check data integrity during transfer between the device and an external microcontroller. In applications where the integrity of data transferred is not of concern, the CRC bits can be disabled by operating in SPI modes 1 and 3. The CRC uses the following polynomial:

$$P(x) = x^5 + x^4 + x^2 + x^0$$

The 5-bit CRC value is calculated using the first 19 data bits, padded with the 5-bit initial word 00111. The 5-bit CRC result is then appended to the original data bits to create the 24-bit SPI data frame. When the MAX22192 receives a data frame with a CRC error, the CRC error flag (CRC) in the FAULT1 register is set and, if CRCE is set, $\overline{FFAULT}$ pin is asserted. The CRC bit is not sticky, but does remain set until an error-free frame is received. SPI commands within a corrupted frame are ignored.

SPI Power Status

On the field-side, only the SPI port buffers are powered from the V_{LF} supply; internal SPI circuits are powered from the V_{DD3F} supply. Both V_{DD3F} and V_{LF} must be valid for SPI communication to take place. In addition to powering the SPI circuits, V_{DD3F} also sustains the SPI memory (configuration and status registers). If power is being supplied through V_{DD24F}, then an auxiliary supply for the memory is also available. The auxiliary supply only sustains the memory, and it does not allow SPI communication. The auxiliary supply takes over if V_{DD3F} is lost due to external loading or a thermal shutdown event. When the event is over, the device configuration is maintained and fault information is available in the FAULT registers (Table 4).

The logic-side SPI communication is powered from the V_{DDL} supply regardless of the V_{DD24F} or V_{DD3F} status. The internal digital isolation operates normally as long as V_{LF} and V_{DDL} voltages are in the normal operating range.

Table 4. SPI Port Power Status

V_{DD24F}	V_{DD3F}	V_{LF}	V_{DDL}	SPI REGISTER VALUE	FIELD-SIDE SPI COMMUNICATION	LOGIC-SIDE SPI COMMUNICATION
Valid	Valid	Valid	Valid	Data Maintained	Normal Operation	Normal Operation
Valid	Valid	Valid	Not Valid	Data Maintained	Normal Operation	$\overline{LCS}$ ignored, LSDO is High-Z
Valid	Not Valid	X*	X*	Data Maintained	$\overline{FCS}$ ignored, FSDO is High-Z*	$\overline{LCS}$ ignored, LSDO is High-Z*
Not Valid	Valid	Valid	Valid	Data Maintained	Normal Operation	Normal Operation
Not Valid	Valid	Valid	Not Valid	Data Maintained	Normal Operation	$\overline{LCS}$ ignored, LSDO is High-Z
Not Valid	Not Valid	X*	X*	Data Lost	$\overline{FCS}$ ignored, FSDO is High-Z*	$\overline{LCS}$ ignored, LSDO is High-Z*
X	Valid	Not Valid	X	Data Maintained	$\overline{FCS}$ ignored, FSDO is High-Z	$\overline{LCS}$ ignored, LSDO is High-Z

**When V_{LF} and V_{DDL} are both valid, the internal isolation is powered up and operates normally, and SPI signals are transmitted between field-side and logic-side, no matter if V_{DD24F} or V_{DD3F} is valid or not. This is useful when the isolation channels are shared by multiple field-side devices.*

Daisy-Chaining

For systems with more than eight sensor inputs, multiple field-side devices can be daisy-chained to allow access to all data inputs through a single isolated serial port. When using a daisy-chain configuration on the field-side, connect OSDI to the SDI of the first device in the chain. Connect FSDI to the SDO of the next to last device in the chain. The MAX22192 is the last device in the chain. For all middle links, connect SDI to SDO of the previous device and SDO to SDI of the next device. $\overline{FCS}$ and FSCLK of all devices in the chain should be connected together in parallel, see Figure 12, which illustrates a 24-input application for daisy-chaining and Figure 13, which shows SPI daisy-chian timing for Mode 3.

Configuration Flowchart

The MAX22192 powers on with default register settings and can be used in default mode to read the data inputs, or it can be configured to match the individual application requirements. Before any register access for configuration or reading data, the MCU needs to wait until AFS goes high indicating that the MAX22192 is powered up and ready for use. Next, the MCU needs to clear the $\overline{LFAULT}$ pin that asserts low after every power-up event due to the default state (high) of the POR bit in the FAULT1 register. See Figure 14 for details.

Default Mode (Power-up mode): In this mode, the Wire-Break (WB) function is disabled, all input channel filters (FLT_) are set to BYPASS, all input channels are enabled, and all fault sources are disabled on the $\overline{LFAULT}$ pin except the CRC and POR flags. Upon power-up, the POR flag is set to 1. If the $\overline{LFAULT}$ pin is being used, then a write operation must be performed to the FAULT1 register to reset POR to 0 for normal operating conditions. Now the MAX22192 is ready to be polled to read data from DI register to show the logic state of the eight input channels.

Configurable Mode: The MAX22192 can be configured for different parameters based upon the application requirements. The MCU can write to the various registers to set the options for wire break, input channel filters, enabling different fault sources, or disabling specific input channels. In addition, the user can enable features such as driving the LED matrix or making the $\overline{LFAULT}$ pin sticky or not. Once the configuration is complete, the MAX22192 is ready to be polled to read from DI register to show the logic state of the eight input channels.

$\overline{FAULT}$ Asserted: The MAX22192 uses the open-drain $\overline{LFAULT}$ pin to indicate to the MCU that a fault has occurred, often by using this pin to trigger an interrupt function within the MCU. The MCU can determine the source of the fault by reading regsiter FAULT1. If bit 5 of the FAULT1 register is set, then register FAULT2 is indicating a fault, and the FAULT2 register must also be read. Reading the FAULT_ register clears the fault flag, unless the fault condition persists, which would immediately reset the flag.

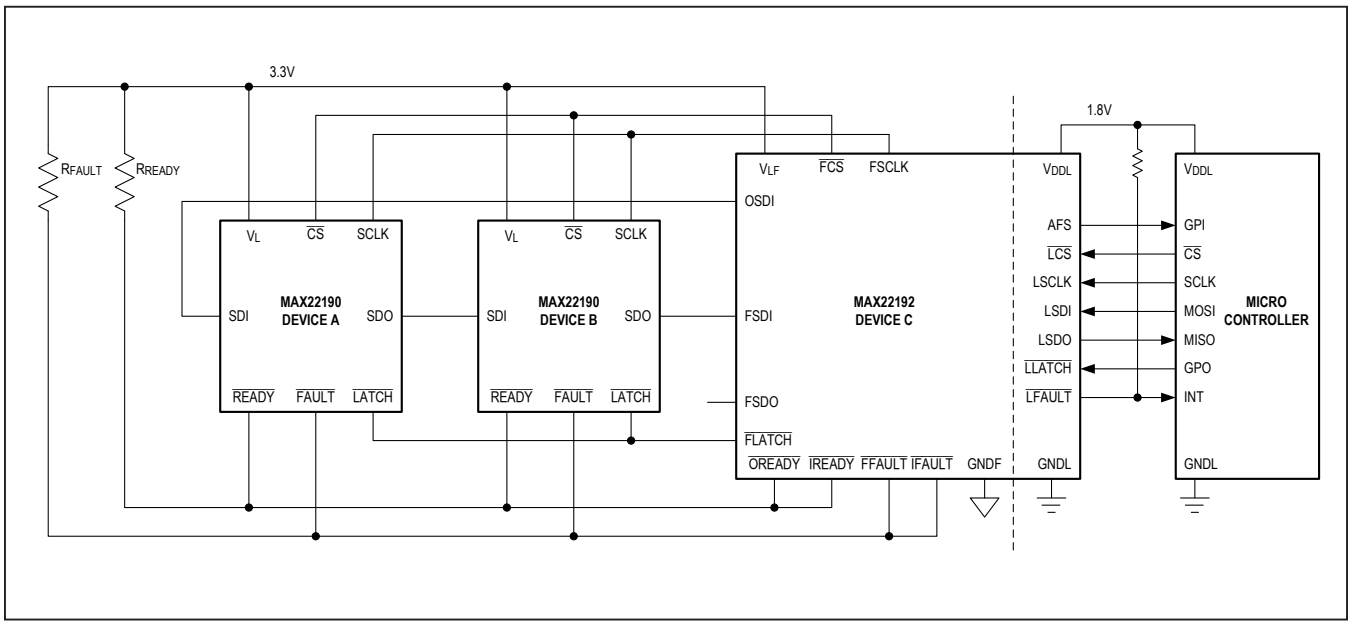


Figure 12. SPI Daisy-Chain Diagram

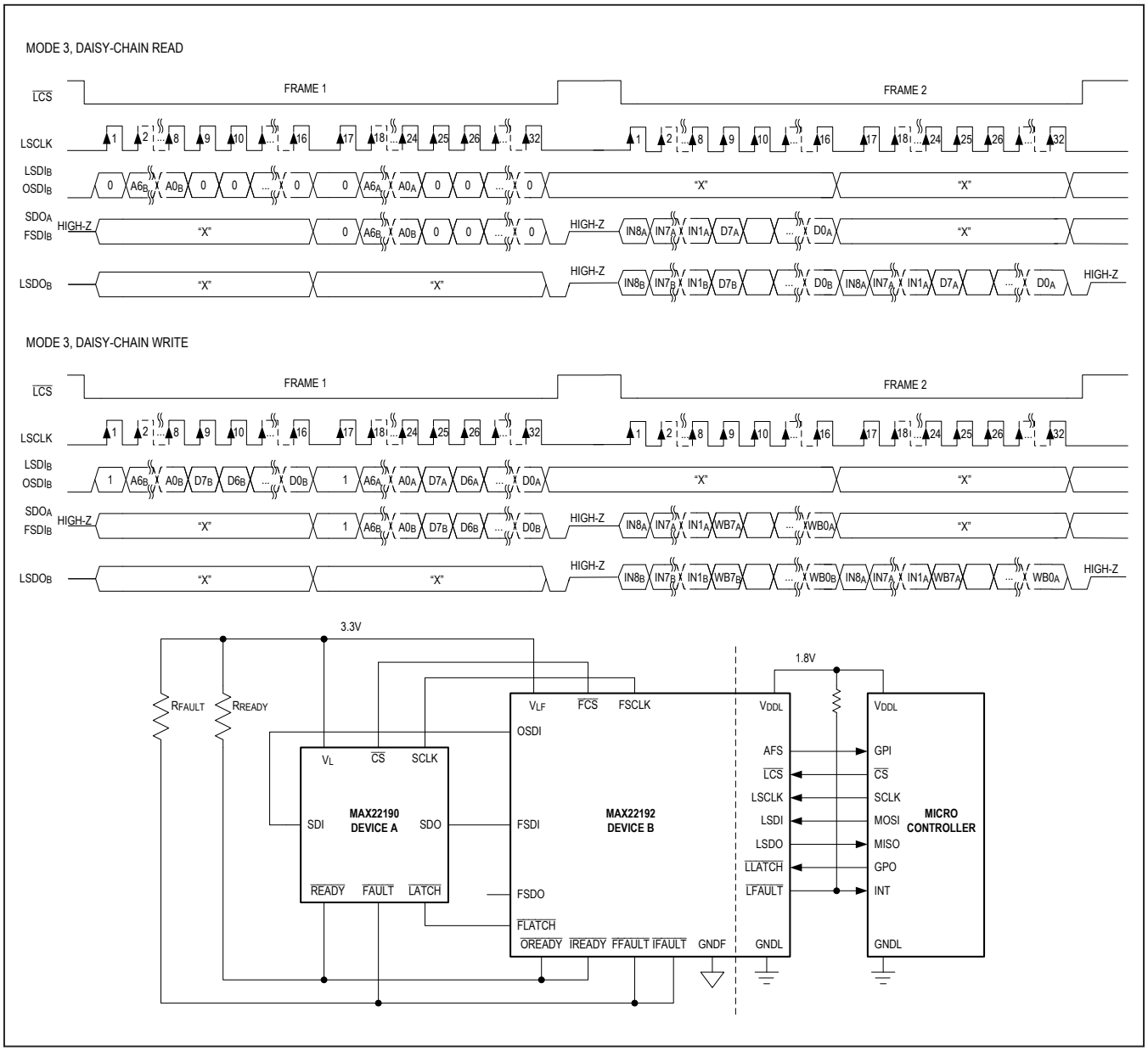


Figure 13. SPI Daisy-Chain Communication Example (Mode 3)

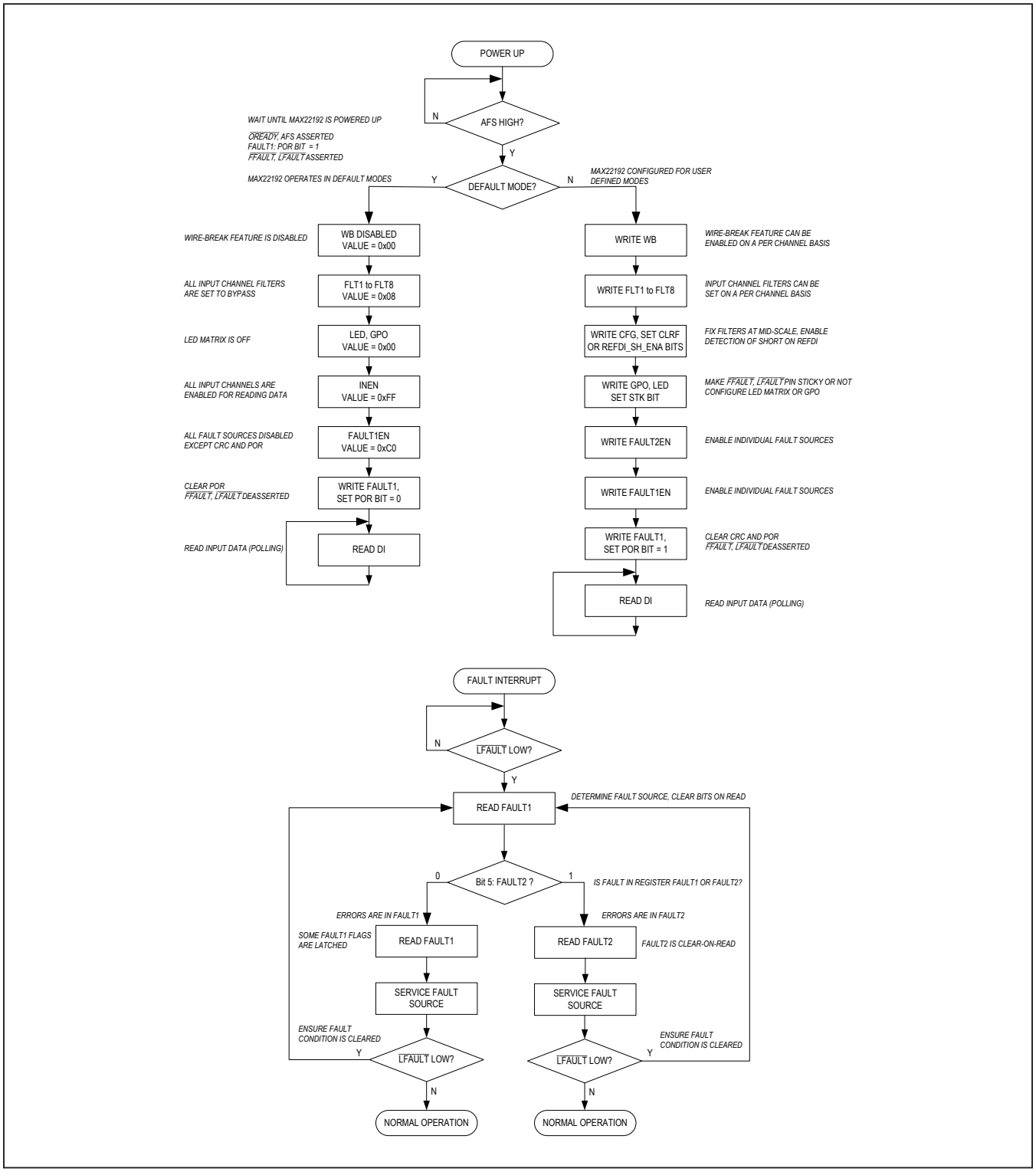


Figure 14. MAX22192 Configuration Flowchart

Table 5. SPI Frames for SPI Modes

Mode 0: M1 = 0, M0 = 0

Write

LSDI	MSB = 1 1-bit	Register Address 7-bits	Write Data 8-bits	000 Fill Data 3-bits			CRC from Host 5-bits LSB
LSDO	Input data: IN8 – IN1 8-bits		WB data: WB7 – WB0 8-bits	24VL	24VM	WBG	CRC from MAX22192 5-bits

Read

LSDI	MSB = 0 1-bit	Register Address 7-bits	0000,0000 Fill Data 8-bits	000 Fill Data 3-bits			CRC from Host 5-bits LSB
LSDO	Input data: IN8 – IN1 8-bits		Register Data: D7 – D0 8-bits	24VL	24VM	WBG	CRC from MAX22192 5-bits

Mode 1: M1 = 0, M0 = 1

Write

LSDI	MSB = 1 1-bit	Register Address 7-bits	Write Data 8-bits
LSDO	Input data: IN8 – IN1 8-bits		WB data: WB7 – WB0 8-bits

Read

LSDI	MSB = 0 1-bit	Register Address 7-bits	0000,0000 Fill Data 8-bits
LSDO	Input data: IN8 – IN1 8-bits		Register Data: D7 – D0 8-bits

Mode 2: M1 = 1, M0 = 0

Write – Preceding frame was a write or no-op

LSDI	MSB = 1 1-bit	Register Address 7-bits	Write Data 8-bits	000 Fill Data 3-bits			CRC from Host 5-bits LSB
LSDO	Input data: IN8 – IN1 8-bits		WB data: WB7 – WB0 8-bits	24VL	24VM	WBG	CRC from MAX22192 5-bits

Write – Preceding frame was a read

LSDI	MSB = 1 1-bit	Register Address 7-bits	Write Data 8-bits	000 Fill Data 3-bits			CRC from Host 5-bits LSB
LSDO	Input data: IN8 – IN1 8-bits		Register Data: D7 – D0 8-bits	24VL	24VM	WBG	CRC from MAX22192 5-bits

Read – Preceding frame was a write or no-op

LSDI	MSB = 0 1-bit	Register Address 7-bits	0000,0000 Fill Data 8-bits	000 Fill Data 3-bits			CRC from Host 5-bits LSB
LSDO	Input data: IN8 – IN1 8-bits		WB data: WB7 – WB0 8-bits	24VL	24VM	WBG	CRC from MAX22192 5-bits

Table 5. SPI Frames for SPI Modes (continued)

Read – Preceding frame was a read

LSDI	MSB = 0 1-bit	Register Address 7-bits	0000,0000 Fill Data 8-bits	000 Fill Data 3-bits			CRC from Host LSB 5-bits
LSDO	Input data: IN8 – IN1 8-bits		Register Data: D7 – D0 8-bits	24VL	24VM	WBG	CRC from MAX22192 5-bits

Mode 3: M1 = 1, M0 = 1

Write – Preceding frame was a write or no-op

LSDI	MSB = 1 1-bit	Register Address 7-bits	Write Data 8-bits
LSDO	Input data: IN8 – IN1 8-bits		WB data: WB7 – WB0 8-bits

Write – Preceding frame was a read

LSDI	MSB = 1 1-bit	Register Address 7-bits	Write Data 8-bits
LSDO	Input data: IN8 – IN1 8-bits		Register Data: D7 – D0 8-bits

Read – Preceding frame was a write or no-op

LSDI	MSB = 0 1-bit	Register Address 7-bits	0000,0000 Fill Data 8-bits
LSDO	Input data: IN8 – IN1 8-bits		WB data: WB7 – WB0 8-bits

Read – Preceding frame was a read

LSDI	MSB = 0 1-bit	Register Address 7-bits	0000,0000 Fill Data 8-bits
LSDO	Input data: IN8 – IN1 8-bits		Register Data: D7 – D0 8-bits

Notes:

LSDI: CRC generated by external device such as MCU, Data D7–D0 clocked out from MCU

LSDO: CRC generated by MAX22192, Data D7–D0 clocked out from MAX22192 Register

NO-OP: No Operation, i.e., write cycle with no valid data to specified address

Write Cycle: DI[7:0] and WB[7:0] are from internal latches, whose outputs are frozen when $\overline{LCS}$ or $\overline{LLATCH}$ goes low. Bits 24VL, 24VM and WBG are frozen by $\overline{LCS}$ going low but not by $\overline{LLATCH}$.

Read Cycle: D7–D0 are the register data addressed through LSDI. Bits 24VL, 24VM, and WBG reflect the corresponding bits in the FAULT1 register.

Input Channel: Pins are numbered IN1–IN8, so input IN1 maps to bit DI0, input IN2 to bit DI1 ... and input IN8 to bit DI7

Table 6. Register Map

REGISTER	ADDRESS	SYMBOL	TYPE	POR (DEFAULT)	7	6	5	4	3	2	1	0
Wire Break	0x00	WB	COR	0x00	WB7	WB6	WB5	WB4	WB3	WB2	WB1	WB0
Digital Input	0x02	DI	R	0x00	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
Fault 1	0x04	FAULT1	MIXED	0x46	CRC	POR	FAULT2	ALRMT2	ALRMT1	24VL	24VM	WBG
Filter IN1	0x06	FLT1	RW	0x08	0	0	0	WBE	FBP	DELAY[2:0]		
Filter IN2	0x08	FLT2	RW	0x08	0	0	0	WBE	FBP	DELAY[2:0]		
Filter IN3	0x0A	FLT3	RW	0x08	0	0	0	WBE	FBP	DELAY[2:0]		
Filter IN4	0x0C	FLT4	RW	0x08	0	0	0	WBE	FBP	DELAY[2:0]		
Filter IN5	0x0E	FLT5	RW	0x08	0	0	0	WBE	FBP	DELAY[2:0]		
Filter IN6	0x10	FLT6	RW	0x08	0	0	0	WBE	FBP	DELAY[2:0]		
Filter IN7	0x12	FLT7	RW	0x08	0	0	0	WBE	FBP	DELAY[2:0]		
Filter IN8	0x14	FLT8	RW	0x08	0	0	0	WBE	FBP	DELAY[2:0]		
Configuration	0x18	CFG	RW	0x00	0	0	0	24VF	CLRF	0	0	REFDI_SH_ENA
Input Enable	0x1A	INEN	RW	0xFF	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
Fault 2	0x1C	FAULT2	COR	0x02	0	0	FAULT8CK	OTSHDN	RFDIO	RFDIS	RFWBO	RFWBS
Fault 2 Enables	0x1E	FAULT2EN	RW	0x00	0	0	FAULT8CKE	OTSHDNE	RFDIOE	RFDISE	RFWBOE	RFWBSE
Auxiliary LED Drive	0x20	LED	RW	0x00	R2C1	R2C0	R1C2	R1C1	R1C0	R0C2	R0C1	R0C0
GPO	0x22	GPO	RW	0x00	STK	DIR	R2	R1	R0	C2	C1	C0
Fault 1 Enables	0x24	FAULT1EN	RW	0xC0	CRCE	PORE	FAULT2E	ALRMT2E	ALRMT1E	24VLE	24VME	WBGE
No-Op	0x26	NOP	NA	-	Dummy register. Contents of registers DI and WB are clocked out normally during attempted SPI writes to this register. Useful for daisy-chain modes.							

Register Type Legend:

R: Read only
RW: Read and Write
COR: Clear-On-Read
MIXED: Some bits are Clear-On-Read type, others are cleared differently. See the *Register Detailed Description* section for details.
0 = Reserved, always 0.

Register Detailed Description

WB (Clear-On-Read)
Address = 0x00
Default = 0x00

BIT	NAME	DESCRIPTION
7:0	WB[7:0]	0: WBx = 0, No wire-break condition detected for channel x 1: WBx = 1, Wire-break condition detected for channel x Wire-break status for each channel. The bit remains high even if the wire-break condition disappears and is only cleared upon reading the register. Not cleared if the wire-break condition is still present upon reading the register

Note: Input Channels are numbered IN1–IN8, so IN1 maps to WB0, IN2 to WB1 ... and IN8 to WB7.

DI (Read)
Address = 0x02
Default = 0x00

BIT	NAME	DESCRIPTION
7:0	DI[7:0]	0: DIx = 0, Channel x is driven low 1: DIx = 1, Channel x is driven high Digital input state, DI_ is the state of the corresponding input pin.

Note: Input Channels are numbered IN1–IN8, so IN1 maps to DI0, IN2 to DI1 ... and IN8 to DI7.

FAULT1 (Mixed)
Address = 0x04
Default = 0x46

BIT	NAME	DESCRIPTION
7	CRC	0: The last received SPI frame was not corrupted 1: The last received SPI frame was corrupted It is not cleared upon read, but when an uncorrupted SPI frame is received. CRC is only active in SPI Interface Modes 0 and 2
6	POR	0: Normal operating conditions 1: POR event has reset the register map to its power-on-reset state This bit is cleared only if the user writes “0” to it. The other bits in this register are unaffected by the write access.
5	FAULT2	0: An enabled bit in the FAULT2 register is not set 1: An enabled bit in the FAULT2 register is set This bit is cleared on read only if the FAULT2 register is cleared or the bit is disabled.
4	ALRMT2*	0: Temperature Alarm 2 threshold has not been exceeded 1: Temperature Alarm 2 threshold has been exceeded Cleared upon reading this register.
3	ALRMT1*	0: Temperature Alarm 1 threshold has not been exceeded 1: Temperature Alarm 1 threshold has been exceeded Cleared upon reading this register.
2	24VL*	0: 24V supply is normal (above the 24VL threshold) 1: 24V supply is low (below the 24VL threshold) Cleared upon reading this register. If bit 4 in the CFG Register (24VF) is 0, 24VL can also be cleared after any SPI transaction while operating in mode 0 or 2.

BIT	NAME	DESCRIPTION
1	24VM*	0: 24V supply is normal (above the 24VM threshold) 1: 24V supply is missing (below the 24VM threshold) Cleared upon reading this register. If bit 4 in the CFG Register (24VF) is 0, 24VM can also be cleared after any SPI transaction while operating in mode 0 or 2.
0	WBG	0: No bit in the WB register is set 1: One or more bits in the WB register are set Cleared upon reading the WB register.

*These flags are “latched” and they remain set until read even if the fault goes away, and are not cleared if the fault condition is still present when the register is read.

FLT1 to FLT8 (Read/Write)

Address = 0x06 – 0x14 (increments of 2)

Default = 0x08

BIT	NAME	DESCRIPTION
7:5	0	Reserved
4	WBE	0: Wire-Break detection is disabled for channel x 1: Wire-Break detection is enabled for channel x If WBE = 0, the corresponding WBx bit is always low and the WB detection circuits for channel x are off. The REFWB resistor on pin REFWB can be removed if the WBE bits of all the channels are low. The RFWBO bit in the FAULT2 register is set if WBE bits of all channels are low.
3	FBP	0: Programmable filter on INx is used 1: Programmable filter on INx is bypassed
2:0	DELAY[2:0]	Programmable filter values for INx (the wire-break filter value is 20ms and is not programmable). DELAY[2:0] = 000 = 50µs DELAY[2:0] = 001 = 100µs DELAY[2:0] = 010 = 400µs DELAY[2:0] = 011 = 800µs DELAY[2:0] = 100 = 1.6ms DELAY[2:0] = 101 = 3.2ms DELAY[2:0] = 110 = 12.8ms DELAY[2:0] = 111 = 20ms

CFG (Read/Write)

Address = 0x18

Default = 0x00

BIT	NAME	DESCRIPTION
7:5	0	Reserved
4	24VF	0: Flags 24VL and 24VM are cleared after any full frame SPI transaction or by reading the FAULT1 register 1: 24VL and 24VM are cleared only by reading the FAULT1 register Only affects SPI Interface Modes 0 and 2
3	CLRF	0: Filters (input filters and wire-break filters) operate normally 1: All the filters (input filters and wire-break filters) are fixed at the mid-scale value for the chosen delay The filters resume normal operation when CLRF is cleared.
2:1	0	Reserved
0	REFDI_ SH_ENA	0: Disables the detection of a short-circuit condition on the REFDI pin 1: Enables the detection of a short-circuit condition on the REFDI pin

INEN (Read/Write)
Address = 0x1A
Default = 0xFF

BIT	NAME	DESCRIPTION
7:0	CH[7:0]	0: CHx = 0, INx is disabled, the current source is set to 0mA, and the DIx bit in the DI register is set to 0 1: CHx = 1, INx is enabled

Note: Input Channels are numbered IN1–IN8, so IN1 maps to CH0, IN2 to CH1 ... and IN8 to CH7.

FAULT2 (Clear-On-Read)
Address = 0x1C
Default = 0x02

BIT	NAME	DESCRIPTION
7:6	0	Reserved
5	FAULT8CK	0: SPI receives a number of clock pulses equal to a multiple of eight, valid transaction 1: SPI receives a number of clock pulses not equal to a multiple of eight, the SPI command is rejected
4	OTSHDN	0: Normal operating conditions 1: Overtemperature Shutdown (the safe operating temperature has been exceeded) Overtemperature Shutdown: all inputs and LED drivers are turned off to reduce power dissipation and protect the device. The SPI interface and internal regulator remain active and if the temperature continues to rise, the regulator is turned off.
3	RFDIO	0: Normal operating conditions 1: Open condition is detected on the REFDI pin This bit remains 1 even if the fault condition disappears and is cleared upon reading this register. This bit is 1 when thermal shutdown happens because REFDI function turns off in thermal shutdown. No action on the intput channels when this condition occurs.
2	RFDIS	0: Normal operating conditions 1: Short condition is detected on the REFDI pin The bit remains 1 even if the fault condition disappears and is cleared upon reading this register. All the input channels are disabled as long as the short condition on REFDI is present.
1	RFWBO	0: Normal operating conditions 1: Open condition is detected on the REFWB pin This bit remains 1 even if the fault condition disappears and is cleared upon reading this register. This bit is 1 when thermal shutdown happens because REFWB function turns off in thermal shutdown. This bit is 1 after power-on-reset when all input channel's wire-break detection functions are off. No action on the input channels when this condition occurs and one or more channels' wire-break function is enabled.
0	RFWBS	0: Normal operating conditions 1: Short condition is detected on the REFWB pin This bit remains 1 even if the fault condition disappears and is cleared upon reading this register. No action on the input channels when this condition occurs and one or more channels' wire-break function is enabled.

FAULT2EN (Read/Write)
Address = 0x1E
Default = 0x00

BIT	NAME	DESCRIPTION
7:6	0	Reserved
5	FAULT8CKE	0: Disable bit FAULT2 in the FAULT1 register 1: Enable bit FAULT2 in the FAULT1 register to be set when FAULT8CK is high
4	OTSHDNE	0: Disable bit FAULT2 in the FAULT1 register 1: Enable bit FAULT2 in the FAULT1 register to be set when OTSHDN is high
3	RFDIOE	0: Disable bit FAULT2 in the FAULT1 register 1: Enable bit FAULT2 in the FAULT1 register to be set when RFDIO is high
2	RFDISE	0: Disable bit FAULT2 in the FAULT1 register 1: Enable bit FAULT2 in the FAULT1 register to be set when RFDIS is high
1	RFWBOE	0: Disable bit FAULT2 in the FAULT1 register 1: Enable bit FAULT2 in the FAULT1 register to be set when RFWBO is high
0	RFWBSE	0: Disable bit FAULT2 in the FAULT1 register 1: Enable bit FAULT2 in the FAULT1 register to be set when RFWBS is high

LED (Read/Write)
Address = 0x20
Default = 0x00

BIT	NAME	DESCRIPTION
7	R2C1	0: The LED located at row 2, column 1 of the LED matrix is off 1: The LED lcoated at row 2, column 1 of the LED matrix is on Note: the LEDs of the matrix are scanned with a duty cycle of 33%. The LED located at row 2, column 2 is reserved to show the status of the V_{DD24F} voltage monitoring. It is on when V_{DD24F} voltage is above the voltage missing threshold (24VM).
6	R2C0	0: The LED located at row 2, column 0 of the LED matrix is off 1: The LED lcoated at row 2, column 0 of the LED matrix is on
5	R1C2	0: The LED located at row 1, column 2 of the LED matrix is off 1: The LED lcoated at row 1, column 2 of the LED matrix is on
4	R1C1	0: The LED located at row 1, column 1 of the LED matrix is off 1: The LED lcoated at row 1, column 1 of the LED matrix is on
3	R1C0	0: The LED located at row 1, column 0 of the LED matrix is off 1: The LED lcoated at row 1, column 0 of the LED matrix is on
2	R0C2	0: The LED located at row 0, column 2 of the LED matrix is off 1: The LED lcoated at row 0, column 2 of the LED matrix is on
1	R0C1	0: The LED located at row 0, column 1 of the LED matrix is off 1: The LED lcoated at row 0, column 1 of the LED matrix is on
0	R0C0	0: The LED located at row 0, column 0 of the LED matrix is off 1: The LED lcoated at row 0, column 0 of the LED matrix is on

GPO (Read/Write)
Address = 0x22
Default = 0x00

BIT	NAME	DESCRIPTION
7	STK	0: $\overline{\text{FFAULT}}$ pin is not sticky. $\overline{\text{FFAULT}}$ condition is determined by the logical OR of the unmasked real-time FAULT1 register sources, and not the FAULT1 register bits. 1: $\overline{\text{FFAULT}}$ pin is sticky. If at least one bit in the FAULT1 register is set and unmasked, $\overline{\text{FFAULT}}$ remains low until FAULT1 register is read (Figure 8).
6	DIR	0: LEDR_ and LEDC_ pins are configured as LED drivers, and are controlled by the LED register 1: LEDR_ and LEDC_ pins are configures as GPO drivers, and are controlled by GPO register bits [5:0]
5	R2	0: Set LEDR2 pin low 1: Set LEDR2 pin high
4	R1	0: Set LEDR1 pin low 1: Set LEDR1 pin high
3	R0	0: Set LEDR0 pin low 1: Set LEDR0 pin high
2	C2	0: Set LEDC2 pin low 1: Set LEDC2 pin high
1	C1	0: Set LEDC1 pin low 1: Set LEDC1 pin high
0	C0	0: Set LEDC0 pin low 1: Set LEDC0 pin high

FAULT1EN (Read/Write)
Address = 0x24
Default = 0xC0

BIT	NAME	DESCRIPTION
7	CRCE	0: $\overline{\text{FFAULT}}$ pin is not asserted when CRC is 1 1: $\overline{\text{FFAULT}}$ pin is asserted when CRC is 1
6	PORE	0: $\overline{\text{FFAULT}}$ pin is not asserted when POR is 1 1: $\overline{\text{FFAULT}}$ pin is asserted when POR is 1
5	FAULT2E	0: $\overline{\text{FFAULT}}$ pin is not asserted when FAULT2 is 1 1: $\overline{\text{FFAULT}}$ pin is asserted when FAULT2 is 1
4	ALRMT2E	0: $\overline{\text{FFAULT}}$ pin is not asserted when ALRMT2 is 1 1: $\overline{\text{FFAULT}}$ pin is asserted when ALRMT2 is 1
3	ALRMT1E	0: $\overline{\text{FFAULT}}$ pin is not asserted when ALRMT1 is 1 1: $\overline{\text{FFAULT}}$ pin is asserted when ALRMT1 is 1
2	24VLE	0: $\overline{\text{FFAULT}}$ pin is not asserted when 24VL is 1 1: $\overline{\text{FFAULT}}$ pin is asserted when 24VL is 1
1	24VME	0: $\overline{\text{FFAULT}}$ pin is not asserted when 24VM is 1 1: $\overline{\text{FFAULT}}$ pin is asserted when 24VM is 1
0	WBGE	0: $\overline{\text{FFAULT}}$ pin is not asserted when WBG is 1 1: $\overline{\text{FFAULT}}$ pin is asserted when WBG is 1

NOP (N/A)
Address = 0x26
Default = N/A

BIT	NAME	DESCRIPTION
7:0	NOP[7:0]	Dummy register. DI[7:0] and WB[7:0] are clocked out normally during attempted SPI writes to this register. Useful for daisy-chain modes.

Applications Information

Power Supply Sequencing

The MAX22192 does not require special power supply sequencing. The field-side SPI interface logic level (V_{LF}) is set independently from the field supply (V_{DD24F}) or LDO output (V_{DD3F}) levels. The logic levels of field-side and logic-side SPI are also set independently by V_{LF} and V_{DDL}. Each supply can be present over the entire specified range regardless of the level or presence of the other supply.

Power Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{DD24F}, V_{DD3F}, and V_{LF} with a low-ESR and low-ESL 0.1µF ceramic capacitor in parallel with a 1µF ceramic capacitor to GNDF, respectively. Bypass V_{DDL} with a low-ESR and low-ESL 0.1µF ceramic capacitor in parallel with a 1µF ceramic capacitor to GNDL.

Place the bypass capacitors as close as possible to each power supply input pins.

PCB Layout Recommendations

The PCB designer should follow some critical recommendations in order to get the best performance from the design.

- Keep the input/output traces as short as possible. To keep signal paths low-inductance, avoid using vias.
- Keep the area underneath the MAX22192 isolation barrier free from ground and signal planes. Any galvanic or metallic connection between the field-side and logic-side defeats the isolation.
- Maximize the metal coverage for all layers, especially for top and bottom layer to optimize the heat dissipation.
- Use 2oz. copper for top and bottom layer if possible so that more heat can be drawn to the PCB.
- Maximize the number of vias under the package for thermal purposes. If possible, fill the via with copper, which further enhances the vertical heat transfer through the PCB.

EMC Standard Compliance

The MAX22192 is required to operate reliably in harsh industrial environments. Maxim does board-level immunity testing for products such as the MAX22192 to address IEC 61000-4-x Transient Immunity Standards:

- IEC 61000-4-2 Electrostatic Discharge (ESD)
- IEC 61000-4-4 Electrical Fast Transient /Burst (EFT)
- IEC 61000-4-5 Surge Immunity

Maxim's proprietary process technology provides high ESD support with internal ESD structures, but external components are also required to absorb energy from burst and surge transients. The circuit with external components shown in Figure 15 allows the device to operate in harsh industrial environments. Components were chosen to assist in suppression of voltage burst and surge transients, allowing the system to meet or exceed international EMC requirements. The system shown in Figure 15, using the components shown in Table 7, is designed to be robust against IEC ESD, EFT, and Surge specifications (see Table 9).

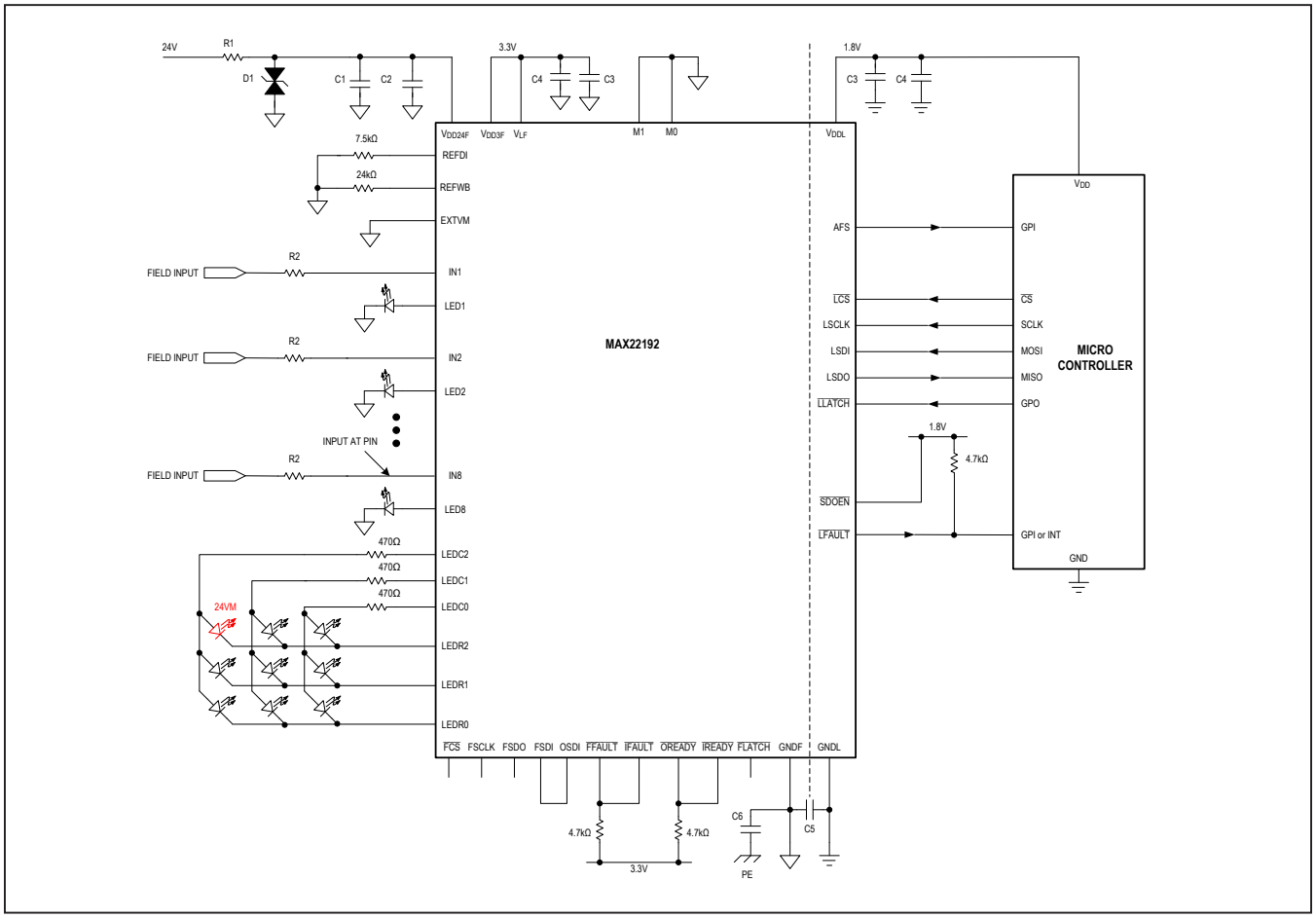


Figure 15. Typical EMC Protection Circuitry for the MAX22192

Table 7. Recommended Components

COMPONENT	DESCRIPTION	REQUIRED/RECOMMENDED
C1	1µF, 100V ceramic capacitor	Required
C2	0.1µF, 100V ceramic capacitor	Required
C3	1µF, 10V ceramic capacitor	Required
C4	0.1µF, 10V ceramic capacitor	Required
C5	1000pF safety rated Y capacitor (2220 or similar)	Recommended
C6	3300pF safety rated Y capacitor (2220 or similar)	Required
D1	Bidirectional TVS diode (SMAJ33CA or SM30T39AY)	Required
R1	150Ω, 1W pulse withstanding resistor (CMB0207 or similar)	Recommended
R2	1.5kΩ or 1kΩ, 1W pulse withstanding resistor (CMB0207 or similar)	Required
All other Resistors	1/8W resistor	Required
All LEDs	LEDs for visual input status indication	Recommended

Test Levels and Methodology

The MAX22192 is tested for transient immunity standards as specified in IEC 61000-4-x. These tests are for industrial equipment which are subjected to various transients. The three main tests are:

- IEC 61000-4-2: This ESD standard covering surges of tens of ns duration, is more stressful than other standards such as human body model (HBM) or machine model (MM), both of which are tested as standard for all Maxim products.
- IEC 61000-4-4: This standard indicates the capability of the device or equipment to survive repetitive electrical fast transients and bursts which often occur from arcing contacts in switches and relays.
- IEC 61000-4-5: This standard indicates the capability of the device or equipment to survive surges caused by events such as lightning strikes or industrial power surges caused by switching heavy loads or short-circuit fault conditions.

In all these tests, the part or DUT is soldered onto an application board with necessary external components. In the case of MAX22192, the standard Evaluation Kit (MAX22192EVKIT#) is used for these tests. Table 8 details all equipment used in the Surge, EFT and ESD tests. The test results are shown in Table 9.

Table 8. Equipment Used for EMC Tests

EQUIPMENT	DESCRIPTION	TEST(S)
MAX22192EVKIT#	Evaluation board with MAX22192 and recommended operating circuit	All
ESD Test Generator	Teseq NSG438 with Air-Gap Discharge Tip 403-826	Contact ESD and Air-Gap ESD
EFT/Surge Generator	Haefely Technology ECOMPACT4	EFT and Surge
Signal & Data Line Coupling Network	Teseq CDN 117	Surge
Coupler with 0.5µF Capacitor	INA 174A	Surge
Burst/EFT Data Line Coupling Clamp	Teseq CDN 3425	EFT

Table 9. Transient Immunity Test Results

TEST		RESULT
IEC 61000-4-2 Electrostatic Discharge (ESD)	Contact ESD	±8kV
	Air-Gap ESD	±15kV
IEC 61000-4-4 Electrical Fast Transient/Burst (EFT)	Line-to-Earth	±1kV
	Field Supply-to-Earth	±1kV
IEC 61000-4-5 Surge Immunity	Line-to-Line	±2kV
	Line-to-Ground	±1kV

IEC 61000-4-2 Electrostatic Discharge (ESD):

This is an international standard which gives immunity requirements and test procedures related to “electrostatic discharge”.

Contact Discharge method: the electrode of the test generator is held in contact with the EUT, and the discharge actuated by the discharge switch within the generator.

Air-Gap Discharge method: the charged electrode of the generator is brought close to the EUT, and the discharge actuated by a spark to the EUT.

An ESD Test Generator is used with a “sharp point” to make direct connection to the EUT (pin) under test for Contact ESD testing, and a “round tip” is added to the generator for Air-Gap ESD testing.

Output Voltage	Up to 8kV (nominal) for contact discharge up to 15kV (nominal) for air gap discharge
Polarity of the Output Voltage	Positive and negative
Holding Time	At least 5 seconds
Number of Applications	10 consecutive ESD discharges for each polarity

Transient voltage suppression (TVS) diodes are used to meet the ESD transient immunity requirements of IEC 61000-4-2. These diodes have extremely fast response time in order to respond to the 1ns rise time of the ESD pulse, Figure 16a shows the IEC 61000-4-2 ESD generator equivalent circuit, and Figure 16b shows the current waveform for IEC 61000-4-2 ESD Contact Discharge Test. The TVS diode clamps the incoming transients at a safe level to avoid damage to the semiconductor device.

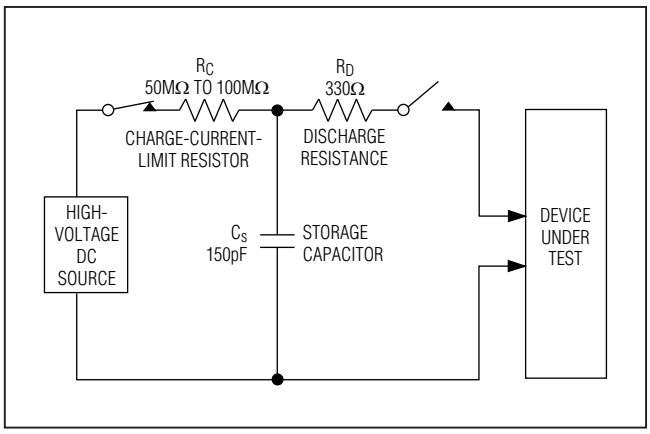


Figure 16a. ESD Generator Equivalent Circuit

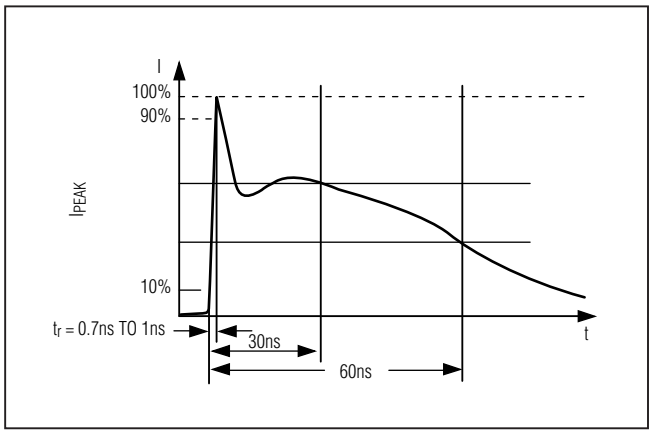


Figure 16b. ESD Contact Discharge Test Waveform

IEC 61000-4-4 Electrical Fast Transient / Burst (EFT)

An EFT/surge generator with an output voltage range with 50Ω load of up to 1kV is used to generate the voltage waveforms defined by the IEC specification. The capacitive coupling clamp provides the ability to couple the fast transients (burst) from the EFT generator to the pins of the MAX22192 without any galvanic connection to the MAX22192's pins. The waveform is shown in Figure 17.

Polarity	Positive and negative
Test Voltage	Up to 1kV
Repetition Frequency	5kHz
Burst Duration	15ms (at 5kHz)
Burst Period	300ms
Signal Applied To	Input Ports and Voltage Supply (V_{DD24F})
Test Duration	60 seconds

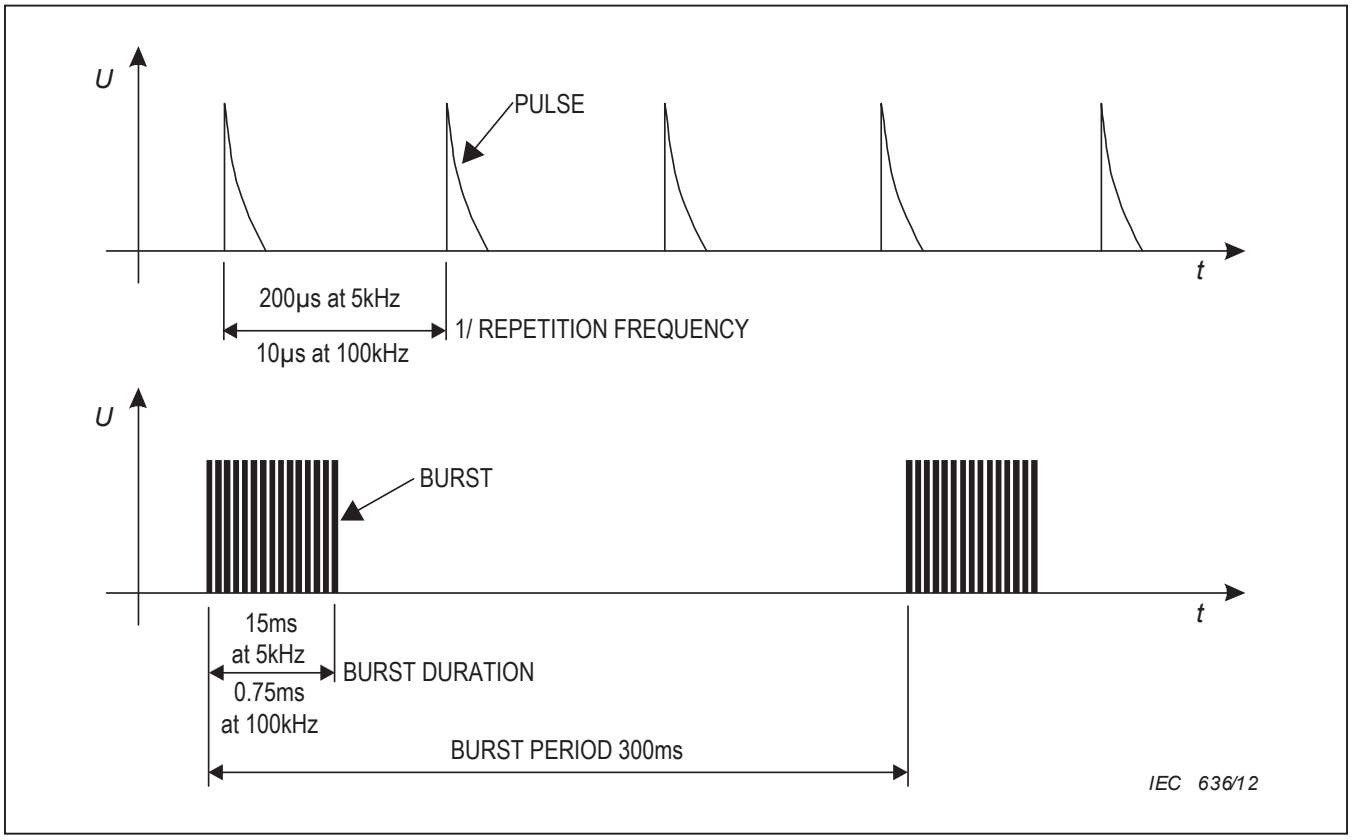


Figure 17. Electrical Fast Transient/Burst Waveform

IEC 61000-4-5 Surge Immunity

This standard specifies different wave generator specifications. The 1.2/50µs combination wave generator is used for testing ports intended for power lines and short-distance signal connections. This is the test Maxim uses and the waveform is shown in Figure 18.

Polarity	Positive and negative
Test Voltage	Up to 2kV
Waveform Parameters	Front time 1.2µs Time to half-value 50µs
Signal Applied to	Input port-to-Input port, Input port-to-Ground
Repetition Rate	1 per minute

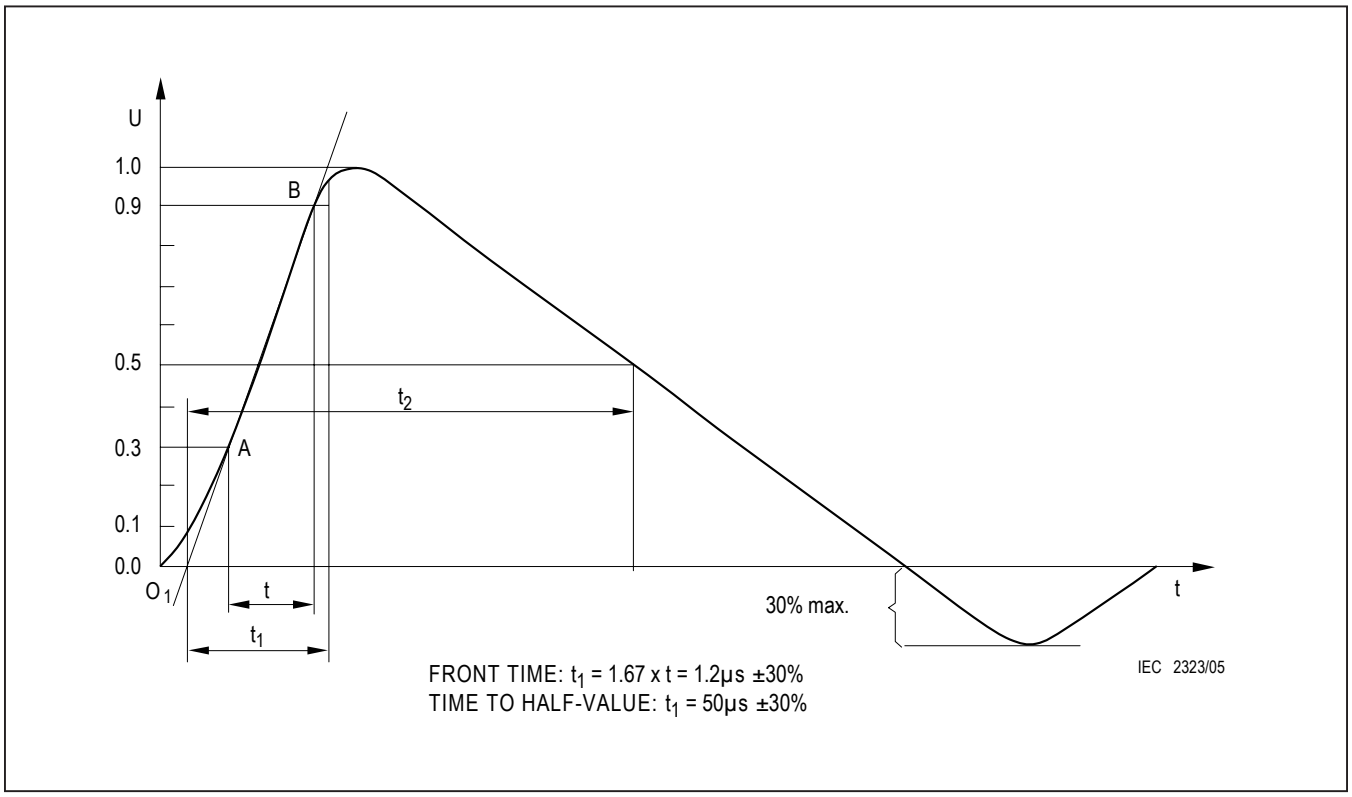


Figure 18. 1.2/50µs Surge Voltage Waveform

The standard defines 6 classes of test levels which depend on the installation conditions (see Annex A, table A.1 in IEC 61000-4-5 standard). The class determines the protection with corresponding voltage levels from 25V to 4kV. In addition, this defines the coupling mode (line-to-line or line-to-ground) and the source impedance (Zs) required. The Class which most closely fits the applications using products such as MAX22192 are Class 3 for unsymetrical operated circuits/lines with suggested test levels of ±2kV for line-to-line and ±1kV for line-to-ground.

The selection of source impedance is discussed in Annex B of IEC 61000-4-5 with recommended Zs of 42Ω. Since the generator has an internal impedance of 2Ω, an external 40Ω resistor is used in series with the generator, as shown in simplified version in Figure 19.

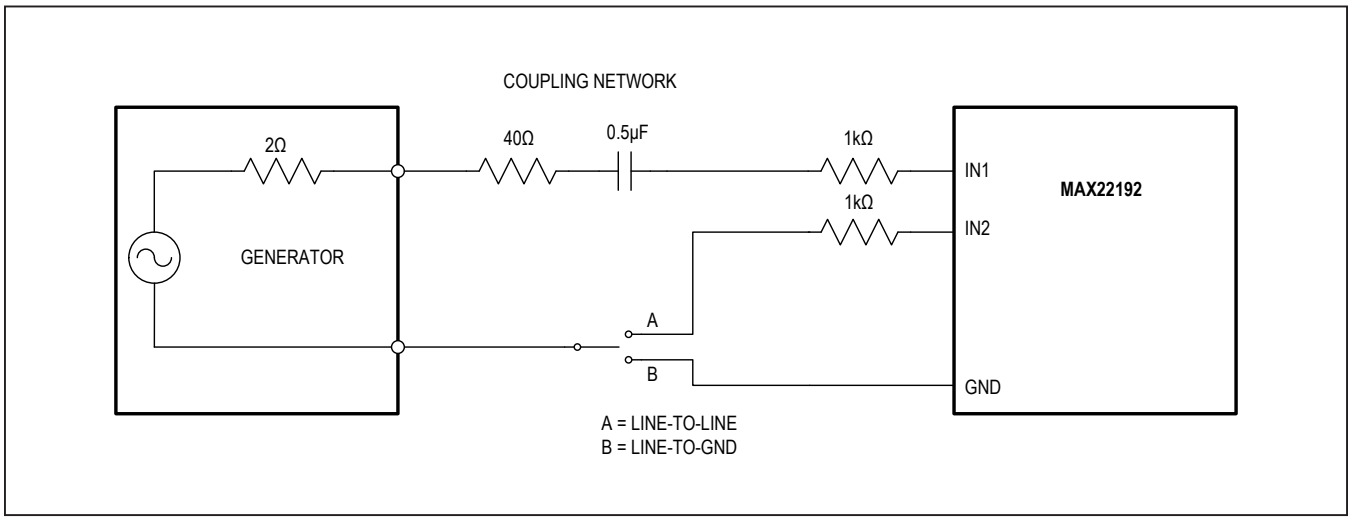
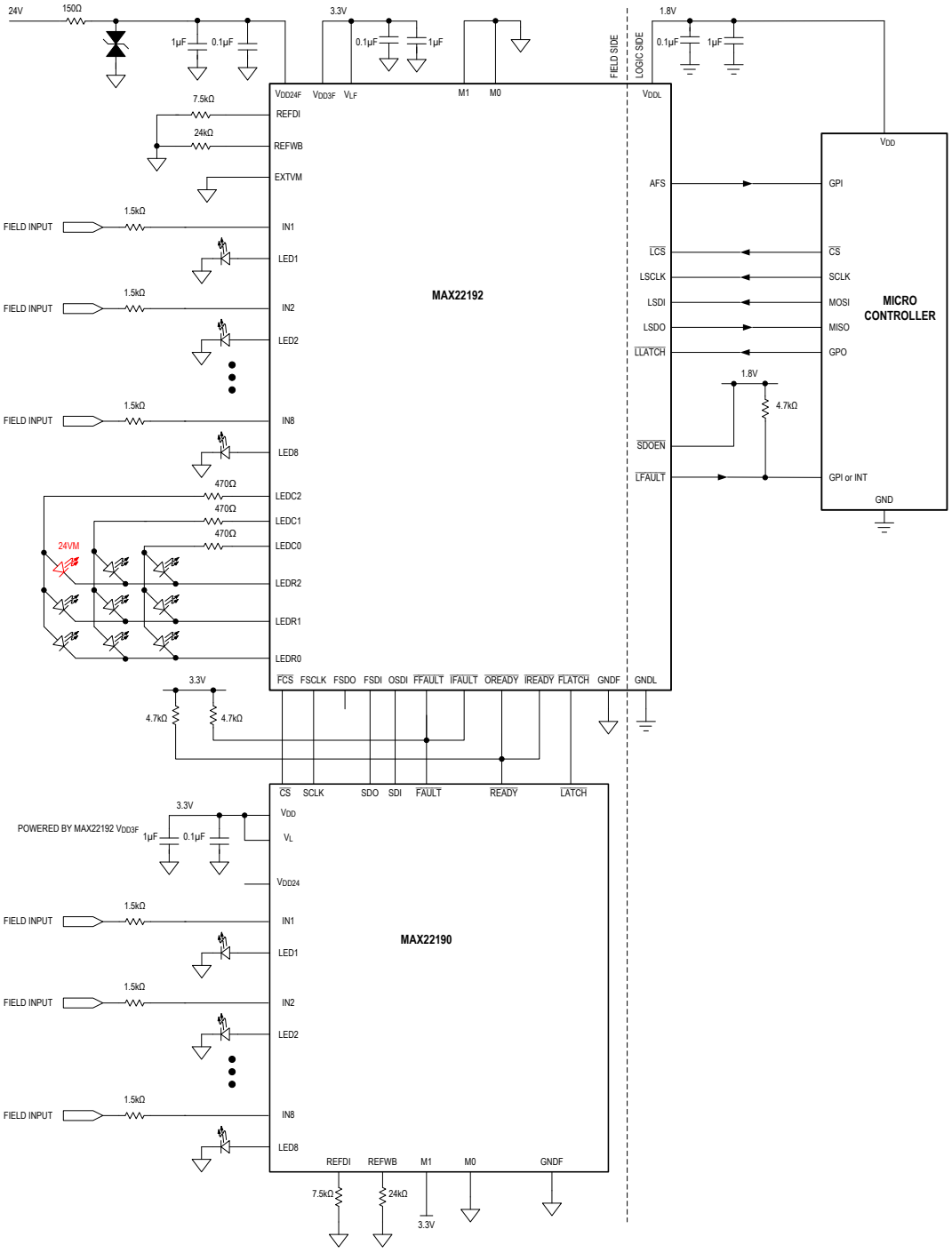


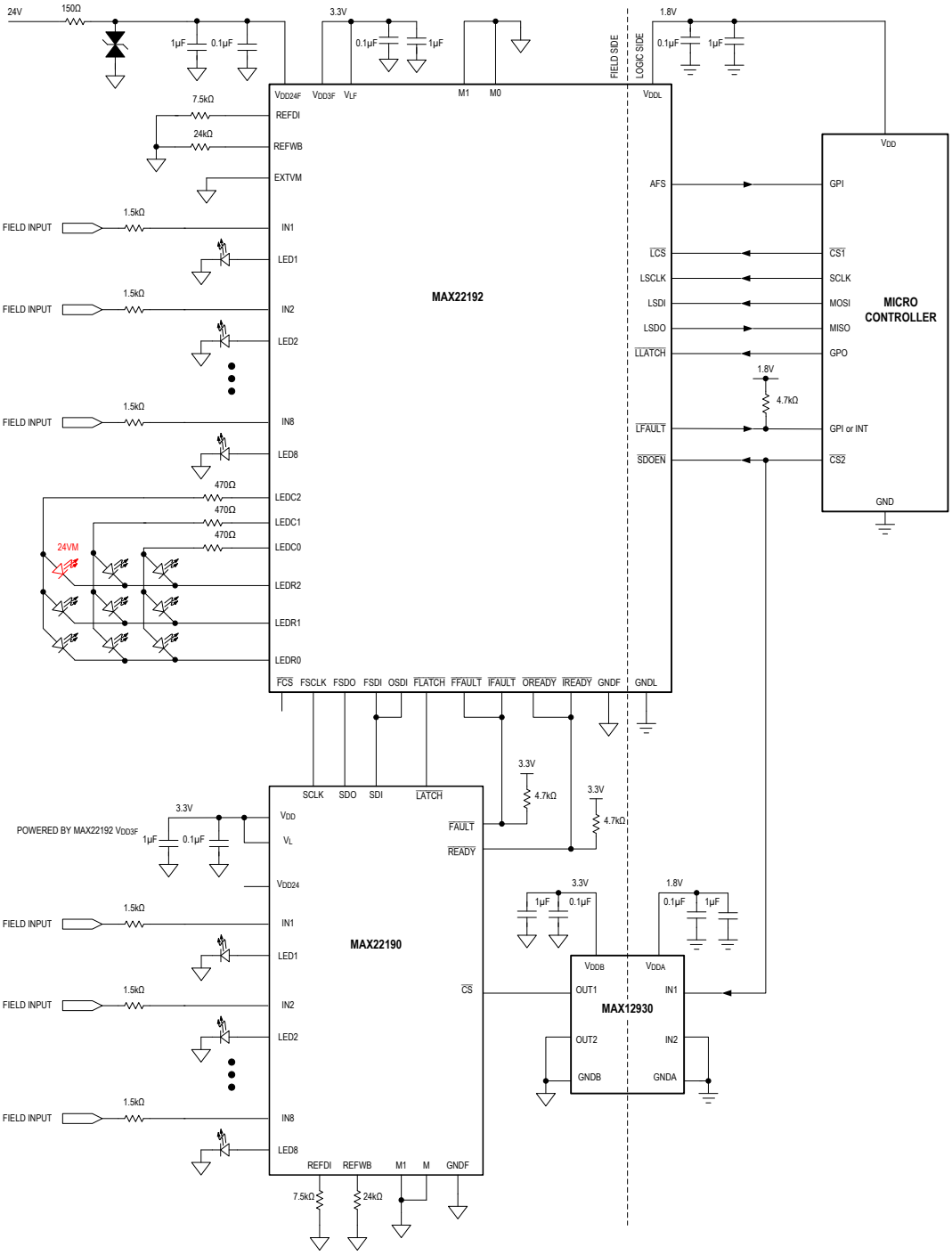
Figure 19. Surge Testing Methods

Typical Operating Circuits



16-CHANNEL, TYPE 1/3, ISOLATED, DIGITAL INPUTS WITH DAISY CHAIN SPI

Typical Operating Circuits (continued)



16-CHANNEL, TYPE 1/3, ISOLATED, DIGITAL INPUTS WITH INDEPENDENT SLAVE SPI

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX22192ARC+	-40°C to +125°C	70-GQFN

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/18	Initial release	—
1	11/18	Updated the *Isolated Octal Digital Input* figure, Figures 6, 10 and 15, *Isolation Channels* and *CRC Generation* sections, Table 7, and *Typical Operating Circuits*	2, 23, 27–28 30, 43, 49–50
2	3/19	Updated the *Safety Regulatory* section and added the *Safety Regulatory Approvals* table	1, 10

