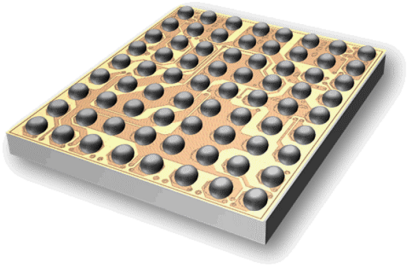
# STWLC68

Datasheet

## Qi-compliant inductive wireless power receiver for 5W applications



Flip Chip (3.29 x 3.70 mm)

## Features

- Up to 5 W output power
- Qi 1.2.4 inductive wireless standard communication protocol compliant
- Integrated 27 V synchronous rectifier with 98% (typ.) efficiency
- Low drop-out linear regulator with output current and input voltage control loops
- 3.6 V to 20 V programmable output voltage with 25 mV resolution
- Up to 80% overall system efficiency
- 32-bit, 64 MHz ARM Cortex microcontroller core
- OTP memory for configuration data
- 8-channels, 10-bit A/D Converter
- 6 configurable GPIOs
- Accurate voltage/current measurement for Foreign Object Detection (FOD)
- Output Over-Voltage clamping protection
- 400 kHz $I^2C$ interface
- On-chip thermal management and protections (Over-voltage, Over-current)
- Enhanced power dissipation capability Chip-Scale Package (CSP)

## Application

- Smartphones and PDAs
- Power banks
- GPS navigators
- Medical and healthcare equipment
- Wearable devices

| Product status link |
|---|
| STWLC68 |

| Product summary | |
|---|---|
| **Order code** | STWLC68JRH |
| **Package** | Flip Chip (3.29 x 3.70 mm) |
| **Packing** | Tape and reel |

## Description

The STWLC68 is an integrated Wireless Power Receiver suitable for portable applications and capable of managing up to 5 W of output power. The chip has been designed to support Qi 1.2.4 specifications for inductive communication protocol and Base Power Profile (BPP).

The STWLC68 shows excellent efficiency performance thanks to the integrated low-loss synchronous rectifier and the low drop-out linear regulator: both elements are dynamically managed by the digital core to minimize the overall power dissipation over a wide range of output load conditions.

Through the $I^2C$ interface the user can access and modify different configuration parameters, tailoring the operation of the device to the needs of custom applications. The configuration parameters can be saved in the embedded OTP memory and automatically retrieved at power-up, allowing the STWLC68 to operate as stand-alone device.
The STWLC68 is housed in a Chip-Scale Package to fit real-estate solutions in wearable devices.

# 1 Introduction

STWLC68 is a Wireless Power Receiver that rectifies the AC voltage developed across the receiving coil and provides a regulated DC voltage at the output.

The 32-bit core MCU is the supervisor of the whole device and manages all the functional blocks to

- establish and maintain communication with the transmitter,
- ensure adherence to Qi standard specifications (wherever required),
- optimize the efficiency by properly adjusting the operating point
- guarantee reliability by monitoring and protecting both the load and the device itself.

In order to execute the above mentioned (and many others) task, the MCU core relies on a resident firmware stored in ROM memory. In addition, some configuration parameters (e.g. output voltage, FOD tuning parameters, etc.) can be saved in the internal One-Time Programmable (OTP) memory and retrieved at power-up, allowing the STWLC68 to operate as a fully autonomuous stand-alone chip.

Applications in which the host system directly monitors or controls the power transfer, the I2C interface provides full access to the internal registers of the STWLC68.

The device is also equipped with six programmable general-purpose I/O pins (GPIOs) to implement specific functions (e.g. driving status LEDs, enabling the output on request, informing the host system about faulty conditions, etc.).

Figure 1 shows the block diagram of the device with simplified interconnections among the functional blocks. The synchronous rectifier converts the AC voltage from the receiving coil into a DC voltage at the VRECT pin. The four switches of the rectifier (that is basically an H-bridge) are controlled by the digital core in order to minimize both conduction and switching losses as a function of the output voltage and current, both monitored by two channels of the ADC. Two bootstrap capacitors are externally connected to the BOOT1-BOOT2 pins to correctly drive the high-side switches of the rectifier.

The output of the rectifier, filtered by an external capacitor, is also the input rail for the main LDO linear regulator and for the auxiliary linear regulators in charge of deriving the 5 V and 1.8 V supply voltages.

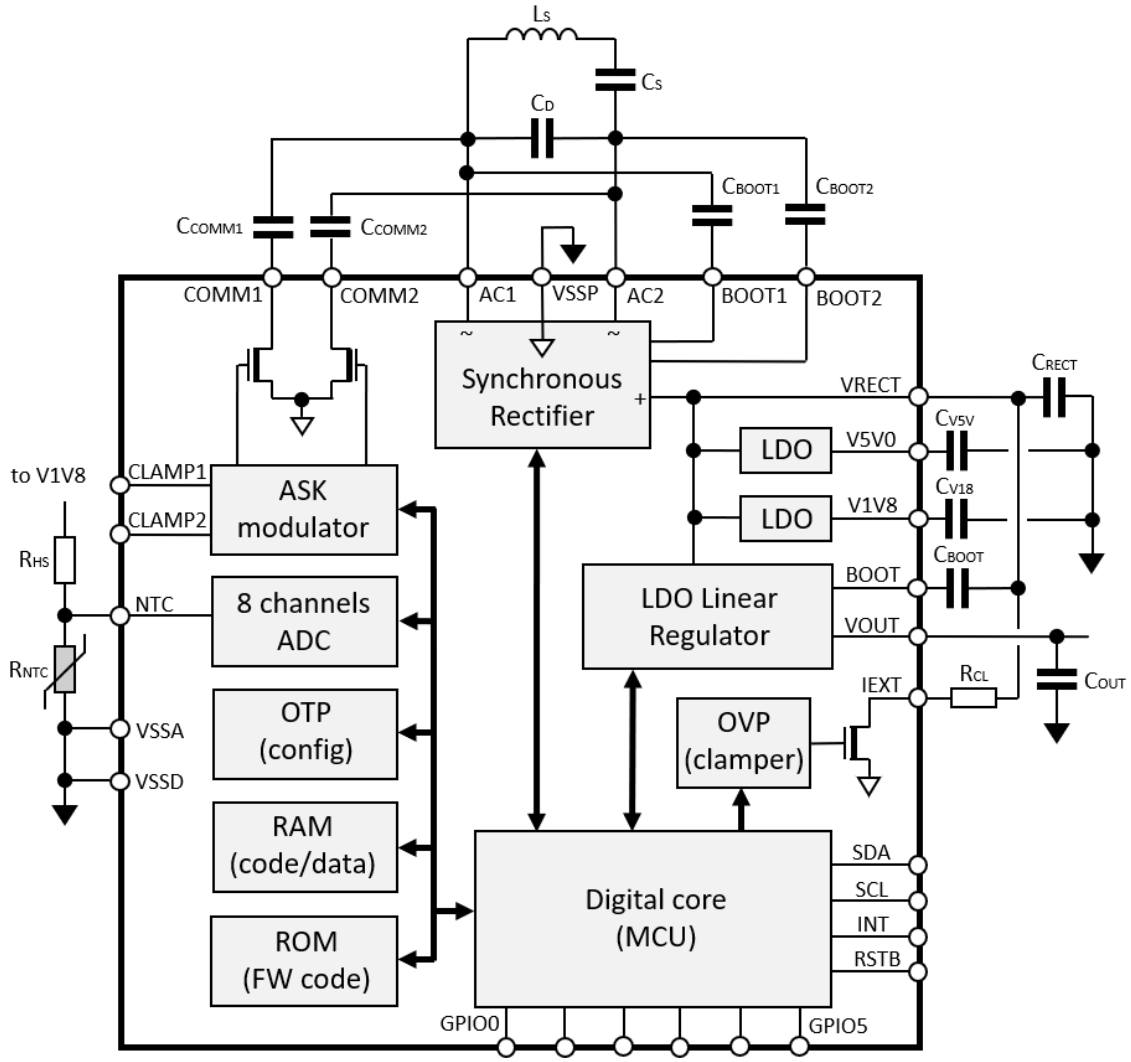
The digital core has full control of the main LDO linear regulator in order to manage the output voltage, the output current and the drop-out voltage: since the most relevant contribution to the total chip power dissipation is due to the main linear regulator, minimizing its drop-out voltage is a key factor.

Of course the minimization of the drop-out voltage requires a closed loop regulation of the voltage at the VRECT pin, i.e. a feedback information that is sent to the transmitter (via ASK modulation) which, in turn, adjusts the delivered power by acting on the supply voltage, the switching frequency or the switching duty-cycle (or a combination of the three) of its own power stage, depending on the adopted technique.

This regulation loop involving the transmitter is an essential part of the wireless power transmission and is extensively described in Qi specifications.

## 2 Block diagram

Figure 1. **Simplfied block diagram**



# 3 Device pinout

Figure 2. **Pin assignment (through top view)**

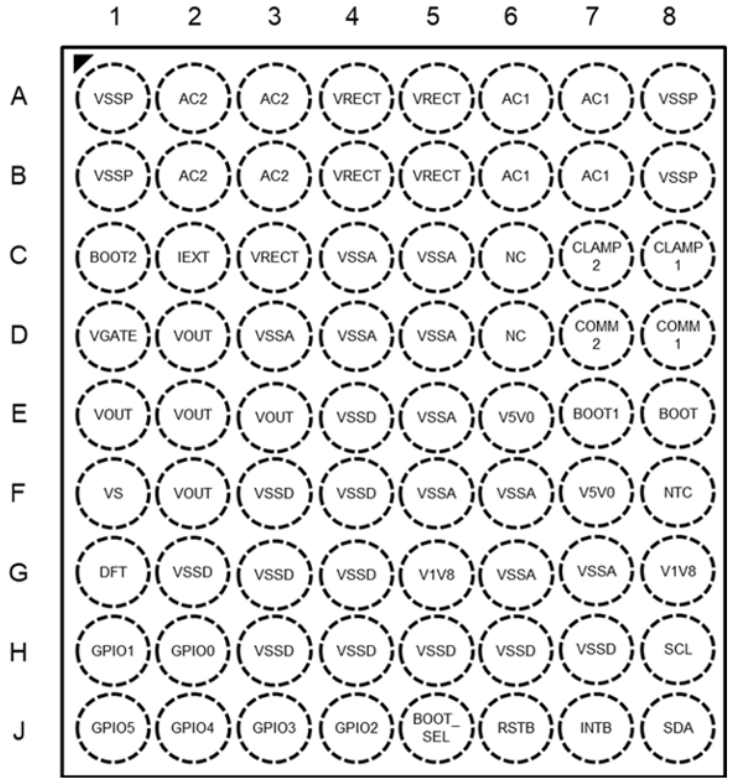



Table 1. **Pin description**

| Pin name | Pin location | Pin function |
|---|---|---|
| VSSA | C4,C5,D3,D4, D5,E5,F5,F6, G6,G7 | Analog ground. Power return for the main LDO and the analog circuitry. |
| VSSD | E4, F3, F4, G2, G3, G4, H3, H4, H5, H6, H7 | Digital ground. Reference for digital input and output signals. |
| VSSP | A1, A8, B1, B8 | Power ground. Power return for the synchronous rectifier. |
| AC1 | A6, A7, B6, B7 | AC power input: input of the synchronous rectifier. Connect to RX series resonant circuit. |
| AC2 | A2, A3, B2, B3 | AC power input: input of the synchronous rectifier. Connect to RX series resonant circuit. |
| BOOT1 | E7 | Synchronous rectifier bootstrap capacitor connection: a 47 nF (typ.) ceramic capacitor is connected between this pin and AC1. |
| BOOT2 | C1 | Synchronous rectifier bootstrap capacitor connection: a 47 nF (typ.) ceramic capacitor is connected between this pin and AC2. |
| BOOT | E8 | Main LDO power transistor bootstrap capacitor. Connect a 4.7 nF (typ.) ceramic capacitor between this pin and VRECT. |
| CLAMP1 | C8 | Auxiliary modulation switches connection: capacitors between CLAMP1 and AC1 and between CLAMP2 and AC2 are used to implement additional ASK modulation. These |

| Pin name | Pin location | Pin function |
|---|---|---|
| CLAMP2 | C7 | pins are optionally used, in conjunction with COMM1 and COMM2 pins, to modify the ASK modulation index in specific operating conditions. |
| VRECT | A4, A5, B4, B5, C3 | Synchronous rectifier output and input for the main LDO linear regulator. A suitable capacitor between these pins and VSSP ensures residual AC ripple filtering and energy storage for proper load transient response. |
| VS | F1 | Reserved: this pin must be left floating. |
| DFT | G1 | Reserved: this pin must be connected to ground. |
| BOOT_SEL | J5 | Reserved: this pin must be connected to ground. |
| NTC | F8 | Coil temperature sensing input: this pin is connected to the center tap of a resistor divider having an NTC in the low-side position. If this function is not used, the pin must be pulled-up to V18 through a 10 kΩ resistor to prevent triggering the coil over-temperature protection. |
| COMM1 | D8 | Modulation switches connection: capacitors between COMM1 and AC1 pin and between COMM2 and AC2 pin are used to implement ASK modulation. |
| COMM2 | D7 | |
| VOUT | D2, E1, E2, E3, F2 | Main LDO linear regulator output voltage. Connect a suitable filtering capacitor between these pins and VSSA to ensure stable operation and proper load transient response in all operating conditions. |
| V1V8 | G5, G8 | 1.8V LDO output and supply rail for the digital core, the ADC and the analog circuitry. Connect a 1 µF filtering capacitor between this pin and ground. |
| V5V0 | F7, E6 | 5V LDO output and supply rail for the auxiliary circuitry. Connect a 1 µF filtering capacitor between this pin and ground. |
| RSTB | J6 | Chip-reset input. If set low, the internal digital core is reset. This pin is eventually used by the host controller to control the power transfer process. Connect to V1V8 pin if not used. |
| IEXT | C2 | Internal pull-down switch for resisitive (dissipative) over-voltage protection: a resistor with adequate power dissipation capability must be connected between this pin and VRECT to damp excessive voltage developing at the output of the rectifier. |
| VGATE | D1 | Gate driver output for the optional VRECT discharging transistor. This pin goes high when the voltage drop across the main LDO (VVRECT – VVOUT) exceeds the programmed threshold. |
| SCL | H8 | I2C bus, clock line input. A pull-up resistor to the supply rail of the host controller is required to ensure correct digital levels. |
| SDA | J8 | I2C bus, data line I/O. A pull-up resistor to the supply rail of the host controller is required to ensure correct digital levels. |
| NC | C6, D6 | Reserved: this pin must be connected to ground or left floating. |
| GPIO0 | H2 | Programmable general-purpose I/Os: the function of these pins depends on the configuration of the device. |
| GPIO1 | H1 | |
| GPIO2 | J4 | |
| GPIO3 | J3 | |
| GPIO4 | J2 | |
| GPIO5 | J1 | |
| INTB | J7 | Interrupt output (active low). Programmable open-drain output used to generate an interrupt on specific events for the host controller. Also used as auxiliary control signal during OTP flash. |

# 4 Electrical and thermal specifications

## 4.1 Absolute maximum ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other condition above those indicated in Table 2 is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

**Table 2. Absolute maximum ratings**

| Parameter | Pin(s) | Min. | Max. | Unit |
|---|---|---|---|---|
| Pin voltage range | AC1, AC2, COMM1, COMM2, CLAMP1 and CLAMP2 respect to ground (VSSA, VSSD and VSSP pins) | -0.9 | 27 | V |
| | BOOT1 to AC1 | -0.3 | 5.5 | |
| | BOOT2 to AC2 | | | |
| | BOOT1 and BOOT2 respect to ground (VSSA, VSSD and VSSP pins) | -0.3 | 27 | |
| | BOOT respect to VRECT | -0.3 | 5.5 | |
| | VRECT, VOUT and IEXT respect to ground (VSSA, VSSD and VSSP pins) | -0.7 | 27 | |
| | V1V8, NTC, VS and DFT respect to ground (VSSA, VSSD and VSSP pins) | -0.3 | 2 | |
| | V5V0, VGATE, GPIO0 through GPIO5, INTB, RSTB, SDA, SCL and BOOT_SEL respect to ground (VSSA, VSSD and VSSP pins) | -0.7 | 5.5 | |
| | Relative voltage between any ground pin (VSSA, VSSD, VSSP) | -0.3 | 0.3 | |
| R.M.S. pin current | AC1, AC2, VRECT, VOUT, VSSP | | 2.5 | A |
| | COMM1, COMM2, IEXT | | 0.5 | |
| | CLAMP1, CLAMP2 | | 1 | |
| Peak pin current (1 ms pulse) | AC1, AC2, VRECT, VOUT, VSSP | | 5 | |
| HBM ESD susceptibility JEDEC JS001-2012 | All pins | | 2000 | V |
| CDM ESD susceptibility JEDEC JS002-2012 | | | 500 | |
| Latch-Up EIA/JESD78E | | -200 | 200 | mA |

## 4.2 Thermal characteristics

**Table 3. Thermal characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $T_{A,OP}$ | Operating ambient temperature | | 0 | | 85 | °C |
| $T_{J,OP}$ | Operating junction temperature | | 0 | | 150 | |
| $R_{\Theta JA}$ (1) | Junction to ambient thermal resistance | 2s2p | | 40 | | °C/W |
| $R_{\Theta JC}$ | Junction to case thermal resistance | | | 30 | | |
| $T_{SHDN}$ | Thermal shutdown threshold | | | 150 | | °C |
| $T_{SHDN,HYST}$ | Thermal shutdown hysteresis | | | 20 | | |

1. *Device mounted on a standard JESD51-5 test board*

## 4.3 Electrical characteristics

0 °C < $T_A$ < 85 °C; $V_{VRECT}$ = 5 V to 10 V. Typical values are at $T_J$ = 25 °C, if not otherwise specified.

**Table 4. Electrical characteristics**

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Supply section** | | | | | | |
| $V_{VRECT,UVLO}$ | VRECT Under-Voltage Lock-Out upper (turn-on) threshold | VRECT pin voltage, rising edge | | 3.0 | 3.3 | V |
| | VRECT Under-Voltage Lock-Out lower (turn-off) threshold | VRECT pin voltage, falling edge | | 2.5 | | |
| $V_{VRECT,MAX}$ | VRECT maximum operating supply voltage | Voltage on VRECT pin | | 16 | | V |
| $I_{VOUT,Q}$ | VOUT current consumption in shut-down mode | RSTB low for more than 1 ms, supply voltage (5 V) applied to VOUT | | 400 | 750 | µA |
| $I_{VRECT,OP}$ | Operating current consumption (not considering the programmed dummy-load current) | RSTB high, supply voltage applied to VRECT | | 9.7 | 13 | mA |
| $I_{VOUT,OP}$ | | RSTB high, supply voltage applied to VOUT | | 9.7 | 13 | |
| **1.8V supply voltage LDO linear regulator** | | | | | | |
| $V_{V1V8}$ | LDO1 output voltage | $I_{V1V8}$ = 5 mA | 1.79 | 1.8 | 1.81 | V |
| | LDO1 load regulation | 0 mA < $I_{V1V8}$ < 10 mA | | 5 | 20 | mV |
| **5V supply voltage LDO linear regulator** | | | | | | |
| $V_{V5V0}$ | LDO2 output voltage | $I_{V5V0}$ = 5 mA, $V_{VRECT}$ = 5.1 V | 4.8 | 5 | 5.2 | V |
| | LDO2 load regulation | 0 mA <$I_{V5V0}$ = 0 mA <10 mA | | 2 | 20 | mV |
| | LDO2 under-voltage lock-out upper threshold | | 2.8 | 3 | 3.2 | V |
| $I_{V5V0,EXT}$ | Maximum current allowed for external load | | | | 10 | mA |
| **Synchronous rectifier** | | | | | | |
| Efficiency | Target rectifier efficiency | $I_{VRECT}$ = 1 A, $V_{VRECT}$= 5.2 V, $f_{AC}$ = 100 kHz to 250 kHz | | 97 | | % |

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Efficiency | Target rectifier efficiency | $I_{VRECT}$ = 1 A, $V_{VRECT}$ = 9.2 V, $f_{AC}$ = 100 kHz to 250 kHz | | 97 | | % |
| $R_{DSON,ACx}$ | Synchronous rectifier switches on-resistance | low resistance mode (dynamically selected) | 60 | 70 | 80 | m Ω |
| | | high resistance mode (dynamically selected) | 150 | 250 | 350 | |
| **ASK modulator** | | | | | | |
| $R_{DSON,COMMx}$ | COMM1-COMM2 modulation switches on-resistance | $V_{VRECT}$ = 5 V | | 1 | 2 | Ω |
| $R_{DSON,CLAMPx}$ | CLAMP1-CLAMP2 modulation switches on-resistance | $V_{VRECT}$ = 5 V | | 1 | | Ω |
| $I_{DMYL,MAX}$ | Dummy load current (internally drawn from VRECT when enabled) | $V_{VRECT}$ = 5 V to 12 V, $I_{VRECT}$ = 0 A, IDMYL_SET = 0x1F | | 310 | | mA |
| $I_{DMYL,STEP}$ | | | | 10 | | |
| **Main LDO linear regulator** | | | | | | |
| $V_{OUT}$ | Output voltage range | VOUT_SET = 0x00C8 | 4.95 | 5.0 | 5.05 | V |
| | | VOUT_SET = 0x0320 | 19.92 | 20 | 20.08 | |
| | Vout Line regulation | $I_{VOUT}$ = 0.1 A, $V_{OUT}$ = 5 V, 6 V < $V_{VRECT}$ < 15 V | | 3 | 15 | mV |
| | Vout Load regulation | $V_{VRECT}$ = 5.5 V, $V_{OUT}$ = 5 V, 1 mA < $I_{VOUT}$ < 800mA | | 30 | 70 | mV |
| $V_{OUT_STEP}$ | Programmable step size | | | 25 | | mV |
| $V_{DROP}$ | Linear regulator drop-out voltage | $I_{OUT}$ = 1 A | | 100 | 200 | mV |
| $I_{OUT_CL}$ | Linear regulator overcurrent protection | | 1.4 | 1.5 | 1.6 | A |
| **Thermal protection (external NTC)** | | | | | | |
| $V_{NTC,OTP}$ | External over-temperature NTC pin upper threshold | | 0.55 | 0.59 | 0.65 | V |
| | External over-temperature NTC pin hysteresis | | 50 | 125 | 150 | mV |
| $I_{NTC,BIAS}$ | NTC pin bias current | $V_{NTC}$ = 1.5 V | | 1 | 2 | µA |
| **Over-Voltage Protection** | | | | | | |
| $V_{VRECT,OVPH}$ | Hard OVP (AC1-AC2 short to VSSP) upper threshold | | 24.2 | 24.7 | 25.2 | V |
| | Hard-OVP hysteresis | | 0.5 | 1.0 | 1.5 | |
| $V_{VRECT,OVPS}$ | Adjustable Soft OVP (IEXT clamping) upper threshold | VRECT_OVP = 0x2EE0 | 11.5 | 12 | 12.5 | V |
| | | VRECT_OVP = 0x4650 | 17.5 | 18 | 18.5 | |
| | Fixed Soft OVP (IEXT clamping) upper threshold | | 22.5 | 23 | 23.5 | |
| $I_{IEXT,MAX}$ | IEXT clamping switch current capability | Non-repetitive 100 ms rectangular pulse | | | 0.3 | A |
| $R_{IEXT,ON}$ | IEXT switch on-resistance | $I_{IEXT}$ = 250 mA | | 1.8 | 3 | Ω |
| **Digital signals** | | | | | | |
| $V_{IL}$ | Low level input voltage | | | | 0.55 | V |
| $V_{IH}$ | High level input voltage | | 1.14 | | | |

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | GPIOx high level output voltage | Output high, $I_{SOURCE}$ = 3mA | 1.25 | | | V |
| $I_{OH}$ | GPIOx pin current capability | Output high | 3 | | | mA |
| $V_{OL}$ | Low level output voltage | Output low, $I_{SINK}$=3mA | | 360 | | mV |
| $I_{IPU}$ | Internal pull-up current | GPIOx, INTB, SCL, SDA pins | 10 | 16 | 22 | µA |
| | | RSTB pin | 4 | 8 | 13 | |
| $I_{IPD}$ | Internal pull-down current | GPIOx, INTB, SCL, SDA pins | 10 | 16 | 22 | |
| | | RSTB pin | 4 | 8 | 13 | |

## 4.4 Recommended operating conditions

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **DC characteristics** | | | | | | |
| $V_{VRECT,OP}$ | Operating VRECT supply voltage range | | 4.5 | | 16 | V |
| $V_{VRECT,BPP}$ | Operating VRECT supply voltage range in BPP mode | $V_{VOUT}$ = 5 V, $I_{VOUT}$ = 0.5 A | 5.1 | 5.2 | 8 | |
| **AC characteristics** | | | | | | |
| $V_{ACIN}$ | AC peak-to-peak voltage between AC1 and AC2 input pins | | | | 24 | V |
| $I_{AC,MAX}$ | AC1 and AC2 pins maximum RMS current capability | Sinusoidal waveform at AC1-AC2 terminals | | | 2 | A |
| $f_{AC}$ | AC synchronous rectifier input frequency range | | 50 | | 500 | kHz |

# 5 Device description

## 5.1 Chip reset pin

The RSTB pin, active low, can block the operation of the device by forcing the digital core in reset state. After releasing the RSTB pin, the STWLC68 re-starts and retrieves the default configuration data from the OTP. If not used, the RSTB pin should be connected to the V1V8 or to the V1V8 rail.

## 5.2 Synchronous rectifier

The synchronous rectifier of the STWLC68 is a key block in charge of converting the AC input power from the receiving coil into a DC supply rail for the following linear regulator. In principle it consists of four N-channel MOSFETs arranged in a H-bridge, conveniently driven by a control block that monitors the voltage at the AC1 and AC2 pins to optimize the commutations and to charge the external bootstrap capacitors for the high-side switches. Different driving schemes are possible for the switches of the rectifier and the MCU core dynamically selects the optimal one to maximize the overall efficiency as a function of the operating point. When designing the filtering capacitor at the output of the synchronous rectifier, it must be taken into account that it has to minimize the AC residual ripple and to provide energy storage to sustain load transients, without impacting on the ASK communication with the transmitter.

## 5.3 Main linear regulator

The main linear regulator of the STWLC68 ensures a constant output voltage with minimum power loss. Excellent line and load regulation are demanded to the analog circuitry of this block, while the optimal operating point is managed by the MCU core. The minimization of the power loss is achieved by adjusting the drop-out voltage according to a programmed target curve: to do so, the MCU core handles the communication with the transmitter to get the desired VRECT rail voltage. Key voltages and currents in the block are constantly monitored to optimize the performance of the linear regulator and to to provide multiple proctection levels (see related section).

The main linear regulator has three independent control loops acting on the power pass element:

- Output voltage regulation loop: this loop regulates the output voltage at the nominal value set in the dedicated register;
- Input current regulation loop: in order to prevent a collapse at the output of the synchronous rectifier, the current through the linear regulator is limited to a fixed 1.5 A limit. This loop overdrives the previous one, reducing the output voltage as a consequence.
- Input voltage regulation loop: this loop works in conjunction with the input current one and avoids that the VRECT rail drops below a programmable value.

Both input current and input voltage regulation loops play an important role: since the output of the rectifier is a highly variable voltage source (especially because of unpredictable changes in coupling of the coils), extra care is needed to avoid voltage drops that could lead to an undesirable MCU core reset. The pass transistor is an N-channel MOSFET and the BOOT pin is dedicated to its bootstrap capacitor, ensuring correct driving and lower on-resistance also in case of drop-out condition. A filtering capacitance higher than 20 µF has to be connected to the output rail (VOUT) in order to ensure stable operation of the linear regulator.

## 5.4 ASK communication

Robust and reliable in-band ASK modulation is critical to the operation of any Qi compliant devices. STWLC68 has dedicated hardware on top of the firmware algorithm to improve the performance of the in-band communication. Parameters controlling the ASK modulation used during communication (e.g. modulation index as a function of the load) are programmable via OTP. At ping-up and in light-load or no-load conditions the modulation index may result critical, especially in case of poor magnetic coupling of the coils: an internal, programmable dummy load at VRECT can be enabled to enhance the ASK modulation, resulting is a quicker transaction with the transmitter. The dummy current is automatically drawn from VRECT at power-up and it is gradually reduced as the output current increases: this operation ensures a constant load baseline that exits the game once the external load prevails.

## 5.5 Protections

**Over-voltage protection**

The STWLC68 integrates different Over-Voltage Protection circuits to protect itself, the load connected to its output rail and the external components from damage due to overheating and/or exceeding AMR condition. Under normal operating conditions the voltage at the output of the synchronous rectifier is slightly higher than the output one thanks to the communication with the transmitter. A sudden change in the coupling factor between transmitting and receiving coils, for example due to abrupt reciprocal repositioning of the coils, easily leads to unpredicatable voltage peaks at the AC input terminals: the TX-RX regulation loop is not fast enough to prevent such an event and additional precautions must be taken.

Both the VRECT and VOUT outputs are constantly monitored. The VRECT rail has three concurrent OVP mechanism: two fixed, analog ones based on a HW comparator (OVPH and Fixed-OVPS) and a digital ones (Adj-OVPS), implemented in the FW and relying on the ADC readings (OVPS). In case the $V_{VRECT} > V_{VRECT,OVPH}$ condition occurs, the protection circuit immediately shorts both AC1 and AC2 pins to ground. This clamping action is released as soon as the voltage at the V5V0 pin falls down below its power-good level (4V typ.). Normally (it actually depends on the output load) the transmitter reacts to this protection by cutting-off the power transfer.

Both OVPS (Fixed and Adjustable) protections activate a different mechanism compared to OVPH: the IEXT pin goes low and an external resistor starts drawing current from VRECT (see block diagram). The digital OVP protection (Adj-OVPS) has an adjustable threshold and can be taylored for the application. In most of cases both soft OVP protections do not interrupt the ongoing power transfer, but a significant energy could be dissipated in the external resistor and a careful design is required. Optionally, the STWLC68 can be programmed to issue an End-of-Power-Transfer (EPT) packet to the transmitter on any OVP event.

**Over-temperature protection**

The STWLC68 is equipped with three over-temperature detection circuits based on different sources:

1) Synchronous rectifier temperature sensor

2) Main linear regulator temperature sensor

3) Coil (external NTC) temperature sensor

The signals coming from the two internal temperature sensors and the NTC pin (analog input) are conditioned and routed to the multi-channel ADC. The temperature of both the rectifier and the linear regulator can be directly read via dedicated registers. The external sensor, typically placed very close to the coil to prevent over-heating, is often a low-sided NTC of a resistor divider whose center tap is connected to the NTC pin, while the high-side resistor is connected to the V1V8 pin.

Reading the temperature of the external sensor requires some calculation from the host, since it depends on the NTC characterisitcs (beta, nominal value), the high-side resistor and the input range of the NTC pin (0 V - 1.5 V).

The internal sensors are also monitored and compared to a fixed 125°C threshold (10°C hysteresis) to trigger a HOVP event (AC1 and AC2 shorted to ground).

In addition, the STWLC68 allows the user to define for each source a threshold with associated set of actions.

The selectable actions are any combination of:

- EPT packet generation
- Output disconnection
- INT pin status change

For example, a chip over-temperature alert could be sent to the host system by setting two temperature thresholds (e.g. 100°C for the rectifier and 90°C for the linear regulator) and linking the INT pin to the related interrupts.

**Over-current protection**

As mentioned in the description of the main linear regulator, the current through the pass transitor is sensed and limited to a fixed 1.5 A threshold. An internal interrupt is generated in such a case and specific actions could be linked to it. In any case, a severe over-load condition quikly leads to an output voltage drop: if VOUT drops below a fixed 1.25 V threshold (e.g. in case of output short-circuit), the linear regulator is disabled an an interrupt is generated. A programmable threshold allows the user to define an early over-load alert interrupt and a set of associated actions.

## 5.6 GPIOx and INTB pins

The GPIO0 through GPIO5 pins are programmable general-purpose I/O pins whose functions can be assigned in OTP memory. These pins can be configured both as inputs and outputs (either push-pull or open-drain) according to the selected function.

The INTB pin is an interrupt output line that can be associated to any internal interrupt condition and used to inform the host system about specific events. The INTB pin can be programmed to be push-pull or open-drain type as well.

The following table reports the available functions that can be assigned by writing the corresponding GPIOx-FS register.

**Table 5. List of selectable functions for GPIOx pins**

| GPIO function and type | | GPIOx-FS register | Description |
|---|---|---|---|
| GPIOF_NONE | I | 0x00 | No function |
| GPIOF_XINT_OD | O | 0x03 | Interrupt signal status (inverted), open-drain |
| GPIOF_XINT_PP | O | 0x04 | Interrupt signal status (inverted), push-pull |
| GPIOF_OUT_INH | I | 0x05 | Output voltage inhibit control (input):<br>low = enable VOUT, high = inhibit VOUT |
| GPIOF_OUT_MON | O | 0x06 | Output status monitor<br>low = VOUT disabled, high = VOUT enabled |
| GPIOF_OUT_XMON | O | 0x07 | Output status monitor (inverted)<br>low = VOUT enabled, high = VOUT disabled |
| GPIOF_OUT_XMON_OD | O | 0x08 | Output status monitor (inverted, open-drain)<br>low = VOUT enabled, high = VOUT disabled |
| GPIOF_ADC_TICK | O | 0x0F | ADC sampling toggling ticker (debug) |
| GPIOF_CORE_XRDY | O | 0x1D | Digital core ready (inverted). If low, core and I2C interface are ready. |

*Note: the INTB pin is also used as auxiliary control signal by the Graphical User Interface (GUI) during OTP flashing. This signal must be conveniently routed to the programming connector in the application (see evaluation boards as a reference)*

## 5.7 Wireless power interface

The blocks that refer to the wireless power interface are the synchronous rectifier, the main LDO linear regulator and the ASK modulator, as well as the digital core as supervisor. As previously mentioned, the power transfer from the transmitter to the receiver is actually the result of a procedure that involves different phases.

In brief, a power transfer begins after the transmitter has properly detected a valid receiver and a specific communication has been established between the two parts. Without entering the details of the different phases, the basic sequence of events taking place when a receiver is properly placed on the transmitting coil are summarized as:

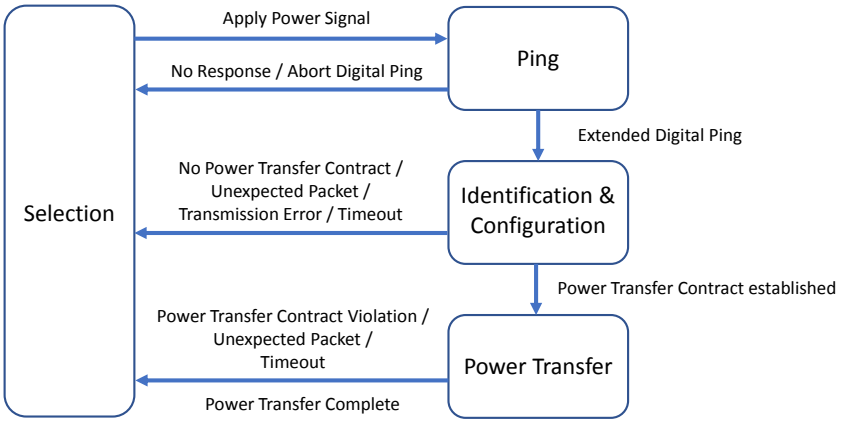
- Analog ping: this is the initial step of the so-called “selection phase”. A brief AC burst is periodically generated by the transmitter in order to detect the presence of a potential receiver on its transmitting surface. Through analog ping the transmitter could eventually be able to discriminate foreign objects.
- Digital ping: this step is an interrogation session based on a more energetic AC burst during which the potential receiver is expected to reply through amplitude shift-keying (ASK) modulation.
- Identification & configuration: this is the following step aiming to identify the receiver and to gather information about its power transfer capability. The transmitter generates a so-called “Power Transfer Contract” tailoring some parameters that will characterize the following power transfer phase.

- Power transfer: this is the final step, where the transmitter initially increases and subsequently modulates the transmitted power in response to the control (feedback) data from the receiver.

**Power Receiver Interface**

The flow-chart visible in Figure 3 reports the whole process leading to a power transfer in Base Power Profile (BPP), the only power profile supported by STWLC68 due to a maximum output power of 5 W (1.0 A @ 5 V).

**Figure 3. Power transfer phases for Baseline Power Profile**




In case of Qi-mode the STWLC68 goes autonomously through Selection, Ping, Identification & Configuration phases, entering Power Transfer phase if no error occurs. During the Power Transfer phase, the device sends Received-Power and Control-Error packets periodically as feedback information for the transmitter. If a critical event like over-voltage, over-current or over-temperature occurs, the STWLC68 automatically sends the End-Power-Transfer packet.

When the Power Transfer is up and running, the End-Power-Transfer packet (with any response value) or any custom packet (e.g. Proprietary packet or Charge-Status packet) can be sent to the transmitter simply through commands via $I^2C$ interface. Sending a custom packet may result in a reply (either a data packet or a pattern response from the transmitter) or no reply at all: if a response is received, the content is captured and stored in specific $I^2C$ registers.

Important notes:

- Changing the output voltage must respect the overall system design (selected coil, transmitter type, etc.).
- Output load transient response strongly depends on correct design of the output capacitors. Severe load transients may lead to temporary output voltage collapse due to the overall TX-RX response time.
- A minimum output load significantly helps in increasing the signal-to-noise ratio during digital pin and it is advisable to ensure interoperability with all transmitters. For this purpose, the STWLC68 allows the user to set a dummy load (reservoir current) that is dynamically managed to fade-out when an output load is applied.
- The initial load at power-up should not exceed 2.5 W, smoothly ramping-up to full power subsequently.

## 5.8 I2C interface

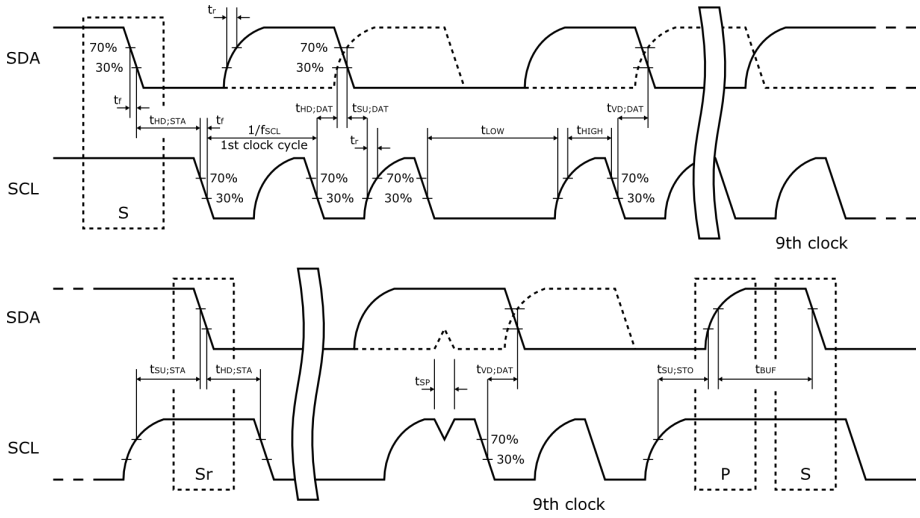
The STWLC68 can operate fully independently, i.e. without being interfaced with any host controller. In applications in which the STWLC68 has to be part of the peripherals managed by the host system, the two SDA and SCL pins could be connected to the existing I²C bus.

Thedevice works as an I²C slave and supports both standard (100 kbit/s) and fast (400 kbit/s) data transfer modes.

Through the I²C interface, maximum device flexibility is obtained and full access to the internal resources is possible. The host controller typically polls for device status and power transfer operation, demands for custom commands execution or reconfigures the default parameters.

The STWLC68 has been assigned 0x61 as 7-bit hardware address, resulting in 0xC2 and 0xC3 8-bit addresses for write and read operations respectively. Since both SDA and SCL pins of the STWLC68 have an open-drain output stage, the high level is determined by external pull-up resistors at system level. The pins are tolerant up to 5 V and the pull-up resistors should be selected as a trade-off between communication speed (lower resistors lead to faster edges) and data integrity (the input logic levels have to be guaranteed to preserve communication reliability).

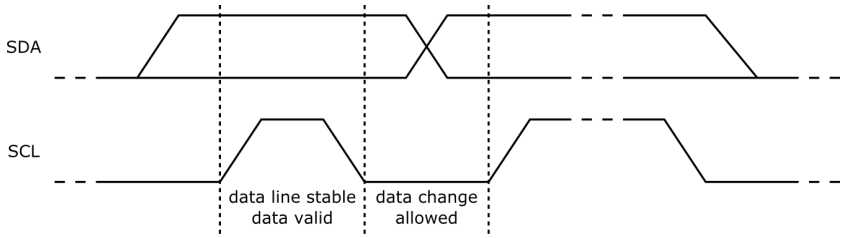
**Figure 4. I²C timing reference**




### Data Validity

As shown in Figure 5, the data on the SDA line must be stable during the high period of the clock. The high and low states of the SDA line can only change when the SCL clock signal is low.

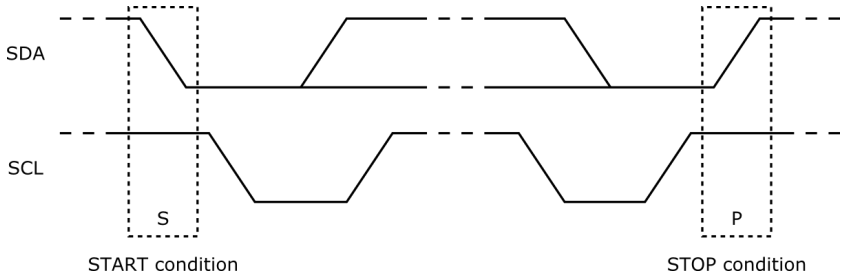
**Figure 5. Data validity on the I²C bus**




### Start and Stop Conditions

Both SDA and SCL lines remain high when the I²C bus is not busy. As shown in Figure 6, a start condition is a high-to-low transition of the SDA line when SCL is high, while the stop condition is a low-to-high transition of the SDA line when SCL is high. A STOP condition must be sent before each START condition.

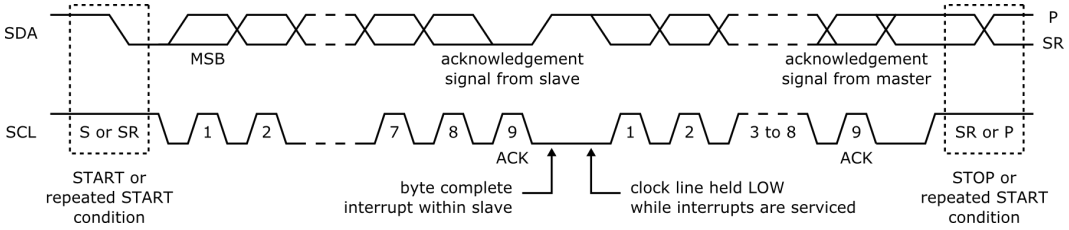
Figure 6. **Start and Stop Condition on the I²C Bus**




### Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte sent to the STWLC68 is generally followed by an acknowledge (ACK) bit. The MSB is transferred first. One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high state of each SCL clock pulse.

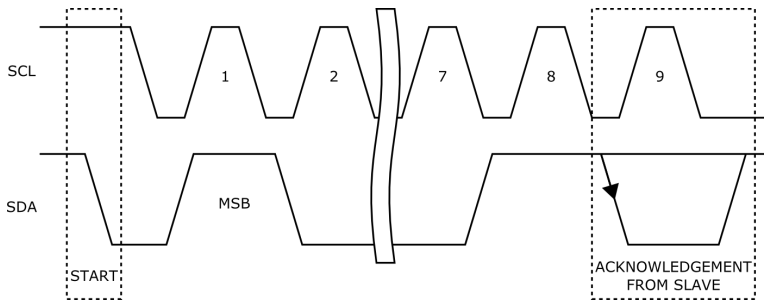
Figure 7. **Byte transfer**




### Acknowledge

The I²C master releases the SDA line during the 9th SCL clock pulse in order to detect the ACK pulse eventually generated by the slave (Figure 8). The STWLC68 generates the ACK pulse (by pulling-down the SDA line during the acknowledge clock pulse) to confirm the correct device address or the received data bytes: the missing ACK pulse is a so-called not-acknowledge condition (NACK) and, apart specific cases, the master aborts the ongoing operation in such an event. If the supply voltage of the STWLC68 is too low, the I²C interface is disabled and no ACK pulses are genarated (see Under-Voltage Lockout thresholds in the Electrical Characteristics).

Figure 8. **Acknowledge on the I²C bus**




### Interface protocol

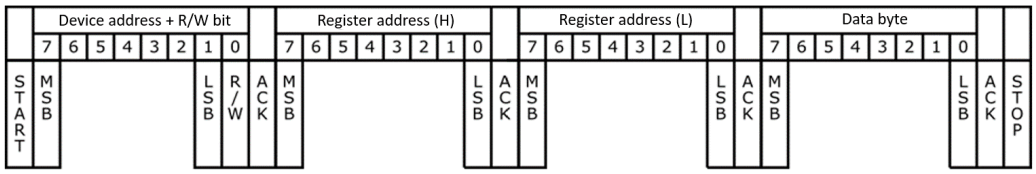
The interface protocol consists of (see Figure 9):

- start condition (START)
- 7-bit device address (0x61) + R/W bit (read =1 / write =0)
- Register pointer, high-byte
- Register pointer, low-byte
- Data sequence: N x (data byte + ACK)

- Stop condition (STOP)

The register pointer (or address) byte defines the destination register to which the read or write operation applies. When the read or write operation is finished, the register pointer is automatically incremented.

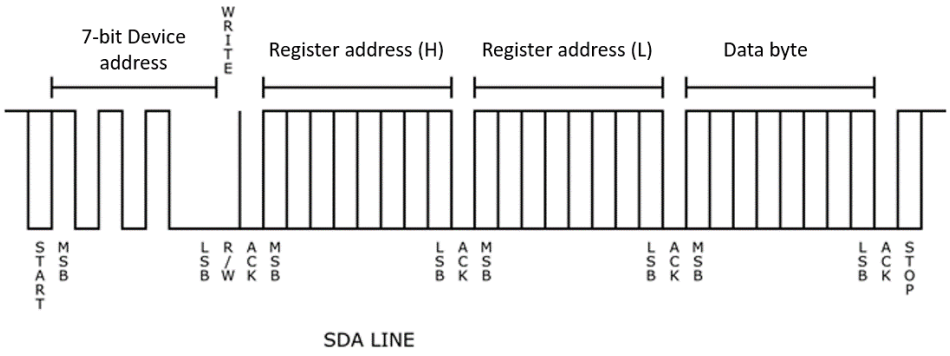
**Figure 9. Interface protocol**




### Writing to a single register

Writing to a single register begins with a START condition followed by device address 0xC2 (7-bit device address plus R/W bit cleared), two bytes of the register pointer and data byte to be written in the destination register. Each transmitted byte is acknowledged by the STWLC68 through an ACK pulse (Figure 10)

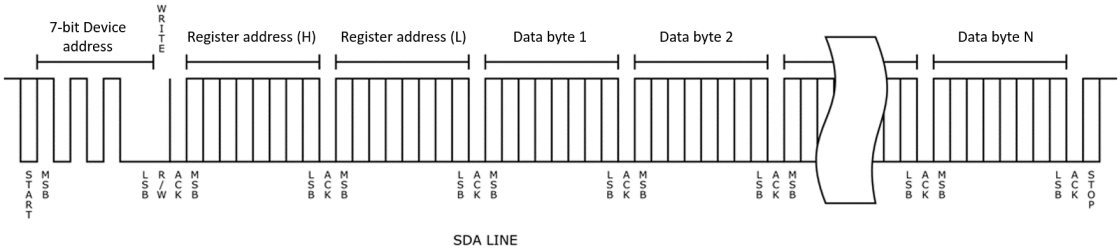
**Figure 10. Writing to a single register**




### Writing to multiple registers (page write)

The STWLC68 supports writing to multiple registers with auto-incremental addressing. When data is written into a register, the register pointer is automatically incremented, therfore transferring data to a set of subsequent registers (also know as page write) is a straightforward operation.

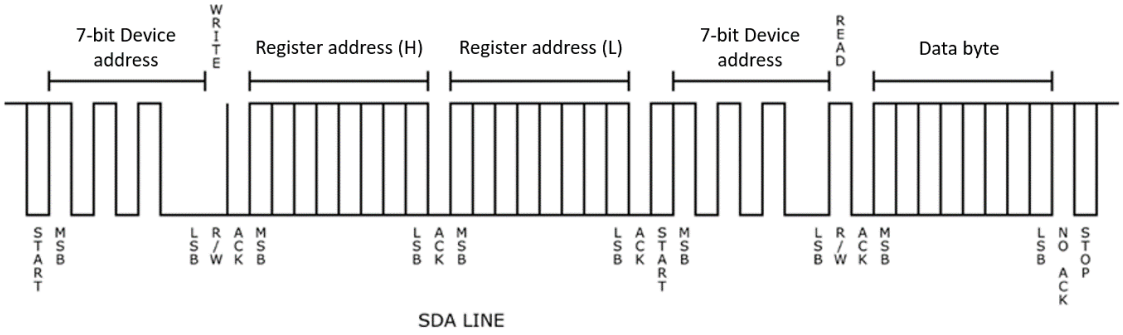
**Figure 11. Writing to multiple registers**



### Reading from a single register

Reading from a single register begins with a START condition followed by device address byte 0xC2 (7-bit device address plus R/W bit cleared) and two bytes of register pointer, then a re-START condition is generated and the device address 0xC3 (7-bit device address plus R/W bit asserted) is sent, followed by data reading. As shown in Figure 12, an ACK pulse is generated by the STWLC68 at the end of each byte, but not for data bytes retrieved from the register. A STOP condition is finally generated to terminate the operation.

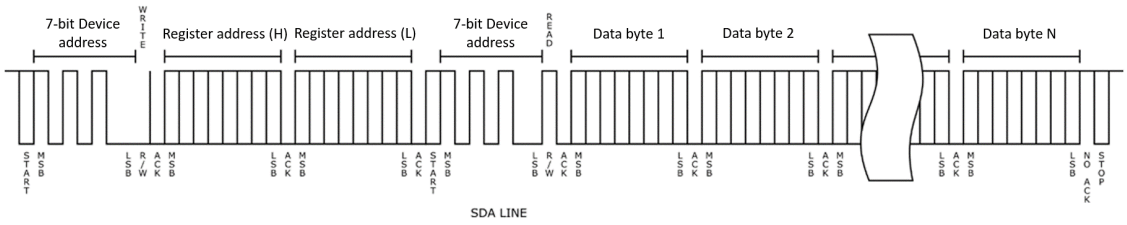
**Figure 12. Reading from a single register**




### Reading from multiple registers (page reading)

Similarly to multiple (page) writing, reading from subsequent registers relies on auto-increment of the register: the master can extend data reading to the following registers by generating and ACK pulse at the end of each byte. Data reading starts immediately and the stream is terminated by a NACK pulse at the end of the last data byte, followed by a STOP condition (Figure 13).

**Figure 13. Reading from multiple registers**




## 5.9 Register map

The STWLC68 can be monitored and controlled by accessing the internal registers via I2C interface. The following registers map reports the accessible addresses. Registers marked with † are read-only and should not be altered by the user. Addresses not shown in the map and blank bits have to be considered reserved and not altered as well.

**Table 6. Registers map**

| Register Address | Register name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0x0000 | CHIP_ID† | Chip ID | | | | | | | |
| 0x0001 | | | | | | | | | |
| 0x0002 | CHIP_REV† | Chip Revision | | | | | | | |
| 0x0006 | ROM_ID† | ROM ID | | | | | | | |

| Register Address | Register name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0x0007 | ROM_ID† | ROM ID | | | | | | | |
| 0x0008 | CFG_ID† | OTP memory configuration ID | | | | | | | |
| 0x0009 | | | | | | | | | |
| 0x000A | TRIM_ID† | Production trimming version ID | | | | | | | |
| 0x000B | | | | | | | | | |
| 0x000C | PATCH_ID† | OTP patch version ID | | | | | | | |
| 0x000D | | | | | | | | | |
| 0x0010 | INT_EN | Out_Off_Int_En | Out_On_Int_En | | | | OVP_Int_En | OCP_Int_En | OTP_Int_En |
| 0x0011 | | | | | | Vrect_Rdy_Int_En | Sig_Str_Int_En | | |
| 0x0012 | INT_CLR | Out_Off_Int_Clr | Out_On_Int_Clr | | | | OVP_Int_Clr | OCP_Int_Clr | OTP_Int_Clr |
| 0x0013 | | | | | | Vrect_Rdy_Int_Clr | Sig_Str_Int_Clr | | |
| 0x0014 | INT_LATCH† | Out_Off_Int_Latch | Out_On_Int_Latch | | | | OVP_Int_Latch | OCP_Int_Latch | OTP_Int_Latch |
| 0x0015 | | | | | | Vrect_Rdy_Int_Latch | Sig_Str_Int_Latch | | |
| 0x0016 | INT_STA† | Out_Off_Int_Flag | Out_On_Int_ Flag | | | | OVP_Int_ Flag | OCP_Int_ Flag | OTP_Int_ Flag |
| 0x0017 | | | | | | Vrect_Rdy_Int_ Flag | Sig_Str_Int_ Flag | | |
| 0x0018 | OTP_LATCH† | | | | | | NTC_OTP_Latch | Rect_OTP_Latch | Lin_Reg_OTP_Latch |
| 0x0019 | OVP_LATCH† | | | | | | | Fxd_OVPS_Latch | Adj_OVPS_Latch |
| 0x001A | OCP_LATCH† | | | | | | | | OCP_Latch |
| 0x001C | SYS_ERR0† | | | | | | ECC_Double_Bit_Err | Header_Section_Err | M0_Hard_Fault_Err |
| 0x001D | SYS_ERR1† | Chip_Info_Sector_Error [1:0] | | Patch_Sector_Error [1:0] | | Configuration_Sector_Error [1:0] | | Trimming_Sector_Error [1:0] | |
| 0x001E | SYS_ERR2† | | | | | | | OTP_Memory_Trimming_Sector_Error [1:0] | |
| 0x0020 | DIR_CMD | | | | | | Send_EPT | | Send_Msg |
| 0x0021 | | | | | | | | Out_Off | Out_On |
| 0x0038 | AC_FREQ† | Rectifier Operating Frequency (in kHz) | | | | | | | |
| 0x0039 | | | | | | | | | |
| 0x003A | S_STR_TX† | Signal Strength Level sent to transmitter | | | | | | | |
| 0x003C | VOUT_SET | Output Voltage setting: 25 mV to 22 V (25 mV/step) | | | | | | | |
| 0x003D | | | | | | | | | |
| 0x0040 | VTH_AOE | Voltage threshold for Automatic Output Enable: 240 mV to 1049 mV (16 mV/step) | | | | | | | |
| 0x0041 | LCR_THR | | | Normal-Current Range (NCR) to Low-Current Range (LCR) threshold (4 mA/step) | | | | | |

| Register Address | Register name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0x0042 | LCR_HYST | | | Low-Current Range (LCR) to Normal-Current Range (NCR) hysteresis (4 mA/step) | | | | | |
| 0x0043 | MOD_CFG | | | LCR_Clamp_Mod_En | LCR_Comm_Mod_En | | | NCR_Clamp_Mod_En | NCR_Comm_Mod_En |
| 0x0044 | IDMYL_SET | | | | Dummy Load current: 0 mA to 310 mA (10 mA/step) | | | | |
| 0x0045 | VRECT_MIN | Vrect_Min_Ctrl_En | | | Minimum VRECT voltage (3.5V to 11V, 0,5 V/step) for constant VOUT | | | | |
| 0x0049 | VDROP_V0 | Linear regulator target drop-out voltage, setpoint 0 | | | | | | | |
| 0x004A | VDROP_V1 | Linear regulator target drop-out voltage, setpoint 1 | | | | | | | |
| 0x004B | VDROP_V2 | Linear regulator target drop-out voltage, setpoint 2 | | | | | | | |
| 0x004C | VDROP_V3 | Linear regulator target drop-out voltage, setpoint 3 | | | | | | | |
| 0x004D | VDROP_C1 | Linear regulator target drop-out voltage, current threshold 1 | | | | | | | |
| 0x004E | VDROP_C2 | Linear regulator target drop-out voltage, current threshold 2 | | | | | | | |
| 0x004F | VDROP_C3 | Linear regulator target drop-out voltage, current threshold 3 | | | | | | | |
| 0x0050 | MSG_TX | Message packet content to be sent to transmitter via ASK modulation (see DIR_CMG register) | | | | | | | |
| 0x0051 | | | | | | | | | |
| 0x0052 | | | | | | | | | |
| 0x0053 | | | | | | | | | |
| 0x0054 | | | | | | | | | |
| 0x0055 | | | | | | | | | |
| 0x0056 | | | | | | | | | |
| 0x0057 | | | | | | | | | |
| 0x0058 | | | | | | | | | |
| 0x0062 | EPT_MSG | EPT Message (root cause event) added to EPT packet (see DIR_CMD register) | | | | | | | |
| 0x0080 | FOD_CTC | FOD Current Threshold Calibration | | | | | | | |
| 0x0083 | FOD_GSC | FOD Gain Scaler Calibration | | | | | | | |
| 0x0087 | FOD_OLC | FOD Offset Level Calibration | | | | | | | |
| 0x008B | FOD_DCR | Coil DC-Resistance for FOD calculation | | | | | | | |
| 0x0090 | VRECT_RE† | Voltage Regulation Error (difference in mV) between actual and target VRECT, used to calculate CEP for the transmitter | | | | | | | |
| 0x0091 | | | | | | | | | |
| 0x0092 | RPP_TX† | Received Power (comprehensive of losses) level Packet sent to transmitter | | | | | | | |
| 0x0093 | | | | | | | | | |
| 0x0096 | SS_MIN_TX | Minimum Signal-Strength level for proceeding to PING phase | | | | | | | |
| 0x0097 | CS_OFFS† | Current sensor offset adjustment (in mA) | | | | | | | |
| 0x0098 | IDLE_CC | Chip idle current consumption (in mA) | | | | | | | |
| 0x00A1 | PMAX_PTC | | | Maximum power capability established during Power Transfer Contract | | | | | |
| 0x00A6 | TRECT_OTP | Over-Temperature detection Threshold related to Rectifier Temperature sensor | | | | | | | |
| 0x00A7 | | | | | | | | | |
| 0x00A8 | TLR_OTP | Over-Temperature detection Threshold related to main Linear Regulator Temperature sensor | | | | | | | |
| 0x00A9 | | | | | | | | | |
| 0x00AA | VNTC_OTP | Over-Temperature detection Threshold related to external NTC pin | | | | | | | |

| Register Address | Register name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0x00AB | VNTC_OTP | Over-Temperature detection Threshold related to external NTC pin | | | | | | | |
| 0x00AC | VRECT_OVP | VRECT Over-Voltage detection Threshold (Adjustable OVP-Clamper) | | | | | | | |
| 0x00AD | | | | | | | | | |
| 0x00AE | IRECT_OCP | IRECT Over-Current detection Threshold | | | | | | | |
| 0x00AF | | | | | | | | | |
| 0x00C0 | PROT_EN | | | | | Tshdn_OTP_En | Vntc_OTP_En | Tlr_OTP_En | Trect_OTP_En |
| 0x00C1 | | | | | | | | Fxd_OVPS_En | Adj_OVPS_ En |
| 0x00C2 | | | | | | | | | Irect_OCP_ en |
| 0x00C4 | PROT_EPT | | | | | | Vntc_OTP_ EPT_Req | Tlr_OTP_E PT_Req | Trect_OTP _EPT_Req |
| 0x00C5 | | | | | | | | Fxd_OVPS _EPT_Req | Adj_OVPS _ EPT_Req |
| 0x00C6 | | | | | | | | | Irect_OCP_ EPT_Req |
| 0x00C8 | PROT_OD | | | | | | Vntc_OTP_ Out_Disc | Tlr_OTP_ Out_Disc | Trect_OTP _ Out_Disc |
| 0x00C9 | | | | | | | | | Vrect_OVP _ Out_Disc |
| 0x00CA | | | | | | | | | Irect_OCP_ Out_Disc |
| 0x00D3 | MFR_ID1 | Manufacturer ID (MSByte) | | | | | | | |
| 0x00D4 | MFR_ID0 | Manufacturer ID (LSByte) | | | | | | | |
| 0x00D5 | BDEV_ID3 | Xtd_ID_En | Basic Device ID (MSByte) | | | | | | |
| 0x00D6 | BDEV_ID2 | Basic Device ID | | | | | | | |
| 0x00D7 | BDEV_ID1 | Basic Device ID | | | | | | | |
| 0x00D8 | BDEV_ID0 | Basic Device ID (LSByte) | | | | | | | |
| 0x00D9 | XDEV_ID7 | Extended Device ID (MSByte) | | | | | | | |
| 0x00DA | XDEV_ID6 | Extended Device ID | | | | | | | |
| 0x00DB | XDEV_ID5 | Extended Device ID | | | | | | | |
| 0x00DC | XDEV_ID4 | Extended Device ID | | | | | | | |
| 0x00DD | XDEV_ID3 | Extended Device ID | | | | | | | |
| 0x00DE | XDEV_ID2 | Extended Device ID | | | | | | | |
| 0x00DF | XDEV_ID1 | Extended Device ID | | | | | | | |
| 0x00E0 | XDEV_ID0 | Extended Device ID (LSByte) | | | | | | | |
| 0x00F0 | GPIO0_FS | GPIO0 pin Function Selector | | | | | | | |
| 0x00F1 | GPIO1_FS | GPIO1 pin Function Selector | | | | | | | |
| 0x00F2 | GPIO2_FS | GPIO2 pin Function Selector | | | | | | | |
| 0x00F3 | GPIO3_FS | GPIO3 pin Function Selector | | | | | | | |
| 0x00F4 | GPIO4_FS | GPIO4 pin Function Selector | | | | | | | |
| 0x00F5 | GPIO5_FS | GPIO5 pin Function Selector | | | | | | | |

| Register Address | Register name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0x00F6 | GPIO6_FS | GPIO6 (INT pin) Function Selector | | | | | | | |
| 0x0150 | VRECT_ADC† | VRECT voltage ADC reading (in mV) | | | | | | | |
| 0x0151 | | | | | | | | | |
| 0x0152 | VOUT_ADC† | VOUT voltage ADC reading (in mV) | | | | | | | |
| 0x0153 | | | | | | | | | |
| 0x0154 | IRECT_ADC† | IRECT current ADC reading (in mA) | | | | | | | |
| 0x0155 | | | | | | | | | |
| 0x0158 | TRECT_ADC† | Rectifier Temperature sensor ADC reading (in °C) | | | | | | | |
| 0x0159 | | | | | | | | | |
| 0x015A | TLR_ADC† | Main Linear Regulator Temperature sensor ADC reading (in °C) | | | | | | | |
| 0x015B | | | | | | | | | |
| 0x015E | VNTC_ADC† | External NTC pin Voltage ADC reading (in mV) | | | | | | | |
| 0x015F | | | | | | | | | |

# 6 Application information

This chapter is aimed to provide some application hints. The reference schematic, the PCB layout guidelines, the minimum components to properly run the application and other aspects.

## 6.1 Reference schematic

Figure 14 shows the typical application schematic for the STWLC68. The values reported in Table 7 and Table 8 refer to typical Wireless Power Receiver applications capable of an output power of 2.5 W and 5W respectively.

**Figure 14. STWLC68 basic schematic diagram**

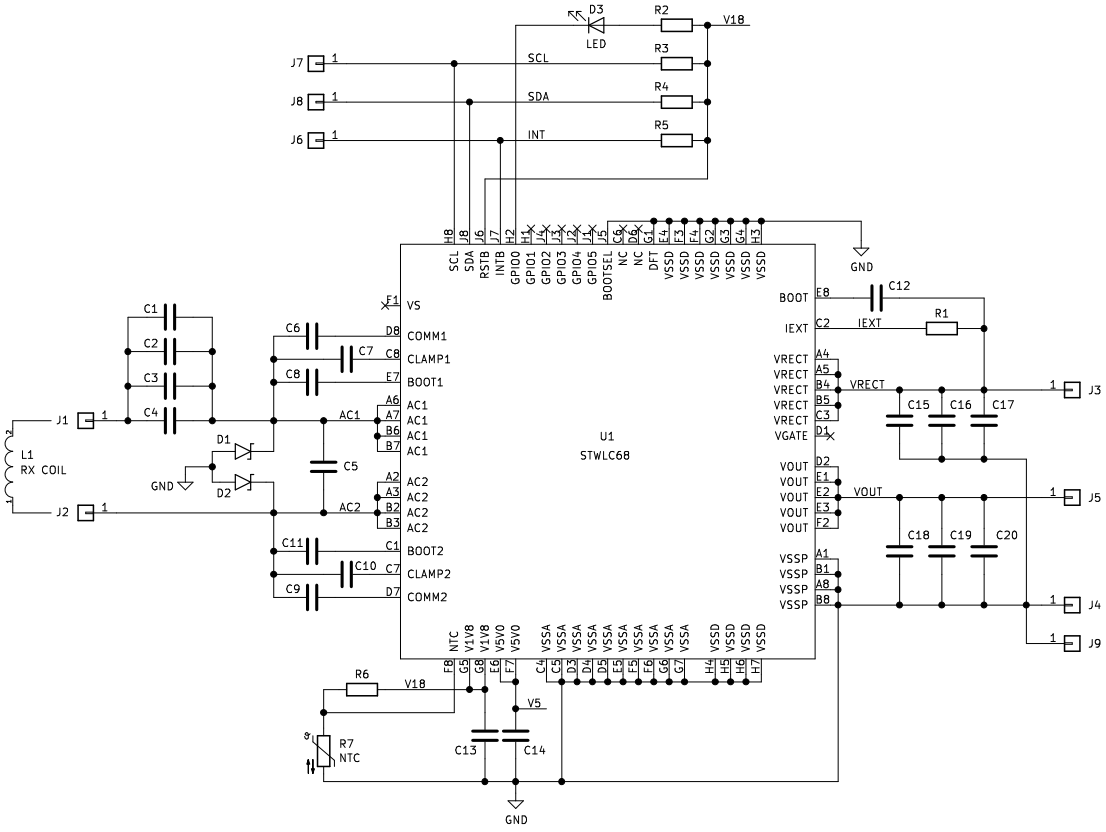



**Table 7. Typical components list for a 2.5 W application**

| Component | Value | Manufacturer | Part Number | Notes |
|---|---|---|---|---|
| L1 | 11.8 µH | Wurth | 760308101219 | Receiving coil (Ls) |
| C1, C2, C3 | 47nF/50V | Murata | GRM155R71H473KE14D | Series resonant capacitor (Cs) |
| C4 | 100nF/50V | Murata | GCM155R71H104KE02D | Series resonant capacitor (Cs) |
| C5 | 1.8nF/50V | Murata | GRM155R71H182JA01D | Detection capacitor (Cd) |
| C8, C11 | 47nF/50V | Murata | GRM155R71H473KE14D | Rectifier bootstrap capacitors |
| C12 | 4n7/50V | Murata | GCM155R71H472KA37D | Main LR bootstrap capacitor |
| C6, C9 | 22nF/50V | Murata | GRM155R71H223KA12D | ASK modulation capacitors |
| C7, C10 | 47nF/50V | Murata | GRM155R71H473KE14D | Auxiliary ASK modulation capacitors |

| Component | Value | Manufacturer | Part Number | Notes |
|---|---|---|---|---|
| C13, C14 | 2.2µF/25V | Murata | GRM155R61E225KE11D | V1V8 and V5V0 filtering capacitors |
| C15, C16, C17 | 10µF/25V | Murata | GRM188R61E106MA73D | VRECT filtering capacitor |
| C18, C19, C20 | 10µF/25V | Murata | GRM188R61E106MA73D | OUT filtering capacitor |
| D1, D2 | 12V TVS | NXP | PESD12VS1UL | ESD protection diodes |
| D3 | | Rohm | SML-P12VTT86R | Red LED (output on) |
| R1 | 100R | TE Connectivity | CRGP0603F100R | OVP clamping resistor (RCL) |
| R2 | 470R | | | |
| R3, R4, R5 | 47k | | | INT and I2C bus lines pull-up resistors |
| R6 | 5k1 1% | | | NTC pin high-side resistor |
| R7 | 10k 3% | Murata | NCU18XH103E60RB | NTC resistor (coil temperature sensor) |

**Table 8. Typical components list for a 5 W application**

| Component | Value | Manufacturer | Part Number | Notes |
|---|---|---|---|---|
| L1 | 8 µH | Wurth | 760308102207 | Receiving coil (Ls) |
| C1, C2, C3, C4 | 100nF/50V | Murata | GCM155R71H104KE02D | Series resonant capacitor (Cs) |
| C5 | 3.9nF/50V | Murata | GRM155R71H392KA01D | Detection capacitor (Cd) |
| C8, C11 | 47nF/50V | Murata | GRM155R71H473KE14D | Rectifier bootstrap capacitors |
| C12 | 4n7/50V | Murata | GCM155R71H472KA37D | Main LR bootstrap capacitor |
| C6, C9 | 22nF/50V | Murata | GRM155R71H223KA12D | ASK modulation capacitors |
| C7, C10 | 22nF/50V | Murata | GRM155R71H223KA12D | Auxiliary ASK modulation capacitors |
| C13, C14 | 2.2µF/25V | Murata | GRM155R61E225KE11D | V1V8 and V5V0 filtering capacitors |
| C15, C16, C17 | 10µF/25V | Murata | GRM188R61E106MA73D | VRECT filtering capacitor |
| C18, C19, C20 | 10µF/25V | Murata | GRM188R61E106MA73D | OUT filtering capacitor |
| D1, D2 | 16V TVS | Littelfuse | SMAJ16A | ESD protection diodes |
| D3 | | Rohm | SML-P12VTT86R | Red LED (output on) |
| R1 | 100R | TE Connectivity | CRGP0603F100R | OVP clamping resistor (RCL) |
| R2 | 470R | | | |
| R3, R4, R5 | 47k | | | INT and I2C bus lines pull-up resistors |
| R6 | 5k1 1% | | | NTC pin high-side resistor |
| R7 | 10k 3% | Murata | NCU18XH103E60RB | NTC resistor (coil temperature sensor) |

*Note: All the above components refer to a typical application. Operation of the device in the application may be limited by the choice of these external components (voltage ratings, current and power dissipation capability, etc.).*

The basic application schematic is relatively simple, since STWLC68 does not require many external parts to operate. Anyway, there are different aspects that must be carefully considered to properly design a customized application. In most of cases the main constrains are the limited PCB size/room and tickness, that unavoidably lead to crowded solutions with far-from-optimal electrical and thermal performance.

## 6.2 External components selection

### RX series resonant circuit components

The design of the receiving series resonant circuit, namely the receiving coil (Ls), the resonant capacitor (Cs) and the detection capacitor (Cd), is out of the scope of this document. In principle the resonant capacitor and the detection capacitor are easily calculated via simple equations involving standardized (Section 6.4 [1],[2]) or customized resonance frequencies. The receiving coil is certainly the bulkiest and most critical component and it will be assumed mechanically and electrically defined for the target application. A coil showing a high quality factor is synonym of good power transfer performance.

Being essential part of the series resonant circuit, both Cs and Cd should show excellent quality factor, relatively high RMS current capability and superior capacitance stability in the frequency range of interest. Thanks to their inner structure, Multi-Layer Ceramic capacitors (MLCCs) are inherently good devices in terms of RMS current capability and quality factor. Capacitance tolerance and stability strongly depend on the dielectric type: NP0, that shows good characteristics, is unfortunately not suitable for compact applications, since typical values in the order of hundreds of nano-Farads are not available in small packages.

Therefore, other dielectric types (like X5R, X7R and similar), are used to achieve higher capacitance per volume at the cost of lower accuracy and undesired dependencies (e.g. DC-biasing, temperature, etc.). In practice, the most critical Cs usually consists of few smaller, low-profile and X5R/X7R dielectric-type capacitors in parallel. The parallel connection also helps in increasing the RMS current capability and in mitigating the effect of capacitance tolerance due to production spread. The voltage rating for these capacitors is usually maximized to take into account the voltage developed in proximity of resonance: 50V-rated capacitors are generally a good choice.

### ASK modulation capacitors

The capacitors at the COMM1/COMM2 pins are connected to the AC1-AC2 terminals through controlled switches (ASK modulator): the de-tuning effect of closing these switches results in an amplitude modulation detected by the transmitter and also visible at the rectified voltage. Positive or negative modulation may occur, depending on the operating frequency and other factors. The ASK modulation index clearly depends on the capacitance value of these capacitors, whose value has to be adjusted in case of heavy negative modulation at VRECT (that is generally undesirable). The same considerations made above for the resonant capacitors is also applicable here, where capacitance tolerance is less critical: X5R dielectric-type are a good choice and an initial value of 47 nF is typically doing the job. CLAMP1 and CLAMP2 pins are basically a replica of COMM1 and COMM2: their function is providing a deeper ASK modulation under particular operating conditions and their activity can be controlled runtime.

### VRECT over-voltage clamping resistor

The voltage at the VRECT pin is primarily dictated by the transmitter, whose operating point is linked to the feedback information received via ASK modulation. Unexpected conditions, however, may increase the VRECT voltage to dangerous values (proximity to AMR levels). A sudden change in relative alignment between the transmitting and receiving coils, for example, could result in a dramatic change in coupling factor and, in turn, in a fast-rising voltage. Since the reaction of the transmitter is relatively slow, the STWLC68 protects itself by closing the switch internally connected to the IEXT pin. This switch is externally connected to VRECT via a resistor ($R_{CL}$) to implement an active clamper. The value of $R_{CL}$ is selected so that most of the power dissipation takes place in it during the clamping action, rather than inside the chip. Special resistors (surge resistors) capable of withstanding higher energy pulses are recommended.

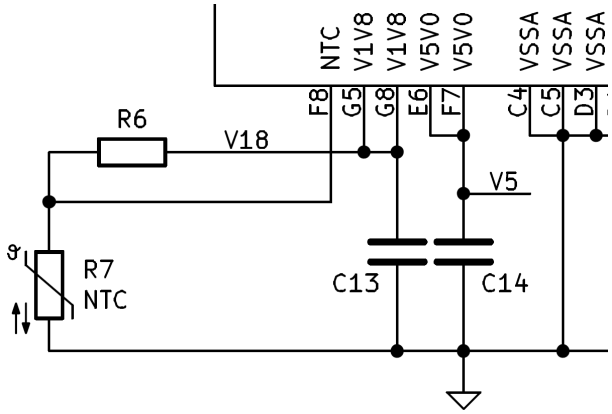
### ESD protection diodes

Since the receiving coil is an easy entry point for ESD (relatively large area with remarkable capacitive coupling), a good application design should consider protections for the most exposed pins: AC1 and AC2. Uni-directional Transient Voltage Suppression (TVS) diodes at both pins is the right choice. ESDs have essentially a common-mode nature and, although the receiving coil has low DC-resistance, its AC impedance may appear quite high to fast voltage spikes: independent clamping at AC1 and AC2 pins is thus madatory. The knee-voltage of the TVS diodes should be selected considering the maximum VRECT voltage plus some margin to avoid non-negligible leakage current at higher temperature, while their energy dissipation capability should be maximized considering the size of the package.

### Coil thermal protection

Maximizing the power transfer is often desirable, but not always possible in all operating conditions: applications in which the wireless power receiver has poor power dissipation capability and/or the power loss in the receiving coil is relevant (e.g. very tiny and slim coils with relatively high DC-resistance) may require some thermal protection. This feature is easily implemented with STWLC68 thanks to its NTC pin. A channel of the internal ADC is routed to the NTC pin, allowing the user to read the voltage across an external NTC thermistor.

**Figure 15. External NTC thermistor connection**




Defining a protection threshold is clearly possible by setting the internal registers of STWLC68. The voltage at the NTC pin is sampled, converted and compared to the threshold every millisecond: if an over-temperature occurs and the corresponding interrupt is enabled, the INT pin goes low. Additionally, one of the following actions (or both) may take place according to the selected option.

1. Main LDO linear regulator output disconnection;
2. End-of-Power-Transfer packet transmission

The value of the NTC thermistor and the high-side resistor (R6 in Figure 15) are not critical. An example for R6 and R7 is shown in Table 7: with these parts the 0.6 V threshold at the NTC pin is crossed at about 65°C.

## 6.3 PCB routing guidelines

1. Auxiliary 1V8 and 5V0 LDO filtering capacitors should be placed as close as possible to the STWLC68. Connection traces should be short and placed in top layer. Capacitors ground can be connected directly into GND plane.
2. $C_{RECT}$ and $C_{OUT}$ capacitors should be placed close to STWLC68 with higher priority than $R_{CL}$ resistor
3. Power traces (AC1, AC2, VRECT, VOUT) should be kept wide enough to sustain high current. Duplicating these traces in inner layers is advisable wherever possible.
4. AC1 and AC2 tracks should be routed closely to minimize the area of the resulting loop antenna.
5. Thermal performance and grounding should be always optimized by preserving bottom layer (usually assigned to ground) integrity.

## 6.4 References

1. The Qi Wireless Power Transfer System; Power Class 0 Specification; Version 1.2.2
2. PMA Inductive Wireless Power Transfer Receiver Specification - System Release 1

# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 7.1 WLCSP72 package information

**Figure 16. WLCSP72 3.265x3.674x0.6 0.4 Pitch 0.25 Ball package outline**

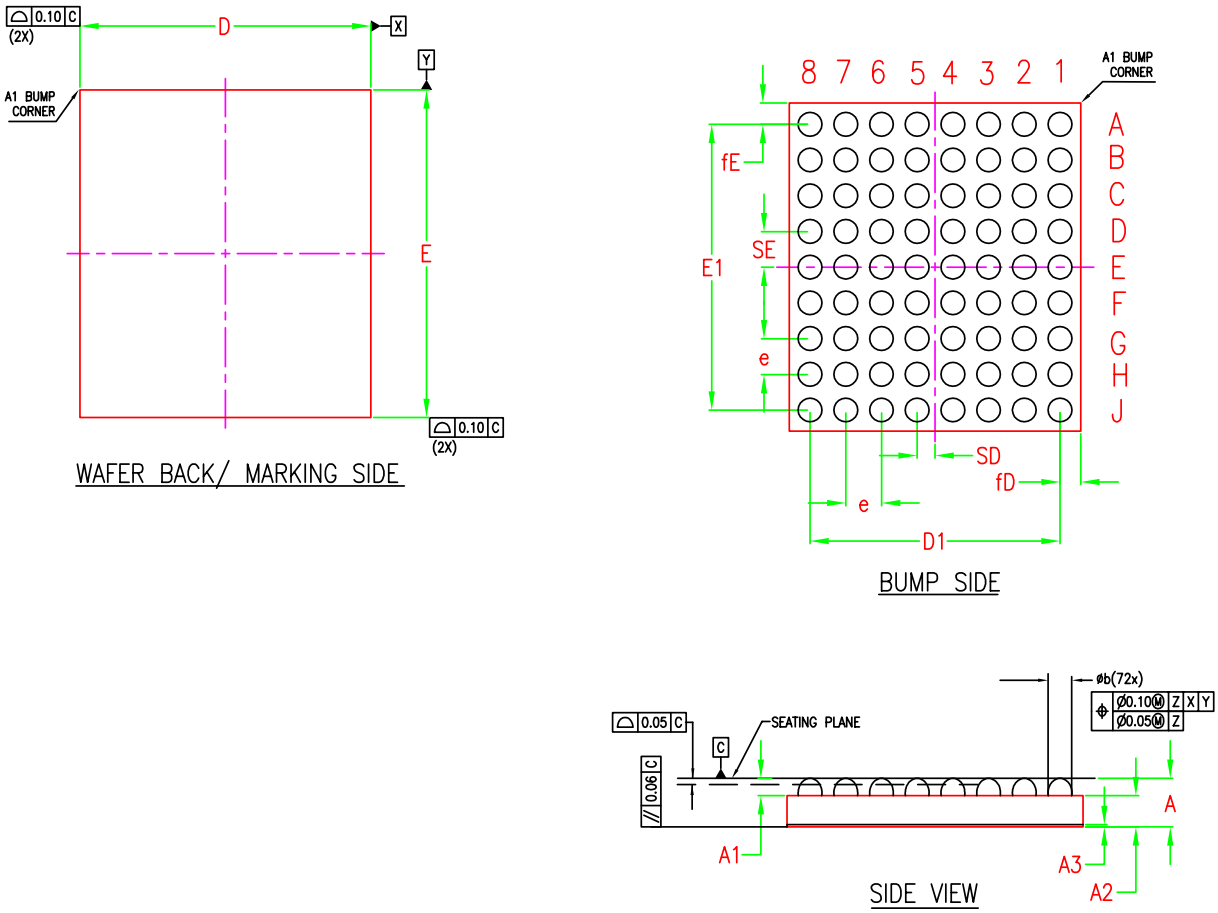
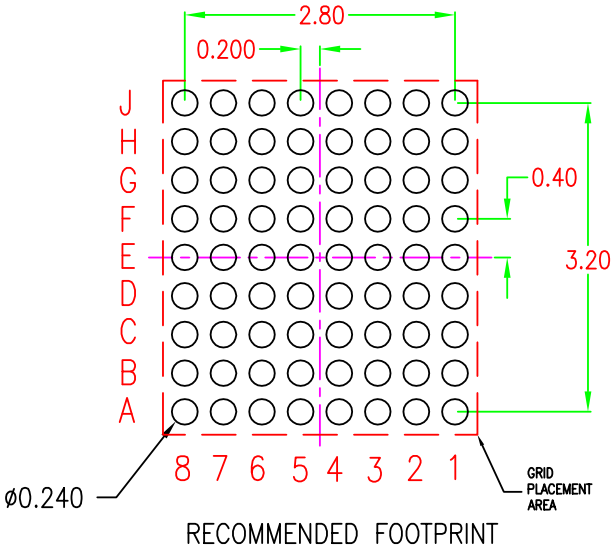


Table 9. **WLCSP72 3.265x3.674x0.6 0.4 Pitch 0.25 Ball mechanical data**

| Ref | Data range (mm) | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | 0.522 | 0.548 | 0.574 |
| A1 | 0.182 | 0.198 | 0.214 |
| A2 | 0.305 | 0.325 | 0.345 |
| A3 | 0.022 | 0.025 | 0.028 |
| b | 0.245 | 0.270 | 0.295 |
| D | 3.245 | 3.265 | 3.285 |
| D1 | | 2.80 | |
| E | 3.654 | 3.674 | 3.694 |
| E1 | | 3.20 | |
| e | | 0.400 | |
| SE | | 0.400 | |
| SD | | 0.200 | |
| fD | | 0.247 | |
| fE | | 0.252 | |
| ccc | | 0.06 | |

Figure 17. **Recommended footprint**



# Revision history

Table 10. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 22-Jan-2020 | 1 | Initial release. |
| 21-Apr-2020 | 2 | Updated: Table 1. Pin description, Section 5.1 Chip reset pin, Section 5.4 ASK communication added note in Section 5.6 GPIOx and INTB pins |

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