LMH6622 Dual Wideband, Low Noise, 160 MHz, Operational Amplifiers

1 Features

- V_S = ±6 V, T_A = 25°C, Typical Values Unless Specified
- Bandwidth (A_V = +2) 160 MHz
- Supply Voltage Range ±2.5 V to ±6 V; + 5 V to +12
- Slew Rate 85V/µs
- Supply Current 4.3 mA/amp
- Input Common Mode Voltage −4.75 V to +5.7 V
- Output Voltage Swing (R_L = 100 Ω) ±4.6 V
- Input Voltage Noise 1.6 nV/√Hz
- Input Current Noise 1.5 pA/√Hz
- Linear Output Current 90 mA
- Excellent Harmonic Distortion 90 dBc

2 Applications

- xDSL Receiver
- Low Noise Instrumentation Front End
- Ultrasound Preamp
- Active Filters
- Cellphone Basestation

3 Description

The LMH6622 is a dual high speed voltage feedback operational amplifier specifically optimized for low noise. A voltage noise specification of 1.6nV/√Hz, a current noise specification 1.5pA/√Hz, a bandwidth of 160 MHz, and a harmonic distortion specification that exceeds 90 dBc combine to make the LMH6622 an ideal choice for the receive channel amplifier in ADSL, VDSL, or other xDSL designs. The LMH6622 operates from ±2.5 V to ±6 V in dual supply mode and from +5 V to +12 V in single supply configuration. The LMH6622 is stable for $A_V \geq 2$ or $A_V \leq -1$. The fabrication of the LMH6622 on TI's advanced VIP10 process enables excellent (160 MHz) bandwidth at a current consumption of only 4.3 mA/amplifier. Packages for this dual amplifier are the 8-lead SOIC and the 8-lead VSSOP.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH6622	SOIC (8)	4.90 mm × 3.91 mm
LMH6622	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

XDSL Analog Front End

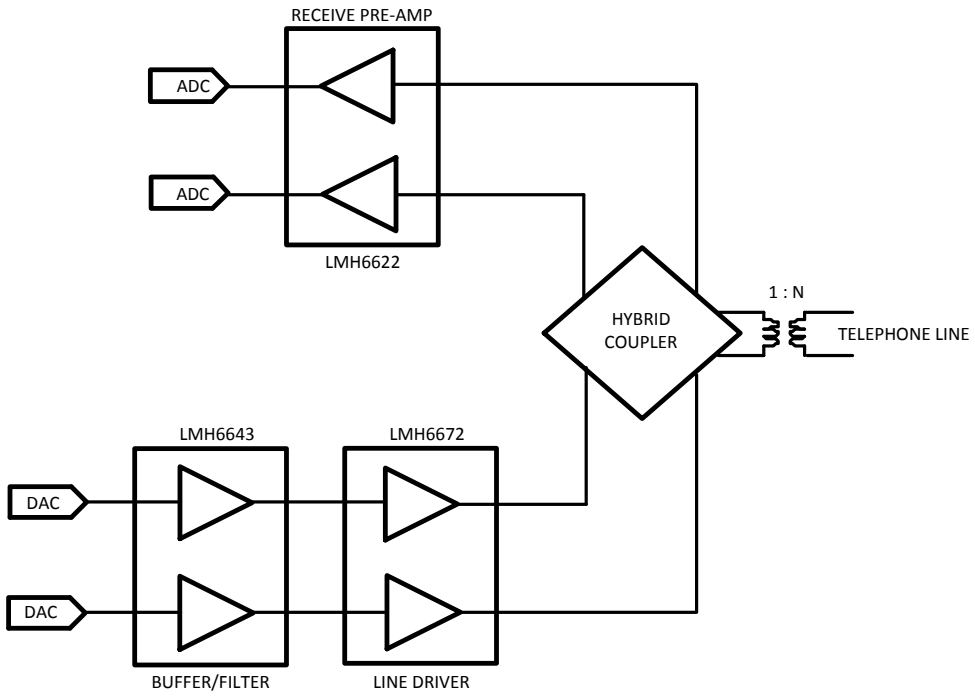


Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 Handling Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 ±6 V Electrical Characteristics ... 5
6.6 ±2.5 V Electrical Characteristics ... 6
6.7 Typical Performance Characteristics ... 9
7 Parameter Measurement Information ... 14
7.1 Test Circuits ... 14
8 Detailed Description ... 16
8.1 Overview ... 16
8.2 Functional Block Diagram ... 16
8.3 Feature Description ... 16
8.4 Device Functional Modes ... 16
9 Application and Implementation ... 17
9.1 DSL Receive Channel Applications ... 17
9.2 Receive Channel Noise Calculation ... 19
9.3 Differential Analog-to-Digital Driver ... 20
9.4 Typical Application ... 21
10 Power Supply Recommendations ... 22
10.1 Driving Capacitive Load ... 22
11 Layout ... 22
11.1 Layout Guidelines ... 22
11.2 Layout Examples ... 23
12 Device and Documentation Support ... 25
12.1 Trademarks ... 25
12.2 Electrostatic Discharge Caution ... 25
12.3 Glossary ... 25
13 Mechanical, Packaging, and Orderable Information ... 25

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2013) to Revision E — **Page**

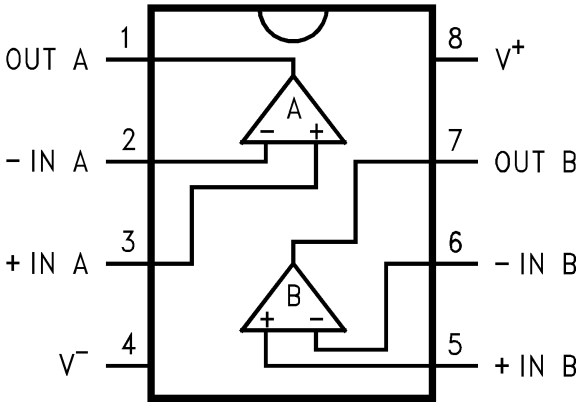
- Changed data sheet flow and layout to conform with new TI standards. Added the following sections: Device Information Table, Application and Implementation; Power Supply Recommendations; Layout; Device and Documentation Support; Mechanical, Packaging, and Ordering Information ... 1
- Changed R_G to R_C. Changed A_V from +10 to +9 for Figure 38 ... 20
- Changed R_G to R_C. Changed A_V from +10 to +9 for Figure 39 ... 20

Changes from Revision C (March 2013) to Revision D — **Page**

- Changed layout of National Data Sheet to TI format ... 1

5 Pin Configuration and Functions

8-Pin SOIC and VSSOP
D and DGK Packages
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT A	1	O	ChA Output
-IN A	2	I	ChA Inverting Input
+IN A	3	I	ChA Non-inverting Input
V-	4	I	V- Supply Pin
+IN B	5	I	ChB Non-inverting Input
-IN B	6	I	ChB Inverting Input
OUT B	7	I	ChB Output
V+	8	I	V+ Supply Pin

6 Specifications

6.1 Absolute Maximum Ratings[1][2]

	MIN	MAX	UNIT
V_{IN} Differential		±1.2	V
Supply Voltage ($V^+ – V^-$)		13.2	V
Voltage at Input Pins		V^+ +0.5, V^- −0.5	V
SOLDERING INFORMATION			
Infrared or Convection (20 sec)		235	°C
Wave Soldering (10 sec)		260	°C
Junction Temperature [3]		+150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$ and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} − T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65°	+150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]		2000[2]	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[3]		200[2]	

(1) JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human body model, 1.5 kΩ in series with 100 pF. Machine model, 0 Ω in series with 200 pF.
(3) JEDEC document JEP157 states that 200-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions[1]

	MIN	MAX	UNIT
Supply Voltage ($V^+ – V^-$)	±2.25	±6	V
Temperature Range[2][3]	−40	+85	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$ and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} − T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

6.4 Thermal Information

THERMAL METRIC[1]		LMH6622 Package D 8 PINS	LMH6622 Package DGK 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	166°	211°	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$ and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} − T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

6.5 ±6 V Electrical Characteristics

Unless otherwise specified, T_J = 25°C, V^+ = 6 V, V^- = −6 V, V_{CM} = 0 V, A_V = +2, R_F = 500 Ω, R_L = 100 Ω. Some limits apply at the temperature extremes as noted in the table.

PARAMETER		TEST CONDITIONS	TEMPERATURE EXTREMES			ROOM TEMPERATURE			UNIT
			MIN(1)	TYP(2)	MAX(1)	MIN(1)	TYP(2)	MAX(1)	
DYNAMIC PERFORMANCE									
f_{CL}	−3dB BW	V_O = 200 mV_{PP}					160		MHz
$BW_{0.1dB}$	0.1dB Gain Flatness	V_O = 20 0mV_{PP}					30		MHz
SR	Slew Rate(3)	V_O = 2 V_{PP}					85		V/µs
TS	Settling Time	V_O = 2 V_{PP} to ±0.1%					40		ns
		V_O = 2 V_{PP} to ±1.0%					35		
Tr	Rise Time	V_O = 0.2 V Step, 10% to 90%					2.3		ns
Tf	Fall Time	V_O = 0.2 V Step, 10% to 90%					2.3		ns
DISTORTION and NOISE RESPONSE									
e_n	Input Referred Voltage Noise	f = 100 kHz					1.6		nV/√Hz
i_n	Input Referred Current Noise	f = 100 kHz					1.5		pA/√Hz
DG	Differential Gain	R_L = 150 Ω, R_F = 470 Ω, NTSC					0.03%		
DP	Differential Phase	R_L = 150 Ω, R_F = 470 Ω, NTSC					0.03		deg
HD2	2nd Harmonic Distortion	f_c = 1 MHz, V_O = 2 V_{PP}, R_L = 100 Ω					−90		dBc
		f_c = 1 MHz, V_O = 2 V_{PP}, R_L = 500 Ω					−100		
HD3	3rd Harmonic Distortion	f_c = 1 MHz, V_O = 2 V_{PP}, R_L = 100 Ω					−94		dBc
		f_c = 1 MHz, V_O = 2 V_{PP}, R_L = 500 Ω					−100		
MTPR	Upstream	V_O = 0.6 V_{RMS}, 26 kHz to 132 kHz (see Figure 33)					−78		dBc
	Downstream	V_O = 0.6 V_{RMS}, 144 kHz to 1.1 MHz (see Figure 33)					−70		
INPUT CHARACTERISTICS									
V_{OS}	Input Offset Voltage	V_{CM} = 0 V	−2		+2	−1.2	+0.2	+1.2	mV
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0 V(4)					−2.5		µV/°C
I_{OS}	Input Offset Current	V_{CM} = 0V	−1.5		1.5	−1	−0.04	1	µA
I_B	Input Bias Current	V_{CM} = 0V			15		4.7	10	µA
R_{IN}	Input Resistance	Common Mode					17		MΩ
		Differential Mode					12		kΩ
C_{IN}	Input Capacitance	Common Mode					0.9		pF
		Differential Mode					1.0		pF
CMVR	Input Common Mode Voltage Range	CMRR ≥ 60dB					−4.75	−4.5	V
						5.5	+5.7		
CMRR	Common-Mode Rejection Ratio	Input Referred, V_{CM} = −4.2 V to +5.2 V	75			80	100		dB

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the slowest of the rising and falling slew rates.
(4) Offset voltage average drift is determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

±6 V Electrical Characteristics (continued)

Unless otherwise specified, T_J = 25°C, V^+ = 6 V, V^- = −6 V, V_{CM} = 0 V, A_V = +2, R_F = 500 Ω, R_L = 100 Ω. Some limits apply at the temperature extremes as noted in the table.

PARAMETER		TEST CONDITIONS	TEMPERATURE EXTREMES			ROOM TEMPERATURE			UNIT
			MIN(1)	TYP(2)	MAX(1)	MIN(1)	TYP(2)	MAX(1)	
TRANSFER CHARACTERISTICS									
A_{VOL}	Large Signal Voltage Gain	V_O = 4 V_{PP}	70			74	83		dB
X_t	Crosstalk	f = 1 MHz					−75		dB
OUTPUT CHARACTERISTICS									
V_O	Output Swing	No Load, Positive Swing	4.6			4.8	5.2		V
		No Load, Negative Swing			−4.4		−5.0	−4.6	
		R_L = 100 Ω, Positive Swing	3.8			4.0	4.6		
		R_L = 100 Ω, Negative Swing			−3.8		−4.6	−4	
R_O	Output Impedance	f = 1 MHz					0.08		Ω
I_{SC}	Output Short Circuit Current	Sourcing to Ground ΔV_{IN} = 200 mV(5),(6)				100	135		mA
		Sinking to Ground ΔV_{IN} = −200 mV(5),(6)				100	130		
I_{OUT}	Output Current	Sourcing, V_O = +4.3 V Sinking, V_O = −4.3 V					90		mA
POWER SUPPLY									
+PSRR	Positive Power Supply Rejection Ratio	Input Referred, V_S = +5 V to +6 V	74			80	95		dB
−PSRR	Negative Power Supply Rejection Ratio	Input Referred, V_S = −5 V to −6 V	69			75	90		
I_S	Supply Current (per amplifier)	No Load			6.5		4.3	6	mA

(5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(6) Short circuit test is a momentary test. Output short circuit duration is infinite for $V_S \leq$ ±2.5 V, at room temperature and below. For $V_S >$ ±2.5 V, allowable short circuit duration is 1.5ms.

6.6 ±2.5 V Electrical Characteristics

Unless otherwise specified, T_J = 25°C, V+ = 2.5 V, V− = −2.5 V, V_{CM} = 0 V, A_V = +2, R_F = 500 Ω, R_L = 100 Ω. Some limits apply at the temperature extremes as noted in the table.

PARAMETER		TEST CONDITIONS	TEMPERATURE EXTREMES			ROOM TEMPERATURE			UNIT
			MIN(1)	TYP(2)	MAX(1)	MIN(1)	TYP(2)	MAX(1)	
DYNAMIC PERFORMANCE									
f_{CL}	−3 dB BW	V_O = 200 mV_{PP}					150		MHz
$BW_{0.1dB}$	0.1dB Gain Flatness	V_O = 200 mV_{PP}					20		MHz
SR	Slew Rate (3)	V_O = 2 V_{PP}					80		V/µs
T_S	Settling Time	V_O = 2 V_{PP} to ±0.1%					45		ns
		V_O = 2 V_{PP} to ±1.0%					40		
T_r	Rise Time	V_O = 0.2 V Step, 10% to 90%					2.5		ns
T_f	Fall Time	V_O = 0.2 V Step, 10% to 90%					2.5		ns

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the slowest of the rising and falling slew rates.

±2.5 V Electrical Characteristics (continued)

Unless otherwise specified, T_J = 25°C, V+ = 2.5 V, V− = −2.5 V, V_{CM} = 0 V, A_V = +2, R_F = 500 Ω, R_L = 100 Ω. Some limits apply at the temperature extremes as noted in the table.

PARAMETER		TEST CONDITIONS	TEMPERATURE EXTREMES			ROOM TEMPERATURE			UNIT
			MIN(1)	TYP(2)	MAX(1)	MIN(1)	TYP(2)	MAX(1)	
DISTORTION and NOISE RESPONSE									
e_n	Input Referred Voltage Noise	f = 100 kHz					1.7		nV/√Hz
i_n	Input Referred Current Noise	f = 100 kHz					1.5		pA/√Hz
HD2	2nd Harmonic Distortion	fc = 1 MHz, V_O = 2V_{PP}, R_L = 100 Ω					−88		dBc
		fc = 1 MHz, V_O = 2V_{PP}, R_L = 500 Ω					−98		
HD3	3rd Harmonic Distortion	fc = 1 MHz, V_O = 2 V_{PP}, R_L = 100 Ω					−92		dBc
		fc = 1 MHz, V_O = 2 V_{PP}, R_L = 500 Ω					−100		
MTPR	Upstream	V_O = 0.4V_{RMS}, 26kHz to 132kHz (see Figure 33)					−76		dBc
	Downstream	V_O = 0.4 V_{RMS}, 144 kHz to 1.1 MHz (see Figure 33)					−68		
INPUT CHARACTERISTICS									
V_{OS}	Input Offset Voltage	V_{CM} = 0 V	−2.3		+2.3	−1.5	+0.3	+1.5	mV
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0 V(4)					−2.5		µV/°C
I_{OS}	Input Offset Current	V_{CM} = 0 V	−2.5		2.5	−1.5	+0.01	1.5	µA
I_B	Input Bias Current	V_{CM} = 0 V			15		4.6	10	µA
R_{IN}	Input Resistance	Common Mode					17		MΩ
		Differential Mode					12		kΩ
C_{IN}	Input Capacitance	Common Mode					0.9		pF
		Differential Mode					1.0		pF
CMVR	Input Common Mode Voltage Range	CMRR ≥ 60dB					−1.25	−1	V
						2	+2.2		
CMRR	Common Mode Rejection Ratio	Input Referred, V_{CM} = −0.7 V to +1.7 V	75			80	100		dB
TRANSFER CHARACTERISTICS									
A_{VOL}	Large Signal Voltage Gain	V_O = 1 V_{PP}				74	82		dB
X_t	Crosstalk	f = 1 MHz					−75		dB

(4) Offset voltage average drift is determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

±2.5 V Electrical Characteristics (continued)

Unless otherwise specified, T_J = 25°C, V+ = 2.5 V, V− = −2.5 V, V_{CM} = 0 V, A_V = +2, R_F = 500 Ω, R_L = 100 Ω. Some limits apply at the temperature extremes as noted in the table.

PARAMETER		TEST CONDITIONS	TEMPERATURE EXTREMES			ROOM TEMPERATURE			UNIT
			MIN(1)	TYP(2)	MAX(1)	MIN(1)	TYP(2)	MAX(1)	
OUTPUT CHARACTERISTICS									
V_O	Output Swing	No Load, Positive Swing	1.2			1.4	1.7		V
		No Load, Negative Swing			−1		−1.5	−1.2	
		R_L = 100 Ω, Positive Swing	1			1.2	1.5		
		R_L = 100 Ω, Negative Swing			−0.9		−1.4	−1.1	
R_O	Output Impedance	f = 1 MHz					0.1		Ω
I_{SC}	Output Short Circuit Current	Sourcing to Ground ΔV_{IN} = 200 mV(5)(6)				100	137		mA
		Sinking to Ground ΔV_{IN} = −20 0mV(5)(6)				100	134		
I_{OUT}	Output Current	Sourcing, V_O = +0.8 V Sinking, V_O = −0.8 V					90		mA
POWER SUPPLY									
+PSRR	Positive Power Supply Rejection Ratio	Input Referred, V_S = +2.5 V to +3 V	72			78	93		dB
−PSRR	Negative Power Supply Rejection Ratio	Input Referred, V_S = −2.5 V to −3 V	70			75	88		dB
I_S	Supply Current (per amplifier)	No Load			6.4		4.1	5.8	mA

(5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(6) Short circuit test is a momentary test. Output short circuit duration is infinite for $V_S \leq \pm 2.5$ V, at room temperature and below. For $V_S >$ ±2.5 V, allowable short circuit duration is 1.5ms.

6.7 Typical Performance Characteristics

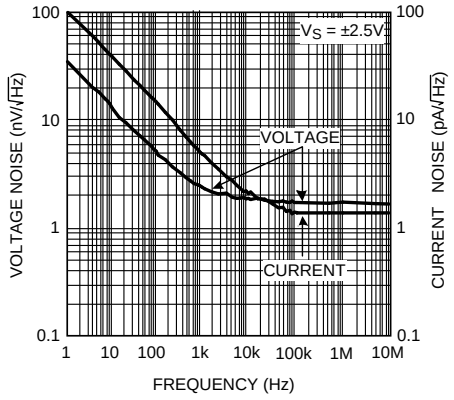


Figure 1. Current and Voltage Noise vs. Frequency

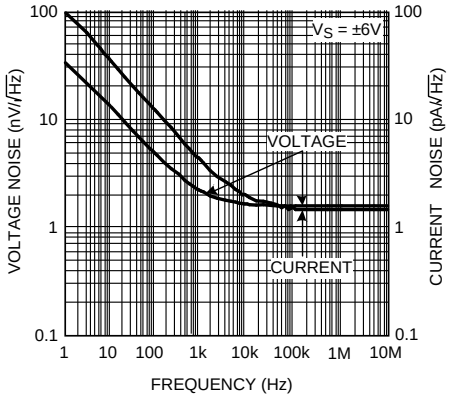


Figure 2. Current and Voltage Noise vs. Frequency

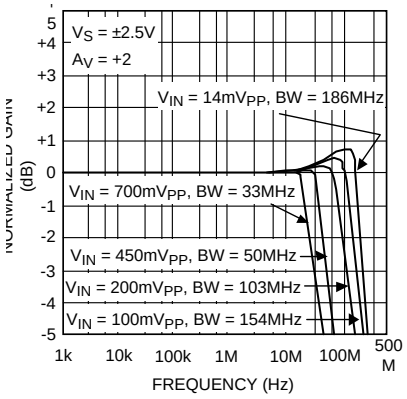


Figure 3. Frequency Response vs. Input Signal Level

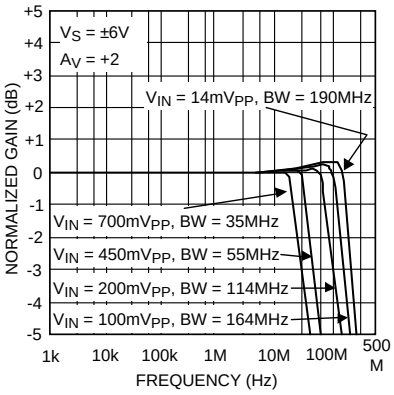


Figure 4. Frequency Response vs. Input Signal Level

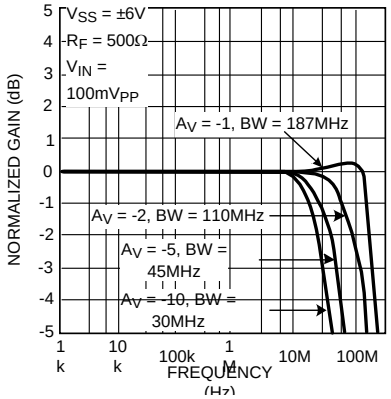


Figure 5. Inverting Amplifier Frequency Response

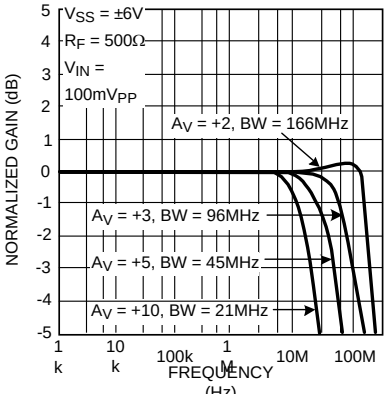


Figure 6. Non-Inverting Amplifier Frequency Response

Typical Performance Characteristics (continued)

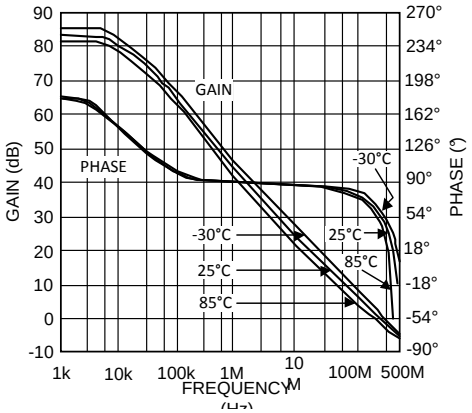


Figure 7. Open Loop Gain and Phase Response

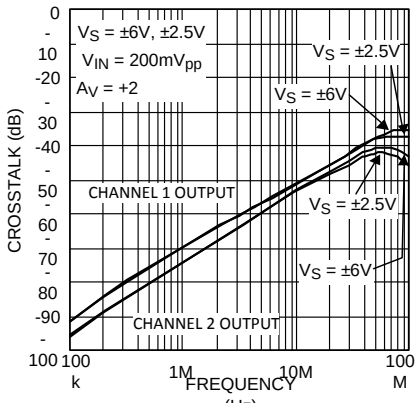


Figure 8. Crosstalk vs. Frequency

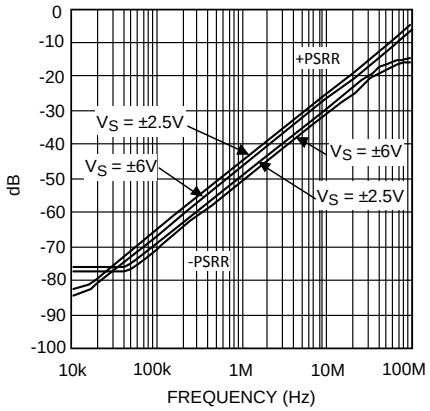


Figure 9. PSRR vs. Frequency

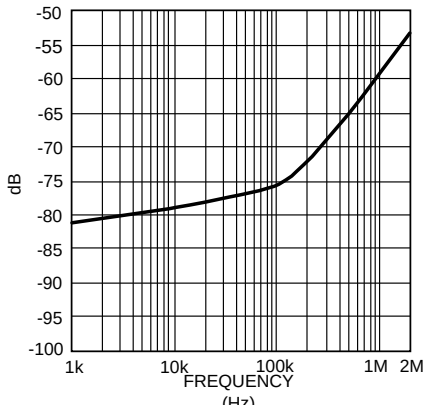


Figure 10. CMRR vs. Frequency

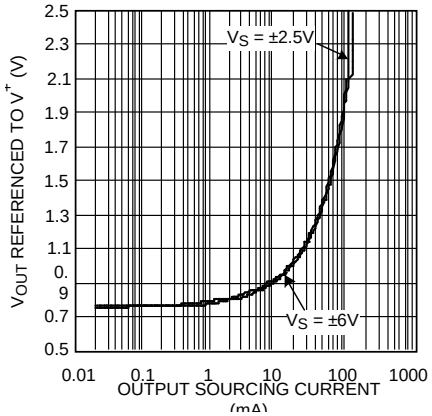


Figure 11. Positive Output Swing vs. Source Current

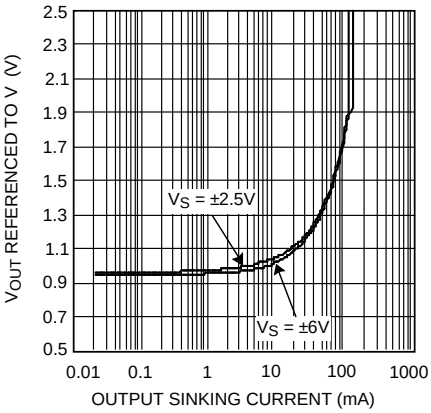


Figure 12. Negative Output Swing vs. Sink Current

Typical Performance Characteristics (continued)

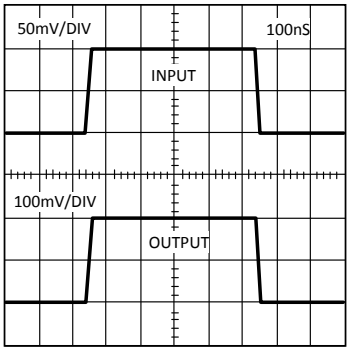


Figure 13. Non-Inverting Small Signal Pulse Response
V_S = ±2.5 V, R_L = 100 Ω, A_V = +2, R_F = 500 Ω

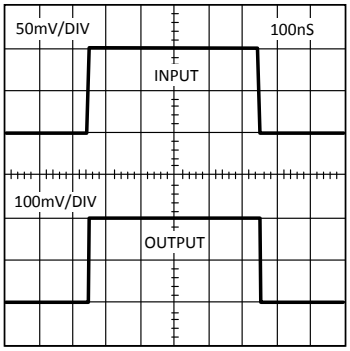


Figure 14. Non-Inverting Small Signal Pulse Response
V_S = ±6 V, R_L = 100 Ω, A_V = +2, R_F = 500 Ω

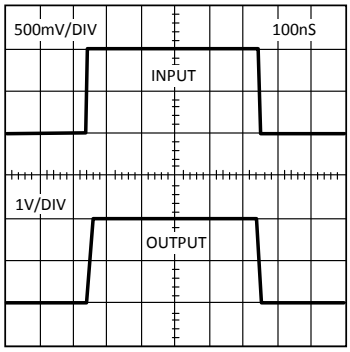


Figure 15. Non-Inverting Large Signal Pulse Response
V_S = ±2.5 V, R_L = 100 Ω, A_V = +2, R_F = 500 Ω

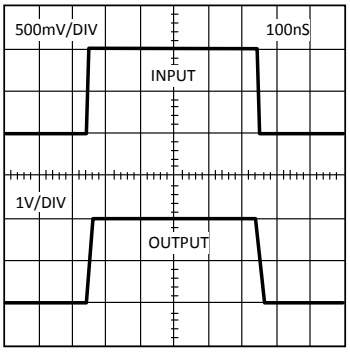


Figure 16. Non-Inverting Large Signal Pulse Response
V_S = ±6 V, R_L = 100 Ω, A_V = +2, R_F = 500 Ω

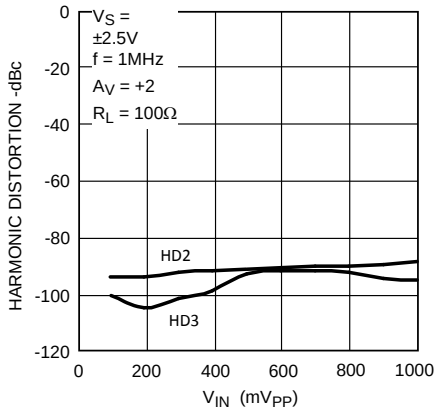


Figure 17. Harmonic Distortion vs. Input Signal Level

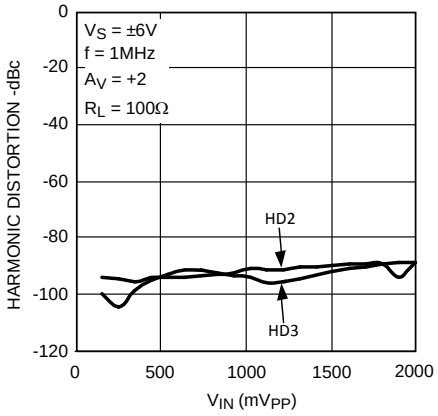


Figure 18. Harmonic Distortion vs. Input Signal Level

Typical Performance Characteristics (continued)

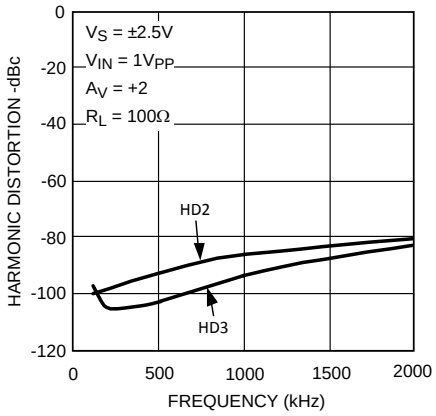


Figure 19. Harmonic Distortion vs. Frequency

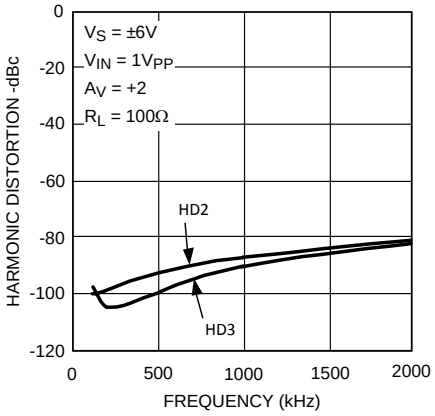


Figure 20. Harmonic Distortion vs. Frequency

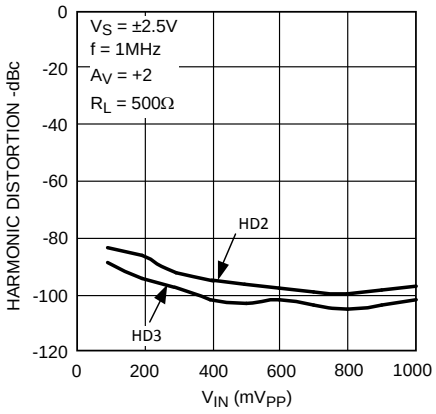


Figure 21. Harmonic Distortion vs. Input Signal Level

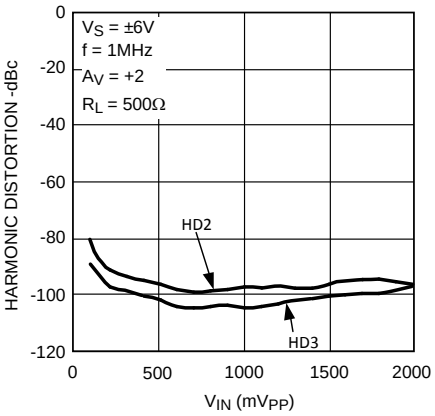


Figure 22. Harmonic Distortion vs. input Signal Level

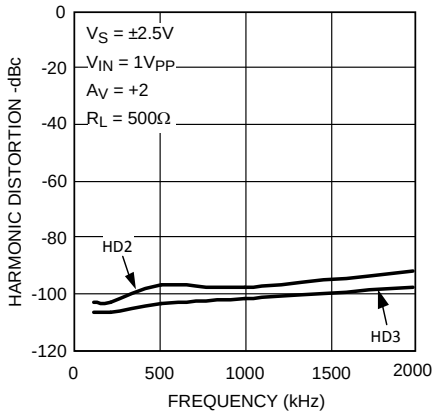


Figure 23. Harmonic Distortion vs. Input Frequency

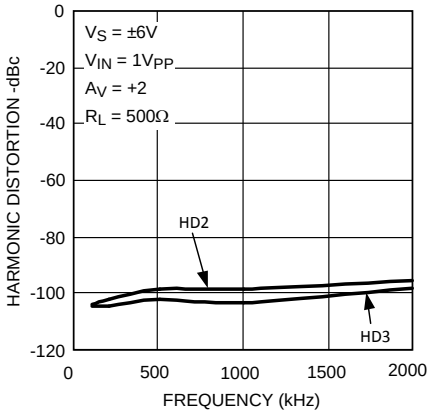


Figure 24. Harmonic Distortion vs. Input Frequency

Typical Performance Characteristics (continued)

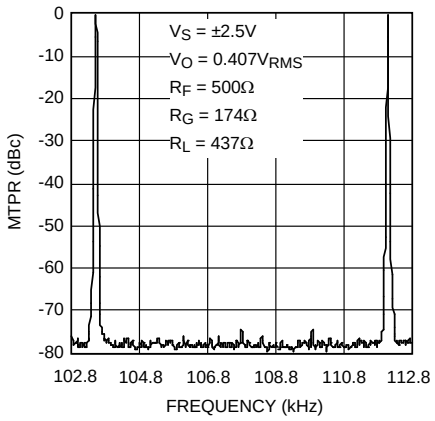


Figure 25. Full Rate ADSL (DMT) Upstream MTPR @ V_S = ±2.5 V

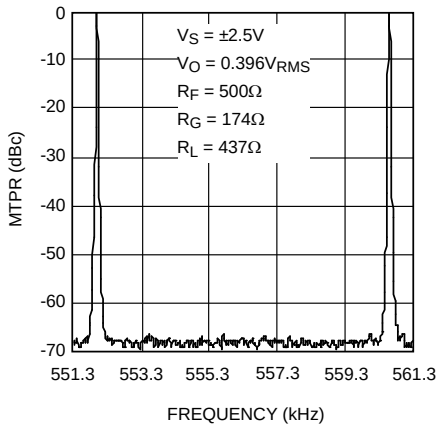


Figure 26. Full Rate ADSL (DMT) Downstream MTPR @ V_S = ±2.5 V

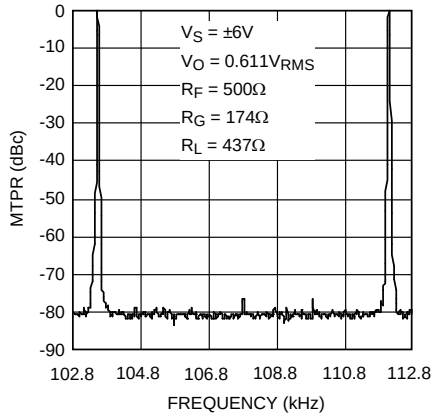


Figure 27. Full Rate ADSL (DMT) Upstream MTPR @ V_S = ±6 V

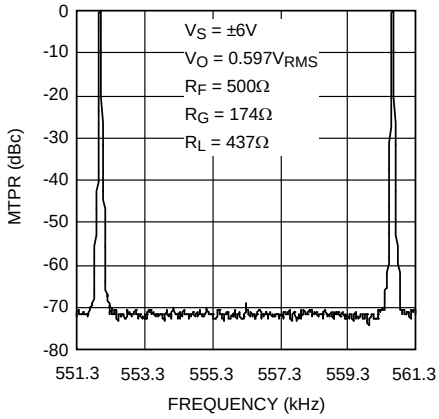


Figure 28. Full Rate ADSL (DMT) Downstream MTPR @ V_S = ±6 V

7 Parameter Measurement Information

7.1 Test Circuits

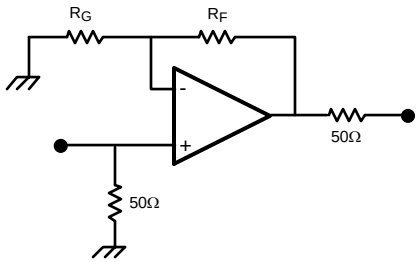


Figure 29. Non-Inverting Amplifier

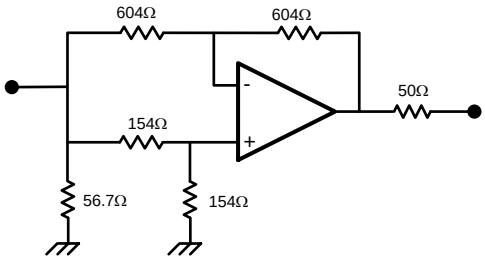


Figure 30. CMRR

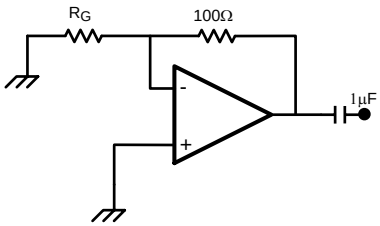


Figure 31. Voltage Noise
R_G = 1 Ω for f ≤ 100 kHz, R_G = 20 Ω for f > 100 kHz

Test Circuits (continued)

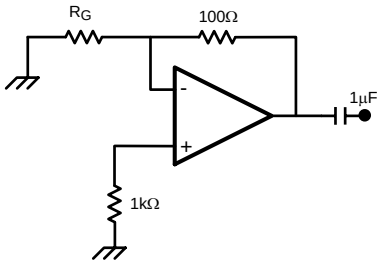


Figure 32. Current Noise
R_G = 1 Ω for f ≤ 100 kHz, R_G = 20 Ω for f > 100 kHz

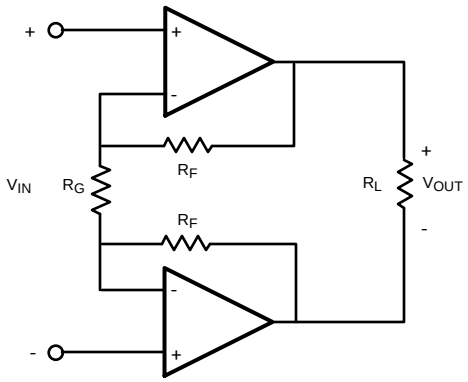


Figure 33. Multitone Power Ratio, R_F = 500 Ω, R_G = 174 Ω, R_L = 437 Ω

8 Detailed Description

8.1 Overview

The LMH6622 is a dual high speed voltage operational amplifier specifically optimized for low noise. The LMH6622 operates from ±2.5 V to ±6 V in dual supply mode and from +5 V to +12 V in single supply configuration.

8.2 Functional Block Diagram

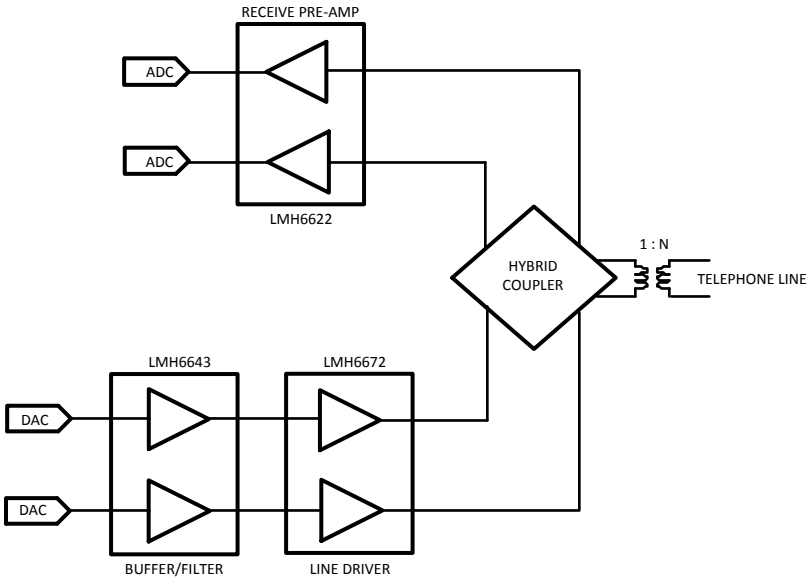


Figure 34. xDSL Analog Front End

8.3 Feature Description

- 4.5 V to 12 V supply range
- Large linear output current of 90 mA
- Excellent harmonic distortion of 90 dBc

8.4 Device Functional Modes

- Single or dual supplies
- Traditional voltage feedback topology for maximum flexibility

9 Application and Implementation

9.1 DSL Receive Channel Applications

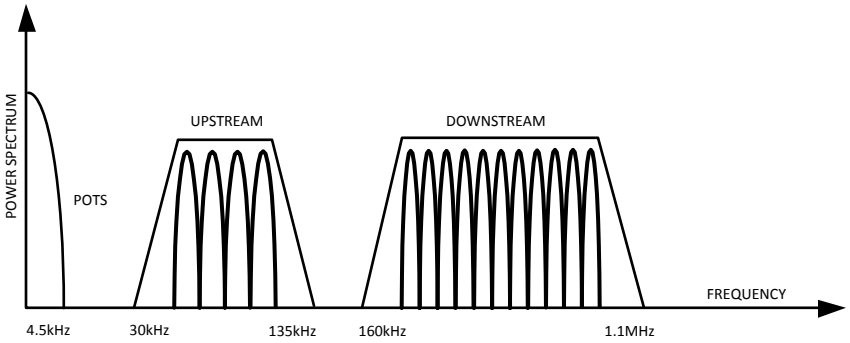


Figure 35. ADSL Signal Description

The LMH6622 is a dual, wideband operational amplifier designed for use as a DSL line receiver. In the receive band of a Customer Premises Equipment (CPE) ADSL modem it is possible that as many as 255 Discrete Multi-Tone (DMT) QAM signals will be present, each with its own carrier frequency, modulation, and signal level. The ADSL standard requires a line referred noise power density of -140 dBm/Hz within the CPE receive band of 100 KHz to 1.1 MHz. The CPE driver output signal will leak into the receive path because of full duplex operation and the imperfections of the hybrid coupler circuit. The DSL analog front end must incorporate a receiver pre-amp which is both low noise and highly linear for ADSL-standard operation. The LMH6622 is designed for the twin performance parameters of low noise and high linearity.

DSL Receive Channel Applications (continued)

Applications ranging from +5 V to +12 V or ±2.5 V to ±6 V are fully supported by the LMH6622. In Figure 36, the LMH6622 is used as an inverting summing amplifier to provide both received pre-amp channel gain and driver output signal cancellation, that is, the function of a hybrid coupler.

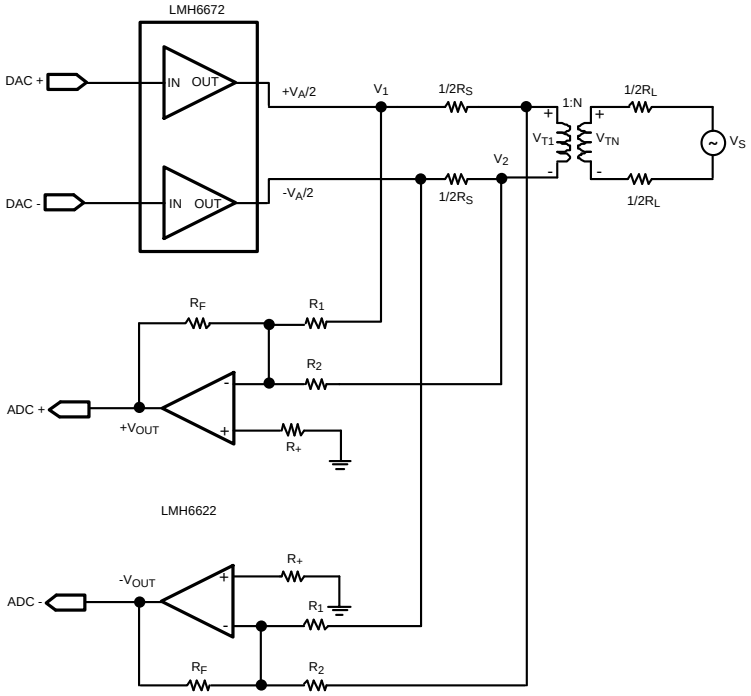


Figure 36. ADSL Receive Applications Circuit

The two R_S resistors are used to provide impedance matching through the 1:N transformer.

$$R_S = \frac{R_L}{N^2}$$

where

- R_L is the impedance of the twisted pair line
- N is the turns ratio of the transformer (1)

The resistors R_2 and R_F are used to set the receive gain of the pre-amp. The receive gain is selected to meet the ADC full-scale requirement of a DSL chipset.

Resistor R_1 and R_2 along with R_F are used to achieve cancellation of the output driver signal at the output of the receiver.

Since the LMH6622 is configured as an inverting summing amplifier, V_{OUT} is found to be,

$$V_{OUT} = -R_F\left[\frac{V_1}{R_1} + \frac{V_2}{R_2}\right] \quad (2)$$

The expression for V_1 and V_2 can be found by using superposition principle.

When $V_S = 0$,

$$V_1 = \frac{1}{2}V_A \quad \text{and} \quad V_2 = -\frac{1}{4}V_A \quad (3)$$

When $V_A = 0$,

$$V_1 = 0 \quad \text{and} \quad V_2 = -\frac{1}{2}V_{T1} \quad (4)$$

DSL Receive Channel Applications (continued)

Therefore,

$$V_1 = \frac{1}{2}V_A \quad \text{and} \quad V_2 = -\frac{1}{4}V_A - \frac{1}{2}V_{T1} \tag{5}$$

And then,

$$V_{OUT} = -R_F\left[\frac{V_A}{2R_1} - \frac{V_A}{4R_2} - \frac{V_{T1}}{2R_2}\right] \tag{6}$$

Setting $R_1 = 2*R_2$ to cancel unwanted driver signal in the receive path, then we have

$$V_{OUT} = \frac{R_F}{2R_2}V_{T1} \tag{7}$$

We can also find that,

$$V_{TN} = \frac{1}{2}V_S \text{ and } V_{T1} = \frac{1}{N}V_{TN} = \frac{1}{2N}V_S \tag{8}$$

And then

$$V_{OUT} = \frac{R_F}{4NR_2}V_S \tag{9}$$

In conclusion, the peak-to-peak voltage to the ADC would be,

$$2\ V_{OUT} = \frac{R_F}{2NR_2}V_S \tag{10}$$

9.2 Receive Channel Noise Calculation

The circuit of Figure 36 also has the characteristic that it cancels noise power from the drive channel.

The noise gain of the receive pre-amp is found to be:

$$A_n = 1 + \frac{R_F}{R_1 / R_2} \tag{11}$$

Noise power at each of the output of LMH6622:

$$e^2_o = A^2_n\,[V^2_n + i^2_{non\text{-}inv}\,R_+{}^2 + 4kT\,R_+] + i^2_{inv}\,R^2_F + 4kT\,R_F\,A_n$$

where

- V_n is the Input referred voltage noise
- i_n is the Input referred current noise
- $i_{non\text{-}inv}$ is the Input referred non-inverting current noise
- i_{inv} is the Input referred inverting current noise
- k is the Boltzmann's constant, K = 1.38 x 10^{-23}
- T is the Resistor temperature in k
- R_+ is the source resistance at the non-inverting input to balance offset voltage, typically very small for this inverting summing applications

(12)

For a voltage feedback amplifier,

$$i_{inv} = i_{non\text{-}inv} = i_n \tag{13}$$

Therefore, total output noise from the differential pre-amp is:

$$e^2_{TotalOutput} = 2\,e^2_o \tag{14}$$

The factor '2 ' appears here because of differential output.

9.3 Differential Analog-to-Digital Driver

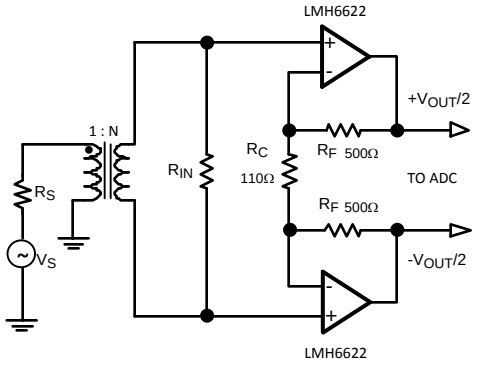


Figure 37. Circuit for Differential A/D Driver

The LMH6622 is a low noise, low distortion high speed operational amplifier. The LMH6622 comes in either SOIC-8 or VSSOP-8 packages. Because two channels are available in each package the LMH6622 can be used as a high dynamic range differential amplifier for the purpose of driving a high speed analog-to-digital converter. Driving a 1 kΩ load, the differential amplifier of Figure 37 provides 20 dB gain, a flat frequency response up to 6 MHz, and harmonic distortion that is lower than 80 dBc. This circuit makes use of a transformer to convert a single-ended signal to a differential signal. The input resistor R_{IN} is chosen by the following equation,

$$R_{IN} = \frac{1}{N^2} R_S \tag{15}$$

The gain of this differential amplifier can be adjusted by R_C and R_F,

$$A_V = 2 \frac{R_F}{R_C} \tag{16}$$

See Figure 38 and Figure 39 below for plots related to the discussion of Figure 37.

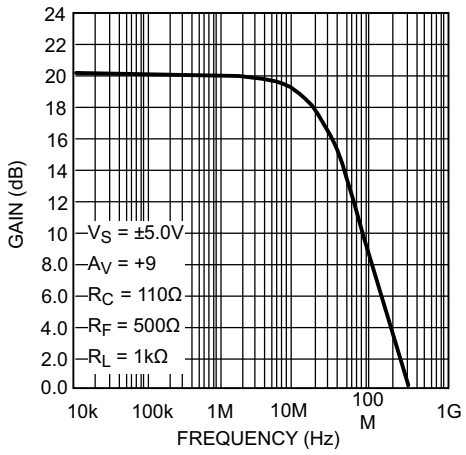


Figure 38. Frequency Response

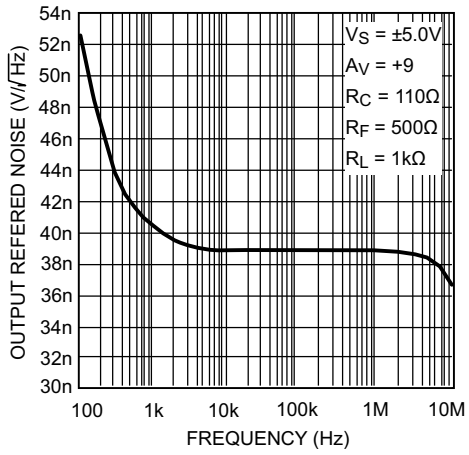


Figure 39. Total Output Referred Noise Density

9.4 Typical Application

See Figure 40 for application circuit.

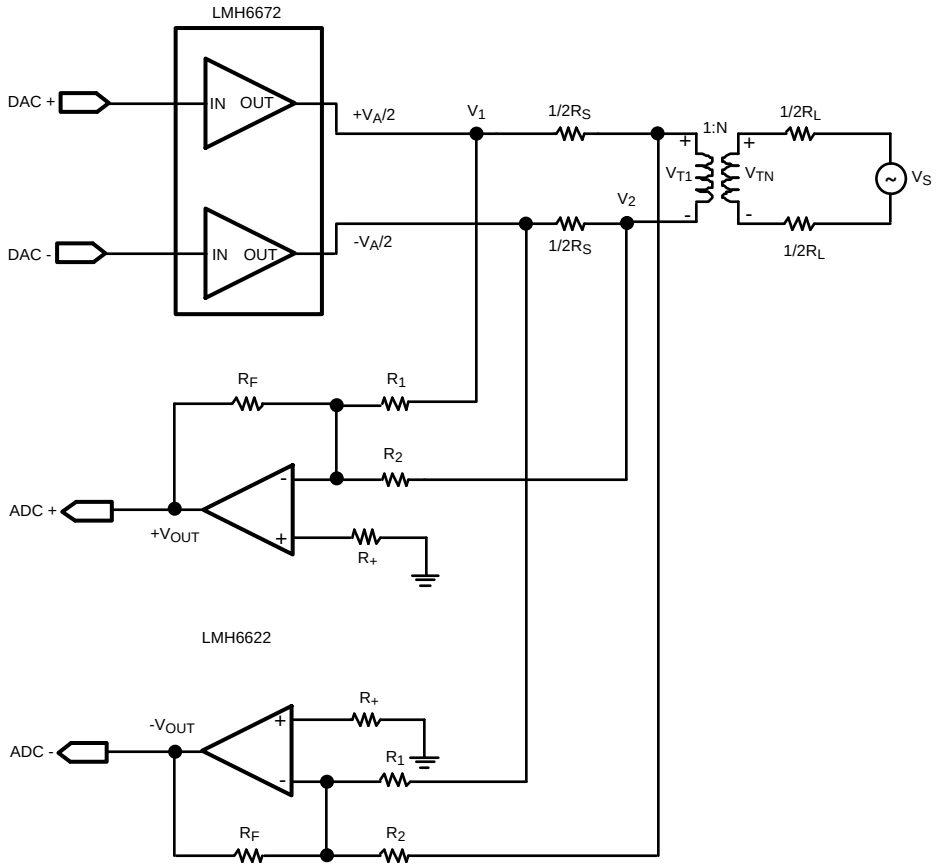


Figure 40. ADSL Receive Applications Circuit

9.4.1 Design Requirements

All normal precautions / considerations with Op Amps apply

9.4.2 Detailed Design Procedure

- Use power supply decoupling capacitors close to supply pins
- Beware of junction temperature rise at elevated ambient temperature and / or heavy output(s) load current especially at higher supply voltages
- Ground plane near sensitive input pins can be removed to minimize parasitic capacitance

9.4.3 Application Curves

See Figure 38 and Figure 39.

10 Power Supply Recommendations

10.1 Driving Capacitive Load

Capacitive Loads decrease the phase margin of all op amps. The output impedance of a feedback amplifier becomes inductive at high frequencies, creating a resonant circuit when the load is capacitive. This can lead to overshoot, ringing and oscillation. To eliminate oscillation or reduce ringing, an isolation resistor can be placed between the load and the output. In general, the bigger the isolation resistor, the more damped the pulse response becomes. For initial evaluation, a 50 Ω isolation resistor is recommended.

11 Layout

11.1 Layout Guidelines

11.1.1 Circuit Layout Considerations

Texas Instruments suggests the copper patterns on the evaluation boards listed below as a guide for high frequency layout. These boards are also useful as an aid in device testing and characterization. As is the case with all high-speed amplifiers, accepted-practice R_F design technique on the PCB layout is mandatory. Generally, a good high frequency layout exhibits a separation of power supply and ground traces from the inverting input and output pins. Parasitic capacitances between these nodes and ground will cause frequency response peaking and possible circuit oscillations (see SNOA367, Application Note OA-15, for more information). High quality chip capacitors with values in the range of 1000 pF to 0.1 µF should be used for power supply bypassing. One terminal of each chip capacitor is connected to the ground plane and the other terminal is connected to a point that is as close as possible to each supply pin as allowed by the manufacturer's design rules. In addition, a tantalum capacitor with a value between 4.7 µF and 10 µF should be connected in parallel with the chip capacitor. Signal lines connecting the feedback and gain resistors should be as short as possible to minimize inductance and microstrip line effect. Input and output termination resistors should be placed as close as possible to the input/output pins. Traces greater than 1 inch in length should be impedance matched to the corresponding load termination.

Symmetry between the positive and negative paths in the layout of differential circuitry should be maintained so as to minimize the imbalance of amplitude and phase of the differential signal.

DEVICE	PACKAGE	EVALUATION BOARD P/N
LMH6622MA	SOIC-8	LMH730036
LMH6622MM	VSSOP-8	LMH730123

Component value selection is another important parameter in working with high speed/high performance amplifiers. Choosing external resistors that are large in value compared to the value of other critical components will affect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These parasitic capacitors could either be inherent to the device or be a by-product of the board layout and component placement. Moreover, a large resistor will also add more thermal noise to the signal path. Either way, keeping the resistor values low will diminish this interaction. On the other hand, choosing very low value resistors could load down nodes and will contribute to higher overall power dissipation and worse distortion.

11.2 Layout Examples

11.2.1 SOIC Layout Example

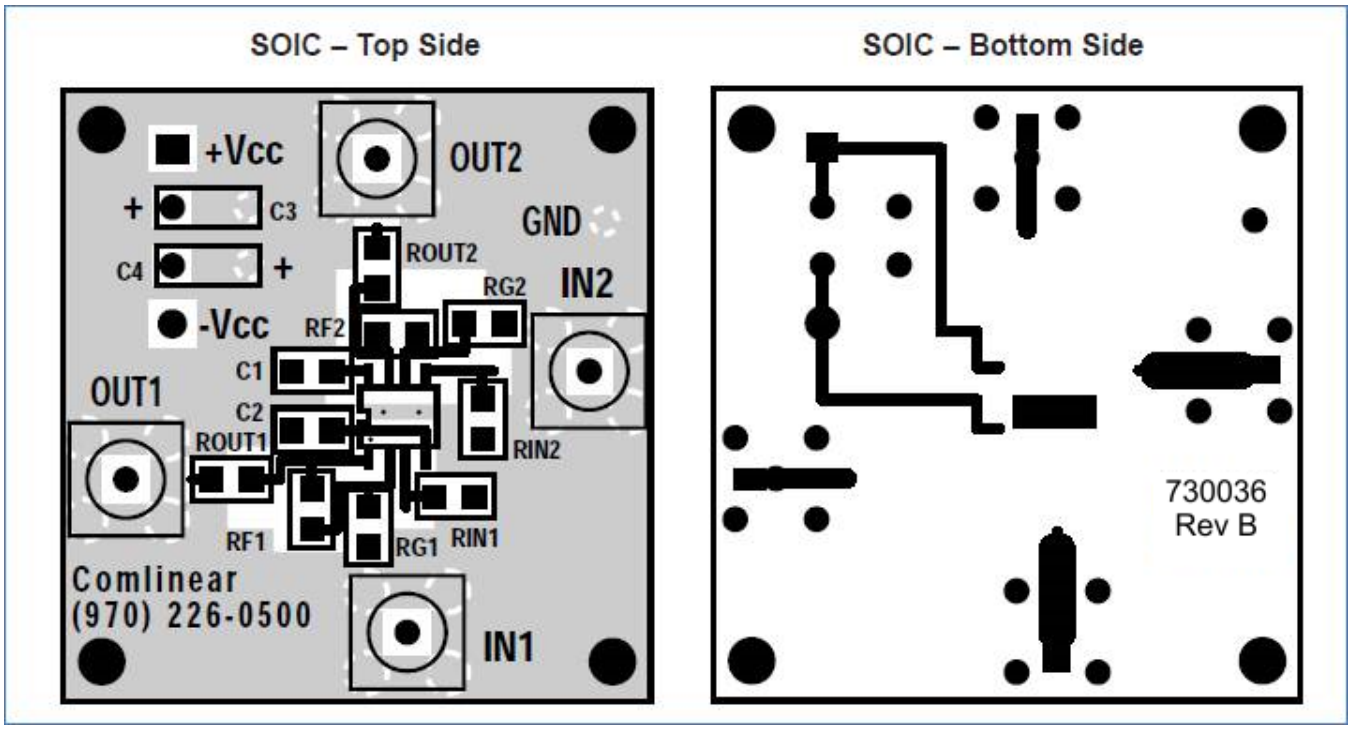
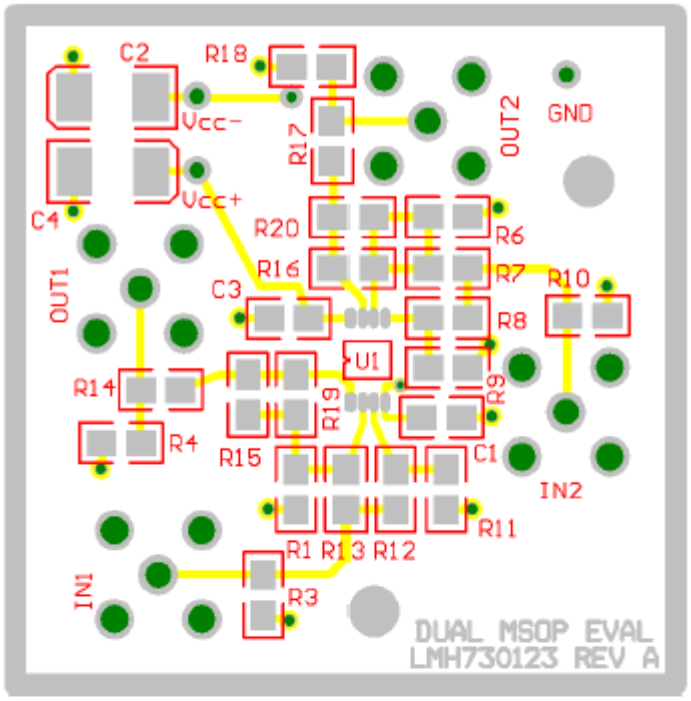


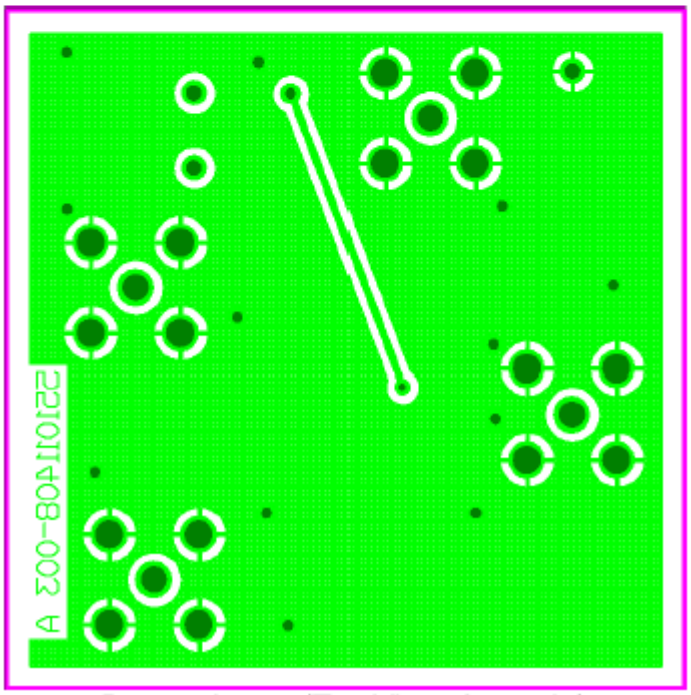
Figure 41. LMH6622 Layout Example - SOIC

Layout Examples (continued)

11.2.2 VSSOP Layout Example



Top Layer (2x scale)



Bottom Layer (Top View, 2x scale)

Figure 42. LMH6622 Layout Example - VSSOP

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6622MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 22MA	Samples
LMH6622MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 22MA	Samples
LMH6622MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	A80A	Samples
LMH6622MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	A80A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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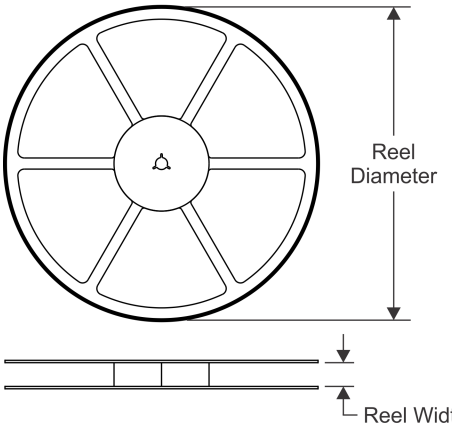
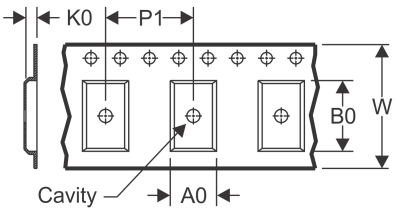
TAPE AND REEL INFORMATION

REEL DIMENSIONS

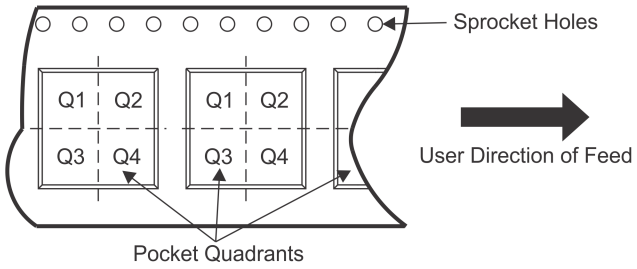


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

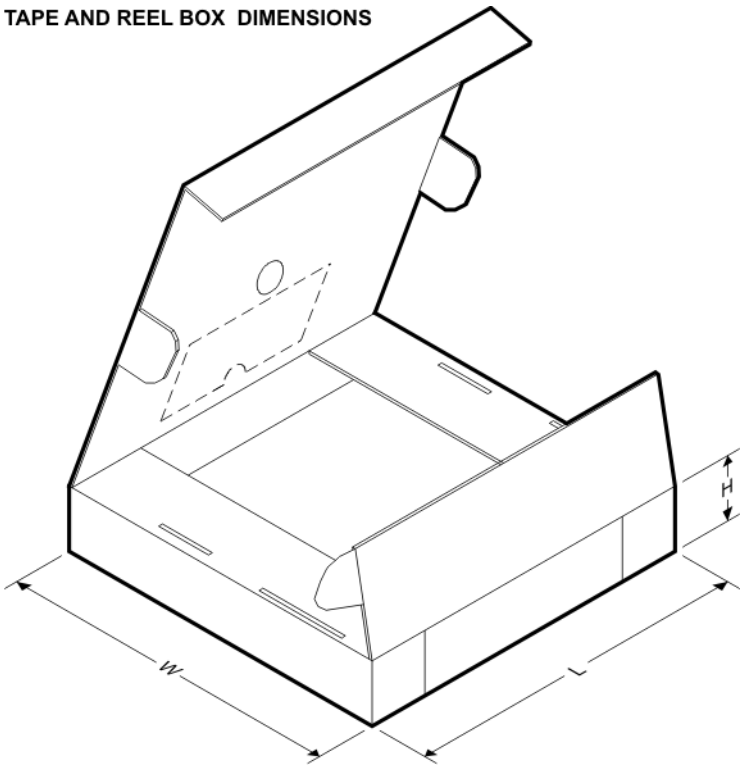
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

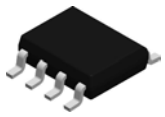
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6622MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6622MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6622MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6622MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6622MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMH6622MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

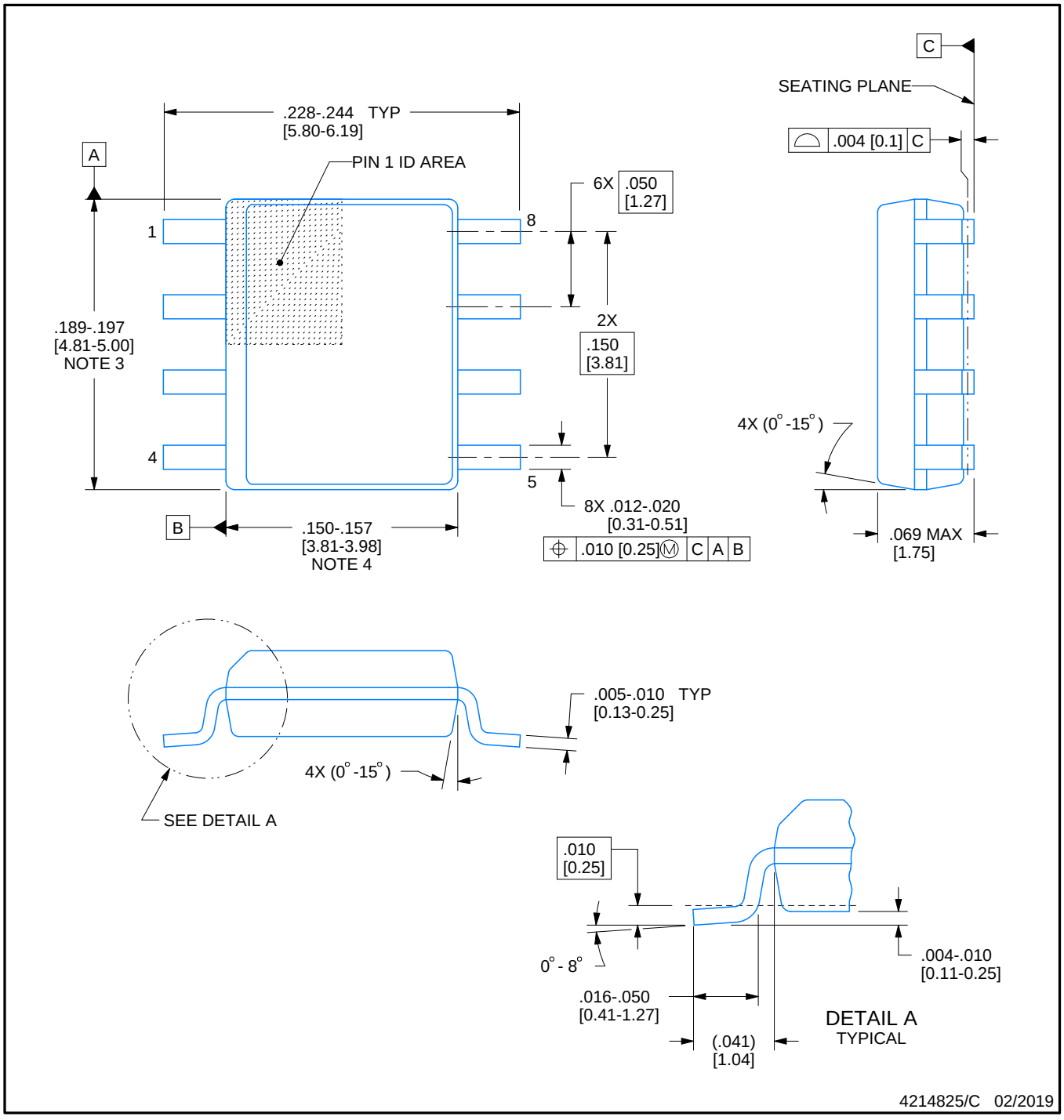


PACKAGE OUTLINE

D0008A

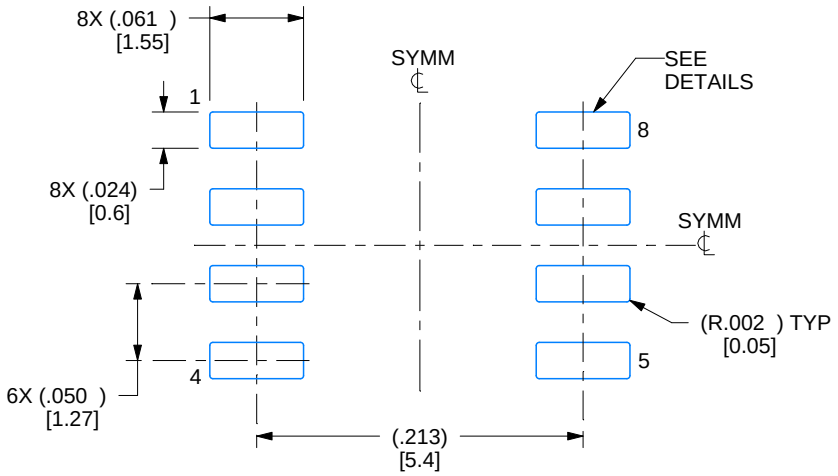
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

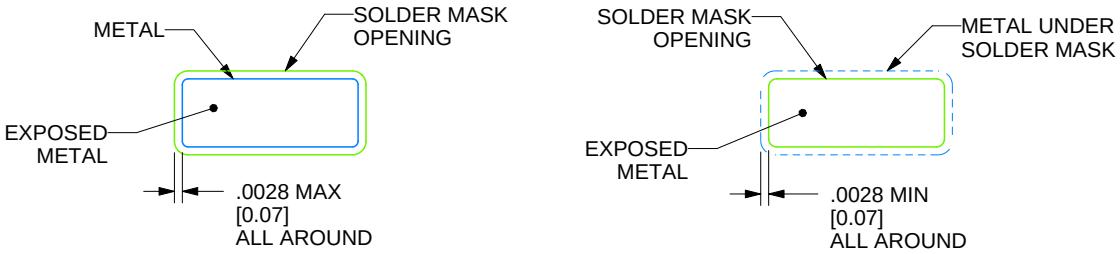


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

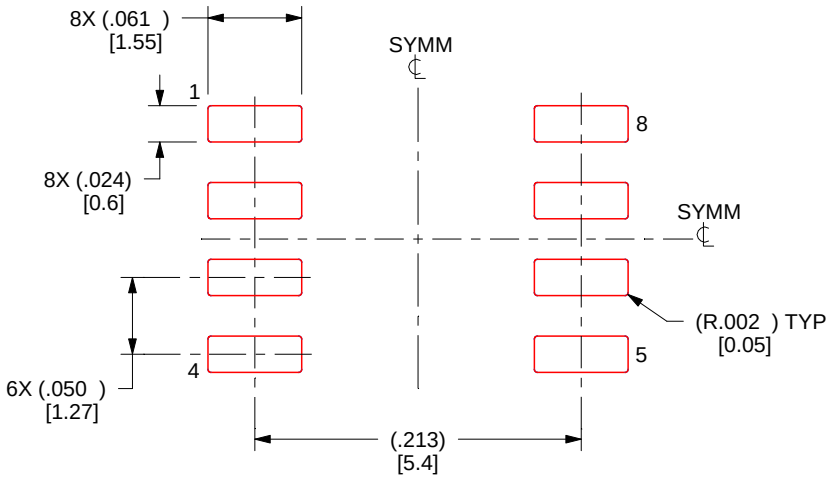
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



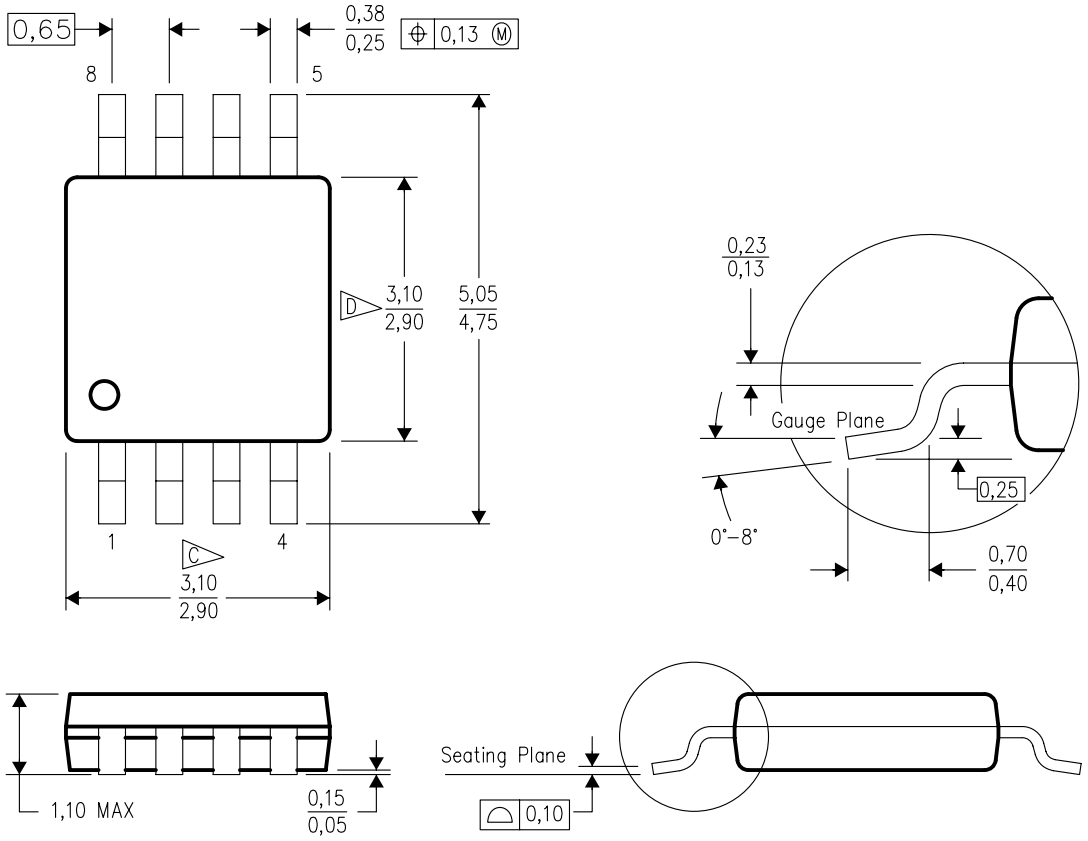
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

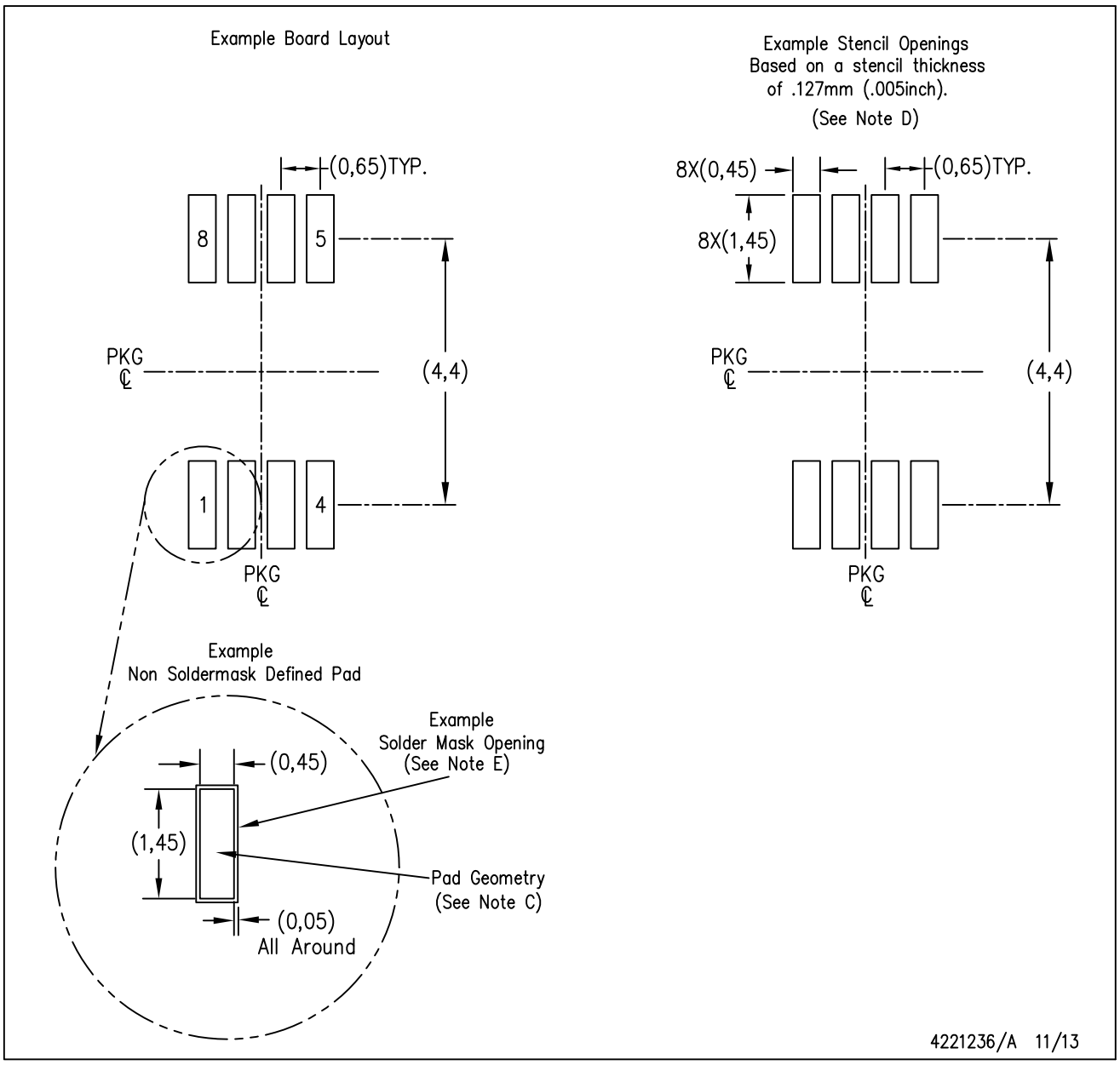
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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