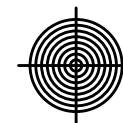
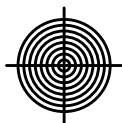
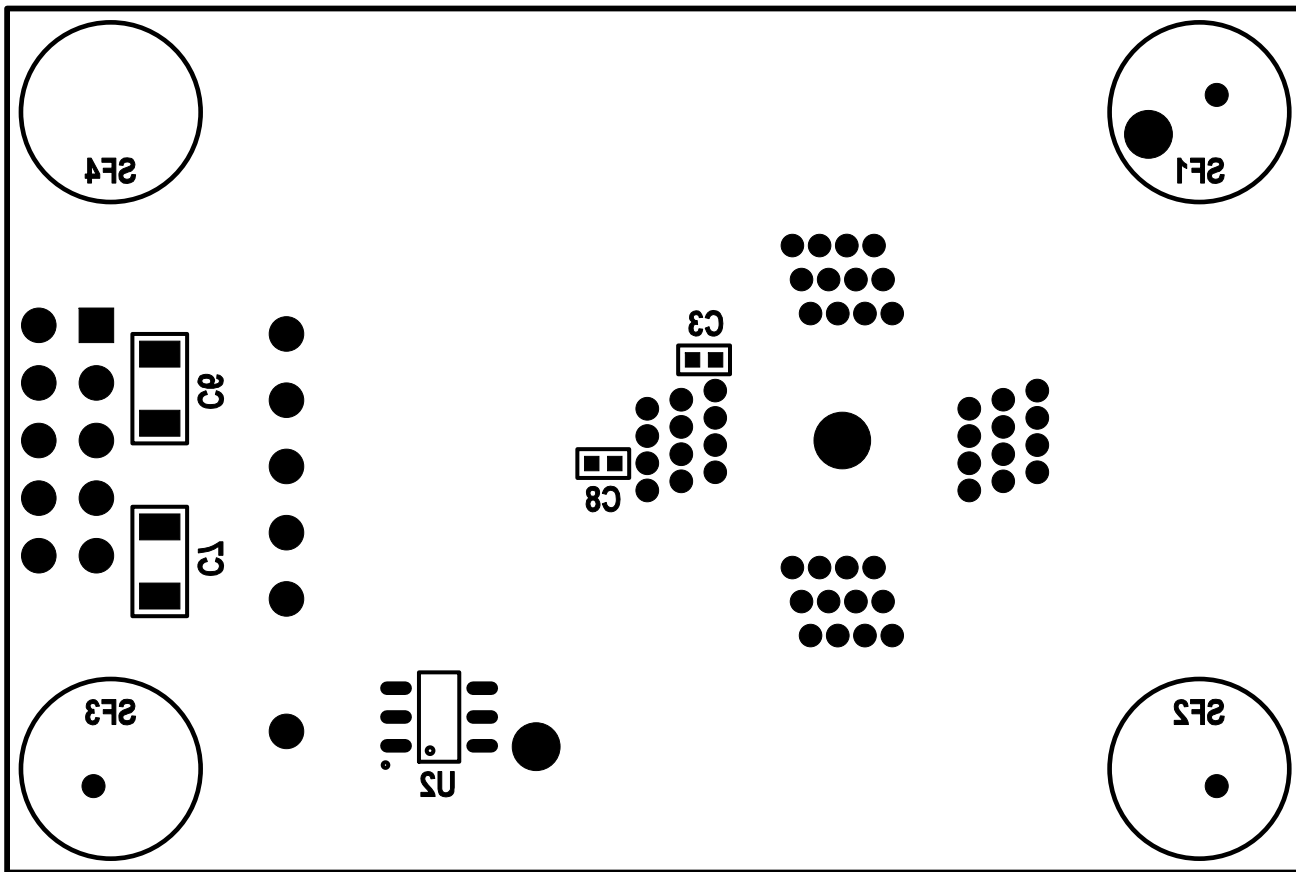
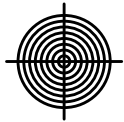
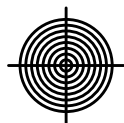
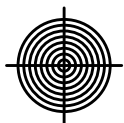


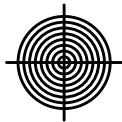
PRIMARY SILKSCREEN





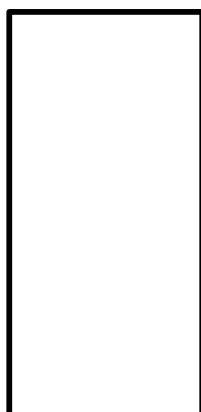
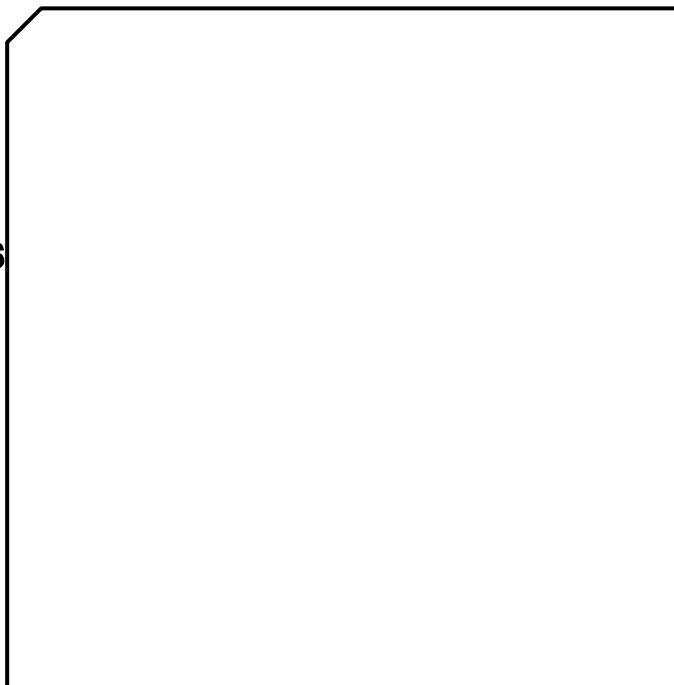
SECONDARY SILKSCREEN





SiLabs® 48-Pin Clock Gen SKT REV 1.0

U1



X1

GND

SCLK

SDA

○ TP2
VDDA_VDDS

○ TP8
SCLK

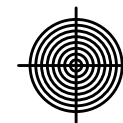
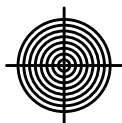
○ TP9
SDA

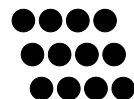
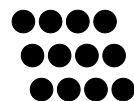
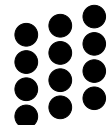
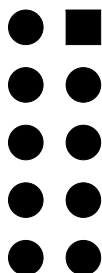
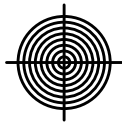
○ TP1
VDD

○ TP7
GND

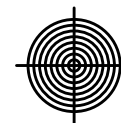
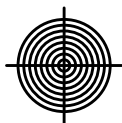
○ TP6
ID

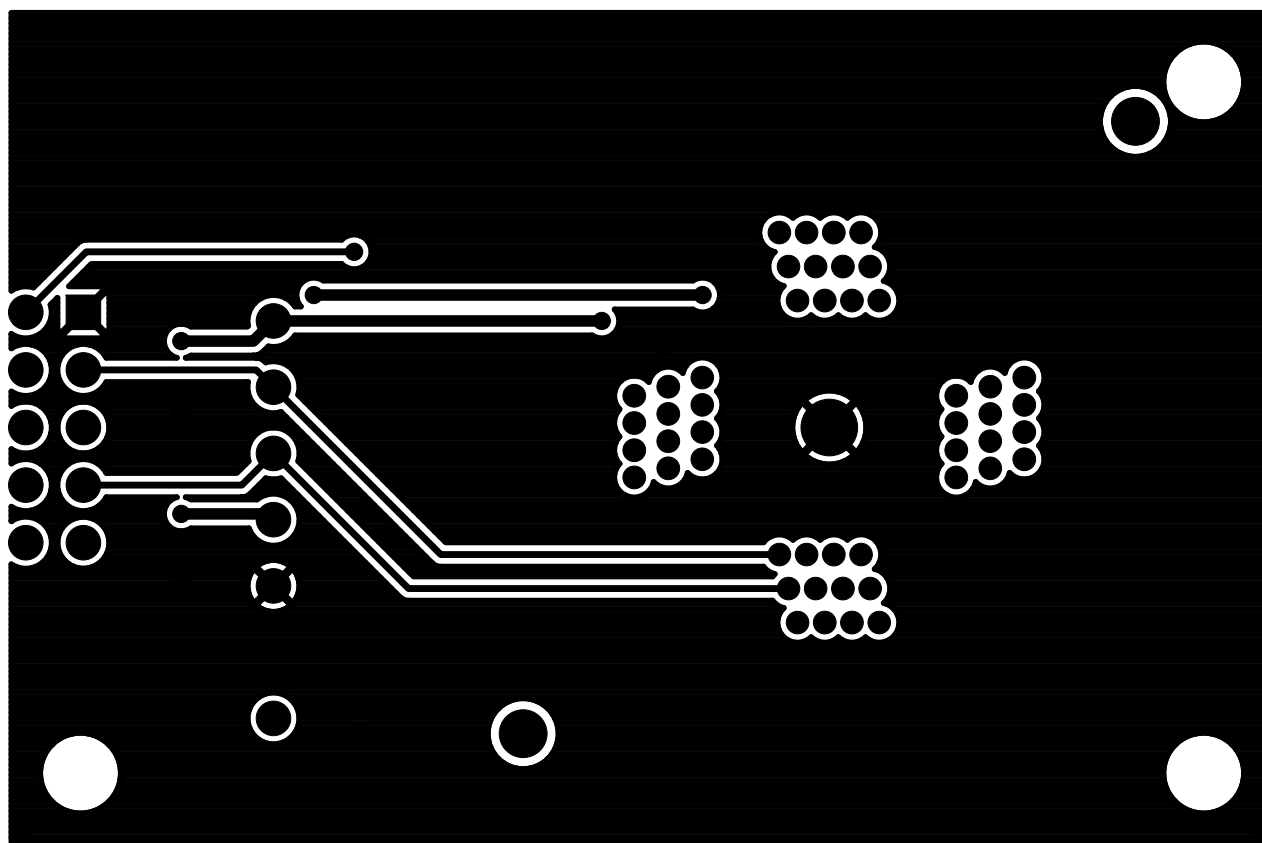
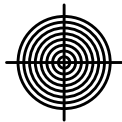
PRIMARY SILKSCREEN



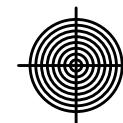
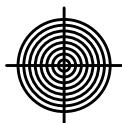


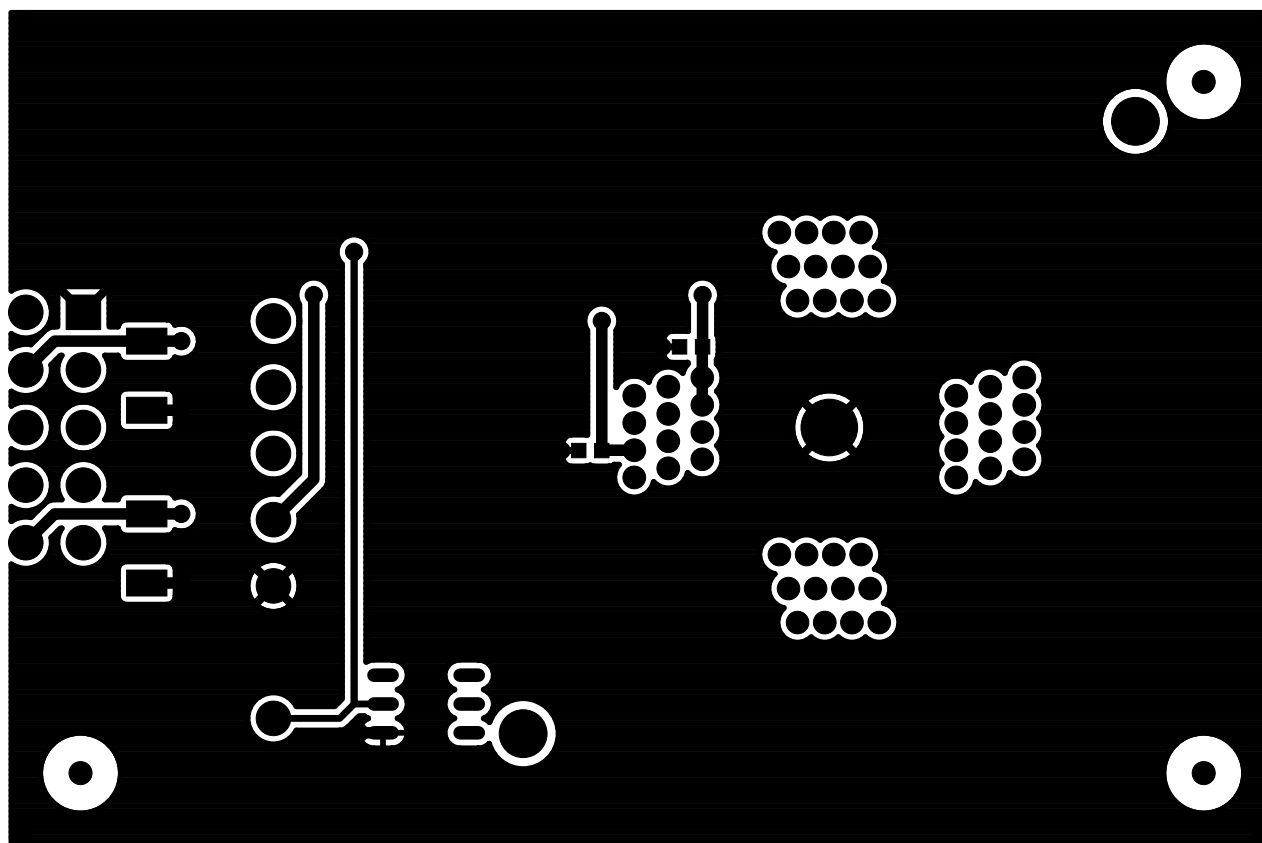
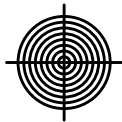
PRIMARY SOLDER MASK



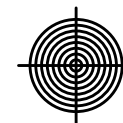
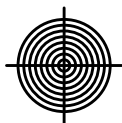


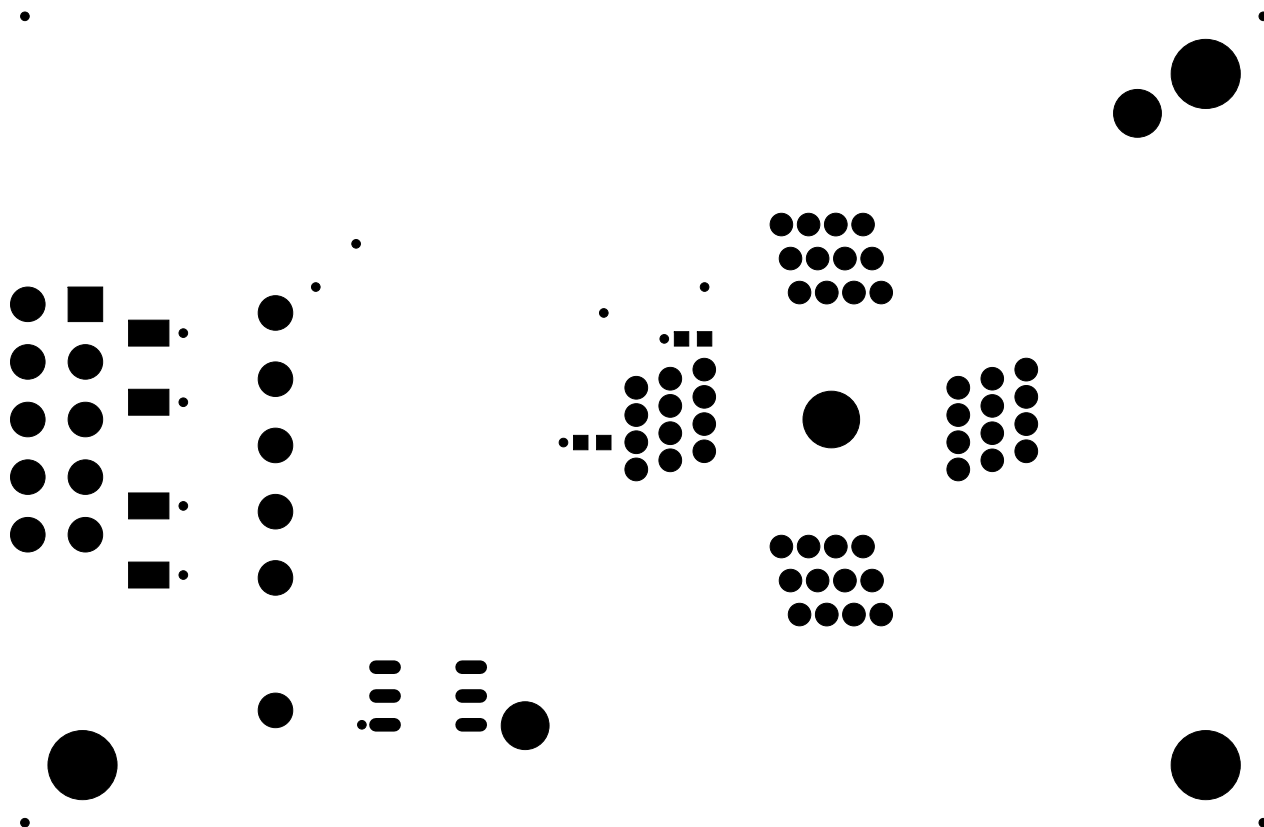
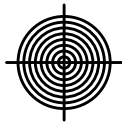
PRIMARY SIDE



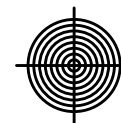
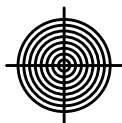


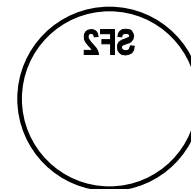
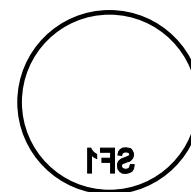
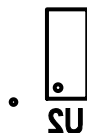
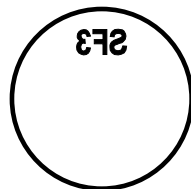
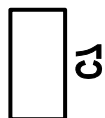
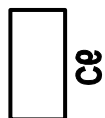
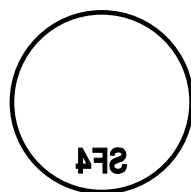
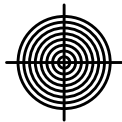
BOTTOM SIDE



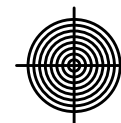
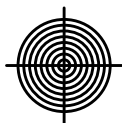


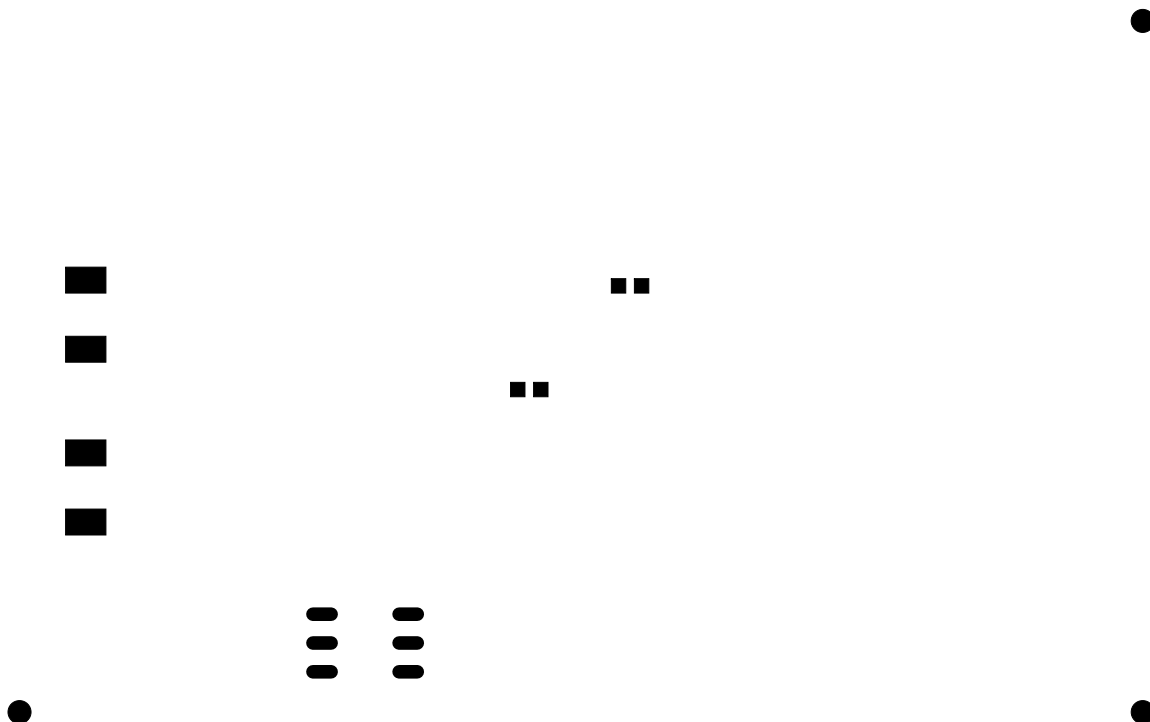
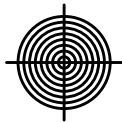
SECONDARY SOLDER MASK



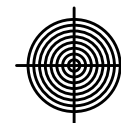
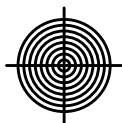


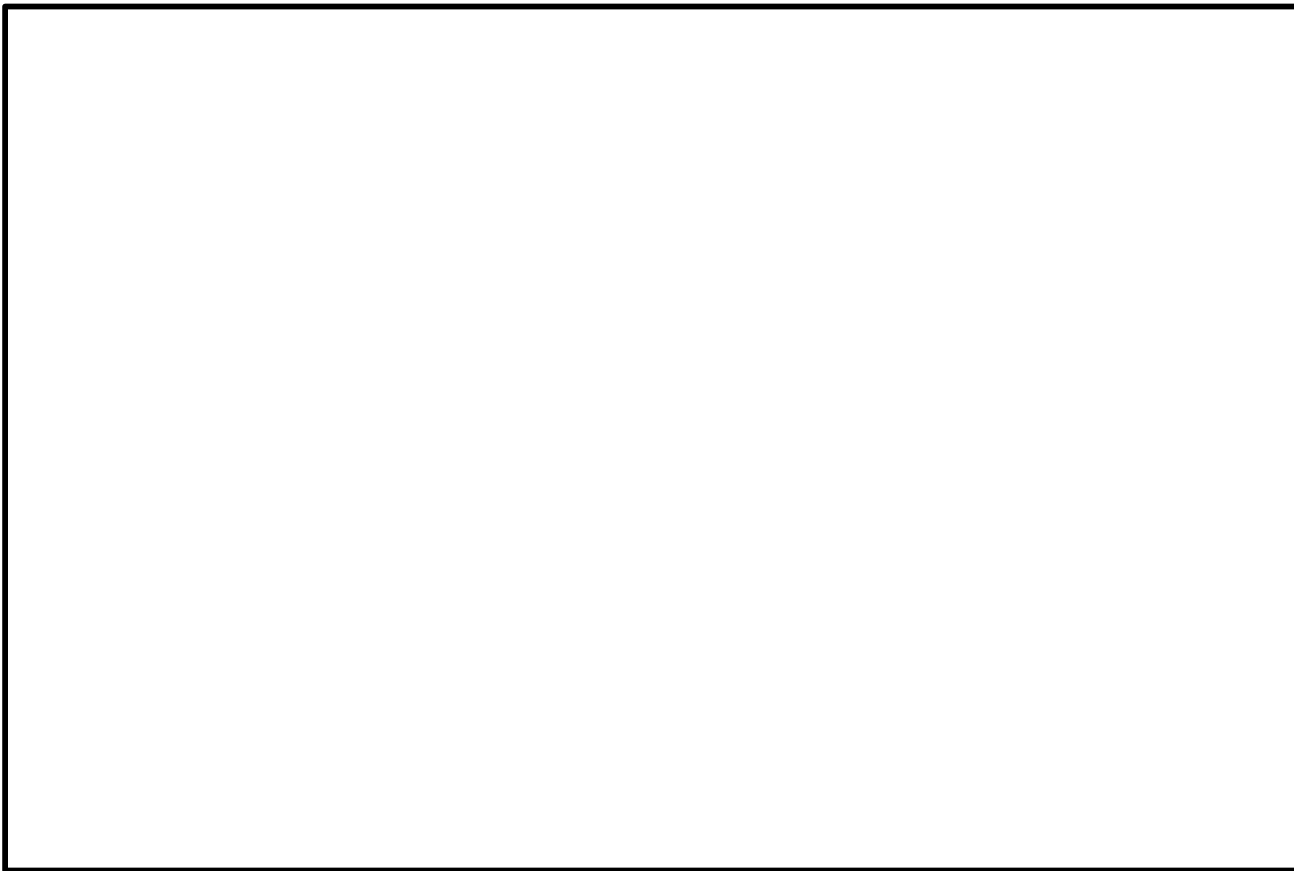
SECONDARY SILKSCREEN

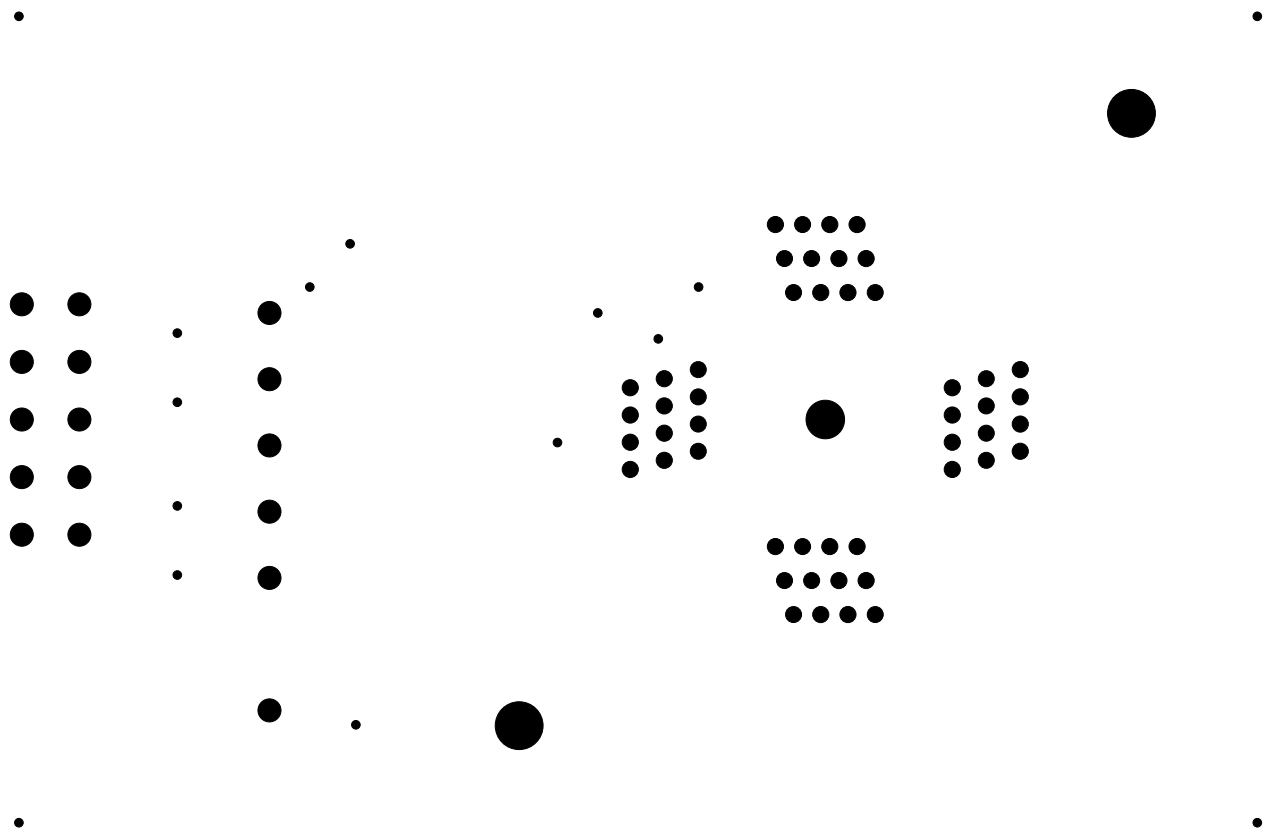




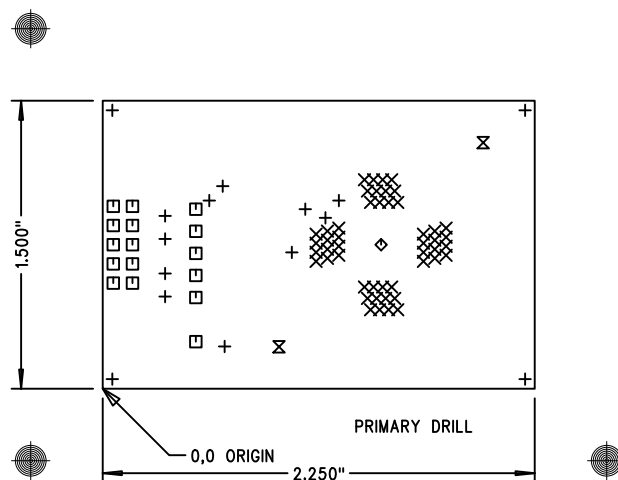
SECONDARY SOLDER PASTE








1. MANUFACTURE IN ACCORDANCE WITH IPC-6012, TYPE 3, CLASS 2.
2. END PRODUCT FEATURES SHALL NOT VARY MORE THAN 20% FROM ARTWORK ORIGINALS.
3. LAMINATE AND PREPREG SHALL BE AS PER IPC-4101/26,83,98 WITH A DECOMPOSITION TEMPERATURE $\geq 345^{\circ}\text{C}$, COLOR, NATURAL.
4. COPPER WEIGHT SHALL BE 1.0 OZ./SQ. FT. BEFORE PLATING.
5. ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF 0.001" COPPER.
6. DRILL HOLE TOLERANCE AFTER PLATING SHALL BE ± 0.003 ".
7. MINIMUM ANNULAR RING SHALL BE 0.001".
8. MINIMUM ANNULAR RING AT EMERGENT CONDUCTORS SHALL BE 0.003".
9. FINAL PCB THICKNESS SHALL BE $0.062" \pm 10\%$.
10. WARP/TWIST SHALL NOT EXCEED 1.0%
11. FINISH SHALL BE LPI, BLUE S.M.O.B.C., BALANCE ENIG.
12. SILKSCREEN WITH NONCONDUCTIVE WHITE EPOXY INK.
13. REFERENCE ADDITIONAL FAB NOTES IN FILE README.TXT

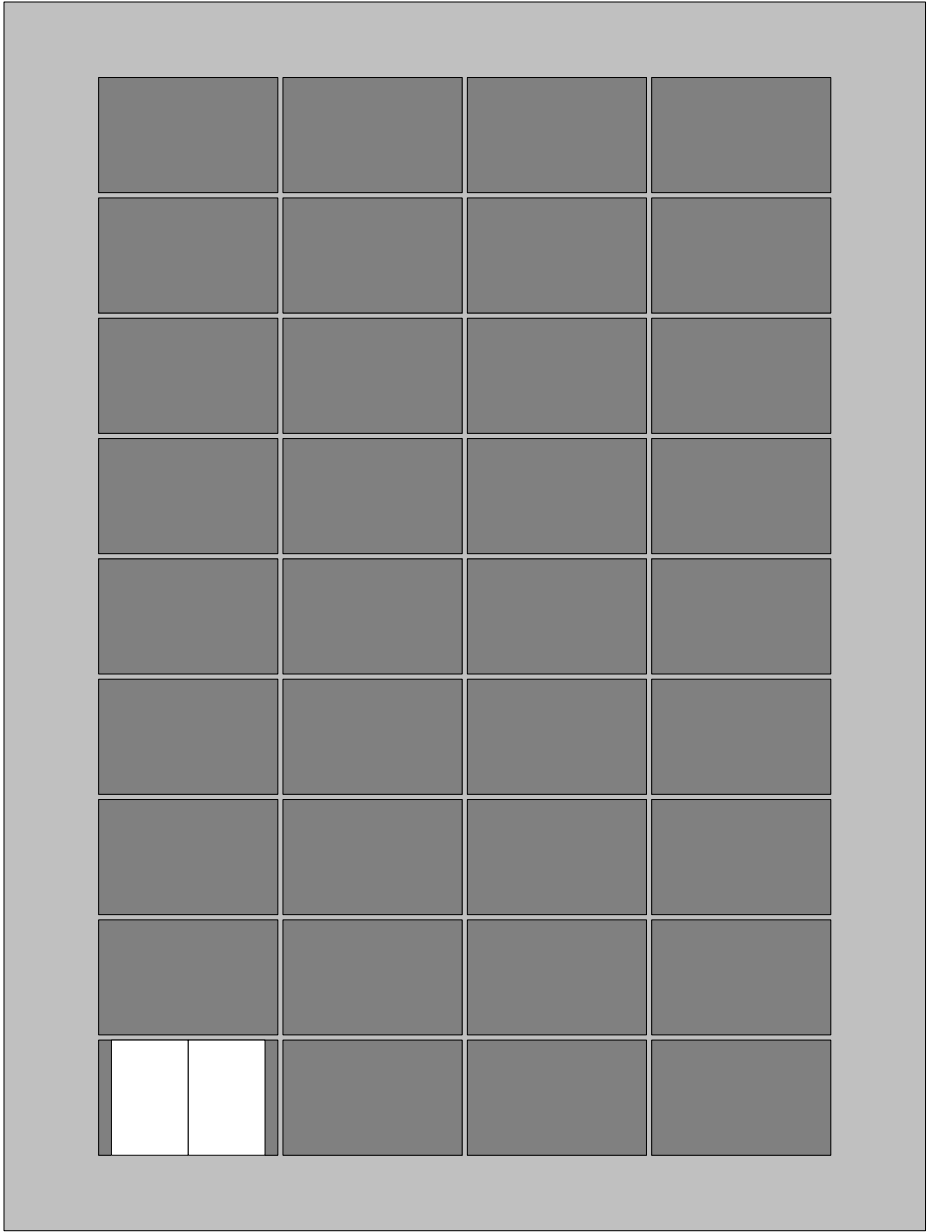


PRIMARY SILKSCREEN	5332-48SKT_PSS.PHO
PRIMARY SOLDERMASK	5332-48SKT_PSM.PHO
PRIMARY SIDE	5332-48SKT_PRI.PHO
SECONDARY SIDE	5332-48SKT_SEC.PHO
SECONDARY SOLDERMASK	5332-48SKT_SSM.PHO
SECONDARY SILKSCREEN	5332-48SKT_SSS.PHO

SCALE: NONE

SIZE	QTY	SYM	PLT	TOOL	TO
0.015	15	+	P	1	+0/-0.015
0.028	48	×	P	2	+/-0.002
0.040	16	□	P	3	+/-0.002
0.067	1	◇	P	4	+/-0.002
0.083	2	⊗	N	5	+/-0.002

UNLESS OTHERWISE SPECIFIED			THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART, WITHOUT THE WRITTEN CONSENT OF SILICON LABORATORIES, INC..			COMPANY: <div></div> <div>400 W Cesar Chavez AUSTIN, TX 78701 (512)416-8500 www.silabs.com</div>			
DIMENSIONS ARE IN INCHES AND APPLY AFTER FINISH DIMENSIONS IN BRACKETS [] ARE IN MILLIMETERS INTERPRET DRAWING PER MIL-D-1000									
TOLERANCES									
HOLE TOLERANCES PER 78027									
DECIMALS .XX +/- .XXX +/-	ANGLES +/-	SURFACES MICROINCHES ✓				NAME: Si5332-48SKT			REV 1.0
PART TO BE FREE OF BURRS			DESIGN	TT	31MAY2017	SIZE A	PART NUMBER:		
BREAK EDGES			LAYOUT	AA	31MAY2017	SCALE 1:1			FABRICATION DRAWING
BEND RADIUS			DO NOT SCALE DRAWING			SHEET 1 OF			
BEND RELIEF									



Si5332-48SKT Rev1.0

Size:

Panel: 18.0 x 24.0

Array: 3.5 x 2.25

Part: 1.5 x 2.25

Panel Yield:

36 Arrays of 2 Parts

72 Parts Total

65.6% Material Utilization

Matrix:

On Panel: 4 x 9, Origin: X1.85 Y1.475

On Array: 2 x 1

Spacing:

On Panel: 0.1 x 0.1

On Array: 0.0 x 0.0

Panel Borders:

Left: 1.85 Right: 1.85

Top: 1.475 Bottom: 1.475

Array Borders:

Left: 0.25 Right: 0.25

Top: 0.0 Bottom: 0.0

Notes:

Please add 4, 0.125" NP tooling holes located 0.125" from tab corners and 3, 40/120 fiduials to each side of array located 0.25" from tooling holes.