UCC2742x-Q1 Dual 4-A High-Speed Low-Side MOSFET Drivers With Enable

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C6
- Industry-Standard Pinout
- Enable Functions for Each Driver
- High-Current Drive Capability of ±4 A
- Unique Bipolar and CMOS True Drive Output Stage Provides High Current at MOSFET Miller Thresholds
- Inputs Independent of Supply Voltage Compatible With TTL and CMOS
- 20-ns Typical Rise and 15-ns Typical Fall Times With 1.8-nF Load
- Typical Propagation Delay Times of 25 ns With Input Falling and 35 ns With Input Rising
- 4-V to 15-V Supply Voltage
- Dual Outputs Can Be Paralleled for Higher Drive Current
- Available in Thermally Enhanced MSOP PowerPAD™ Package
- Rated From –40°C to +125°C

2 Applications

- Switch Mode Power Supplies
- DC-DC Converters
- Motor Controllers
- Line Drivers
- Class D Switching Amplifiers

3 Description

The UCC2742x-Q1 family of devices are high-speed dual MOSFET drivers capable of delivering large peak currents into capacitive loads. Two standard logic options are offered: dual inverting and dual noninverting drivers. They are offered in the standard 8-pin SOIC (D) package. The thermally enhanced 8-pin PowerPAD Package MSOP package (DGN) drastically lowers the thermal resistance to improve long-term reliability.

Using a design that inherently minimizes shoot-through current, these drivers deliver 4-A current where it is needed most, at the Miller plateau region, during the MOSFET switching transition. A unique bipolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing and sinking at low supply voltages.

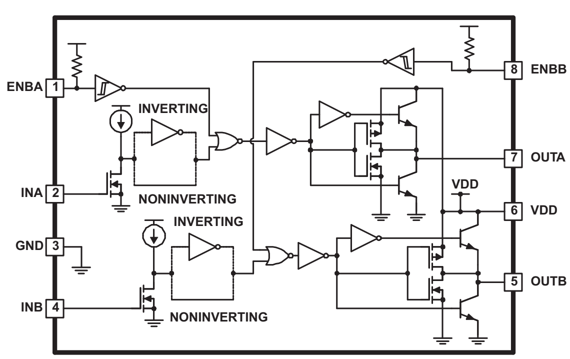
The UCC2742x-Q1 provide enable (ENBL) functions to have better control of the operation of the driver applications. ENBA and ENBB are implemented on pins 1 and 8, which were previously left unused in the industry standard pinout. They are internally pulled up to V_{DD} for active-high logic and can be left open for standard operation.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC2742x-Q1	SOIC (8)	4.90 mm × 3.91 mm
	MSOP With PowerPAD (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (May 2016) to Revision H	Page
• Changed the UCC27424-Q1 pinout drawing to show two, noninverting channels	4
• Changed the units of the capacitors in the *Parallel Outputs* figure from mF to µF	15
• Added the *Receiving Notification of Documentation Updates* section	23

Changes from Revision F (September 2012) to Revision G	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Added MSOP package information to *Features* and *Description* sections	1

Changes from Revision E (July, 2012) to Revision F	Page
• Changed the word terminal to pin per new standards	4
• Removed derating factor column in dissipation ratings table, and changed the θ_{JC} value from 4.7 to 11.9, the θ_{JA} value from 50–59 to 63, and the power rating T_A = 70°C (mW) value from 1370 to 873 for the DGN package.	8

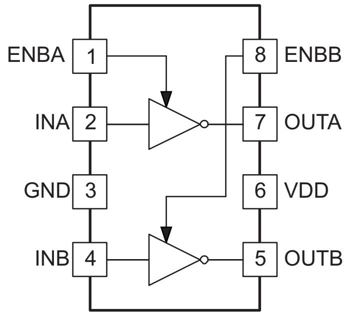
5 Device Comparison Table(1)(2)

T_A	CONFIGURATION	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	Dual Inverting	UCC27423QDGNRQ1	EADQ
	Dual Noninverting	UCC27424QDGNRQ1	EPJQ
	Dual Inverting	UCC27423QDRQ1	27423Q
	Dual Noninverting	UCC27424QDRQ1	27424Q
	One Inverting, One Noninverting	UCC27425QDRQ1	27425Q

(1) For the most current package and ordering information, see *Mechanical, Packaging, and Orderable Information*, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

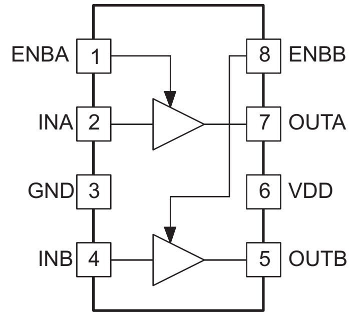
6 Pin Configuration and Functions

**UCC27423-Q1: D or DGN Package
8-Pin SOIC or MSOP With PowerPAD
Top View**



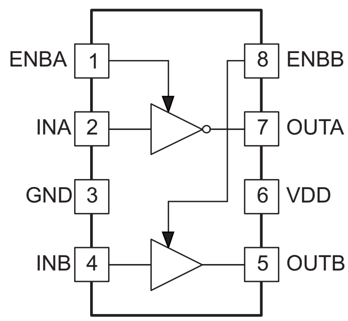
Dual Inverting

**UCC27424-Q1: D or DGN Package
8-Pin SOIC or MSOP With PowerPAD
Top View**



Dual Noninverting

**UCC27425-Q1: D or Package
8-Pin SOIC
Top View**



One inverting, one noninverting

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	ENBA	I	Enable input for the driver A with logic-compatible threshold and hysteresis. The driver output can be enabled and disabled with this pin. It is internally pulled up to V_{DD} with 100-kΩ resistor for active high operation. The output state when the device is disabled is low, regardless of the input state.
2	INA	I	Input A. Input signal of the A driver which has logic-compatible threshold and hysteresis. If not used, this input must be tied to either V_{DD} or GND. It must not be left floating.
3	GND	—	Common ground. This ground must be connected very closely to the source of the power MOSFET which the driver is driving.
4	INB	I	Input B. Input signal of the A driver which has logic-compatible threshold and hysteresis. If not used, this input must be tied to either V_{DD} or GND. It must not be left floating.
5	OUTB	O	Driver output B. The output stage is capable of providing 4-A drive current to the gate of a power MOSFET.
6	VDD	—	Supply voltage and the power input connection for this device.
7	OUTA	O	Driver output A. The output stage is capable of providing 4-A drive current to the gate of a power MOSFET.
8	ENBB	I	Enable input for the driver B with logic-compatible threshold and hysteresis. The driver output can be enabled and disabled with this pin. It is internally pulled up to V_{DD} with 100-kΩ resistor for active-high operation. The output state when the device is disabled is low, regardless of the input state.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
V_{DD}	Supply voltage		–0.3	16	V
I_{OUT}	Output current	DC		0.3	A
		Pulsed, 0.5 µs		4.5	
V_{IN}	Input voltage	INA, INB	–5	6(3) or (V_{DD} + 0.3)(3)	V
V_{EN}	Enable voltage	ENBA, ENBB	–0.3	6(3) or (V_{DD} + 0.3)(3)	V
P_D	Power dissipation	T_A = 25°C (D package)		650	mW
		T_A = 25°C (DGN package)		3	W
T_J	Junction operating temperature		–55	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into, negative out of, the specified terminal.
(3) Whichever is larger.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	4	15	V
INA	Input voltage	–2	15	V
INB				
ENA	Enable voltage	0	15	V
ENB				
T_J	Operating junction temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		UCC2742x-Q1		UNIT
		D (SOIC)	DGN (MSOP With PowerPAD)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.6	63	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.5	53.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.8	35.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.8	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.3	35.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	11.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

V_{DD} = 4.5 V to 15 V, T_A = –40°C to 125°C, $T_A = T_J$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT (INA, INB)						
V_{IH}	Logic 1 input threshold		2			V
V_{IL}	Logic 0 input threshold				1	V
I_{IN}	Input current	V_{IN} = 0 V to V_{DD}	–10	0	10	µA
OUTPUT (OUTA, OUTB)						
I_{OUT}	Output current	V_{DD} = 14 V (1) (2)		4		A
V_{OH}	High-level output voltage	$V_{OH} = V_{DD} – V_{OUT}$, I_{OUT} = –10 mA, V_{DD} = 14 V		330	450	mV
V_{OL}	Low-level output voltage	I_{OUT} = 10 mA, V_{DD} = 14 V		22	40	mV
R_{OH}	Output resistance high	T_A = 25°C, I_{OUT} = –10 mA, V_{DD} = 14 V (3)	25	30	35	Ω
		T_A = full range, I_{OUT} = –10 mA, V_{DD} = 14 V (3)	18		45	
R_{OL}	Output resistance low	T_A = 25°C, I_{OUT} = 10 mA, V_{DD} = 14 V (3)	1.9	2.2	2.5	Ω
		T_A = full range, I_{OUT} = 10 mA, V_{DD} = 14 V (3)	1.2		4	
	Latch-up protection (1)		500			mA
ENABLE (ENBA, ENBB)						
V_{IN_H}	High-level input voltage	Low-to-high transition	1.7	2.4	2.9	V
V_{IN_L}	Low-level input voltage	High-to-low transition	1.1	1.8	2.2	V
	Hysteresis		0.15	0.55	0.9	V
R_{ENBL}	Enable impedance	V_{DD} = 14 V, ENBL = GND	75	100	145	kΩ
OVERALL						
I_{DD}	Operating current	Static, V_{DD} = 15 V, ENBA = ENBB = 15 V; UCC27423-Q1; INA = 0 V; INB = 0 V		900	1350	µA
		Static; UCC27423-Q1; INA = 0 V; INB = High		750	1100	
		Static; UCC27423-Q1; INA = High; INB = 0 V		750	1100	
		Static; UCC27423-Q1; INA = High; INB = High		600	900	
		Static; UCC27424-Q1; INA = 0 V; INB = 0 V		300	450	
		Static; UCC27424-Q1; INA = 0 V; INB = High		750	1100	
		Static; UCC27424-Q1; INA = High; INB = 0 V		750	1100	
		Static; UCC27424-Q1; INA = High; INB = High		1200	1800	
		Static; UCC27425-Q1; INA = 0 V; INB = 0 V		600	900	
		Static; UCC27425-Q1; INA = 0 V; INB = High		1050	1600	
		Static; UCC27425-Q1; INA = High; INB = 0 V		450	700	
		Static; UCC27425-Q1; INA = High; INB = High		900	1350	
		Disabled, V_{DD} = 15 V, ENBA = ENBB = 0 V; All; INA = 0 V; INB = 0 V		300	450	
		Disabled; All; INA = 0 V; INB = High		450	700	
		Disabled; All; INA = High; INB = 0 V		450	700	
		Disabled; All; INA = High; INB = High		600	900	

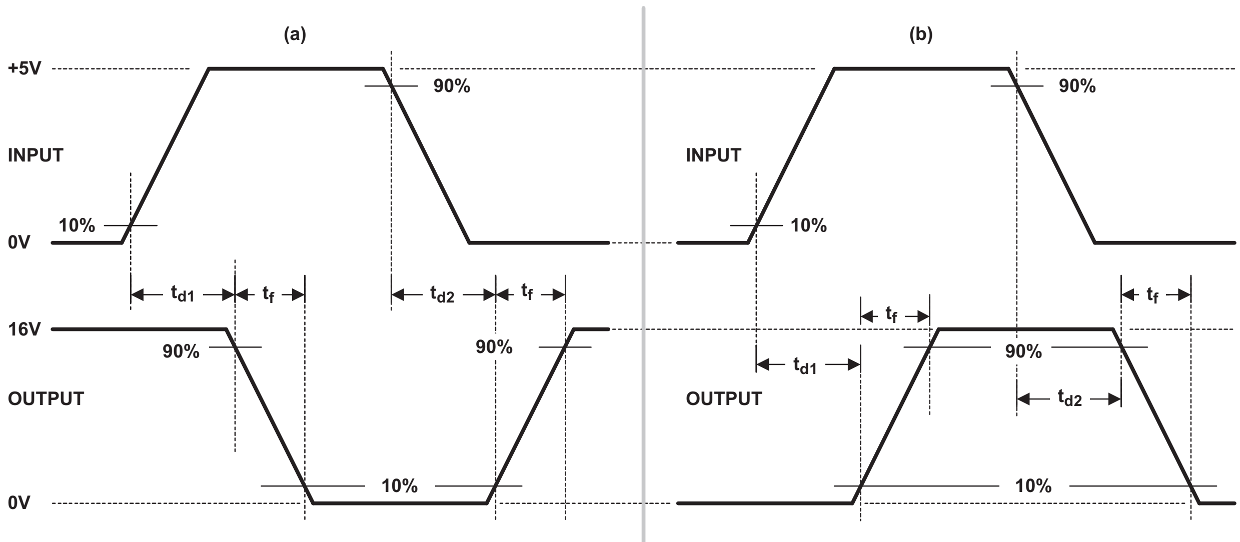
(1) Specified by design
(2) The pullup and pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The pulsed output current rating is the combined current from the bipolar and MOSFET transistors.
(3) The pullup and pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The output resistance is the $R_{DS(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

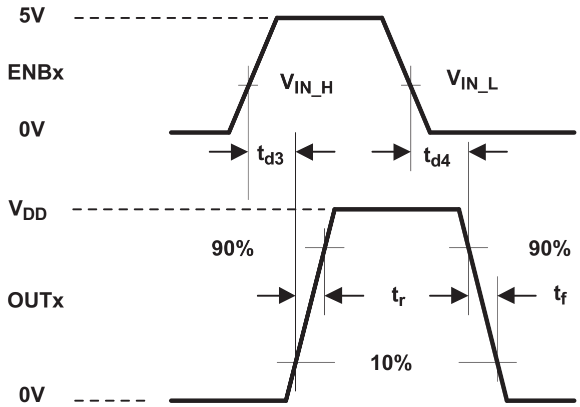
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SWITCHING TIME							
t_r	Rise time (OUTA, OUTB)	C_{LOAD} = 1.8 nF(1)			20	40	ns
t_f	Fall time (OUTA, OUTB)	C_{LOAD} = 1.8 nF(1)			15	40	ns
t_{D1}	Delay time, IN rising (IN to OUT)	C_{LOAD} = 1.8 nF(1)			25	50	ns
t_{D2}	Delay time, IN falling (IN to OUT)	C_{LOAD} = 1.8 nF(1)	UCC27423-Q1, UCC27424-Q1		35	60	ns
			UCC27425-Q1		35	70	
ENABLE (ENBA, ENBB)							
t_{D3}	Propagation delay time(2)	C_{LOAD} = 1.8 nF(1)(3)			30	60	ns
t_{D4}	Propagation delay time(2)	C_{LOAD} = 1.8 nF(1)(3)			100	150	ns

(1) Specified by design
(2) See Figure 2
(3) Not production tested



The 10% and 90% thresholds depict the dynamics of the bipolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

Figure 1. Switching Waveforms for (a) Inverting Driver and (b) Noninverting Driver



The 10% and 90% thresholds depict the dynamics of the bipolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

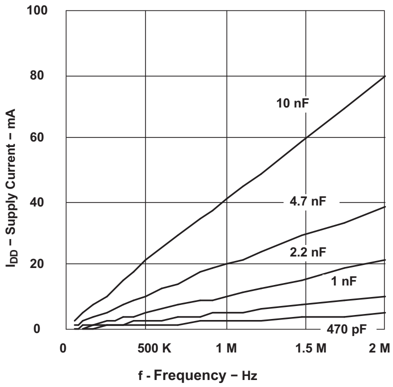
Figure 2. Switching Waveform for Enable to Output

7.7 Dissipation Ratings

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	POWER RATING T_A = 70°C (mW)(1)
D (SOIC-8)	42	84 to 160(2)	344 to 655(2)
DGN (MSOP PowerPAD)(3)	11.9	63	873

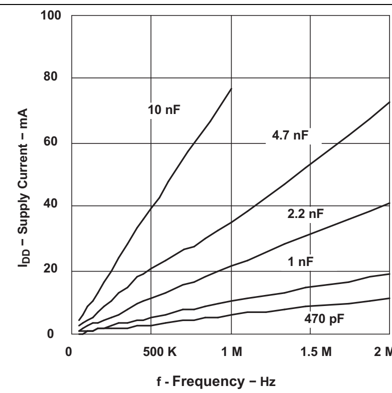
(1) 125°C operating junction temperature is used for power rating calculations.
(2) The range of values indicates the effect of the PCB. These values are intended to give the system designer an indication of the best- and worst-case conditions. In general, the system designer should attempt to use larger traces on the PCB, where possible, to spread the heat away form the device more effectively.
(3) The PowerPAD is not directly connected to any leads of the package. However, it is electronically and thermally connected to the substrate which is the ground of the device.

7.8 Typical Characteristics



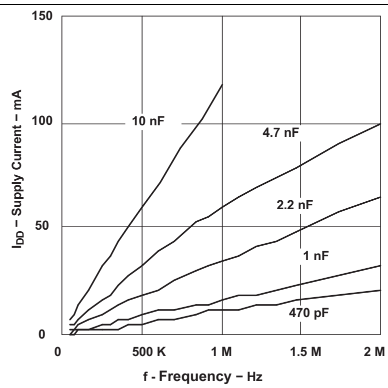
V_{DD} = 4.5 V

Figure 3. Supply Current vs Frequency



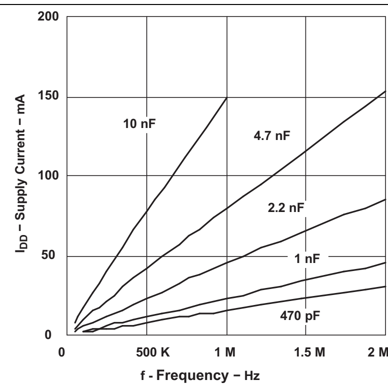
V_{DD} = 8 V

Figure 4. Supply Current vs Frequency



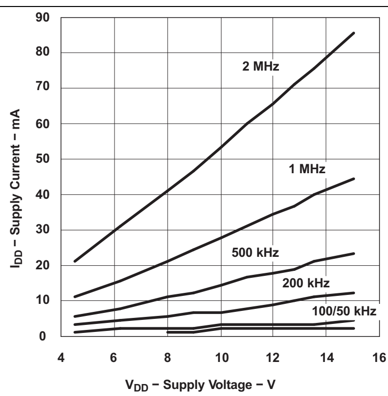
V_{DD} = 12 V

Figure 5. Supply Current vs Frequency



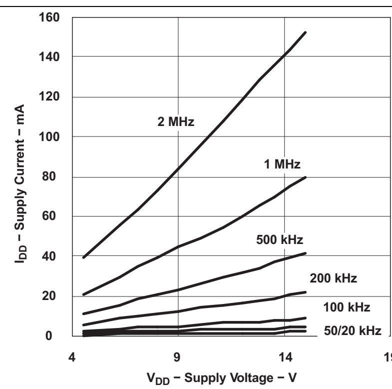
V_{DD} = 15 V

Figure 6. Supply Current vs Frequency



C_{LOAD} = 2.2 nF

Figure 7. Supply Current vs Supply Voltage



C_{LOAD} = 4.7 nF

Figure 8. Supply Current vs Supply Voltage

Typical Characteristics (continued)

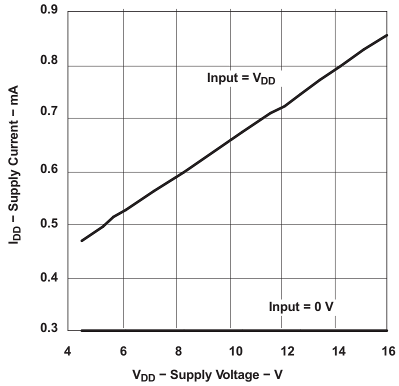


Figure 9. Supply Current vs Supply Voltage (UCC274323)

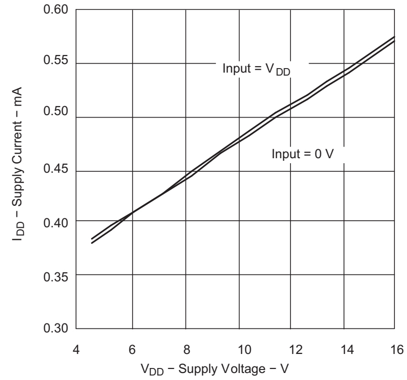


Figure 10. Supply Current vs Supply Voltage (UCC27424)

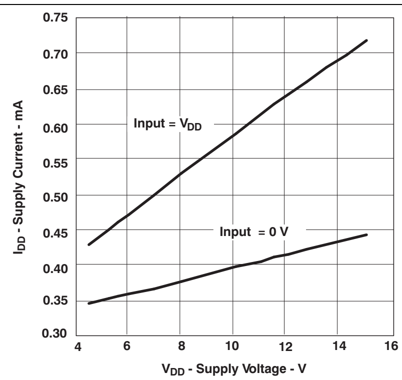


Figure 11. Supply Current vs Supply Voltage (UCC27425-Q1)

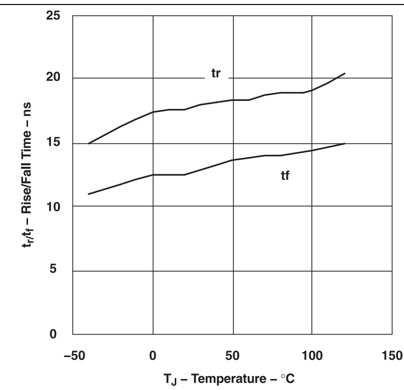


Figure 12. Rise Time and Fall Time Temperature (UCC27423)

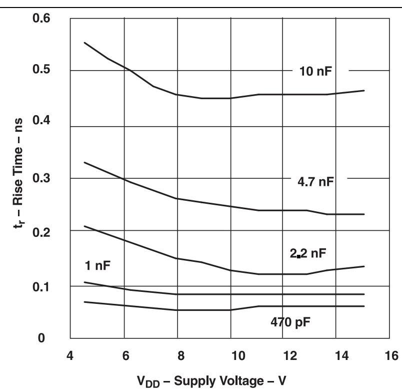


Figure 13. Rise Time vs Supply Voltage

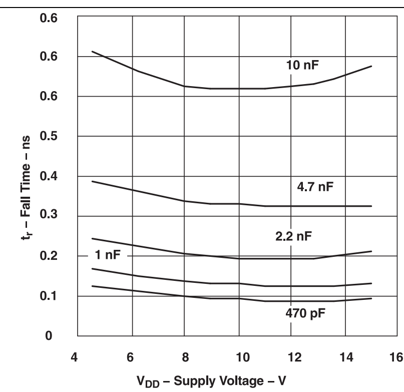


Figure 14. Fall Time vs Supply Voltage

Typical Characteristics (continued)

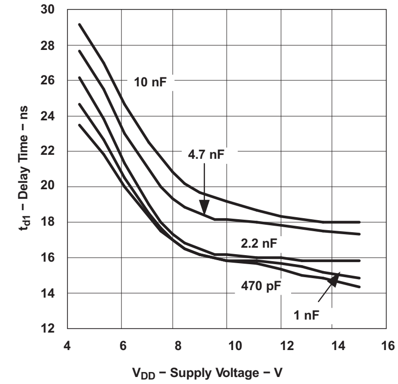


Figure 15. Delay Time (t_D1) vs Supply Voltage (UCC27423)

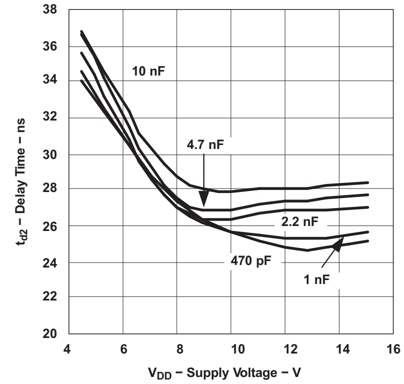


Figure 16. Delay Time (t_D2) vs Supply Voltage (UCC27423)

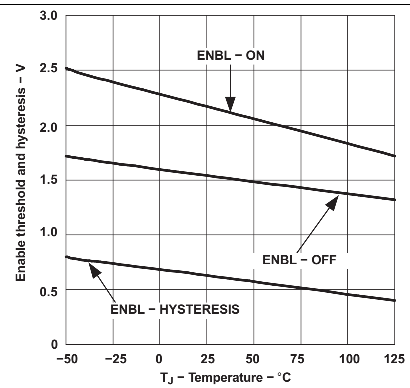


Figure 17. Enable Threshold and Hysteresis vs Temperature

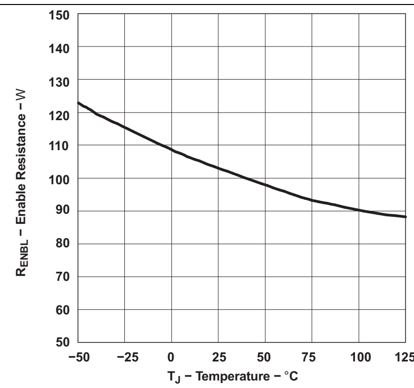


Figure 18. Enable Resistance vs Temperature

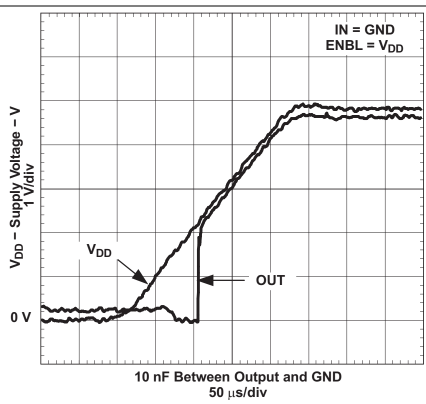


Figure 19. Output Behavior vs Supply Voltage (Inverting)

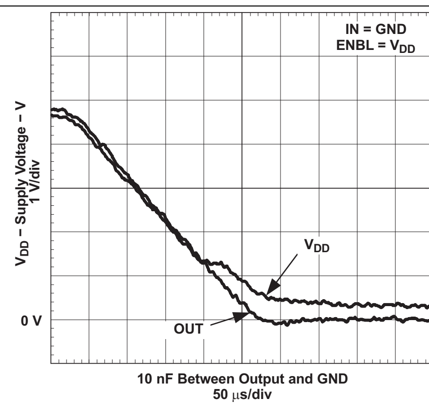


Figure 20. Output Behavior vs Supply Voltage (Inverting)

Typical Characteristics (continued)

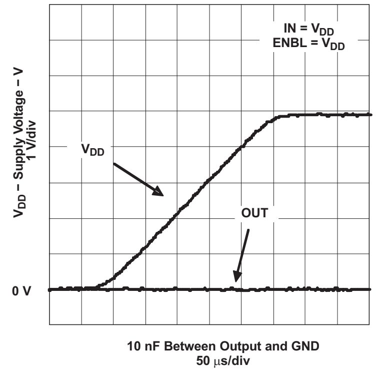


Figure 21. Output Behavior vs VDD (Inverting)

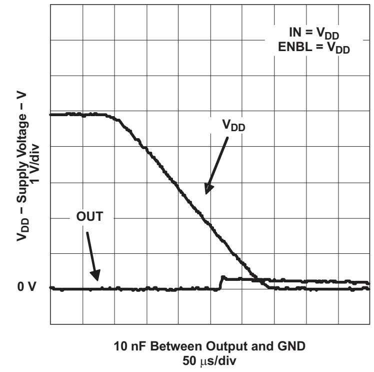


Figure 22. Output Behavior vs VDD (Inverting)

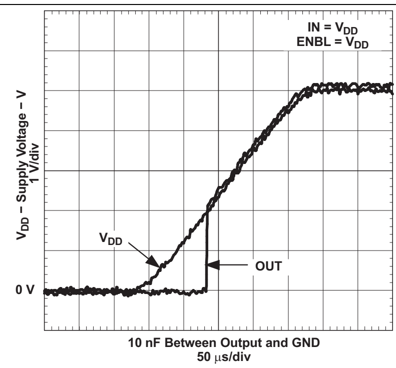


Figure 23. Output Behavior vs VDD (Noninverting)

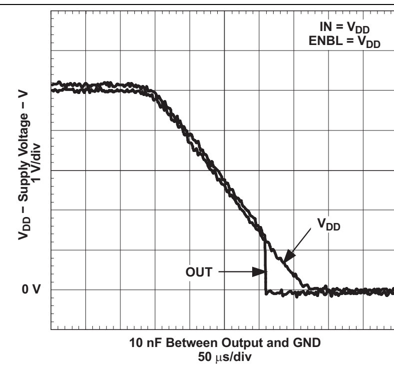


Figure 24. Output Behavior vs VDD (Noninverting)

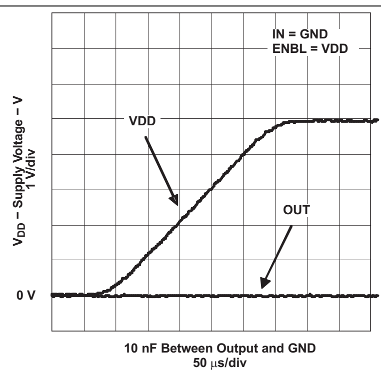


Figure 25. Output Behavior vs VDD (Noninverting)

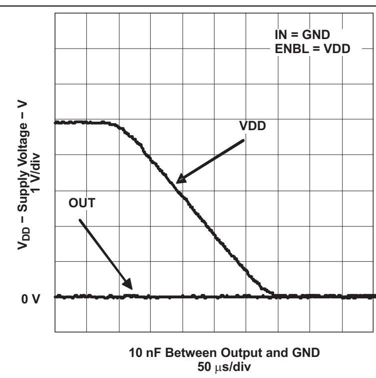


Figure 26. Output Behavior vs VDD (Noninverting)

Typical Characteristics (continued)

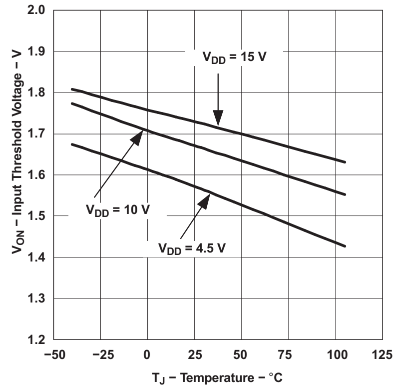


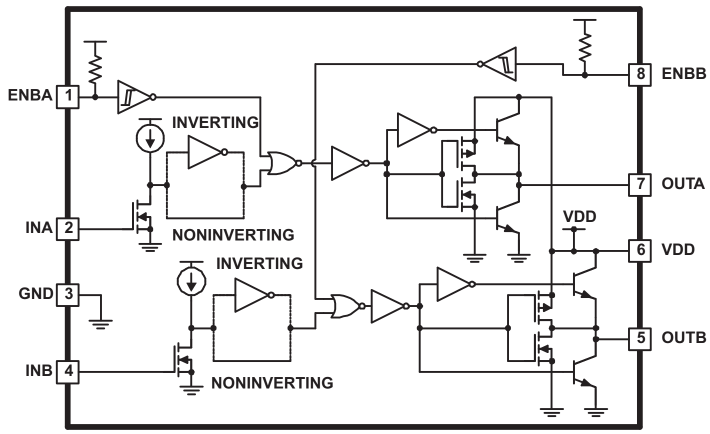
Figure 27. Input Threshold vs Temperature

8 Detailed Description

8.1 Overview

The UCC2742x-Q1 family of high-speed dual MOSFET drivers can deliver large peak currents into capacitive loads. The UCC27423-Q1 offers these standard logic options: dual-inverting drivers, dual noninverting drivers, and one inverting, one noninverting driver. The thermally enhanced 8-pin PowerPAD MSOP package (DGN) drastically lowers the thermal resistance to improve long-term reliability. It is also offered in the standard 8-pin SOIC (D) package. Using a design that inherently minimizes shoot-through current, these drivers deliver 4 A of current where it is needed most at the Miller plateau region during the MOSFET switching transition. A unique Bipolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing and sinking at low supply voltages.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Stage

The input thresholds have a 3.3-V logic sensitivity over the full range of V_{DD} voltages; yet it is equally compatible with 0 to V_{DD} signals. The inputs of UCC2742x-Q1 drivers are designed to withstand 500-mA reverse current without either damage to the IC for logic upset. The input stage of each driver must be driven by a signal with a short rise or fall time. This condition is satisfied in typical power supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition times (< 200 ns). The input stages to the drivers function as a digital gate, and they are not intended for applications where a slow changing input voltage is used to generate a switching output when the logic threshold of the input section is reached. While this may not be harmful to the driver, the output of the driver may switch repeatedly at a high frequency.

Users should not attempt to shape the input signals to the driver in an attempt to slow down (or delay) the signal at the output. If limiting the rise or fall times to the power device is desired, limit the rise or fall times to the power device, then an external resistance can be added between the output of the driver and the load device, which is generally a power MOSFET gate. The external resistor may also help remove power dissipation from the device package, as discussed in the *Thermal Considerations* section.

8.3.2 Output Stage

Inverting outputs of the UCC2742x-Q1 are intended to drive external P-channel MOSFETs. Noninverting outputs of the UCC2742x-Q1 are intended to drive external N-channel MOSFETs.

Feature Description (continued)

Each output stage is capable of supplying ±4-A peak current pulses and swings to both V_{DD} and GND. The pullup and pulldown circuits of the driver are constructed of bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{DS(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor. Each output stage also provides a very low impedance to overshoot and undershoot due to the body diode of the external MOSFET. This means that in many cases, external Schottky-clamp diodes are not required.

The UCC2742x-Q1 family delivers the 4-A gate drive where it is most needed during the MOSFET switching transition—at the Miller plateau region—providing improved efficiency gains. A unique bipolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing at low supply voltages.

8.3.3 Enable

UCC2742x-Q1 provide dual enable inputs for improved control of each driver channel operation. The inputs incorporate logic-compatible thresholds with hysteresis. They are internally pulled up to V_{DD} with 100-kΩ resistor for active-high operation. When ENBA and ENBB are driven high, the drivers are enabled; when ENBA and ENBB are low, the drivers are disabled. The default state of the enable pin is to enable the driver and, therefore, can be left open for standard operation. The output states when the drivers are disabled is low, regardless of the input state. See Table 1 for operation using enable logic.

Enable inputs are compatible with both logic signals and slowly-changing analog signals. They can be directly driven, or a power-up delay can be programmed with a capacitor between ENBA/ENBB and GND. ENBA and ENBB control input A and input B, respectively.

8.3.4 Parallel Outputs

The A and B drivers may be combined into a single driver by connecting the INA/INB inputs together and the OUTA/OUTB outputs together. Then, a single signal can control the paralleled combination as shown in Figure 28.

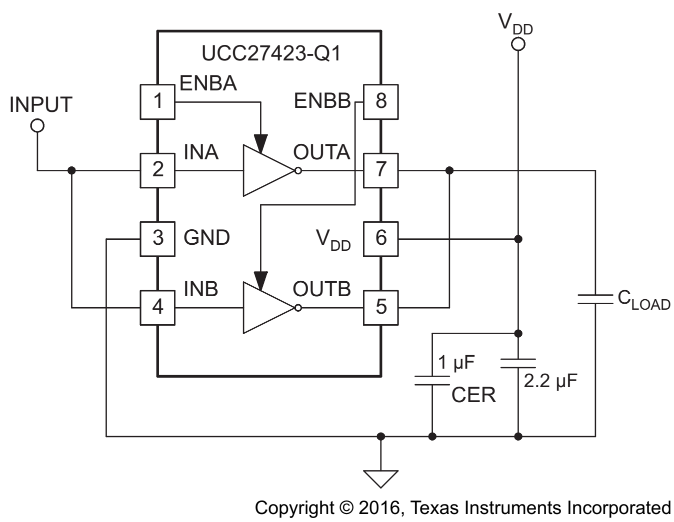


Figure 28. Parallel Outputs

8.3.5 Operational Waveforms and Circuit Layout

Figure 29 shows the circuit performance achievable with a single driver (half of the 8-pin IC) driving a 10-nF load. The input pulse width (not shown) is set to 300 ns to show both transitions in the output waveform. Note the linear rise and fall edges of the switching waveforms. This is due to the constant output current characteristic of the driver as opposed to the resistive output impedance of traditional MOSFET-based gate drivers.

Feature Description (continued)

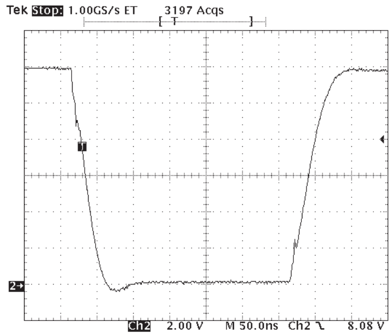


Figure 29. Pulse Response

In a power driver operating at high frequency, it is a significant challenge to get clean waveforms without much overshoot or undershoot and ringing. The low output impedance of these drivers produces waveforms with high di/dt. This tends to induce ringing in the parasitic inductances. Use the upmost care in the circuit layout. It is advantageous to connect the driver IC as close as possible to the leads. The driver IC layout has ground on the opposite side of the output, so the ground must be connected to the bypass capacitors and the load with copper trace as wide as possible. These connections must also be made with a small enclosed loop area to minimize the inductance.

8.3.6 V_{DD}

Although quiescent V_{DD} current is very low, total supply current is higher, depending on OUTA and OUTB current and the programmed oscillator frequency. Total V_{DD} current is the sum of quiescent V_{DD} current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUT current can be calculated from Equation 1.

$$I_{OUT} = Q_g \times f$$

where

- f is frequency (1)

For the best high-speed circuit performance, TI recommends two V_{DD} bypass capacitors to prevent noise problems. TI highly recommends using surface-mount components. A 0.1-µF ceramic capacitor must be located closest to the V_{DD} to ground connection. In addition, a larger capacitor (such as 1 µF) with relatively low ESR must be connected in parallel, to help deliver the high current peaks to the load. The parallel combination of capacitors must present a low impedance characteristic for the expected current levels in the driver application.

8.4 Device Functional Modes

With V_{DD} power supply in the range of 4 V to 16 V, the output stage is dependent on the states of the HI and LI pins. Table 1 shows the UCC2742x-Q1 truth table.

Table 1. Input and Output Logic Table

ENBA	ENBB	INPUTS (V_{IN_L}, V_{IN_H})		UCC27423-Q1		UCC27424-Q1		UCC27425-Q1	
		INA	INB	OUTA	OUTB	OUTA	OUTB	OUTA	OUTB
H	H	L	L	H	H	L	L	H	L
H	H	L	H	H	L	L	H	H	H
H	H	H	L	L	H	H	L	L	L
H	H	H	H	L	L	H	H	L	H
L	L	X	X	L	L	L	L	L	L

Importantly, if INA and INB are not used, they must be tied to either VDD or GND; they must not be left floating.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

High-frequency power supplies often require high-speed, high-current drivers such as the UCC2742x-Q1 family. A leading application is the need to provide a high-power buffer stage between the PWM output of the control IC and the gates of the primary power MOSFET or IGBT switching devices. In other cases, the driver IC is used to drive the power device gates through a drive transformer. Synchronous rectification supplies also have the need to simultaneously drive multiple devices which can present an extremely large load to the control circuitry.

Driver ICs are used when it is not feasible to have the primary PWM regulator IC directly drive the switching devices for one or more reasons. The PWM IC may not have the brute drive capability required for the intended switching MOSFET, limiting the switching performance in the application. In other cases, there may be a desire to minimize the effect of high-frequency switching noise by placing the high current driver physically close to the load. Also, newer ICs that target the highest operating frequencies may not incorporate onboard gate drivers at all. Their PWM outputs are only intended to drive the high impedance input to a driver such as the UCC2742x-Q1. Finally, the control IC may be under thermal stress due to power dissipation, and an external driver can help by moving the heat from the controller to an external package.

9.2 Typical Application

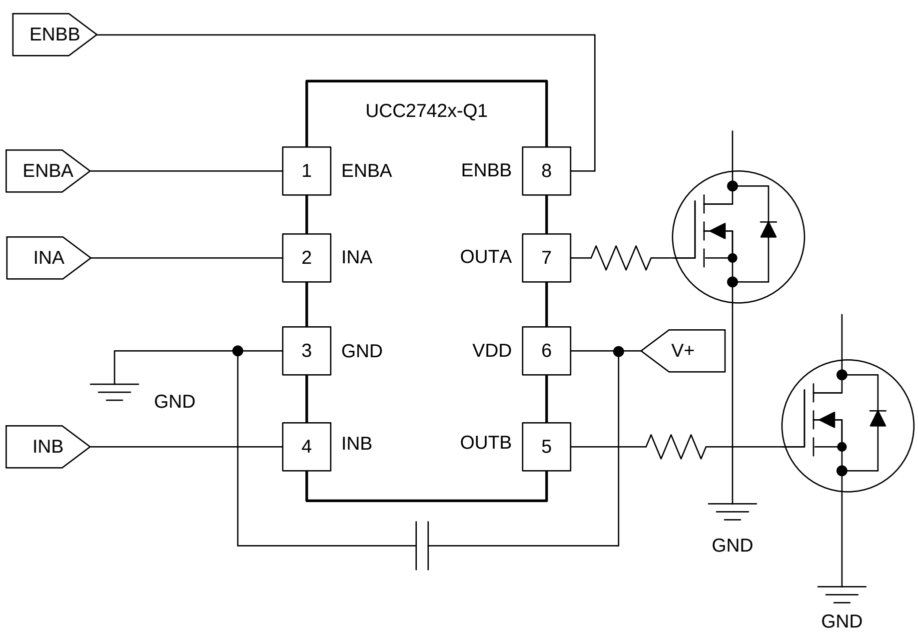


Figure 30. UCC2742x-Q1 Driving Two Independent MOSFETs

9.2.1 Design Requirements

To select proper device from UCC2742x-Q1 family, TI recommends first checking the appropriate logic for the outputs. The UCC27423-Q1 has dual inverting outputs, the UCC27424-Q1 has dual noninverting outputs, and the UCC27425-Q1 has an inverting channel A and noninverting channel B. Moreover, evaluate some considerations to make the most appropriate selection. Among these considerations are V_{DD}, drive current, and power dissipation.

Typical Application (continued)

9.2.2 Detailed Design Procedure

9.2.2.1 Source and Sink Capabilities During Miller Plateau

Large power MOSFETs present a large load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCC2742x-Q1 drivers have been optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging and discharging of the drain-gate capacitance with current supplied or removed by the driver device.

Two circuits are used to test the current capabilities of the UCC2742x-Q1 driver. In each case, external circuitry is added to clamp the output near 5 V while the IC is sinking or sourcing current. An input pulse of 250 ns is applied at a frequency of 1 kHz in the proper polarity for the respective test. In each test, there is a transient period where the current peaked up and then settled down to a steady-state value. The noted current measurements are made at a time of 200 ns after the input pulse is applied, after the initial transient.

The circuit in Figure 31 is used to verify the current sink capability when the output of the driver is clamped around 5 V, a typical value of gate-source voltage during the Miller plateau region. The UCC2742x-Q1 is found to sink 4.5 A at V_{DD} = 15 V and 4.28 A at V_{DD} = 12 V.

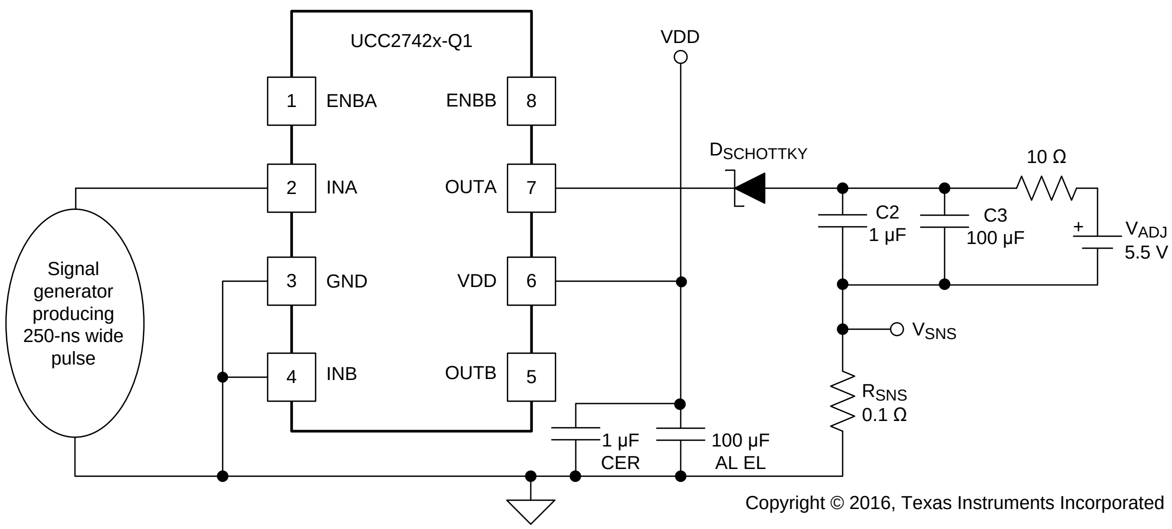


Figure 31. Current Sink Capability Test

The circuit show in Figure 32 is used to test the current source capability with the output clamped around 5 V with a string of Zener diodes. The UCC2742x-Q1 is found to source 4.8 A at V_{DD} = 15 V and 3.7 A at V_{DD} = 12 V.

Typical Application (continued)

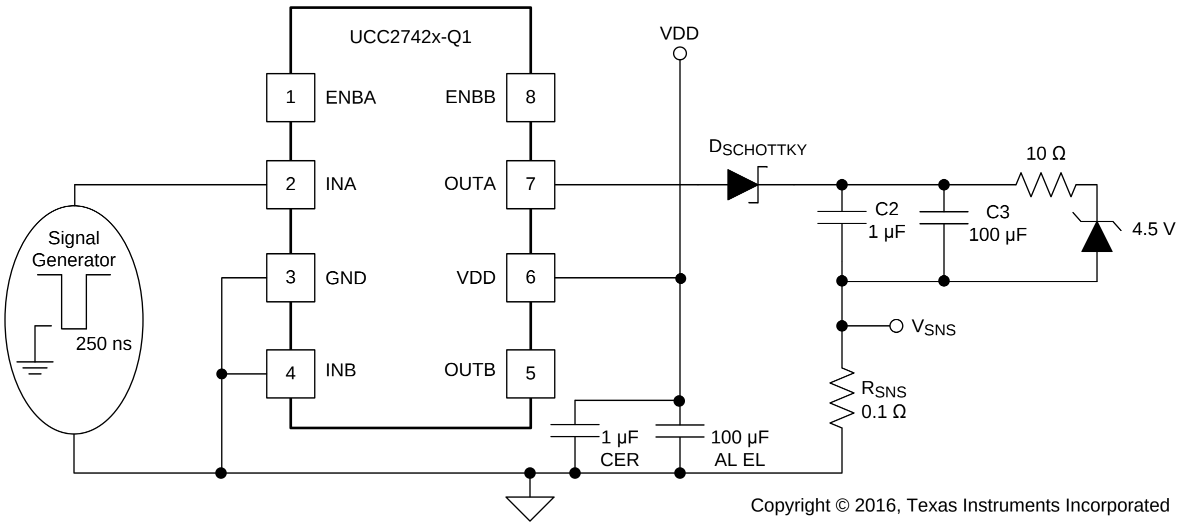


Figure 32. Current Source Capability Test

9.2.2.2 Drive Current and Power Requirements

The UCC2742x-Q1 family of drivers are capable of delivering 4 A of current to a MOSFET gate for a period of several hundred nanoseconds. High-peak current is required to turn the device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. A MOSFET is used in this discussion because it is the most common type of switching device used in high frequency power conversion equipment.

Reference 1 in the *Related Documentation* section discuss the current required to drive a power MOSFET and other capacitive-input switching devices. Reference 1 in includes information on the previous generation of bipolar IC gate drivers.

When a driver IC is tested with a discrete, capacitive load, it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by Equation 2.

$$E = \frac{1}{2}CV^2$$

where

- C = load capacitor
- V = bias voltage (feeding the driver) (2)

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by Equation 3.

$$P = CV^2 \times f$$

where

- f = switching frequency (3)

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An actual example using the conditions of the previous gate drive waveform should help clarify this.

With V_{DD} = 12 V, C_{LOAD} = 10 nF, and f = 300 kHz, the power loss can be calculated as Equation 4.

$$P = 10\ nF \times (12\ V)^2 \times (300\ kHz) = 0.432\ W \quad (4)$$

With a 12-V supply, this would equate to a current of Equation 5.

Typical Application (continued)

$$I = \frac{P}{V} = \frac{0.432\ W}{12\ V} = 36\ mA \tag{5}$$

The actual current measured from the supply was 0.037 A, and is very close to the predicted value. But, consider the I_{DD} current that is due to the IC internal consumption. With no load, the IC current draw is 0.0027 A. Under this condition, the output rise and fall times are faster than with a load. This could lead to an almost insignificant, yet measurable current due to cross-conduction in the output stages of the driver. However, these small current differences are buried in the high-frequency switching spikes, and are beyond the measurement capabilities of a basic lab setup. The measured current with 10-nF load is reasonably close to that expected.

The switching load presented by a power MOSFET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain of the device between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence $Q_g = C_{eff}V$ to provide the power loss in Equation 6.

$$P = C \times V^2 \times f = V \times Q_g \times f \tag{6}$$

Equation 6 allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage.

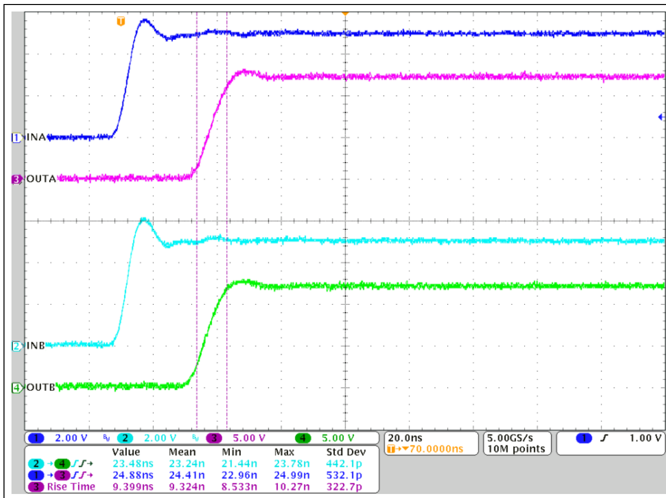
9.2.3 Application Curves

Figure 33 and Figure 34 show rising and falling time and turnon and turnoff propagation delay testing waveform in room temperature for UCC27424-Q1, and waveform measurement data (see the bottom part of the waveform). Each channel, INA/INB/OUTA/OUTB, is labeled and displayed on the left hand of the waveforms.

The load capacitance testing condition is 1.8 nF, V_{DD} = 12 V, and f = 300 kHz.

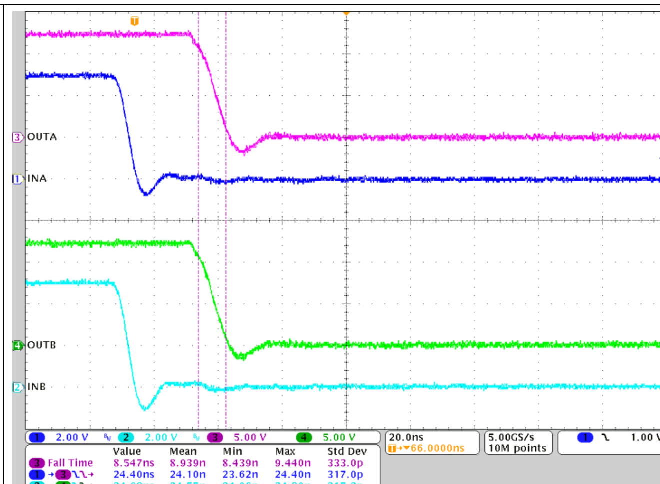
HI and LI share one same input from function generator; therefore, besides the propagation delay and rising or falling time, the difference of the propagation delay between HO and LO gives the propagation delay matching data.

Note the linear rise and fall edges of the switching waveforms. This is due to the constant output current characteristic of the driver as opposed to the resistive output impedance of traditional MOSFET-based gate drivers.



CL = 1.8 nF, V_{DD} = 12 V, f = 300 kHz

Figure 33. Rising Time and Turnon Propagation Delay



CL = 1.8 nF, V_{DD} = 12 V, f = 300 kHz

Figure 34. Falling Time and Turnoff Propagation Delay

10 Power Supply Recommendations

The recommended bias supply voltage range for UCC2742x-Q1 is from 4 V to 15 V. The upper end of this range is driven by the absolute maximum voltage rating of the V_{DD} (16 V). TI recommends keeping proper margin to allow for transient voltage spikes. A local bypass capacitor must be placed between the VDD and GND pins. And this capacitor must be placed as close to the device as possible. A low ESR, ceramic surface-mount capacitor is recommended. TI recommends using 2 capacitors across VDD and GND: a 100-nF ceramic surface-mount capacitor for high-frequency filtering placed very close to VDD and GND pin, and another surface-mount capacitor (220 nF to 10 μF) for IC bias requirements.

11 Layout

11.1 Layout Guidelines

Optimum performance of gate drivers cannot be achieved without taking due considerations during circuit board layout. The following points are emphasized:

1. Low ESR or ESL capacitors must be connected close to the IC between VDD and GND pins to support high peak currents drawn from VDD during the turnon of the external MOSFETs.
2. Grounding considerations:
   – The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gates to a minimal physical area. This decreases the loop inductance and minimizes noise issues on the gate terminals of the MOSFETs. The gate driver must be placed as close as possible to the MOSFETs.
   – Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver is connected to the other circuit nodes such as source of power MOSFET and ground of PWM controller at one, single point. The connected paths must be as short as possible to reduce inductance.
   – Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.
3. In noisy environments, tying inputs of an unused channel of the UCC2742x-Q1 device to VDD or GND using short traces in order to ensure that the output is enabled and to prevent noise from causing malfunction in the output may be necessary.
4. Separate power traces and signal traces, such as output and input signals.

11.2 Layout Example

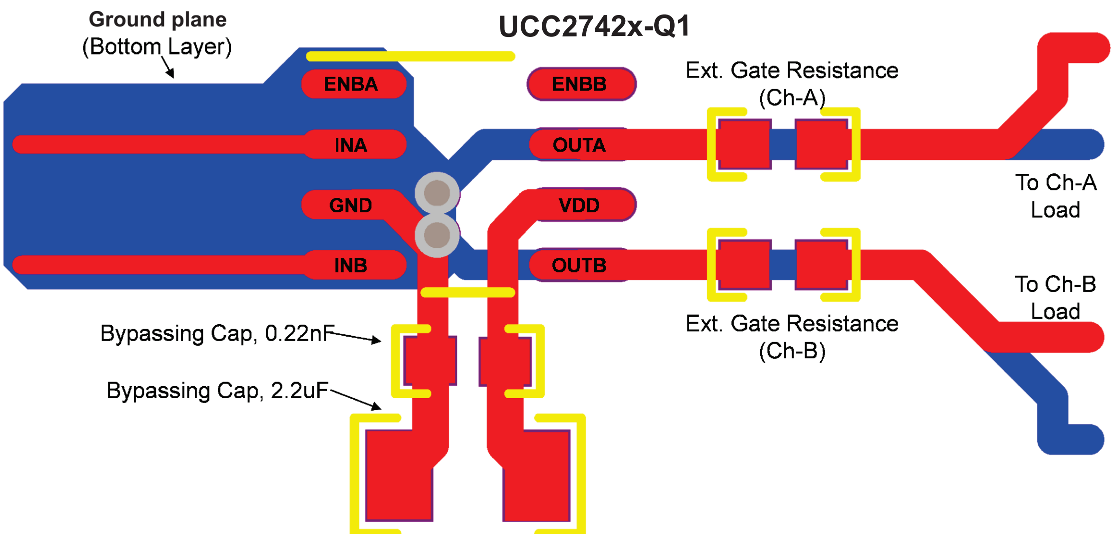


Figure 35. Recommended PCB Layout for UCC2742x-Q1

11.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the IC package. For a power driver to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCC2742x-Q1 family of drivers is available in three different packages to cover a range of application requirements.

As shown in the power dissipation rating table, the 8-pin SOIC (D) package has a power rating of around 0.5 W with T_A = 70°C. This limit is imposed in conjunction with the power derating factor also given in the *Dissipation Ratings* table. Note that the power dissipation in our earlier example is 0.432 W with a 10-nF load, 12 V_{DD}, switched at 300 kHz. Thus, only one load of this size could be driven using the D package, even if the two onboard drivers are paralleled. The difficulties with heat removal limit the drive available in the older packages.

The 8-pin MSOP with PowerPAD (DGN) package significantly relieves this concern by offering an effective means of removing the heat from the semiconductor junction. As described in reference 2 of the *Related Documentation* section, the PowerPAD packages offer a leadframe die pad that is exposed at the base of the package. This pad is soldered to the copper on the PCB directly underneath the IC package, reducing the $R_{\theta JC(bot)}$ down to 5.9°C/W. Data is presented in reference 2 of *Related Documentation* to show that the power dissipation can be quadrupled in the PowerPAD configuration when compared to the standard packages. The PCB must be designed with thermal lands and thermal vias to complete the heat removal subsystem. This allows a significant improvement in heat sinking over that available in the D package, and is shown to more than double the power capability of the D package. Note that the PowerPAD is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate which is the ground of the device.

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

1. *Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits* (SLUA105)
2. *PowerPad Thermally Enhanced Package* (SLMA002)
3. *PowerPAD Made Easy* (SLMA004)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC27423-Q1	Click here	Click here	Click here	Click here	Click here
UCC27424-Q1	Click here	Click here	Click here	Click here	Click here
UCC27425-Q1	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27423QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	EADQ	Samples
UCC27423QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27423Q	Samples
UCC27424QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	EPJQ	Samples
UCC27424QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27424Q	Samples
UCC27425QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27425Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC27423-Q1, UCC27424-Q1, UCC27425-Q1 :

- Catalog: UCC27423, UCC27424, UCC27425

- Enhanced Product: UCC27423-EP, UCC27424-EP

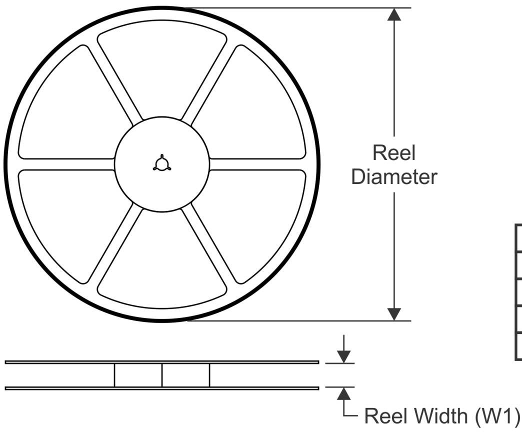
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

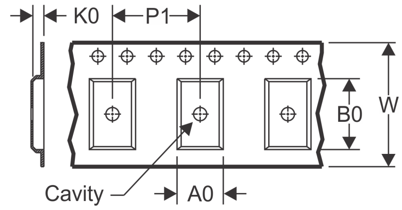
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

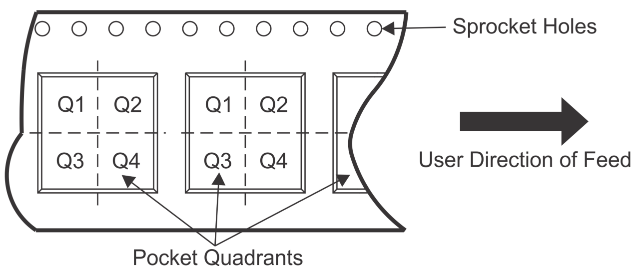


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

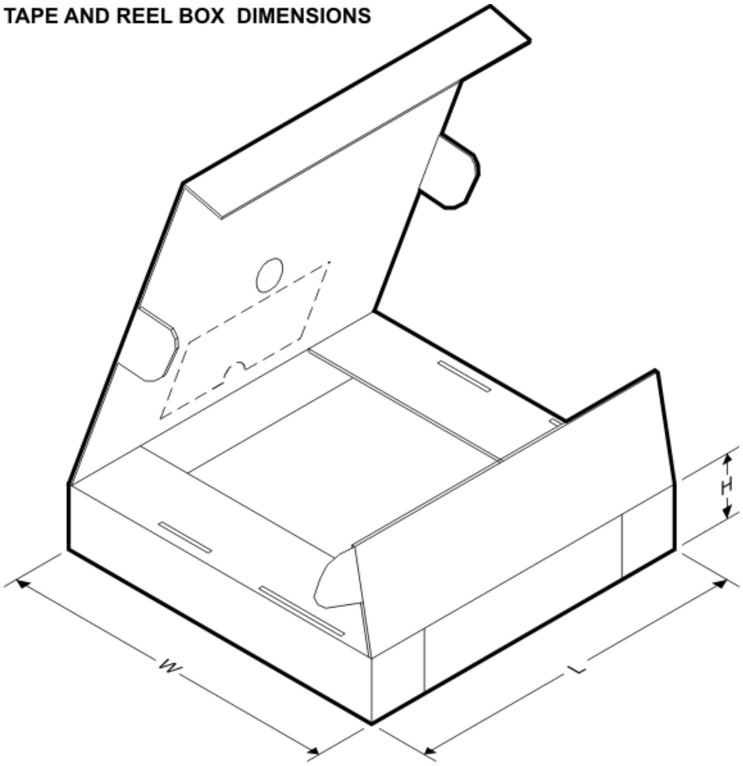
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27423QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27423QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27424QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27424QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27425QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

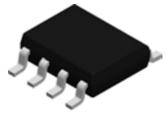
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27423QDGNRQ1	HVSSOP	DGN	8	2500	350.0	350.0	43.0
UCC27423QDRQ1	SOIC	D	8	2500	340.5	338.1	20.6
UCC27424QDGNRQ1	HVSSOP	DGN	8	2500	350.0	350.0	43.0
UCC27424QDRQ1	SOIC	D	8	2500	340.5	338.1	20.6
UCC27425QDRQ1	SOIC	D	8	2500	340.5	338.1	20.6

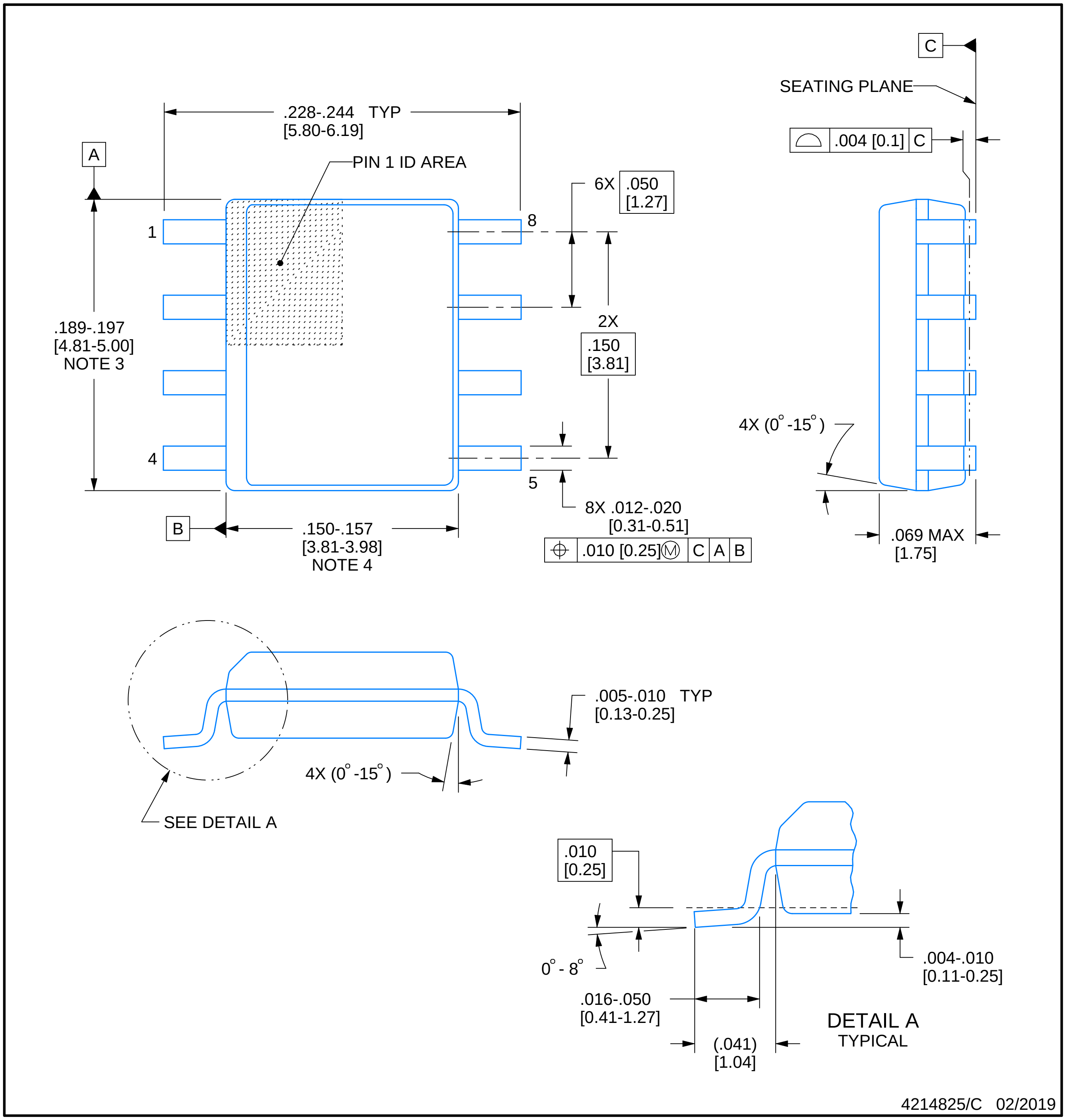
PACKAGE OUTLINE



D0008A

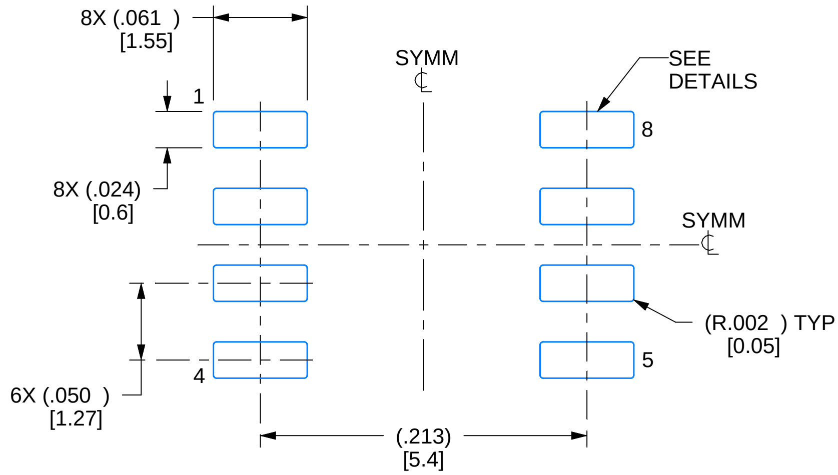
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

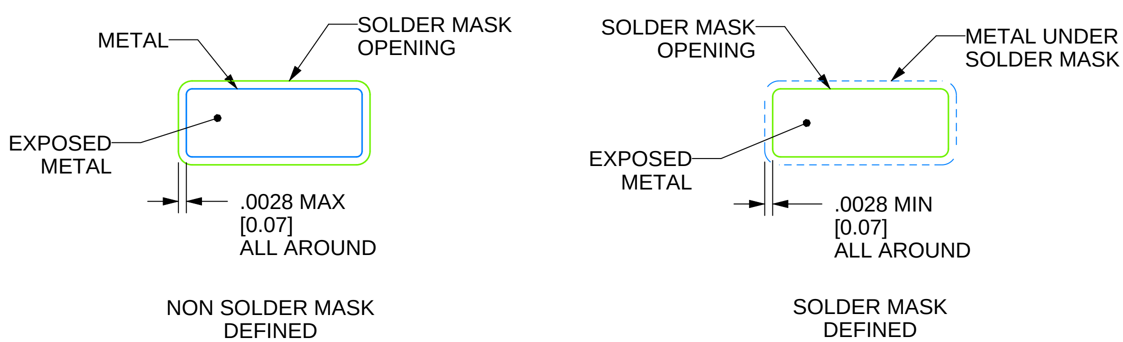


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

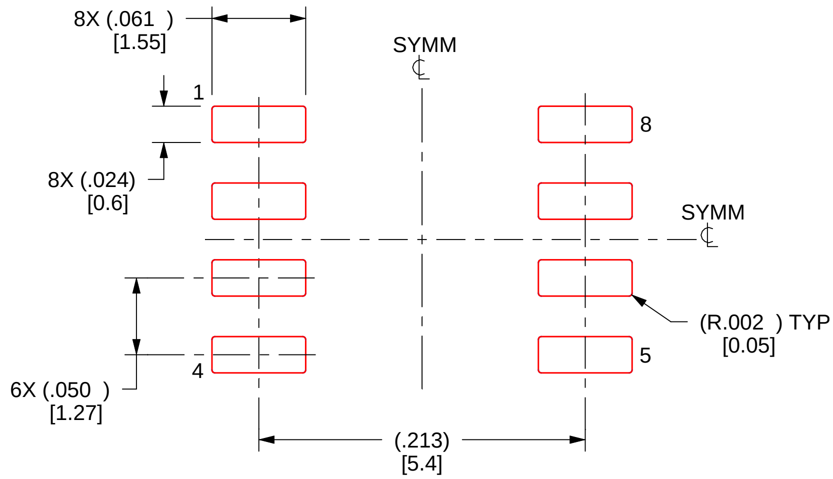


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



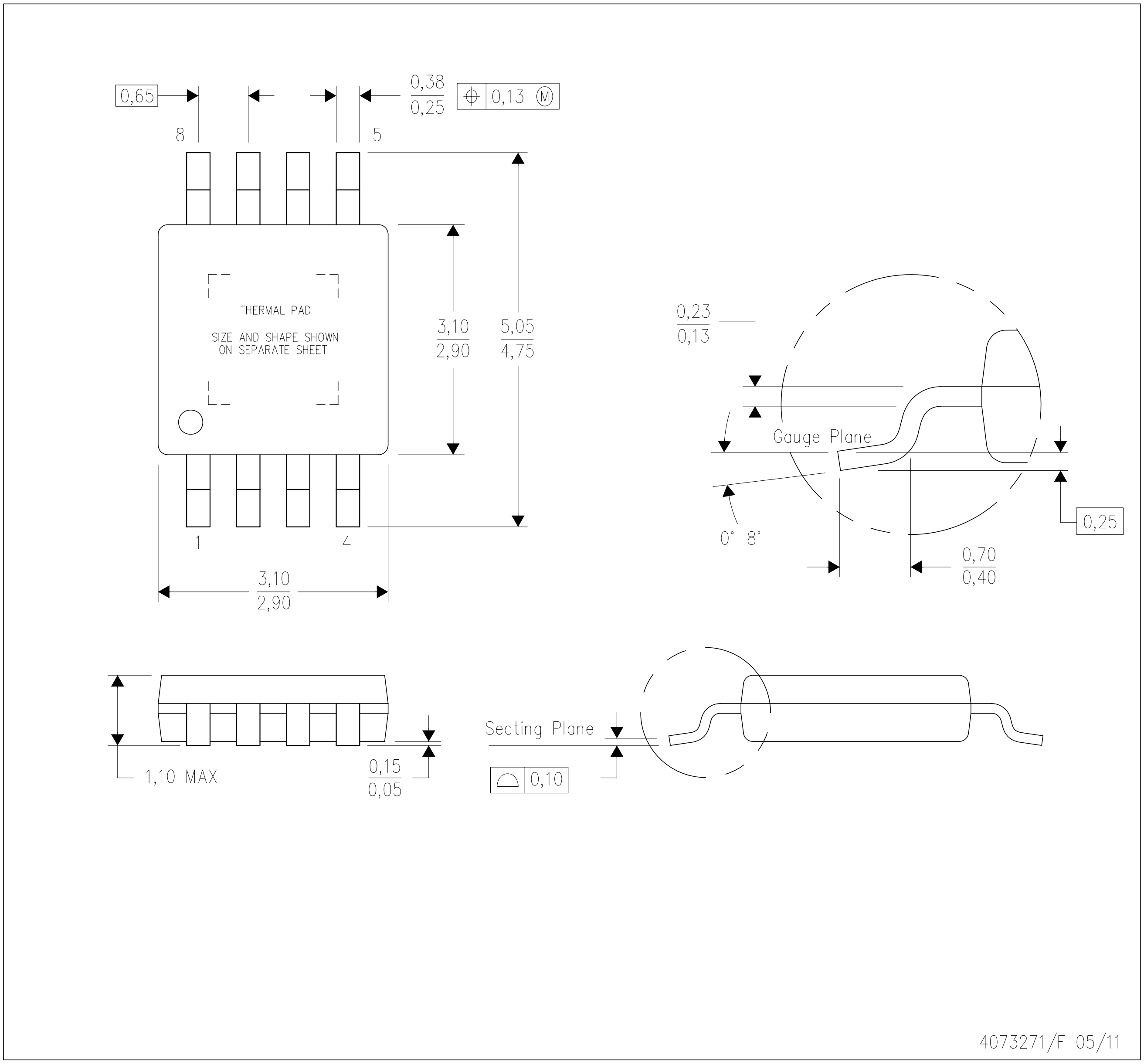
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

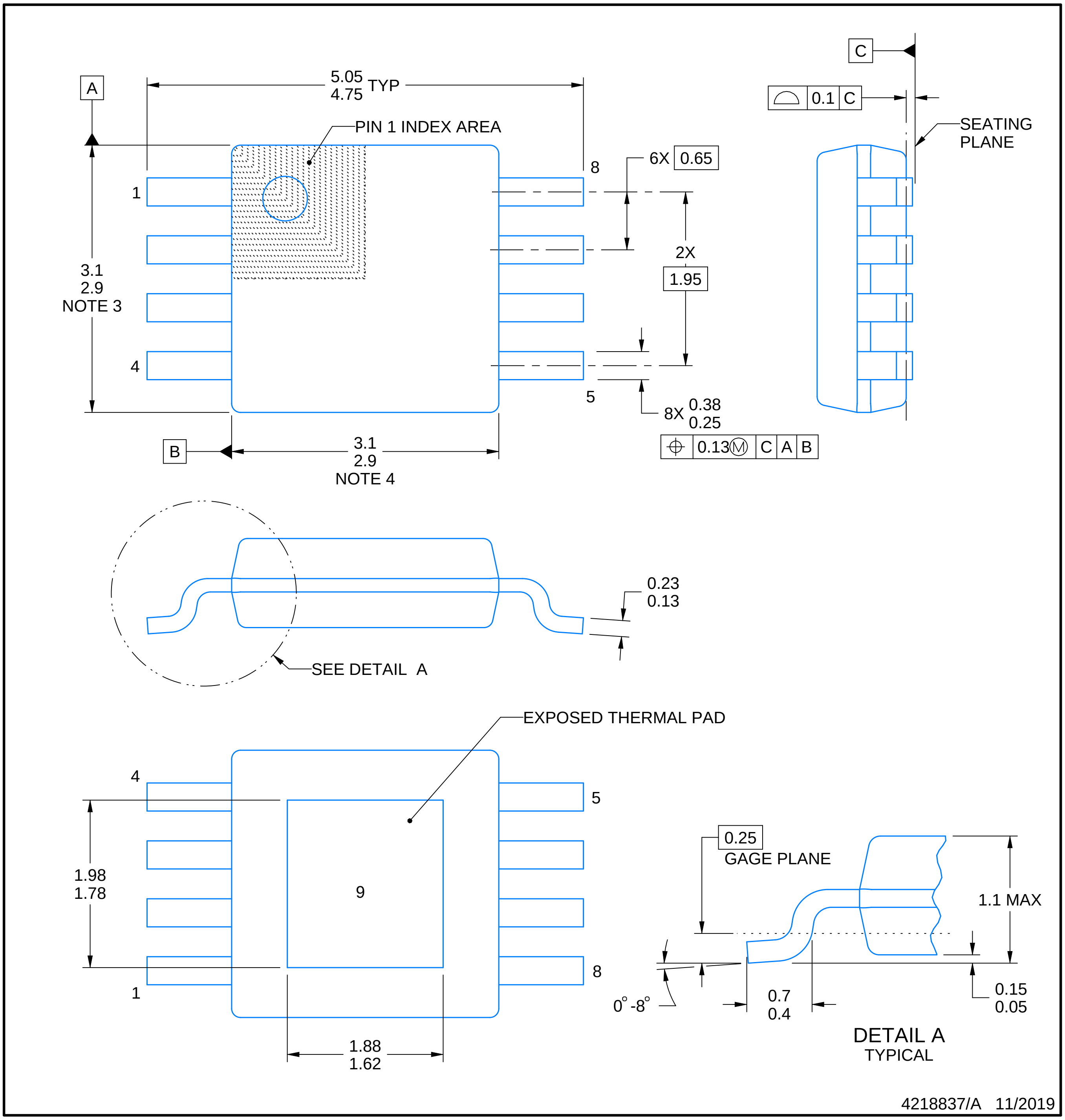
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE



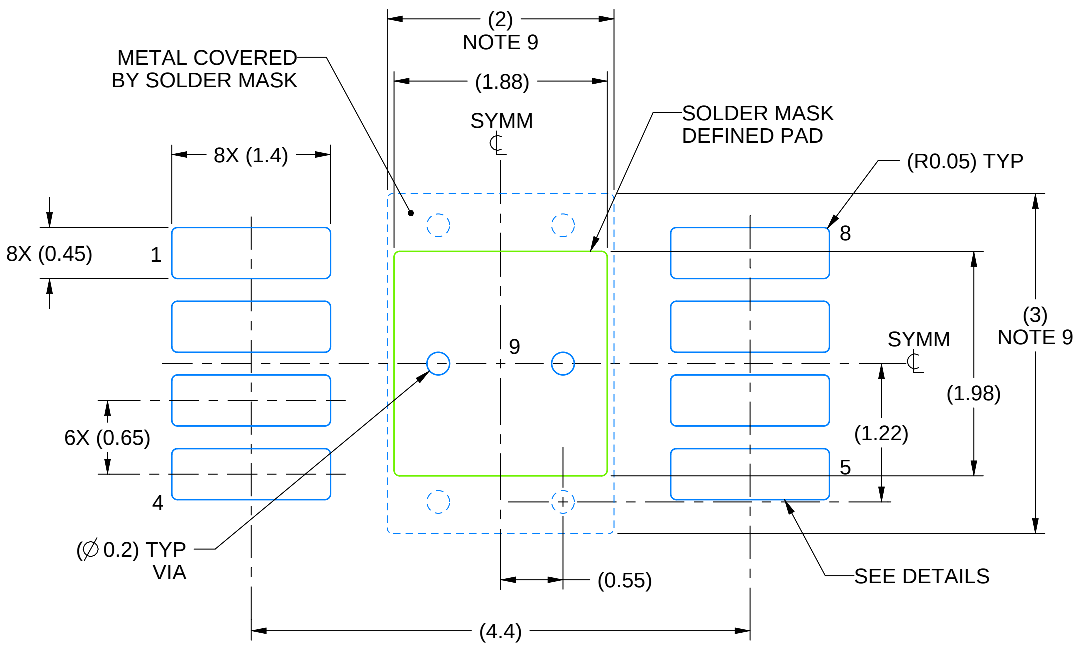
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T



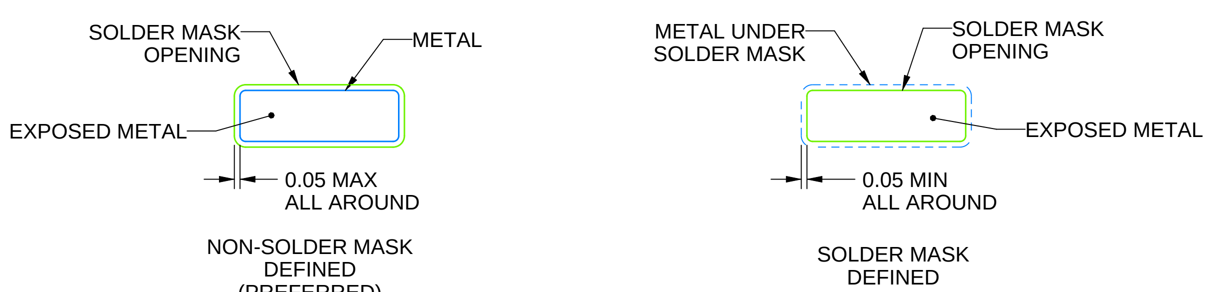
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

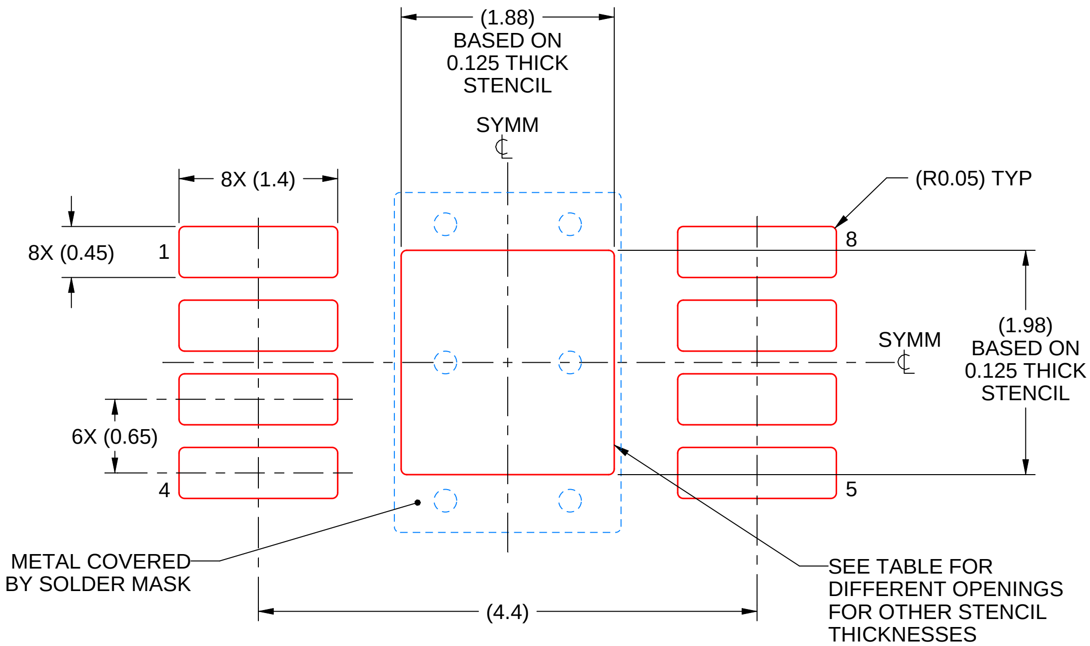


SOLDER MASK DETAILS

4218837/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.10 X 2.21
0.125	1.88 X 1.98 (SHOWN)
0.15	1.72 X 1.81
0.175	1.59 X 1.67

4218837/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER