SJA1124

Quad LIN master transceiver with LIN master controller

Rev. 1 — 8 May 2018 Product data sheet

1 General description

The SJA1124 is a quad Local Interconnect Network (LIN) master channel device. Each of the four channels contains a LIN master controller and LIN transceiver with master termination. LIN master frames are transferred to the physical LIN bus via the LIN physical layer. The SJA1124 is primarily intended for in-vehicle subnetworks using baud rates up to 20 kBd and is compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987-4:2016(12 V LIN) and SAE J2602-1.

A Serial Peripheral Interface (SPI) and an interrupt output provide the interface between the SJA1124 and a microcontroller.

Transmit data streams received on the SPI are converted by the SJA1124 into LIN master frames transmitted on the LIN bus. The LIN master frames are transmitted as optimized bus signals shaped to minimize ElectroMagnetic Emission (EME). The LIN bus output pins are pulled HIGH via internal LIN master termination resistors. Data streams received on the LIN bus input pins can be read by the microcontroller via the SPI.

Power consumption is very low in Low Power mode. However, the SJA1124 can still be woken up via the LIN pins and the SPI interface.

2 Features and benefits

2.1 General

- Four LIN master channels:
  - LIN master controller
  - LIN transceiver
  - LIN master termination consisting of a diode and a 1 kΩ ±10 % resistor
- Compliant with:
  - LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A
  - ISO 17987-3:2016, ISO 17987-4:2016 (12 V LIN)
  - SAE J2602-1
- Very low current consumption in Low Power mode with wake-up via SPI or LIN
- Option to control an external voltage regulator via the INHN output
- Bus signal shaping optimized for baud rates up to 20 kBd
- SPI for communicating with the microcontroller:
  - SPI used for configuration, control, diagnosis and LIN data transfer
  - Flexible SPI length from 3 bytes to 18 bytes
  - Output status pin signals SPI operational state
- Interrupt output pin: interrupts can be configured individually
- Facilitates synchronous LIN frame transmission across multiple SJA1124 devices
- VIO input for direct interfacing with 3.3 V and 5 V microcontrollers

- On-chip Phase-Locked Loop (PLL) for LIN master controller
- Passive behavior in unpowered state
- Undervoltage detection
- Leadless DHVQFN24 package (3.5 mm × 5.5 mm) supporting improved Automated Optical Inspection (AOI) capability

2.2 LIN master controllers

- Independent per LIN channel:
  - Baud rate
  - Operating mode
  - Status and interrupt
- Complete LIN frame handling and transfer
- One interrupt per LIN frame
- Slave response timeout detection
- Programmable break length
- Automatic sync field generation
- Programmable stop bit length
- Hardware parity generation
- Hardware or software checksum generation
- Fault confinement
- Fractional baud rate generator

2.3 Protection

- Excellent ElectroMagnetic Immunity (EMI)
- Very high ESD robustness: ±6 kV according to IEC61000-4-2 for pins LIN1 to LIN4 and BAT
- Bus terminal and battery pin protected against transients in the automotive environment (ISO 7637)
- Bus terminal short-circuit proof to battery and ground
- LIN dominant timeout function
- Thermal protection

3 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SJA1124AHG	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT 815-1

4 Block diagram

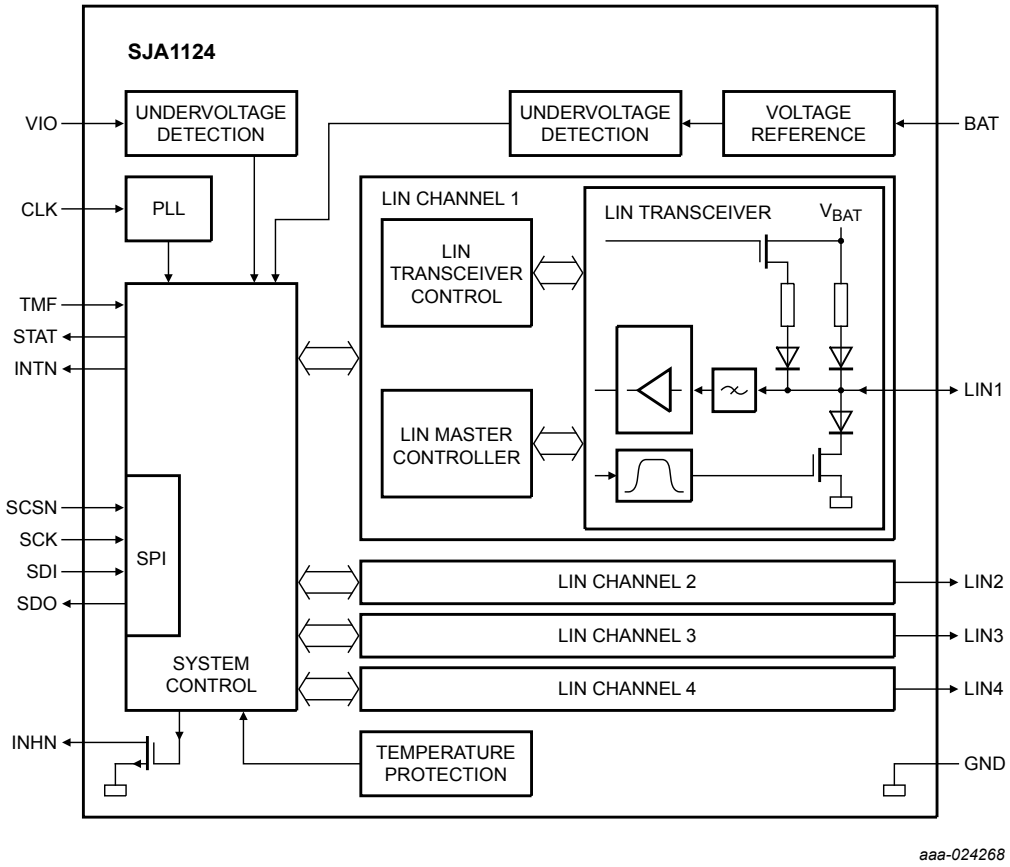


Figure 1. Block diagram

5 Pinning information

5.1 Pinning

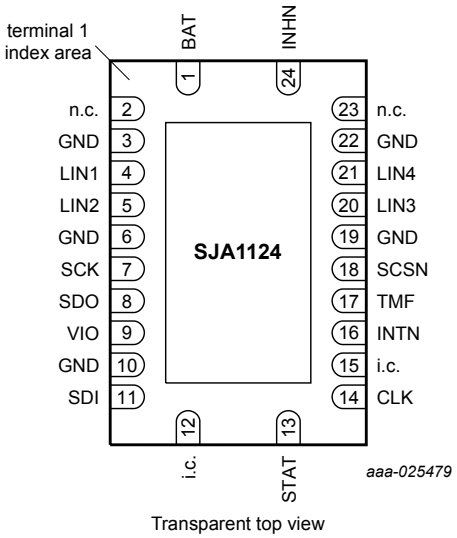


Figure 2. Pin configuration diagram

5.2 Pin description

Table 2. Pin description

Symbol	Pin[1]	Description
BAT	1	battery supply
n.c.	2	not connected
GND	3	ground
LIN1	4	LIN bus line 1 input/output
LIN2	5	LIN bus line 2 input/output
GND	6	ground
SCK	7	SPI clock input
SDO	8	SPI data output
VIO	9	supply voltage for I/O level adapter
GND	10	ground
SDI	11	SPI data input
i.c.	12	internally connected; should be left floating
STAT	13	SPI status output
CLK	14	clock input for PLL
i.c.	15	internally connected; should be connected to ground
INTN	16	interrupt output to microcontroller; active LOW

Symbol	Pin[1]	Description
TMF	17	transmit frame input
SCSN	18	SPI chip select input; active-LOW
GND	19	ground
LIN3	20	LIN bus 3 input/output
LIN4	21	LIN bus 4 input/output
GND	22	ground
n.c.	23	not connected
INHN	24	inhibit output for controlling an external voltage regulator; open-drain; active LOW

[1] For enhanced thermal and electrical performance, solder the exposed center pad of the DHVQFN24 package to board ground.

6 Functional description

The SJA1124 is an SPI-to-LIN bridge with four LIN master channels. Each LIN master channel incorporates a LIN master controller and LIN transceiver with master termination. According to the Open System Interconnect (OSI) model, this device comprises the LIN physical layer and part of the data link layer.

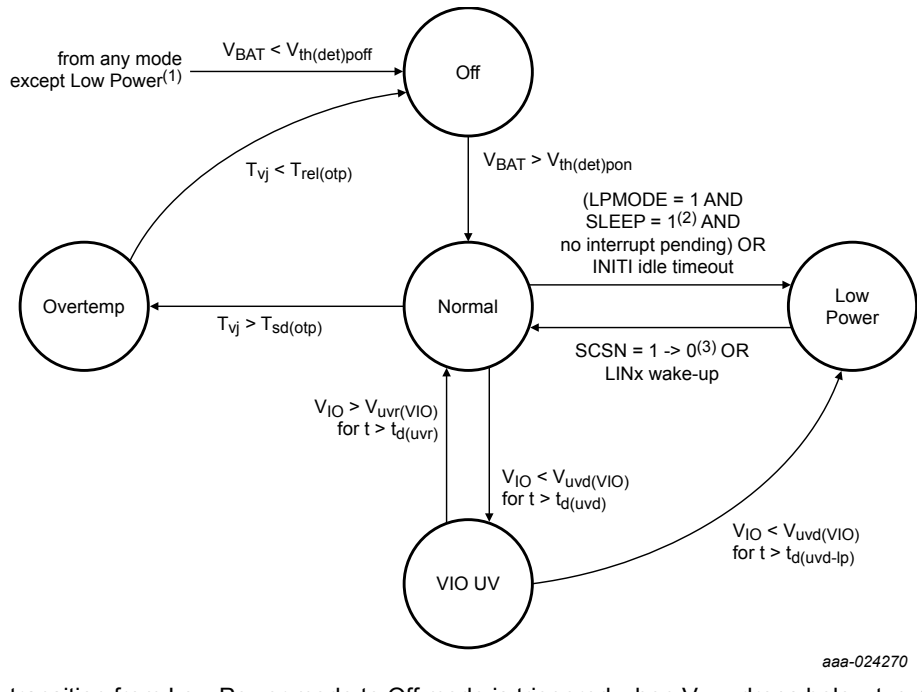
This device is intended for, but not limited to, automotive LIN master applications with multiple LIN master channels. It provides excellent ElectroMagnetic Compatibility (EMC) performance.

6.1 LIN 2.x/SAE J2602 compliance

The SJA1124 is fully compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987-3:2016, ISO 17987-4:2016 (12 V LIN) and SAE J2602-1.

6.2 Operating modes

The SJA1124 supports two main operating modes: Normal mode and Low Power mode. Additional battery supply undervoltage (Off), intermediate VIO undervoltage (VIO UV), and overtemperature protection (Overtemp) modes are supported. The SJA1124 state diagram is shown in Figure 3.



(1) A transition from Low Power mode to Off mode is triggered when V_{BAT} drops below typ. 2.4 V.

(2) All LIN frame transmissions must be completed.

(3) The SCSN input threshold depends on V_{IO}. This mode transition will not take place when $V_{SCSN} > 0.75V_{IO}$.

Figure 3. State diagram

6.2.1 Off mode

When the SJA1124 is in Off mode, all input signals are ignored and all output drivers are off. All register values are reset. The device is in a defined passive, low-power state in Off mode.

The SJA1124 switches to Off mode when the voltage on pin BAT drops below the power-off detection threshold, $V_{th(det)poff}$. When the SJA1124 is in Overtemp mode, it switches to Off mode when the junction temperature drops below $T_{rel(otp)}$.

6.2.2 Low Power mode

The SJA1124 consumes significantly less power in Low Power mode than in Normal mode. All LIN master controllers and the PLL are disabled. While current consumption is very low in Low Power mode, the SJA1124 can still detect SPI (see Section 6.5.2) and remote wake-up events on pins LINx (see Section 6.5.1).

When the SJA1124 switches to Low Power mode, pin INHN is set floating, SPI register access is disabled and all register values are reset.

The SJA1124 switches from Normal mode to Low Power mode when bit LPMODE in the Mode register is set (see Table 16), provided all LIN channels are in LIN Sleep mode (SLEEP = 1 in the LCFG1 register; see Table 27), there is no ongoing LIN frame transmission and no interrupts are pending.

Note: Low Power mode should not be confused with LIN Sleep mode, which is a sub-mode of Normal mode (see Section 6.2.3.1).

6.2.3 Normal mode

Normal mode is the normal operating state of the SJA1124. Registers can be accessed via the SPI. The PLL is enabled and can be configured. For LIN frame transmission, a LIN channel needs to be in LIN Normal mode and the PLL should be locked.

The SJA1124 switches from Off mode to Normal mode when the voltage on pin BAT exceeds the power-on detection threshold, $V_{th(det)pon}$.

The SJA1124 switches from Low Power mode to Normal mode when a remote wake-up is detected on one of the LINx pins (see Section 6.5.1) or an SPI wake-up event is triggered (see Section 6.5.2).

Registers will contain default values after a transition from Off or Low Power to Normal mode. The initialization status interrupt (INITI; see Table 21) is set and the INTN output is forced LOW. INITI must be cleared before the INITI idle timeout time, $t_{to(idle)INITI}$, expires. Otherwise, the SJA1124 switches to Low Power mode. The transitions to Normal mode takes $t_{init(norm)}$.

Note: Normal mode should not be confused with LIN Normal mode (see section Section 6.2.3.2), which is a sub-mode of the Normal mode.

Four sub-modes of Normal mode are described in the following sections.

6.2.3.1 LIN Sleep mode

A LIN channel can detect remote LIN wake-up events on the associated LIN pin in LIN Sleep mode (see Section 6.5.1). Typically, a LIN channel is set to LIN Sleep mode after

the transmission of a so-called LIN go-to-sleep command, which is a special LIN master request frame issued to force LIN slave nodes to LIN network sleep state.

A LIN channel switches to LIN Sleep mode when bit SLEEP in the associated LIN configuration register is set to 1 and LIN frame transmission has been completed.

6.2.3.2 LIN Normal mode

In LIN Normal mode, a LIN channel can be used for LIN frame transmission.

A LIN channel switches to LIN Normal mode when bit SLEEP in the associated LIN configuration register is set to 0, provided bit INIT = 0 (see Table 27). After switching to LIN Normal mode, the LIN channel will be ready for LIN frame transmission after a short initialization period ($t_{init(LIN)}$).

6.2.3.3 LIN Initialization mode

The LIN channels can be initialized in this mode. All message transfers to and from the LIN bus are aborted when the SJA1124 enters LIN Initialization mode. Therefore, the state of the LIN channel should be checked (via the LIN state register; see Table 41) before switching to LIN Initialization mode. The LIN bus outputs, LINx, are in recessive state (HIGH) in this mode.

The SJA1124 switches to LIN Initialization mode when bit INIT in LIN configuration register 1 (Table 27) is set to 1 (provided LIN Sleep mode is not selected; SLEEP = 0).

6.2.3.4 LIN High-Speed mode

In LIN High-Speed mode, the associated LIN transceiver supports baud rates higher than 20 kBd. Otherwise, behavior is identical to LIN Normal mode.

A LIN channel switches to LIN High-Speed mode when the associated LxHC bit in the LIN Communication register 1 is set (see Table 25).

6.2.4 VIO UV mode

In VIO UV mode, the LINx outputs are recessive, INHN and STAT outputs are LOW, SDO is floating, INTN is HIGH and the digital inputs are ignored.

The SJA1124 switches from Normal mode to VIO UV mode when the voltage on pin VIO drops below the VIO undervoltage detection threshold, $V_{uvd(VIO)}$, for longer than $t_{d(uvd)}$.

6.2.5 Overtemp mode

Overtemp mode prevents the SJA1124 from being damaged by excessive temperatures. If the junction temperature exceeds the shutdown threshold, $T_{sd(otp)}$, the thermal protection circuit disables the LIN channel output drivers, the LIN master pull-ups (see Section 6.10.11) and the PLL. The LIN master controller aborts LIN frame transmission. The STAT output is LOW in Overtemp mode.

6.3 Interrupt

The interrupt function of the SJA1124 provides an event signal on pin INTN to inform the microcontroller about system control, status and error events. Interrupt events are

enabled via dedicated interrupt enable bits. Pin INTN is forced LOW in response to an enabled interrupt event.

Pin INTN features a forced interrupt release time. After an interrupt status bit is cleared, pin INTN is released for at least $t_{to(int)}$. The INTN pin is enabled again to signal interrupt events once the release time has elapsed. Interrupts will still be captured in the interrupt status registers during the forced interrupt release time, but will not be forwarded to pin INTN. The interrupt registers can be read at any time.

Pin INTN is an active-LOW digital output with integrated pull-up. Typically, it is connected directly to a microcontroller.

A dedicated interrupt status bit is associated with each interrupt source. Top-level interrupt status bits are contained in the interrupt registers (INT1, INT2 and INT3; see Section 6.9.4). Second level interrupts related to the LIN master controller are in the the LIN status registers (LS, see Table 43) and LIN error status registers (LES; see Table 42).

Once an interrupt source has been identified, the interrupt should be cleared by writing logic 1 to the associated interrupt status bit. A number of interrupts can be cleared with a single write access by writing 1 to the relevant bits. Writing logic 0 to an interrupt has no effect. The interrupt pin, INTN, is released once all interrupts have been cleared.

6.4 Synchronous LIN frame transmission

LIN header transmission can be synchronized across multiple SJA1124 devices. A rising edge on pin TMF triggers the start of a synchronous LIN header transmission (when the function is enabled). The minimum LOW and HIGH TMF pulse widths needed to trigger transmission are, respectively, $t_{tmf(L)}$ and $t_{tmf(H)}$.

Note: once LIN header transmission has been triggered via pin TMF, additional TMF trigger pulses should not be applied until the LIN frame transmission has been completed. Otherwise, a second LIN frame transmission might be triggered in error.

Synchronous LIN frame transmission is enabled for a LIN channel by setting the relevant LxTMFE bit in the LCOM1 register (Table 25).

If synchronous LIN header transmission is only needed for one SJA1124 device, it can be enabled per LIN channel via bits LxHTRQ in the LCOM2 register (Table 26). Pin TMF does not need to be activated in this case.

Note: after setting bit LxHTRQ, it should not be set again until LIN frame transmission has been completed. Otherwise, a second LIN frame transmission might be triggered in error.

6.5 Device wake-up

6.5.1 Remote wake-up via the LIN bus

A falling edge on pin LINx followed by a dominant level maintained for $t_{wake(dom)LIN}$, followed by a recessive level, is regarded as a remote wake-up request. The detection of a remote LIN wake-up event is signaled via bits LxWUI in the INT1 register (see Table 21) in Normal mode, provided the bus level on LINx is recessive.

The SJA1124 can also detect remote LIN wake-up events in Normal mode when a LIN channel is in LIN Sleep mode (see Section 6.2.3.1).

6.5.2 Wake-up via the SPI

A LOW level on pin SCSN lasting $t_{wake(low)SCSN}$ is interpreted as an SPI wake-up request. Register access is not possible until the device has been initialized (after t_{init}) and the transition to Normal mode has been completed (see Section 6.2.3), or if pin STAT is driven LOW.

6.6 SPI

The Serial Peripheral Interface (SPI) provides the communication link with the microcontroller, supporting multi-slave operations.

The SPI uses full duplex data transfer. With full duplex data transfer, status information is returned when new control data is shifted in. The interface also offers a read-only access option, allowing registers to be read back by the application without changing the register content. Furthermore, the SPI data transfer format provides variable data length with up to 16 data bytes.

The SPI uses four interface signals for synchronization and data transfer:

- SCSN - SPI chip select; active LOW
- SCK - SPI clock
- SDI - SPI data input
- SDO - SPI data output; floating when pin SCSN is HIGH

Bit sampling is performed on the falling clock edge and data is shifted on the rising clock edge as illustrated in Fig 4.

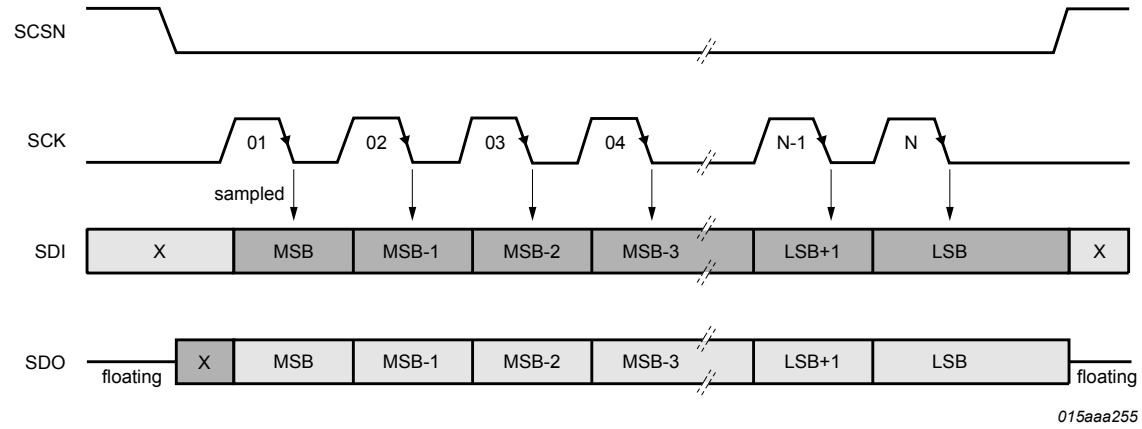


Figure 4. SPI timing protocol

Data in the SJA1124 is arranged in byte-length registers. Each register is assigned an 8-bit address. A write operation to the SJA1124 consists of between 3 and 18 data bytes. The first SPI byte is the address byte, containing the 8-bit address. The second byte is the control byte, containing a read-only bit (RO) and four data length code bits (DLC). For write register access, the RO bit must be set to logic 0 (if set to 1, data transmitted to the SJA1124 is ignored). The DLC specifies the number of data bytes transmitted, which may vary from 1 to 16 (see Table 3). The first data byte is written to the specified address. Subsequent data bytes are written to consecutive register addresses. So, an SPI write access consists of a minimum of 3 bytes and a maximum of 18 bytes. The SPI data transfer format is illustrated in Figure 5.

Table 3. SPI data length code

DLC	Number of data bytes
0h	1
1h	2
...	...
Fh	16

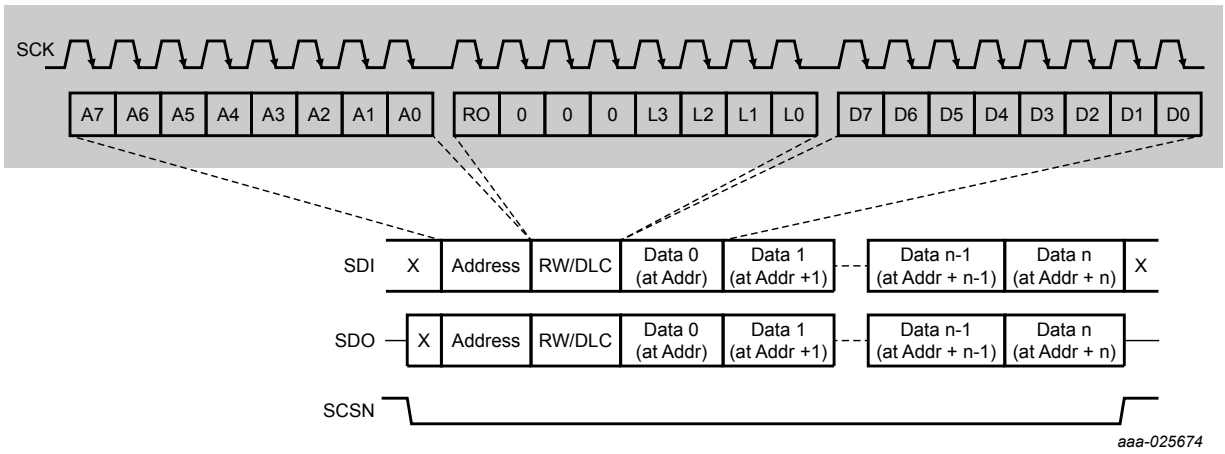


Figure 5. SPI data transfer format

The SJA1124 monitors the number of data bits transmitted. If the number of bits is not between 24 and 144, is not a factor of 8, or the number of bytes does not match the DLC in the SPI conrol byte, the write access is ignored and an SPI error interrupt (SPIEI) is triggered (see Table 22).

After the SPI data transfer is completed, as indicated by a rising edge on SCSN, the received data is processed internally. The SPI processing delay time is $t_{d(SPI)}$.

6.6.1 Full duplex data transfer

During an SPI data transfer, the contents of the address byte and the associated data byte are returned via the SDO pin. For a read-only access (RO bit is set to logic 1), the transmitted data bytes are ignored. If more than one SJA1124 device is connected to a single SPI, the data (SDI and SDO) and the clock lines (SCK) are shared. Only the chip select (SCSN) inputs must be connected individually (see connection example in Figure 6).

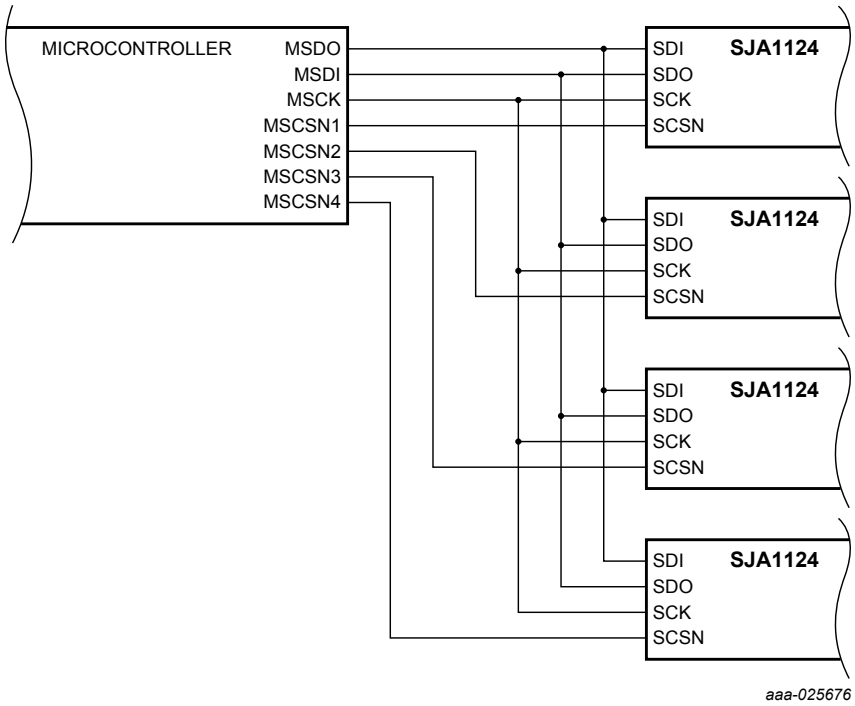


Figure 6. SPI connection example for full duplex data transfer

6.6.2 Status output

The status output pin (STAT) provides SPI access availability status information. It is driven LOW in VIO UV, Overtemp and Low Power modes. In Off mode, it is LOW if V_{BAT} is above the power-on detection threshold, $V_{th(det)pon}$. In Normal mode, the STAT output is in a high impedance state.

STAT is a digital open-drain active-LOW output, typically connected to a microcontroller. An external pull-up resistor to VIO is needed to provide a HIGH-level reference.

6.7 Register mapping overview

A register map overview is provided in Table 4 to Table 11. Detailed register descriptions are given in the following sections. Reserved bits return 0 when read.

Table 4. Overview of system control registers

Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	MODE	RST	reserved						LPMODE
01h	PLLCFG	reserved				PLLMULT			
02h	INT1EN	reserved				L4WUIE	L3WUIE	L2WUIE	L1WUIE
03h	INT2EN	reserved		OTWIE	PLLOLIE	PLLILIE	PLLIFFIE	SPIEIE	reserved
04h	INT3EN	L4EIE	L3EIE	L2EIE	L1EIE	L4SIE	L3SIE	L2SIE	L1SIE

Table 5. Overview of system status registers

Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10h	INT1	INITI	reserved			L4WUI	L3WUI	L2WUI	L1WUI
11h	INT2	reserved		OTWI	PLLOLI	PLLILI	PLLIFFI	SPIEI	LPRFI
12h	INT3	L4EI	L3EI	L3EI	L1EI	L4SI	L3SI	L2SI	L1SI
13h	STATUS	reserved		OTW	reserved	PLLIL	PLLIFF	reserved	

Table 6. Overview of LIN master controller global registers

Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
20h	LCOM1	L4HS	L3HS	L2HS	L1HS	L4TMFE	L3TMFE	L2TMFE	L1TMFE
21h	LCOM2	reserved				L4HTRQ	L3HTRQ	L2HTRQ	L1HTRQ

Table 7. Overview of LIN channel initialization registers

Address				Register	Bit							
LIN1	LIN2	LIN3	LIN4		7	6	5	4	3	2	1	0
30h	60h	90h	C0h	LCFG1	CCD	MBL				reserved	SLEEP	INIT
31h	61h	91h	C1h	LCFG2	TBDE	IOBE	reserved					
32h	22h	92h	C2h	LITC	reserved						IOT	reserved
33h	63h	93h	C3h	LGC	reserved						STOP	SR
34h	64h	94h	C4h	LRTC	reserved				RTO			
35h	65h	95h	C5h	LFR	reserved				FBR			
36h	66h	96h	C6h	LBRM	IBR[15:7]							
37h	67h	97h	C7h	LBRL	IBR[7:0]							
38h	68h	98h	C8h	LIE	SZIE	TOIE	BEIE	CEIE	reserved	DRIE	DTIE	FEIE

Table 8. Overview of LIN channel send frame registers

Address				Register	Bit							
LIN1	LIN2	LIN3	LIN4		7	6	5	4	3	2	1	0
39h	69h	99h	C9h	LC	reserved			WURQ	reserved		ABRQ	HTRQ
3Ah	6Ah	9Ah	CAh	LBI	reserved		ID					
3Bh	6Bh	9Bh	CBh	LBC	reserved			DFL			DIR	CCS
3Ch	6Ch	9Ch	CCh	LCF	CF							
3Dh	6Dh	9Dh	CDh	LBD1	DATA0							
3Eh	6Eh	9Eh	CEh	LBD2	DATA1							
3Fh	6Fh	9Fh	CFh	LBD3	DATA2							
40h	70h	A0h	D0h	LBD4	DATA3							
41h	71h	A1h	D1h	LBD5	DATA4							
42h	72h	A2h	D2h	LBD6	DATA5							
43h	73h	A3h	D3h	LBD7	DATA6							
44h	74h	A4h	D4h	LBD8	DATA7							

Table 9. Overview of LIN channel get status registers

Address				Register	Bit							
LIN1	LIN2	LIN3	LIN4		7	6	5	4	3	2	1	0
4Fh	7Fh	AFh	DFh	LSTATE	RXBSY	reserved			LINS			
50h	80h	B0h	E0h	LES	SZF	TOF	BEF	CEF	reserved			FEF
51h	81h	B1h	E1h	LS	reserved	DRBNE	reserved			DRF	DTF	reserved
52h	82h	B2h	E2h	LCF	CF							
53h	83h	B3h	E3h	LBD1	DATA0							
54h	84h	B4h	E4h	LBD2	DATA1							
55h	85h	B5h	E5h	LBD3	DATA2							
56h	86h	B6h	E6h	LBD4	DATA3							
57h	87h	B7h	E7h	LBD5	DATA4							
58h	88h	B8h	E8h	LBD6	DATA5							
59h	89h	B9h	E9h	LBD7	DATA6							
5Ah	8Ah	BAh	EAh	LBD8	DATA7							

Table 10. Overview of LIN master termination configuration registers

Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F0h	MCFG	M4CFG		M3CFG		M2CFG		M1CFG	
F1h	MMTPS	DFR	FRS	WRCNTS					
F2h	MCFGCRC	CRC							

Table 11. Overview of other registers

Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FEh	MTPCS	MTPCS							
FFh	ID	reserved		ID					

6.8 Non-volatile configuration

6.8.1 Programming non-volatile memory

The SJA1124 contains Multiple Time Programmable (MTP) non-volatile memory (NVM) cells that allow the default configuration of the LIN master pull-up to be programmed.

Programming of the NVM cells is performed in two steps. First, the required values are written to the LIN master pull-up configuration register and, if necessary, the NVM status register (Table 12 and Table 13). The CRC value is then written to the NVM CRC register (Table 14). If the CRC value is correct, programming is confirmed. Otherwise, the operation is aborted. A system reset is generated after a successful NVM programming cycle. Note that the NVM cells cannot be read while they are being programmed.

During NVM programming, the supply voltage must remain within the battery supply voltage operating range.

After an NVM programming cycle has been completed, the non-volatile memory is protected against overwriting. Factory preset values, indicated by '*', need to be restored before the NVM cells can be re-programmed (see Section 6.8.2).

Table 12. LIN master pull-up configuration register (MCFG, address F0h)

Bit	Symbol	Access	Value	Description
7:6	M4CFG	R/W		master termination configuration channel 4
			00	Low Power mode off and Normal mode off
			01	Low Power mode off and Normal mode 10 % accurate
			10*	Low Power mode 25 % accurate and Normal mode 10 % accurate
			11	Low Power mode 10 % accurate and Normal mode 10 % accurate
5:4	M3CFG	R/W		master termination configuration channel 3
			00	Low Power mode off and Normal mode on
			01	Low Power mode off and Normal mode off
			10*	Low Power mode 25 % accurate and Normal mode 10 % accurate
			11	Low Power mode 10 % accurate and Normal mode 10 % accurate
3:2	M2CFG	R/W		master termination configuration channel 2
			00	Low Power mode off and Normal mode off
			01	Low Power mode off and Normal mode 10 % accurate
			10*	Low Power mode 25 % accurate and Normal mode 10 % accurate
			11	Low Power mode 10 % accurate and Normal mode 10 % accurate

Bit	Symbol	Access	Value	Description
1:0	M1CFG	R/W		master termination configuration channel 1
			00	Low Power mode off and Normal mode off
			01	Low Power mode off and Normal mode 10 % accurate
			10*	Low Power mode 25 % accurate and Normal mode 10 % accurate
			11	Low Power mode 10 % accurate and Normal mode 10 % accurate

The MMTPS register contains the MTPNVM write counter value WRCNTS, the factory restore status bit FRS and the disable factory restore bit DFR. The WRCNTS value is incremented with each MTPNVM program cycle until it reaches the maximum value of 3Fh (no overflow). Note that this counter is provided for information only and will not prevent re-programming when it reaches its maximum value.

The FRS signals the device configuration status. Bit DFR can be used to lock the device restore function.

Table 13. NVM status register (MMTPS, address F1h)

Bit	Symbol	Access	Value	Description
7	DFR	R/W		enable/disable facory restore (MTPNVM lock)
			0*	factory restore function enabled
			1	factory restore function disabled
6	FRS	R		factory restore status
			0	device is configured and MTPNVM is protected against overwriting
			1*	device in factory restore state and MTPNVM can be programmed
5:0	WRCNTS	R	[1]	write counter status
			xxh	contains the number of MTPNVM program cycles

[1] Value depends on number of MTPNVM program cycles; initial value is 00h

The cyclic redundancy check value stored in the NVM CRC control register (MCFGCRC, see Table 14) is calculated using the data written to registers MCFG (address F0h) and MMTPS (address F1h).

Table 14. NVM CRC control register (MCFGCRC, address F2h)

Bit	Symbol	Access	Value	Description
7:0	MCFGCRC	R/W		cyclic redundancy check control
			xxh	CRC control data

The CRC value is calculated using the data representation shown in Figure 7 and the modulo-2 division with the generator polynomial: $X^8 + X^5 + X^3 + X^2 + X + 1$. The result of this operation must be bitwise inverted.

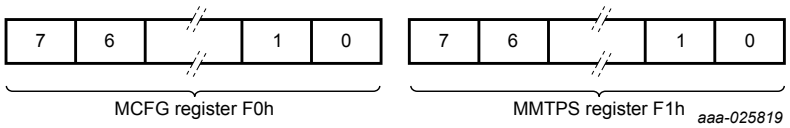


Figure 7. Data representation for CRC calculation

The following parameters can be used to calculate the CRC value (e.g. via the AUTOSAR method):

Table 15. Parameter for CRC coding

Parameter	Value
CRC value	8 bits
Polynomial	2Fh
Initial value	FFh
Input data reflected	no
Result data reflected	no
XOR value	FFh

6.8.2 Restoring factory preset values

Factory preset values are restored by writing 00h to register MCFG (Table 12) and then writing a correct CRC value to register MCFGCRC (Table 14). A minimum delay of $t_{idl(SPI)MTPNVM}$ must be inserted between the two write operations.

The factory restore operation will be aborted if:

- the write operation to MCFGCRC starts before the MTPNV SPI idle time ($t_{idl(SPI)MTPNVM}$) has elapsed.
- any SPI register access is initiated between the MCFG and MCFGCRC write operations
- Factory restore is disabled (DFR = 1)

The SJA1124 performs a system reset after the factory preset values have been restored.

6.9 System control and status registers

Reset values are indicated by '*'.

6.9.1 Mode register

The mode register (MODE) is used to reset the SJA1124 and to select Low Power mode. Operating modes are described in Section 6.2.

Table 16. Mode register (MODE, address 00h)

Bit	Symbol	Access	Value	Description
7	RST[1]	W		device reset
			1*	reset device
			0	no reset
6:1	reserved	R	00h*	
0	LPMODE[1]	W		Low Power mode
			1[2]	switch to Low Power mode
			0*	Normal mode

[1] Bit is cleared automatically after a write operation; reading always returns 0.
[2] The preconditions listed in Section 6.2.2 must be met to trigger a transition to Low Power mode.

6.9.2 PLL configuration register

The SJA1124 uses a Phase-Locked Loop (PLL) to generate a high-frequency clock signal from an external reference clock ($f_{clk(PLL)in}$) on the CLK input pin. The internal PLL output signal ($f_{clk(PLL)out}$; see Section 6.9.2.3) is used as the input clock for the baud rate generators in the LIN master controllers (see Section 6.10.5.5).

6.9.2.1 External clock reference

A good quality input clock is necessary for proper PLL performance. The frequency of the reference clock on pin CLK should be within the specified operating range, $f_{clk(PLL)in}$.

To meet LIN master requirements for baud rate deviation, the tolerance of the external clock reference should be within ±0.3%.

6.9.2.2 PLL in lock

The PLL lock status (PLLIL) can be read from the STATUS register (see Table 24). The PLL is in lock if the deviation from the nominal internal PLL output clock $f_{clk(PLL)out}$ is within $\Delta_{lock(PLL)}$.

The PLL in-lock and out-of-lock interrupts (PLLILI and PLLOLI) in register INT2 (see Table 22) can be enabled via register INT2EN (see Table 19).

6.9.2.3 Selecting the multiplication factor

The PLL output frequency $f_{clk(PLL)out}$ depends on the PLL multiplication-factor M, and can be calculated using the following formula:

$$f_{clk(PLL)out} = M \times f_{clk(PLL)in} \quad (1)$$

Preconfigured settings for M are provided in the PLL configuration register (PLLCFG; Table 17). The settings for M (PLLMULT) are defined for specific input clock frequency ranges to provide sufficient LIN baud rate accuracy.

If the reference frequency, $f_{clk(PLL)in}$, is outside the defined input clock frequency range for the configured PLLMULT setting, bit PLLIFF in the status register is set to signal the failure (see Table 24). A PLL input frequency fail interrupt (PLLIFF) is generated, if enabled via register INT2EN (see Table 19).

Table 17. PLL configuration register (PLLCFG; address 01h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	0h*	
3:0	PLLMULT	R/W		PLL multiplication of input frequency
			0h	$f_{clk(PLL)in}$ = 0.4 MHz to 0.5 MHz multiplication factor: M = 78
			1h	$f_{clk(PLL)in}$ = 0.5 MHz to 0.7 MHz multiplication factor: M = 65

Bit	Symbol	Access	Value	Description
			2h	$f_{clk(PLL)in}$ = 0.7 MHz to 1.0 MHz multiplication factor: M = 39
			3h	$f_{clk(PLL)in}$ = 1.0 MHz to 1.4 MHz multiplication factor: M = 28
			4h	$f_{clk(PLL)in}$ = 1.4 MHz to 1.9 MHz multiplication factor: M = 20
			5h	$f_{clk(PLL)in}$ = 1.9 MHz to 2.6 MHz multiplication factor: M = 15
			6h	$f_{clk(PLL)in}$ = 2.6 MHz to 3.5 MHz multiplication factor: M = 11
			7h	$f_{clk(PLL)in}$ = 3.5 MHz to 4.5 MHz multiplication factor: M = 8.5
			8h	$f_{clk(PLL)in}$ = 4.5 MHz to 6.0 MHz multiplication factor: M = 6.4
			9h	$f_{clk(PLL)in}$ = 6.0 MHz to 8.0 MHz multiplication factor: M = 4.8
			Ah*	$f_{clk(PLL)in}$ = 8.0 MHz to 10.0 MHz multiplication factor: M = 3.9
			other	not used

6.9.3 Interrupt enable registers

The interrupt enable registers (INT1EN, INT2EN, INT3EN) are used to enable interrupt sources. When an enabled interrupt is generated, the associated interrupt status bit (in INT1, INT2 or INT3) is set and pin INTN is forced LOW.

A number of second-level interrupt sources are associated with each of the interrupts in INT3. Second-level interrupts are enabled individually via the LIN interrupt enable registers (Table 35). The status of second-level interrupts can be read from the LIN error status registers (LES, Table 42) and LIN status registers (LS, Table 43).

When a second level interrupt is generated, the associated interrupt status bits in INT3 and LES/LS are set if both the first and second level interrupts are enabled.

Table 18. Interrupt enable register 1 (INT1EN, address 02h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	0h*	
3	L4WUIE	R/W		L4WUI interrupt enable
			1*	enable L4WUI interrupt
			0	disable L4WUI interrupt
2	L3WUIE	R/W		L3WUI interrupt enable
			1*	enable L3WUI interrupt
			0	disable L3WUI interrupt
1	L2WUIE	R/W		L2WUI interrupt enable
			1*	enable L2WUI interrupt

Bit	Symbol	Access	Value	Description
			0	disable L2WUI interrupt
0	L1WUIE	R/W		L1WUI interrupt enable
			1*	enable L1WUI interrupt
			0	disable L1WUI interrupt

Table 19. Interrupt enable register 2 (INT2EN, address 03h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R	0h*	
5	OTWIE	R/W		OTWI interrupt enable
			1	enable OTWI interrupt
			0*	disable OTWI interrupt
4	PLLOLIE	R/W		PLLOLI interrupt enable
			1	enable PLLOLI interrupt
			0*	disable PLLOLI interrupt
3	PLLILIE	R/W		PLLILI interrupt enable
			1	enable PLLILI interrupt
			0*	disable PLLILI interrupt
2	PLLIFFIE	R/W		PLLIFFI interrupt enable
			1	enable PLLIFFI interrupt
			0*	disable PLLIFFI interrupt
1	SPIEIE	R/W		SPIEI interrupt enable
			1	enable SPIEI interrupt
			0*	disable SPIEI interrupt
0	reserved	R	0*	

Table 20. Interrupt enable register 3 (INT3EN, address 04h)

Bit	Symbol	Access	Value	Description
7	L4EIE	R/W		L4EI interrupt enable
			1	enable L4EI interrupt
			0*	disable L4EI interrupt
6	L3EIE	R/W		L3EI interrupt enable
			1	enable L3EI interrupt
			0*	disable L3EI interrupt
5	L2EIE	R/W		L2EI interrupt enable
			1	enable L2EI interrupt
			0*	disable L2EI interrupt

Bit	Symbol	Access	Value	Description
4	L1EIE	R/W		L1EI interrupt enable
			1	enable L1EI interrupt
			0*	disable L1EI interrupt
3	L4SIE	R/W		L4SI interrupt enable
			1	enable L4SI interrupt
			0*	disable L4SI interrupt
2	L3SIE	R/W		L3SI interrupt enable
			1	enable L3SI interrupt
			0*	disable L3SI interrupt
1	L2SIE	R/W		L2SI interrupt enable
			1	enable L2SI interrupt
			0*	disable L2SI interrupt
0	L1SIE	R/W		L1SI interrupt enable
			1	enable L1SI interrupt
			0*	disable L1SI interrupt

6.9.4 Interrupt registers

The top-level interrupts are listed in the interrupt registers (INT1, INT2, INT3). An interrupt is signalled on the open-drain output pin INTN. The status of individual interrupts can be read from the interrupt registers. With the exception of the initialization status (INITI) and low power request fail (LPRFI) interrupts, the interrupts can be enabled and disabled individually via the interrupt enable registers (see Section 6.9.3).

Table 21. Interrupt register 1 (INT1, address 10h)

Interrupt status bits are cleared by writing 1; writing 0 has no effect.

Bit	Symbol	Access	Value	Description
7	INITI	R/W		initialization status interrupt
			1*[1]	device has been initialized
			0	no initialization event detected
6:4	reserved	R	0h*	
3	L4WUI	R/W		LIN 4 wake-up interrupt
			1	wake-up request detected on LIN4
			0*	no wake-up event detected on LIN4
2	L3WUI	R/W		LIN 3 wake-up interrupt
			1	wake-up request detected on LIN3
			0*	no wake-up event detected on LIN3
1	L2WUIE	R/W		LIN 2 wake-up interrupt
			1	wake-up request detected on LIN2
			0*	no wake-up event detected on LIN2

Bit	Symbol	Access	Value	Description
0	L1WUIE	R/W		LIN 1 wake-up interrupt
			1	wake-up request detected on LIN1
			0*	no wake-up event detected on LIN1

[1] INITI must be cleared within $t_{to(idle)INITI}$.

INT2 interrupts signal out-of-range conditions and error states.

Table 22. Interrupt register 2 (INT2, address 11h)

Interrupt status bits are cleared by writing 1; writing 0 has no effect.

Bit	Symbol	Access	Value	Description
7:6	reserved	R	0h*	
5	OTWI	R/W		overtemperature warning interrupt
			1	chip junction temperature warning threshold ($T_{w(otp)}$) exceeded
			0*	chip temperature OK
4	PLLOLI	R/W		PLL out-of-lock interrupt
			1	PLL is out of lock
			0*	no interrupt detected
3	PLLILI	R/W		PLL in-lock interrupt
			1	PLL in-lock detected
			0*	no interrupt event
2	PLLIFFI	R/W		PLL input frequency fail interrupt
			1	PLL input frequency fail detected
			0*	PLL input frequency OK
1	SPIEI	R/W		SPI error interrupt
			1	SPI error detected
			0*	no SPI error detected
0	LPRFI	R/W		low power request fail interrupt
			1	low power request fail detected
			0*	no low power request fail interrupt detected

Interrupt register 3 (INT 3) provides LIN master controller status information. When set, LxEI bits indicate that a LIN error status interrupt has been generated (if enabled; see Section 6.10.7.2) and can be identified via the respective LES register (see Table 42). Bits LxSI are set to indicate that a LIN status interrupt has been generated (if enabled; see Section 6.10.7.3) in the associated LS register (see Table 43). INT 3 is a read-only register. Interrupts are cleared by writing 1 to the associated LES or LS register.

Table 23. Interrupt register 3 (INT3, address 12h)

Interrupts are cleared by writing 1 to the associated LES or LS register.

Bit	Symbol	Access	Value	Description
7	L4EI	R/W		LIN 4 controller error interrupt (LES, address E0h; Table 42)
			1	a LIN controller error status interrupt has been generated in LES addr. E0h
			0*	no LES inhterrupt generated
6	L3EI	R/W		LIN 3 controller error interrupt (LES, address B0h; Table 42)
			1	a LIN controller error status interrupt has been generated in LES addr. B0h
			0*	no LES interrupt generated
5	L2EI	R/W		LIN 2 controller error interrupt (LES, address 80h; Table 42)
			1	a LIN controller error status interrupt has been generated in LES addr. 80h
			0*	no LES2 interrupt generated
4	L1EI	R/W		LIN 1 controller error interrupt (LES, address 50h; Table 42
			1	a LIN controller error status interrupt has been generated in LES addr. 50h
			0*	no LES interrupt generated
3	L4SI	R/W		LIN 4 controller status interrupt (LS, address E1h; Table 43)
			1	a LIN controller status interrupt has been generated in LS addr. E1h
			0*	no LS interrupt generated
2	L3SI	R/W		LIN 3 controller status interrupt (LS, address B1h; Table 43)
			1	a LIN controller status interrupt has been generated in LS addr. B1h
			0*	no LS interrupt generated
1	L2SI	R/W		LIN 2 controller status interrupt (LS, address 81h; Table 43)
			1	a LIN controller status interrupt has been generated in LS addr. 81h
			0*	no LS interrupt generated
0	L1SI	R/W		LIN 1 controller status interrupt (LS, address 51h; Table 43)
			1	a LIN controller status interrupt has been generated in LS addr. 51h
			0*	no LS interrput generated

6.9.5 Status register

The status register is read-only.

Table 24. Status register (STATUS, address 13h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R	0h*	
5	OTW	R		overtemperature warning
			1	chip overtemperature warming thershold ($T_{w(otp)}$) exceeded
			0	chip temperature ok
4	reserved	R		
3	PLLIL	R		PLL lock status
			1	PLL in lock
			0	PLL out of lock
2	PLLIFF	R		PLL input frequency fail status
			1	PLL input frequency failure (outside defined range)
			0	PLL input frequency ok (within defined range)
1:0	reserved	R	0h*	

6.10 LIN master controllers

The SJA1124 contains four LIN master controllers. A LIN master controller performs LIN master frame transfer operations. It is designed to manage a large number of LIN messages efficiently and with minimum SPI traffic. LIN messages are handled autonomously once the LIN frame header transmission has been triggered. The next header transmission request can be handled when the ongoing LIN frame response is transmitted or the checksum is received. The LIN master controller also contains an 8-byte buffer for transmission/reception data, respectively.

Register bit reset values are indicated by '*' in the following sections.

6.10.1 LIN frame transmission

A LIN frame transmission is initiated by setting the LIN header transmission request bit (HTRQ) in the LIN control register (LC; Table 36). On receiving a header transmission request, the LIN master controller transmits a LIN frame header, which includes break, sync and protected identifier fields. Depending on the state of the data direction bit (DIR) in the LIN buffer control register (LBC; Table 38), the LIN master controller either transmits the LIN frame response (DIR = 1: LIN master transmits, LIN slave receives) or expects to receive the LIN frame response from a LIN slave (DIR = 0: LIN slave transmits; LIN master receives).

When the LIN master controller transmits the LIN frame response, the data fields stored in the LIN buffer data registers (LBDx; see Table 40) are transmitted automatically. The data field length (DFL) to be transmitted is configured in the LBC register. Finally, the checksum is transmitted. Depending on the CCD bit in the LIN configuration 1 register (LCFG1; Table 27), the checksum is either hardware-generated or needs to be stored

in the LIN checksum field register (LCF; Table 39) by the user. If the checksum is generated automatically, the checksum type (enhanced or classic) can be configured via the CCS bit in the LBC register.

Once LIN header transmission begins, the user should not modify register bits in the LIN buffer identifier (LBI; Table 37) and LIN buffer control (LBC; Table 38) registers until the frame transmission has been completed. The transmitted LIN frame identifier and data are also received by the LIN master controller and copied, respectively, to LBI and LBDx.

When the LIN master controller receives the LIN frame response, the received data fields are stored in LBDx. The expected data field length is configured via bits DFL. The received checksum is stored in the LCF register. If the CCD bit is logic 0, the checksum is calculated autonomously and compared with the received checksum field. The type of checksum calculation (enhanced or classic) depends on the CCS bit.

At the end of a LIN frame transmission, either a data transmission complete flag (DTF) or a data reception complete flag (DRF) is signaled in the LIN status register (LS; see Table 43).

LIN frame transmission is aborted when an error is detected. Instead of DTF or DRF, the corresponding error flag is set in the LIN error status register (LES; Table 42).

Except for the data reception buffer not empty flag (DRBNE), all LS and LES status flags can be enabled for interrupt handling via the LIN interrupt enable (LIE; seeTable 35) and Interrupt 3 enable (INT3EN; Table 20) registers.

6.10.2 LIN receiver bit timing

A LIN byte field contains 10 bits: the dominant start bit followed by 8 data bits and the recessive stop bit. The baud rate generator determines the sample rate (see Section 6.10.5.5). Sampling of each LIN bit consists of 16 baud rate generator output cycles (see Figure 8). The bit time, t_{bit}, is the nominal time needed to transmit one bit.

The LIN receiver synchronizes with the falling edge of the start bit in a LIN byte field, to an accuracy of t_{BFS} (equal to 1 baud rate generator output clock cycle). The bit level is obtained by taking three samples in the middle of the bit (between t_{EBS} and t_{LBS}; see Figure 8). If two or more samples are logic 1, the bit level is taken as one. Otherwise it is 0.

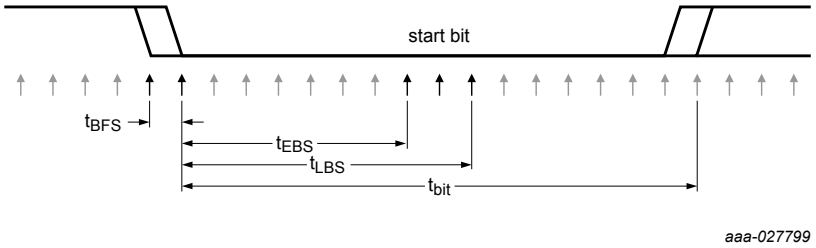


Figure 8. LIN bit sample timing

6.10.3 LIN controller registers

The LIN master controller has associated global and channel registers. The global registers are listed in Table 6. The LIN master controller channel registers are listed in the initialization, send frame and get status registers (Table 7, Table 8 and Table 9).

6.10.4 LIN communication registers

LIN high-speed mode can be enabled to support baud rates higher than 20 kBd (see section Section 6.2.3.4) via bits LxHS in the LIN master controller communication register 1 (LCOM1). Pin TMF can be enabled per LIN channel via bits LxTMFE for synchronous LIN header transmission (see Section 6.4).

Table 25. LIN communication register 1 (LCOM1, address 20h)

Bit	Symbol	Access	Value	Description
7	L4HS	R/W		LIN high-speed mode for LIN 4
			1	enable LIN high-speed mode for LIN 4
			0*	disable LIN high-speed mode for LIN 4
6	L3HS	R/W		LIN high-speed mode for LIN 3
			1	enable LIN high-speed mode for LIN 3
			0*	disable LIN high-speed mode for LIN 3
5	L2HS	R/W		LIN high-speed mode for LIN 2
			1	enable LIN high-speed mode for LIN 2
			0*	disable LIN high-speed mode for LIN 2
4	L1HS	R/W		LIN high-speed mode for LIN 1
			1	enable LIN high-speed mode for LIN 1
			0*	disable LIN high-speed mode for LIN 1
3	L4TMFE	R/W		LIN transmit frame input (TMF) enable for LIN 4
			1[1]	enable TMF for LIN 4
			0*	disable TMF for LIN 4
2	L3TMFE	R/W		LIN transmit frame input (TMF) enable for LIN 3
			1[1]	enable TMF for LIN 3
			0*	disable TMF for LIN 3
1	L2TMFE	R/W		LIN transmit frame input (TMF) enable for LIN 2
			1[1]	enable TMF for LIN 2
			0*	disable TMF for LIN 2
0	L1TMFE	R/W		LIN transmit frame input (TMF) enable for LIN 1
			1[1]	enable TMF for LIN 1
			0*	disable TMF for LIN 1

[1] After setting LxTMFE, the SPI processing delay time $t_{d(SPI)}$ should be considered before triggering a LIN header transmit request via TMF.

Bits LxHTRQ in table LCOM2 are used to initiate LIN header transmission.

Table 26. LIN communication register 2 (LCOM2, address 21h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	0h*	
3	L4HTRQ	R/W		LIN header transmission request for LIN 4

Bit	Symbol	Access	Value	Description
			1[1]	initiate LIN header transmission for LIN 4
			0*	no LIN header transmission for LIN 4
2	L3HTRQ	R/W		LIN header transmission request for LIN 3
			1[1]	initiate LIN header transmission for LIN 3
			0*	no LIN header transmission for LIN 3
1	L2HTRQ	R/W		LIN header transmission request for LIN 2
			1[1]	initiate LIN header transmission for LIN 2
			0*	no LIN header transmission for LIN 2
0	L1HTRQ	R/W		LIN header transmission request for LIN 1
			1[1]	initiate LIN header transmission for LIN 1
			0*	no LIN header transmission for LIN 1

[1] Bit LxHTRQ is cleared automatically after a write operation; reading register LCOM2 always returns 0.

6.10.5 LIN channel initialization registers

6.10.5.1 LIN configuration registers

LIN configuration register 1 (LCFG1) is used to select the operating mode, configure the LIN master break length and to enable/disable the hardware checksum.

Table 27. LIN configuration registers 1 (LCFG1, addresses 30h, 60h, 90h, C0h)

Bit	Symbol	Access	Value	Description
7	CCD[1]	R/W		checksum calculation disable
			1	disable hardware checksum calculation; LCF is read/write
			0*	enable hardware checksum calculation; LCF is read-only
6:3	MBL[1]	R/W		LIN master break length
			0h*	10 bits
			1h	11 bits
			2h	12 bits
			3h	13 bits
			4h	14 bits
			5h	15 bits
			6h	16 bits
			7h	17 bits
			8h	18 bits
			9h	19 bits
			Ah	20 bits

Bit	Symbol	Access	Value	Description
			Bh	21 bits
			Ch	22 bits
			Dh	23 bits
			Eh	36 bits
			Fh	50 bits
2	reserved	R	0*	
1	SLEEP	R/W		LIN mode select
			1*	select LIN Sleep mode
			0	select LIN Normal mode
0	INIT[2]	R/W		initialization request
			1	LIN Initialization mode
			0*	LIN Normal mode

[1] This field can only be overwritten in LIN Initialization mode.
[2] This bit is ignored and handled internally if bit SLEEP is set.

LIN configuration register 2 (LCFG2) is used to configure the sync break delimiter and to determine how the transmitter state machine responds to bit error events. Note that a write access to this register resets the LIN control register (LC; see Table 36).

Table 28. LIN configuration registers 2 (LCFG2, address 31h, 61h, 91h, C1h)

Bit	Symbol	Access	Value	Description
7	TBDE[1]	R/W		2-bit delimiter
			1	2-bit delimiter
			0*	1-bit delimiter
6	IOBE[1]	R/W		idle on bit error
			1*	bit error resets LIN state machine
			0	bit error does not reset LIN state machine
5:0	reserved	R	0h*	

[1] This field can only be overwritten in LIN Initialization mode.

6.10.5.2 LIN idle timeout control registers

The behavior on a LIN idle timeout event is configured via the LIN idle timeout control register (LITC).

Table 29. LIN idle timeout control registers (LITC; addresses 32h, 62h, 92h, C2h)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	00h*	
1	IOT[1]	R/W		idle on timeout
			1*	idle on timeout event resets LIN state machine
			0	no reset

Bit	Symbol	Access	Value	Description
0	reserved	R	0*	

[1] This field can only be overwritten in LIN Initialization mode.

6.10.5.3 LIN global control registers

The LIN global control register (LGC) provides the option to extend the number of stop bits (STOP) and to initiate a soft reset (SR).

STOP determines the number of stop bits in the transmitted data. The STOP bit is configured for all fields (Delimiter, Sync, ID, Checksum and payload). Setting bit SR to 1 executes a soft reset of the LIN master controller (FSMs, timers, status and error registers) without modifying the configuration registers. All LS and LES status bits are reset by a soft reset.

Table 30. LIN global control registers (LGC; addresses 33h, 63h, 93h, C3h)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	00h*	
1	STOP[1]	R/W		stop bit configuration
			1	two stop bits
			0*	one stop bit
0	SR[1][2]	R/W		LIN controller soft reset control
			1	soft reset of LIN controller
			0*	no reset

[1] Field can be written only in LIN Initialization mode.
[2] This bit must be cleared via software (it is not cleared by hardware).

6.10.5.4 LIN response timeout control registers

The RTO field in the LIN response timeout control register (LRTC) defines the time limit for receiving the complete LIN frame response (including checksum). The time base for the timeout timer is bit time t_{bit}, the nominal time required to transmit one bit.

The timer starts at the end of the LIN frame header (i.e. at the end of the stop bit of the protected identifier field).

$$t_{RESPONSE\_MAX} = RTO \times (DFL + 2) \times t_{bit} = (RTO / 10) \times t_{RESPONSE\_MIN} \quad (2)$$

Table 31. LIN response timeout control register (LRTC; 34h, 64h, 94h, C4h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	0h*	
3:0	RTO	R/W		response timeout time
			xh[1]	response time limit in bit time for one byte

[1] The reset value is 0Eh = 14, corresponding to $t_{RESPONSE\_MAX} = 1.4 \times t_{RESPONSE\_MIN}$

6.10.5.5 LIN baud rate generator registers

The LIN baud rate is specified as an unsigned fixed-point number. The mantissa is coded as a 16-bit integer value (IBR) and the fraction is coded as a 4-bit fractional value (FBR).

IBR is split between two registers: the LIN baud rate generator MSB register (LBRM; Table 33) contains the 8 most significant bits; the LIN baud rate generator LSB register (LBRL; Table 34) contains the 8 least significant bits.

FBR is defined in the LIN fractional register (LFR; Table 32).

The output frequency of the baud rate generator is 16 times the baud rate. The input frequency of the baud rate generator is the PLL output clock frequency $f_{clk(PLL)out}$.

The baud rate can be calculated from the following formula:

$$baudrate = \frac{f_{clk(PLL)out}}{16 \times IBR + FBR} \quad (3)$$

The baud rate deviation (ΔBR) from the nominal baud rate (BR_{nom}) depends on the PLL output clock frequency and the nominal baud rate. The baud rate deviation (ΔBR) can be calculated from the nominal baud rate (BR_{nom}) using the following equation:

$$\Delta BR / BR_{nom} = \frac{|BR - BR_{nom}|}{BR_{nom}} \times 100 \leq \frac{BR_{nom}}{f_{clk(PLL)out}} \times 50\,\% \quad (4)$$

Table 32. LIN fractional registers (LFR; 35h, 65h, 95h, C5h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	0h*	
3:0	FBR[1]	R/W		fractional baud rate
			xh	4-bit fraction value of baud rate

[1] Field can be written only in LIN Initialization mode.

Table 33. LIN baud rate generator MSB registers (LBRM; 36h, 66h, 96h, C6h)

Bit	Symbol	Access	Value	Description
7:0	IBR[15:8][1]	R/W		integer baud rate
			xxh[2]	MSB of baud rate integer value

[1] Field can be written only in LIN Initialization mode.
[2] The LIN clock is disabled at the reset value of IBR[15:0] = 0000h.

Table 34. LIN baud rate generator LSB registers (LBRL; 37h, 67h, 97h, C7h)

Bit	Symbol	Access	Value	Description
7:0	IBR[7:0][1]	R/W		integer baud rate
			xh[2]	LSB of baud rate integer value

[1] Field can be written only in LIN Initialization mode.
[2] The LIN clock is disabled at the reset value of IBR[15:0] = 0000h.

6.10.5.6 LIN interrupt enable register

The LIN interrupt enable register (LIE) is used to enable the LIN master controller interrupt sources. The status of the interrupts can be read from the LIN error status register (LES) and LIN status register (LS).

Table 35. LIN interrupt enable register (LIE; 38h, 68h, 98h, C8h)

Bit	Symbol	Access	Value	Description
7	SZIE	R/W		stuck-at-zero interrupt enable; generated when SZF flag in LES register (Table 42; bit 7) is set
			1	enable stuck-at-zero (SZ) interrupt
			0*	disable stuck-at-zero (SZ) interrupt
6	TOIE	R/W		timeout interrupt enable; generated when TOF flag in LES register (Table 42; bit 6) is set
			1	enable timeout error (TO) interrupt
			0*	disable timeout error (TO) interrupt
5	BEIE	R/W		bit error interrupt enable; generated when BEF flag in LES register (Table 42; bit 5) is set
			1	enable bit error (BE) interrupt
			0*	disable bit error (BE) interrupt
4	CEIE	R/W		checksum error interrupt enable; generated when CEF flag in LES register (Table 42; bit 4) is set
			1	enable checksum error (CE) interrupt
			0*	disable checksum error (CE) interrupt
3	reserved	R	0*	
2	DRIE	R/W		data reception complete interrupt enable; generated when DRF flag in LS register (Table 43, bit 1) is set
			1	enable data reception (DR) interupt
			0*	disable data reception (DR) interupt
1	DTIE	R/W		data transmission complete interrupt enable; generated when DTF flag in LS register (Table 43, bit 1) is set
			1	enable data transnission (DT) interrupt
			0*	disable data transnission (DT) interrupt
0	FEIE	R/W		frame error interrupt enable; generated when FEF flag in LES register (Table 42; bit 0) is set
			1	enable frame error (FE) interrupt
			0*	disable frame error (FE) interrupt

6.10.6 LIN channel send frame registers

6.10.6.1 LIN control registers

A wake-up request is generated by writing the wake-up character to LIN buffer data register 1 (LBD1; see Section 6.10.6.5) and setting bit WURQ to 1. The data written to LBDx is transmitted when WURQ is set. The current LIN frame transmission can be aborted by setting bit ARBQ. A LIN header transmission is initiated by setting bit HTRQ. If bit DIR in register LBC is set (see Table 38), the LIN frame response transmission follows automatically.

Table 36. LIN control registers (LC; 39h, 69h, 99h, C9h)

Bit	Symbol	Access	Value	Description
7:5	reserved	R	0h	
4	WURQ[1]	R/W		wake-up generate request
			1[2]	generate wake-up pulse
			0*	no wake-up pulse
3:2	reserved	R	00*	
1	ABRQ	R/W		abort request
			1[3]	abort the current transmission or wake-up; aborts at the end of current bit
			0*	no abort request
0	HTRQ	R/W		LIN header transmission request
			1[2]	generate LIN header transmission
			0*	no LIN header transmission

[1] Bit error is not checked when transmitting the wake-up request.
[2] Cleared by hardware when the request has been completed or on abort request.
[3] Cleared by hardware when the transmission has been aborted. If both HTRQ and ABRQ are set at the same time, then ABRQ has no effect.

6.10.6.2 LIN buffer identifier registers

The LIN buffer identifier registers contain the LIN frame identifiers.

Table 37. LIN buffer identifier registers (LBI; 3Ah, 6Ah, 9Ah, CAh)

Bit	Symbol	Access	Value	Description
7:6	reserved	R	00*	
5:0	ID	R/W	00h*	LIN frame identifier of the protected identifier field, without parity

6.10.6.3 LIN buffer control registers

The LIN buffer control registers are used to configure the LIN checksum version (classic or enhanced), the LIN message response direction (from master to slave or vice versa) and the data field length (number of data bytes to be transferred).

Table 38. LIN buffer control registers (LBC; 3Bh, 6Bh, 9Bh, CBh)

Bit	Symbol	Access	Value	Description
7:5	reserved	R	0h*	
4:2	DFL	R/W	0h*	data field length (DFL = number of data bytes -1)
1	DIR	R/W		direction of LIN frame response
			1	LIN frame response from master to slave (i.e. LIN master controller transmits LIN frame response)
			0*	LIN frame response from slave to master (i.e. LIN master controller expects to receive LIN frame response)
0	CCS	R/W		classic checksum
			1	classic checksum calculation; without protected identifier
			0*	enhanced checksum calculation; with protected identifier

6.10.6.4 LIN checksum field register

When the LIN master controller is transmitting the LIN frame response fields (DIR = 1), the checksum value to be transmitted onto the LIN bus is stored in the LCF register. When the LIN master controller is receiving the response fields (DIR = 0), the checksum received from the slave is stored in the LCF register.

If the checksum calculation disable bit (CCD) in LIN configuration register 1 (LCFG1) is 0, LCF is read only. If CCD is logic 1, write access to the LCF register is enabled and the checksum must be allocated by the microcontroller.

The LCF checksum data can be accessed via two addresses to support send frame and get status requests via a single SPI access. The register mapping is listed in Table 8 (LCF; 3Ch, 6Ch, 9Ch, CCh) and Table 9 (LCF; 52h, 82h, B2h, E2h). For example, the LCF register addresses of LIN channel 2 are 6Ch and 82h.

Table 39. LIN checksum field registers (LCF, address 52h, 82h, B2h, E2h)

Bit	Symbol	Access	Value	Description
7:0	CF	R/W[1]	00h*	hardware (CCD = 0) or software (CCD = 1) calculated checksum value

[1] The LCF register is read-only if CCD = 0.

6.10.6.5 LIN buffer data registers

The LIN buffer data registers are used to allocate LIN data bytes for LIN response transmission or to read LIN bytes after a LIN message response has been received.

Each register can be accessed via two addresses to support send frame and get status requests via a single SPI access. The register mapping is listed in Table 8 (LBD1 to LBD8; 3D to 44h, 6D to 74h, 9D to A4h, CD to D4h) and Table 9 (LBD1 to LBD8; 53 to 5Ah, 83 to 8Ah, B3 to BAh, E3 to EAh). For example, the LBD2 register addresses of LIN channel 3 are 9Eh and B4h.

Table 40. LIN buffer data registers (LBD1 to LBD8)

Bit	Symbol	Access	Value	Description
7:0	DATAx	R/W	00h*	LIN frame response data byte.

6.10.7 LIN channel get status registers

6.10.7.1 LIN state registers

Bit LINS in the LIN state register (LSTATE) indicate the current status of the LIN state machine. Bit RXBYS is set after header reception (if bit DIR = 0 in register LBC, Table 38), to indicate that the receiver is busy. This bit is not an interrupt source.

Table 41. LIN state registers (LSTATE, addresses 4Fh, 7Fh, AFh, DFh)

Bit	Symbol	Access	Value	Description
7	RXBSY	R		receiver busy flag
			1	reception ongoing
			0*	receiver is idle
6:4	reserved	R	0h*	
3:0	LINS	R	xh[1]	LIN state
			0000*	LIN channel in LIN Sleep mode
			0001	LIN channel in LIN Initialization mode
			0010	LIN idle mode [2]
			0011	sync break transmission ongoing
			0100	sync break transmission has been completed and sync delimiter transmission is ongoing
			0101	sync field transmission ongoing
			0110	identifier transmission ongoing
			0111	header transmitted
			1000	response reception ongoing in receiver mode; response transmission ongoing in transmitter mode
			1001	data transmission/reception completed, checksum transmission/reception ongoing

[1] The LINS bits are captured when the bit error flag (BEF; see Table 42) is set and released again when the flag is cleared.
[2] This mode is entered when bits SLEEP and INIT in LIN configuration register 1 (Table 27) are reset by software, a wake-up pulse has been received, or previous frame transmission/reception has been completed/aborted

6.10.7.2 LIN error status registers

The LIN error status registers (LES) contains a number of interrupt sources.

If a dominant pulse lasts for 100 bits or more, bit SZF is set. If the same dominant pulse persists, subsequent SZF settings will be 87 bit times apart (instead of 100 bit times). An interrupt is generated (bit LxEI in INT3 = 1; see Table 23) if bits SZIE in LIE (see Table 35) and LxEIE in INT3EN (see Table 20) are set to enable the interrupt.

The TOF error flag is set when the response timeout value (RTO) is exceeded. The LIN state machine resets to Idle state when this bit and bit IOT in LITC (Table 29) are set. An LxEI interrupt is generated if bit TOIE in LIE and LxEIE in INT3EN are set.

The BEF error flag is set in transmission mode when the value read back from the bus is different from the value transmitted. Bit error is not checked during break field transmission. Transmission of the frame is stopped after the corrupted bit is detected if the IOBE bit in LCFG2 (Table 28) is set. If IOBE is reset, the transmitter continues to transmit in spite of the bit error. An LxEI interrupt is generated if bit BEIE in LIE and LxEIE in INT3EN are set.

The CEF error flag is set when the checksum computed by hardware does not match the received checksum. The received frame is discarded and the LIN master controller returns to idle state. An LxEI interrupt is generated if bits CEIE in LIE and LxEIE in INT3EN are set.

The FEF error flag is set when a dominant state is sampled on a stop bit of the currently received character (sync field, identifier field, data field, checksum field). The received frame is discarded and the LIN master controller returns to idle state. An LxEI interrupt is generated if bits FEIE in LIE and LxEIE in INT3EN are set.

Table 42. LIN error status registers (LES, addresses 50h, 80h, B0h, E0h)

Error status bits are cleared by writing logic 1; writing logic 0 has no effect.

Bit	Symbol	Access	Value	Description
7	SZF	R/W		stuck at zero flag
			1[1]	stuck-at-zero timeout error detected
			0*	no error
6	TOF	R/W		timeout error flag
			1[2]	timeout error detected
			0*	no error
5	BEF	R/W		bit error flag
			1[2]	bit error detected
			0*	no error
4	CEF	R/W		checksum error flag
			1[2][3]	checksum error detected
			0*	no error
3:1	reserved	R	0h*	
0	FEF	R/W		frame error flag
			1[2]	framing error (invalid stop bit) detected
			0*	no error

[1] Bit set when stuck-at-zero error detected; bit should be reset by software.
[2] Reset by hardware in LIN Initialization mode (LCFG1[INIT] = 1).
[3] CEF is never set if checksum calculation is disabled (LCFG1[CCD] = 1).

6.10.7.3 LIN status registers

The LIN status registers (LS) reflect the status of the LIN frame transmission. It contains two LIN frame transfer status interrupt sources.

If the LIN frame response was received successfully, bit DRF is set by hardware. This bit should then be cleared by software. If an error is detected the DRF flag is not set and the corresponding error flag is set in the LIN error status register (see section 8.10.8.2). An interrupt is generated (bit LxSI in INT3 = 1; see Table 23 if bits DRIE in LIE (see Table 35) and LxSIE in INT3EN (see Table 20) are set to enable the interrupt.

If the LIN frame response was sent successfully, DTF is set by hardware (and should be cleared by software). If an error is detected when IOBE is set in LCFG2, the DTF flag is not set and the corresponding error flag is set in the LES register. An LxSI interrupt is generated if bits DTIE in LIE and LxSIE in INT3EN are set.

Bit DRBNE is set by hardware as soon as the first byte of the LIN frame response has been received and stored in LBD1 (when there is at least one data byte in the reception buffer). It is also set when the LIN frame response is transmitted, i.e. DIR is set in LBC. It should be cleared after reading all the buffers. This flag could be checked after a response timeout event.

Table 43. LIN status registers (LS, addresses 51h, 81h, B1h, E1h)

Status bits are cleared by writing logic 1; writing logic 0 has no effect.

Bit	Symbol	Access	Value	Description
7	reserved	R	0*	
6	DRBNE	R/W		data reception buffer not empty flag
			1[1]	first data byte of response received
			0*	no data byte received
5:3	reserved	R	0h*	
2	DRF	R/W		data reception complete flag
			1[1][2]	data reception completed
			0*	data reception not completed
1	DTF	R/W		data transmission complete flag
			1[1][3]	data transmission completed
			0*	data transmission not completed
0	reserved	R	0*	

[1] Reset by hardware in LIN Initialization mode (LCFG1[INIT] = 1).
[2] This flag is not set if a framing or checksum error is detected.
[3] This flag is not set if a bit error occurs and idle on bit error is set (LCFG2[IOBE] = 1).

6.10.8 Operation during automotive cranking pulses

The SJA1124 remains fully operational during automotive cranking pulses because the LIN device is specified down to V_{BAT} = 5 V.

6.10.9 Operation when supply voltage is outside specified operating range

If V_{BAT} > 28 V or V_{BAT} < 5 V, the SJA1124 may remain operational, but parameter values cannot be guaranteed to remain within the operating ranges specified in Table 46 and Table 47.

If the voltage on pin BAT drops below the power-off detection threshold, $V_{th(det)poff}$, the SJA1124 switches to Off mode (see Section 6.2.1).

In Normal mode:

- If the input levels on pins LINx are recessive, the internal receiver outputs will signal recessive.
- If the LIN master controller is not transmitting, the LIN transmitter outputs on pin LINx will be recessive.

6.10.10 LIN dominant timeout function

Each LIN channel has a LIN dominant timeout function. This function switches off the relevant LIN master termination resistor, R_{master} or $R_{master(lp)}$, if the LIN bus level remains dominant for longer than $t_{to(dom)LIN}$. LIN termination resistor R_{slave} remains active as pull-up when R_{master} or $R_{master(lp)}$ is switched off.

Once the LIN bus level is recessive again, the LIN master termination is switched on and the LIN dominant timeout timer is reset.

6.10.11 LIN master pull-up

In Normal mode, the default configuration of the integrated LIN master termination resistor, R_{master}, is a trimmed pull-up of 1 kΩ with a tolerance of ±10 %. In Low Power mode, an untrimmed LIN master termination, $R_{master(lp)}$, is enabled. $R_{master(lp)}$ is a 1.2 kΩ pull-up resistor with a tolerance of ±25 %.

The LIN channel termination depends on the LIN master pull-up configuration. Four configurations are available:

- Off in all states, i.e. terminated with R_{slave}
- R_{master} in Normal mode and off in Low Power mode; Terminated with R_{slave} in Low Power mod
- R_{master} in Normal mode and $R_{master(lp)}$ in Low Power mode
- R_{master} in Normal and Low Power modes.

6.10.12 Fail-safe features

A loss of power (pins BAT and GND) has no impact on the bus lines or on the microcontroller. When battery supply is lost, reverse current $I_{BUS\_NO\_BAT}$ flows from the bus into pins LINx. When the ground connection is lost, current $I_{BUS\_NO\_GND}$ continues to flow from BAT to LINx via an integrated LIN termination resistor, R_{slave}. The current path through the LIN master termination is disabled.

The output driver of each LINx pin is protected against overtemperature conditions (see Section 6.2.5).

7 Limiting values

Table 44. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to pin GND, unless otherwise specified. Positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Max	Unit
V_x [1]	voltage on pin x	pins BAT, INHN		-0.3	+43	V
		pin VIO		-0.3	+6	V
		pins SCSN, SDO, SDI, SCK, INTN, CLK, STAT, TMF		-0.3	V_{IO} + 0.3	V
					+6	V
		pins LINx with respect to any other pin		-43	+43	V
I_{INHN}	input current on pin INHN				3	mA
V_{trt}	transient voltage	on pin BAT with inverse-polarity protection diode and 22 µF capacitor to ground on pins LIN1, LIN2, LIN3, LIN4 coupled via 1 nF capacitor	[2]	-150	+100	V
V_{ESD}	electrostatic discharge voltage	IEC61000-4-2	[3]			
		on pins LIN1, LIN2, LIN3 and LIN4; on pin BAT with capacitor		-6	+6	kV
		Human Body Model (HBM)	[4]			
		on pins LIN1, LIN2, LIN3 and LIN4	[5]	-6	+6	kV
		on pin BAT, INHN		-4	+4	kV
		on pins SCSN, SDO, SDI, SCK, INTN, CLK, STAT, TMF		-2	+2	kV
		Charged Device Model	[6]			
		all pins		-500	+500	V
T_{vj}	virtual junction temperature		[7]	-40	+150	°C
T_{stg}	storage temperature			-55	+150	°C

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.
[2] According to ISO 7637 part 2 automotive transient test pulses 1, 2a, 3a and 3b.
[3] Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor.
[4] According to AEC-Q100-002; equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
[5] BAT and VIO connected to GND, emulating the application circuit.
[6] According to AEC-Q100-011.
[7] Junction temperature in accordance with IEC 60747-1. An alternative definition is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$, where $R_{th(vj-a)}$ is a fixed value. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

8 Thermal characteristics

Table 45. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	DHVQFN24; four-layer	[1]	51	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 µm) and thermal via array under the exposed pad connected to the first inner copper layer

9 Static characteristics

Table 46. Static characteristics

T_{vj} = -40 °C to +150 °C; V_{BAT} = 5.0 V to 28 V; V_{IO} = 2.97 V to 5.5 V; all voltages are referenced to pin GND; positive currents flow into the IC; typical values are given at V_{BAT} = 12 V; unless otherwise specified [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{BAT}	battery supply voltage	operating range	5	-	28	V
V_{IO}	supply voltage on pin VIO	for I/O level adapter; operating range	2.97	-	5.5	V
I_{BAT}	battery supply current	Low Power mode; all channels; bus recessive; MxCFG = 00 or 01; V_{LINx} = V_{BAT}; -40 °C < T_{vj} < 85 °C [2]	-	6	15	µA
		Low Power mode; additional current per LIN channel with MxCFG = 10; V_{LINx} = V_{BAT}; -40 °C < T_{vj} < 85 °C [2]	-	1.3	2.2	µA
		Low Power mode; additional current per LIN channel with MxCFG = 11; V_{LINx} = V_{BAT}; -40 °C < T_{vj} < 85 °C [2]	-	3.7	11	µA
		Normal mode; all LIN channels in LIN Normal mode; bus recessive; V_{LINx} = V_{BAT}	-	12	22	mA
		Normal mode; MCFG = AAh; all LIN channels are in LIN Normal mode; bus dominant; V_{LINx} = 0 V; V_{BAT} = 12 V	-	66	87	mA
I_{IO}	supply current on pin VIO	Low Power mode; -40 °C < T_{vj} < 85 °C	-	6	9	µA
		Normal mode	-	-	1	mA
Supply undervoltage; pins BAT and VIO						
$V_{th(det)poff}$	power-off detection threshold voltage		4.0	-	4.51	V
$V_{th(det)pon}$	power-on detection threshold voltage		4.25	-	4.77	V
$V_{hys(det)pon}$	power-on detection hysteresis voltage		200	-	-	mV
$V_{uvd(VIO)}$	undervoltage detection voltage on pin VIO		2.7	2.8	2.9	V
$V_{uvr(VIO)}$	undervoltage recovery voltage on pin VIO		2.8	2.9	3.1	V
$V_{uvhys(VIO)}$	undervoltage hysteresis voltage on pin VIO		50	-	-	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Serial peripheral interface inputs; pins SDI and SCK; all measurements taken in Normal mode						
$V_{th(sw)}$	switching threshold voltage		$0.25V_{IO}$	-	$0.75V_{IO}$	V
$V_{th(sw)hys}$	switching threshold voltage hysteresis		$0.035V_{IO}$	-	-	V
R_{pd}	pull-down resistance	$V_{I(SPI)} < 0.25\ V_{IO}$	38	60	88	kΩ
R_{pu}	pull-up resistance	$V_{I(SPI)} > 0.75\ V_{IO}$	38	60	88	kΩ
Serial peripheral interface input; pin SCSN						
$V_{th(sw)}$	switching threshold voltage		$0.25V_{IO}$	-	$0.75V_{IO}$	V
$V_{th(sw)hys}$	switching threshold voltage hysteresis		$0.035V_{IO}$	-	-	V
R_{pu}	pull-up resistance		38	60	88	kΩ
Serial peripheral interface data output; pin SDO; all measurements taken in Normal mode						
V_{OH}	HIGH-level output voltage	I_{OH} = -4 mA	$V_{IO} – 0.4$			V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA			0.4	V
$I_{LO(off)}$	off-state output leakage current	V_O = 0 V to V_{IO}; $V_{SCSN} = V_{IO}$	-5		+5	µA
Interrupt output; pin INTN; all measurements taken in Normal mode						
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA			0.4	V
$R_{pu(INTN)}$	pull-up resistance on pin INTN		40	60	80	kΩ
$I_{LO(off)}$	off-state output leakage current	$V_{INTN} = V_{IO}$; V_O = 0 V to V_{IO}	-5		+5	µA
Clock input for PLL; pins CLK and TMF; all measurements taken in Normal mode						
$V_{th(sw)}$	switching threshold voltage		$0.25V_{IO}$	-	$0.75V_{IO}$	V
$V_{th(sw)hys}$	switching threshold voltage hysteresis		$0.035V_{IO}$	-	-	V
$R_{pd(CLK)}$	pull-down resistance on pin CLK	$V_{CLK} < 0.25\ V_{IO}$	38	60	88	kΩ
$R_{pu(CLK)}$	pull-up resistance on pin CLK	$V_{CLK} > 0.75\ V_{IO}$	38	60	88	kΩ
Status output; pin STAT						
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA			0.4	V
$I_{LO(off)}$	off-state output leakage current	V_O = 0 V to V_{IO}; $V_{STAT} = V_{IO}$	-5		+5	µA
Inhibit output; pin INHN						
V_{OL}	LOW-level output voltage	I_{OL} = 0.2 mA			0.4	V
$I_{LO(off)}$	off-state output leakage current		-5		+5	µA
LIN bus line; pins LIN1, LIN2, LIN3, LIN4						
$V_{O(dom)}$	dominant output voltage	Normal mode; V_{BAT} = 7.0 V	-	-	1.4	V
		Normal mode; V_{BAT} = 18.0 V	-	-	3.6	V
I_{BUS_LIM}	current limitation for driver dominant state	V_{BAT} = 18 V; V_{LINx} = 18 V; LIN driver on; R_{master} off	40	-	200	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{BUS\_PAS\_dom}$	receiver dominant input leakage current including pull-up resistor	V_{BAT} = 12 V; V_{LINx} = 0 V; LIN driver off; R_{master} off	-1	-	-	mA
		V_{BAT} = 28 V; V_{LINx} = 0 V; LIN driver off; R_{master} off	-1.5	-	-	mA
$I_{BUS\_PAS\_rec}$	receiver recessive input leakage current	5 V < V_{BAT} < 18 V; 5 V < V_{LINx} < 18 V; $V_{LINx} \geq V_{BAT}$; LIN driver off	-	-	20	µA
		18 V < V_{BAT} < 28 V; 18 V < V_{LINx} < 28 V; $V_{LINx} \geq V_{BAT}$; LIN driver off	-	-	30	µA
$I_{BUS\_NO\_GND}$	loss-of-ground bus current	V_{BAT} = 12 V; V_{GND} = V_{BAT}; 0 V < V_{LINx} < 18 V [2]	-1	-	+1	mA
		V_{BAT} = 12 V; V_{GND} = V_{BAT}; 0 V < V_{LINx} < 28 V [2]	-1.5	-	+1.5	mA
$I_{BUS\_NO\_BAT}$	loss-of-battery bus current	V_{BAT} = 0 V; 0 V < V_{LINx} < 28 V [2]	-	-	30	µA
V_{BUSdom}	receiver dominant state		-	-	$0.4V_{BAT}$	V
V_{BUSrec}	receiver recessive state		$0.6V_{BAT}$	-	-	V
V_{BUS_CNT}	receiver center voltage	Normal mode; V_{BUS_CNT} = (V_{th_rec} + V_{th_dom}) / 2; 7 V ≤ V_{BAT} < 28 V [3]	$0.475V_{BAT}$	$0.5V_{BAT}$	$0.525V_{BAT}$	V
		Normal mode; V_{BUS_CNT} = (V_{th_rec} + V_{th_dom}) / 2; 5 V < V_{BAT} < 7 V	$0.45V_{BAT}$	$0.5V_{BAT}$	$0.55V_{BAT}$	V
		Low Power mode; V_{BUS_CNT} = (V_{th_rec} + V_{th_dom}) / 2	$0.47V_{BAT}$	$0.5V_{BAT}$	$0.54V_{BAT}$	V
V_{HYS}	receiver hysteresis voltage	V_{HYS} = (V_{th_rec} - V_{th_dom}) [3]	-	-	$0.175V_{BAT}$	V
$V_{SerDiode}$	voltage drop at the serial diodes	in pull-up path with R_{master}; $I_{SerDiode}$ = 12 mA [2]	0.4	-	1.0	V
		in pull-up path with R_{slave}; $I_{SerDiode}$ = 0.9 mA	0.4	-	1.0	V
R_{master}	master resistance	Normal mode; including R_{slave}	900	1000	1100	Ω
$R_{master(lp)}$	low power master resistance	Low Power mode; including R_{slave}	900	1200	1500	Ω
R_{slave}	slave resistance	R_{master} off; $R_{master(lp)}$ off	20	30	60	kΩ
C_{LIN}	capacitance on pin LINx	[2]	-	-	20	pF
Thermal shutdown						
$T_{sd(otp)}$	overtemperature protection shutsown temperature	[2]	150	165	179	°C
$T_{rel(otp)}$	overtemperature protection release temperature	[2]	122	137	150	°C
$T_{w(otp)}$	overtemperature protection warning temperature	[2]	122	137	150	°C

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.
[2] Not tested in production; guaranteed by design.
[3] V_{th_dom}: receiver threshold of the recessive to dominant LIN bus edge. V_{th_rec}: receiver threshold of the dominant to recessive LIN bus edge.

10 Dynamic characteristics

Table 47. Dynamic characteristics

T_{vj} = -40 °C to +150 °C; V_{BAT} = 5.0 V to 28 V; V_{IO} = 2.97 V to 5.5V; all voltages are referenced to pin GND; positive currents flow into the IC; typical values are given at V_{BAT} = 12V; unless otherwise specified [1]

Symbols	Parameter	Conditions		Min	Typ	Max	Unit
Duty cycles; pins LIN1, LIN2, LIN3, LIN4							
δ1	duty cycle 1	$V_{th(rec)(max)}$ = 0.744 x V_{BAT}; $V_{th(dom)(max)}$ = 0.581 x V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 7 V to 28 V	[2] [3] [4]	0.396	-	-	
		$V_{th(rec)(max)}$ = 0.744 x V_{BAT}; $V_{th(dom)(max)}$ = 0.581 x V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 5 V to 7 V	[2] [3] [4]	0.37	-	-	
δ2	duty cycle 2	$V_{th(rec)(min)}$ = 0.442 x V_{BAT}; $V_{th(dom)(min)}$ = 0.284 x V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 7.6 V to 28 V	[2] [3] [4]	-	-	0.581	
		$V_{th(rec)(min)}$ = 0.442 x V_{BAT}; $V_{th(dom)(min)}$ = 0.284 x V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 5.6 V to 7.6 V	[2] [3] [4]	-	-	0.581	
δ3	duty cycle 3	$V_{th(rec)(max)}$ = 0.778 x V_{BAT}; $V_{th(dom)(max)}$ = 0.616 x V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 7 V to 28 V	[2] [3] [4]	0.417	-	-	
		$V_{th(rec)(max)}$ = 0.778 x V_{BAT}; $V_{th(dom)(max)}$ = 0.616 x V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 5 V to 7 V	[2] [3] [4]	0.417	-	-	
δ4	duty cycle 4	$V_{th(rec)(min)}$ = 0.389 x V_{BAT}; $V_{th(dom)(min)}$ = 0.251 x V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 7.6 V to 28 V	[2] [3] [4]	-	-	0.590	
		$V_{th(rec)(min)}$ = 0.389 x V_{BAT}; $V_{th(dom)(min)}$ = 0.251 x V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 5.6 V to 7.6 V	[2] [3] [4]	-	-	0.590	
LIN receiver; pins LIN1, LIN2, LIN3, LIN4							
t_{rx_pd}	receiver propagation delay	rising and falling edge; 7 V ≤ V_{BAT} < 28 V	[4]	-	-	6	µs
		rising and falling edge; 5 V < V_{BAT} < 7 V		-	-	6.5	µs
t_{rx_sym}	receiver propagation delay symmetry	rising edge with respect to falling edge	[4]	-2	-	+2	µs
t_{BFS}	byte field synchronization time		[5]	0	-	1/16 t_{bit}	s
t_{EBS}	earliest bit sample time		[5]	7/16 t_{bit}	-	-	s
t_{LBS}	latest bit sample time		[5]	-	-	9/16 t_{bit}	s

Symbols	Parameter	Conditions	Min	Typ	Max	Unit
$t_{wake(dom)LIN}$	LIN dominant wake-up time		30	80	150	µs
$t_{to(dom)LIN}$	LIN dominant time-out time	timer started at falling edge on LINx	17.5	20	23.5	ms
$t_{to(dom)TXD}$	internal TXD dominant time-out time		6	-	10	ms
Serial peripheral interface timing; pins SCSN, SCK, SDI and SDO						
$t_{cy(clk)}$	clock cycle time		250	-	-	ns
$t_{SPILEAD}$	SPI enable lead time		50	-	-	ns
t_{SPILAG}	SPI enable lag time		50	-	-	ns
$t_{clk(H)}$	clock HIGH time		100	-	-	ns
$t_{clk(L)}$	clock LOW time		100	-	-	ns
$t_{su(D)}$	data input set-up time		50	-	-	ns
$t_{h(D)}$	data input hold time		50	-	-	ns
$t_{d(SDI-SDO)}$	SDI to SDO delay time	SPI address byte and setting byte; CL = 20 pF	-	-	50	ns
$t_{v(Q)}$	data output valid time	SPI data bytes; CL = 20 pF		-	50	ns
$t_{WH(S)}$	chip select pulse width HIGH		250	-	-	ns
$t_{d(SCKL-SCSNL)}$	delay time from SCK LOW to SCSN LOW		50	-	-	ns
$t_{wake(low)SCSN}$	SCSN LOW wake-up time		1.75	-	4.65	µs
$t_{d(SPI)}$	SPI processing delay time	[5]	-	-	2	µs
Phase locked loop; pin CLK						
$f_{clk(PLL)in}$	PLL input clock frequency	external reference frequency operating range	0.4		10	MHz
$\Delta_{lock(PLL)}$	PLL in lock deviation from nominal internal PLL output clock	input clock should be within the ±0.3% range; correct multiplication factor should be selected via PLLMULT (Table 17)	-0.1	-	+0.1	%
Interrupt time-out; pin INTN						
$t_{to(int)}$	interrupt time-out time		0.88	1	1.12	ms
Transmit frame input; pin TMF						
$t_{tmf(L)}$	LOW TMF time		1	-	-	µs
$t_{tmf(H)}$	HIGH TMF time		1	-	-	µs
Mode transition						
$t_{init(norm)}$	normal mode initialization time		-	-	1	ms
$t_{init(LIN)}$	LIN initialization time		30	-	50	µs
$t_{d(uvd-lp)}$	delay time from VIO UV to low power mode		175	-	225	ms
$t_{d(uvd)}$	undervoltage detection delay time		5	-	10	µs
$t_{d(uvr)}$	undervoltage recovery delay time		5	-	10	µs
$t_{to(idle)INITI}$	INITI idle timeout time		2.6	3	3.4	s

Symbols	Parameter	Conditions	Min	Typ	Max	Unit
MTP non-volatile memory						
$t_{idl(SPI)MTPNVM}$	MTPNVM SPI idle time		0.9	1	1.1	s

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.

[2] $$\delta 1,\delta 3 = \frac{t_{bus(rec)min}}{2 \times t_{bit}}; \quad \delta 2,\delta 4 = \frac{t_{bus(rec)max}}{2 \times t_{bit}}$$

[3] Bus load conditions: MxCFG = 0; C_{LIN} = 1 nF and R_{LIN} = 1 kΩ; C_{LIN} = 6.8 nF and R_{LIN} = 660 Ω; C_{LIN} = 10 nF and R_{LIN} = 500 Ω.

[4] See timing diagram in Fig 10.

[5] Not tested in production; guaranteed by design.

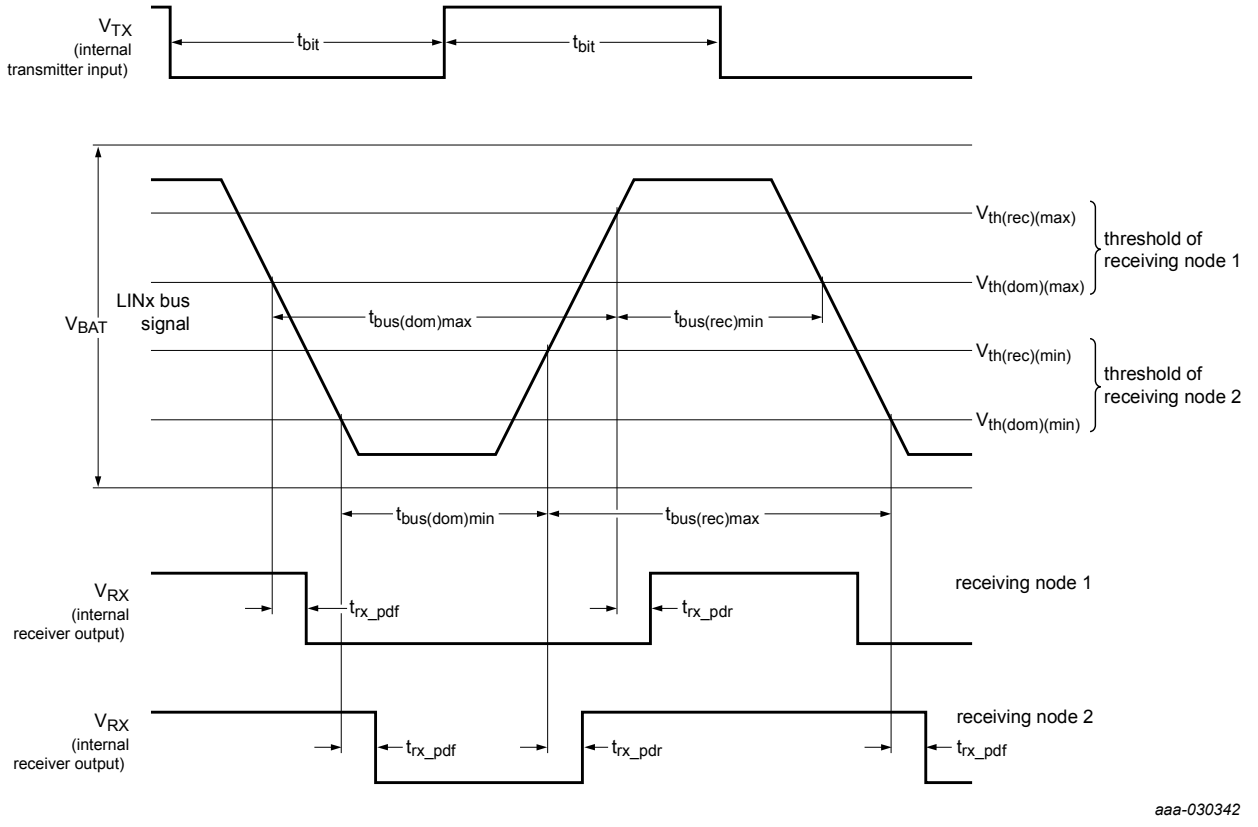
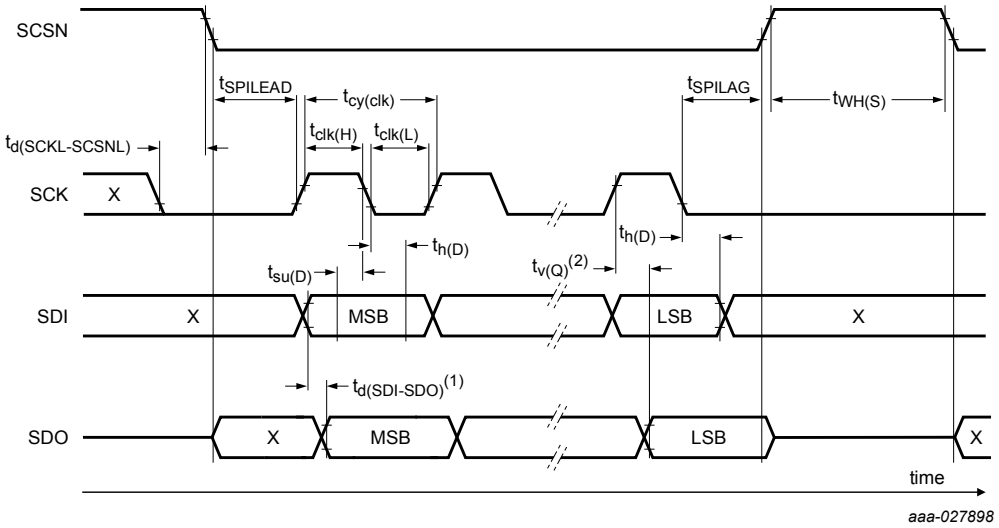


Figure 9. Timing diagram of LIN duty cycle

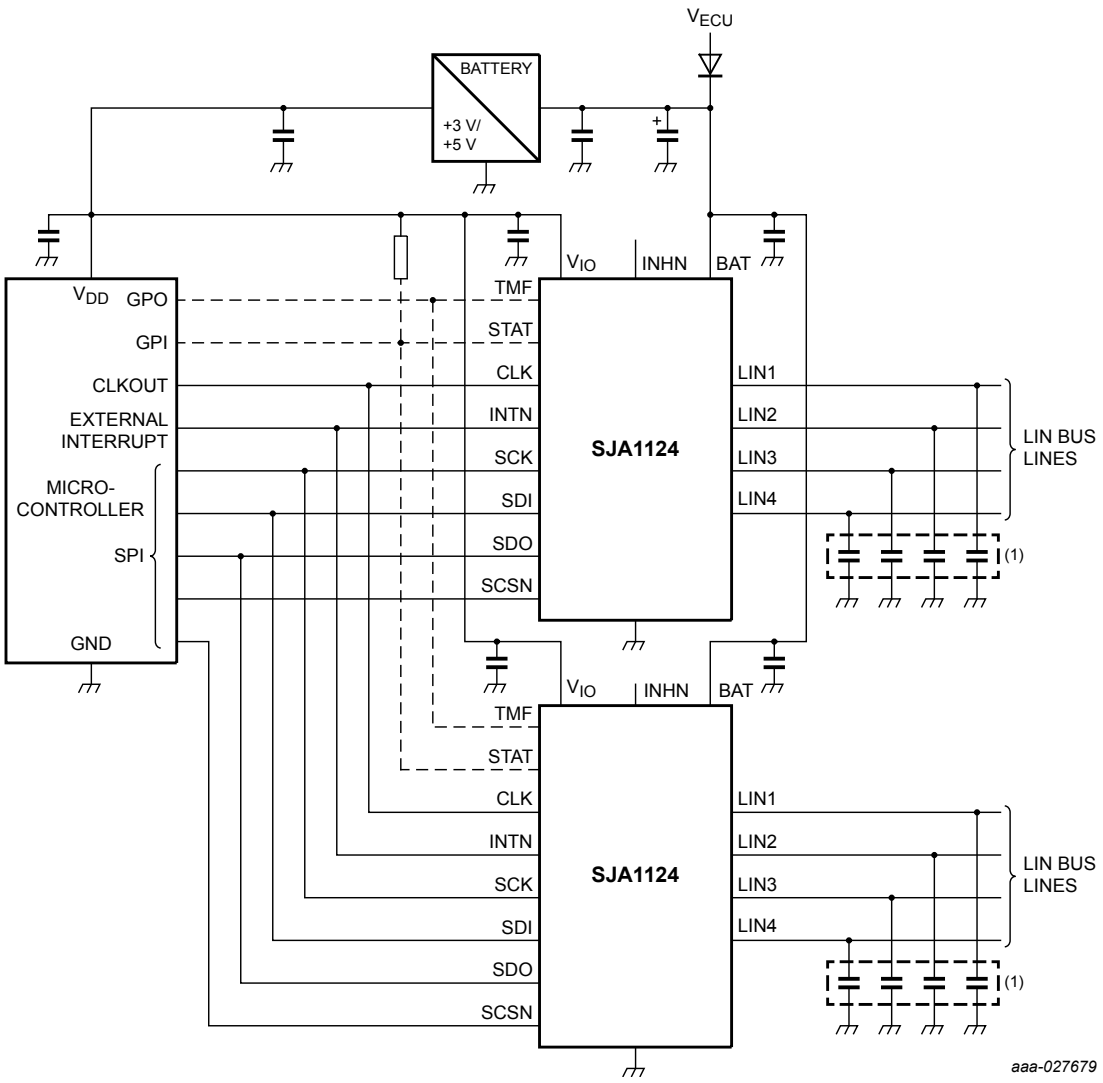


1. The SDI to SDO delay time is valid for SPI address byte and SPI setting byte
2. The data output valid time is valid for SPI data bytes.

Figure 10. SPI timing diagram

11 Application information

11.1 Application diagram



1. Typically specified by car manufacturer, e.g. 680 pF

Figure 11. Application diagram

11.2 ESD robustness according to LIN EMC test specification

ESD robustness (IEC 61000-4-2) has been tested by an external test house according to the LIN EMC test specification (part of Conformance Test Specification Package for LIN 2.1, October 10th, 2008). The test report is available on request.

Table 48. ESD robustness (IEC 61000-4-2) according to LIN EMC test specification

Pin	Test configuration	Value	Unit
LINx	no capacitor connected to LINx pin	±8	kV
	220 pF capacitor connected to LINx pin	±8	kV
BAT	22 µF and 100 nF capacitors connected to pin BAT	>|15|	kV

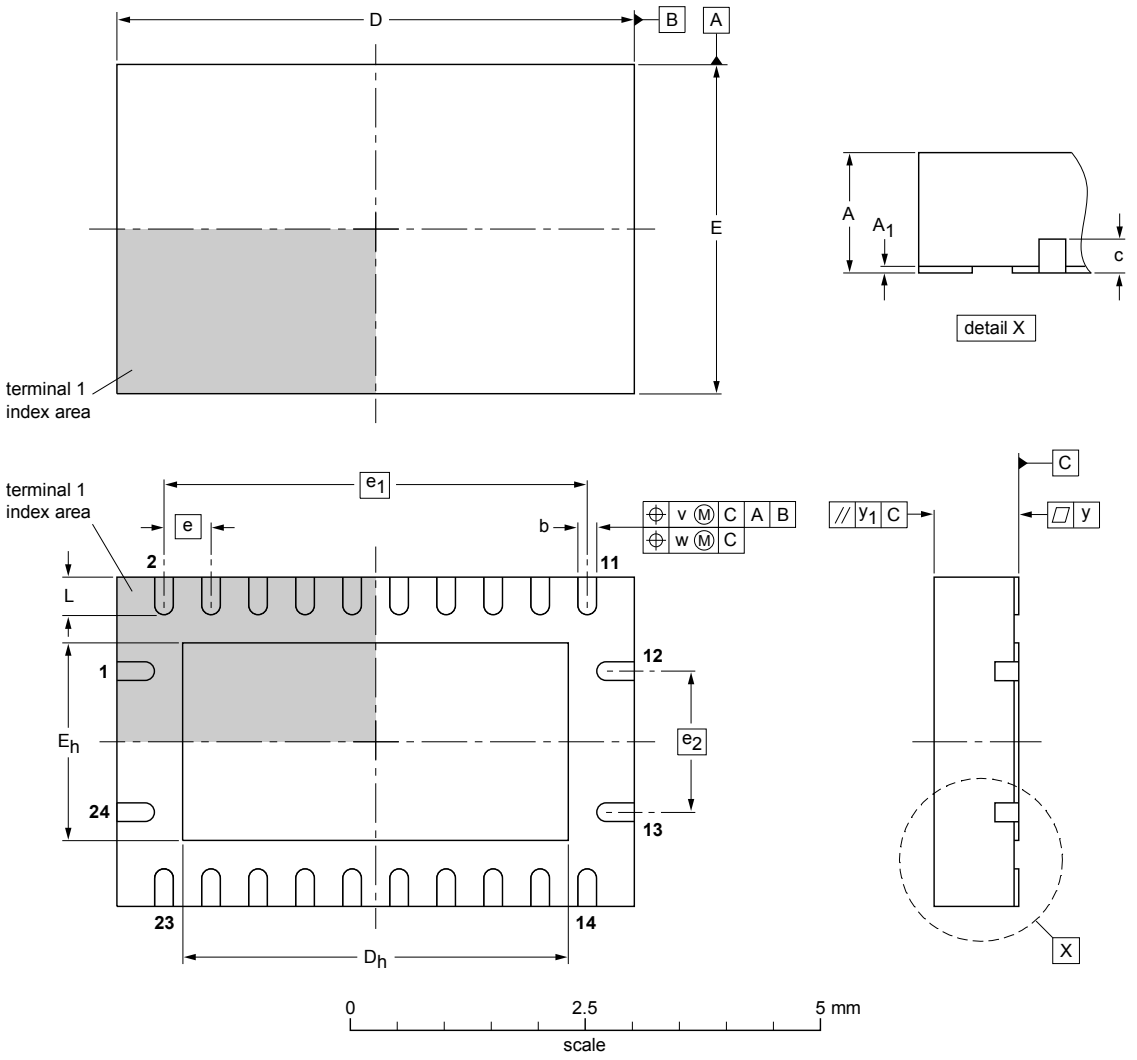
12 Test information

12.1 Quality information

After product release this product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q100 - *Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

13 Package outline

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm **SOT815-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.6 5.4	4.25 3.95	3.6 3.4	2.25 1.95	0.5	4.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT815-1	- - -	- - -	- - -			03-04-29

Figure 12. Package outline DHVQFN24

14 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

15 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 13) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 49 and Table 50.

Table 49. SnPb eutectic process (from J-STD-020D)

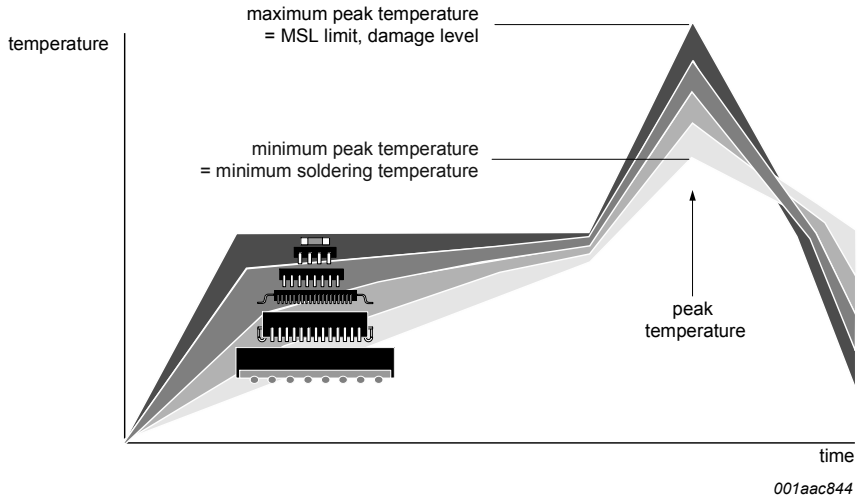
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥350
< 2.5	235	220
≥2.5	220	220

Table 50. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	>2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Fig 14.



MSL: Moisture Sensitivity Level

Figure 13. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16 Soldering of DHVQFN packages

Section 15 contains a brief introduction to the techniques most commonly used to solder Surface Mounted Devices (SMD). A more detailed discussion on soldering HVSON leadless package ICs can be found in the following application notes:

- AN10365 "Surface mount reflow soldering description"
- AN10366 "HVQFN application information"

17 Revision history

Table 51. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SJA1124 v.1	20180508	Product data sheet	-	-

18 Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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