TEXAS INSTRUMENTS

LM27341, LM27342, LM27341-Q1, LM27342-Q1

SNVS497F – NOVEMBER 2008 – REVISED SEPTEMBER 2016

LM2734x and LM2734x-Q1 2-MHz, 1.5-A or 2-A, Wide Input Range, Step-Down, DC-DC Regulator With Frequency Synchronization

1 Features

- Space-Saving, 3 mm × 3 mm 10-Pin WSON and MSOP-PowerPAD Packages
- Wide Input Voltage Range: 3 V to 20 V
- Wide Output Voltage Range: 1 V to 18 V
- LM27341 Delivers 1.5-A Maximum Output Current
- LM27342 Delivers 2-A Maximum Output Current
- High Switching Frequency: 2 MHz
- Frequency Synchronization: 1 MHz < f_{SW} < 2.35 MHz
- 150-mΩ NMOS Switch With Internal Bootstrap Supply
- 70-nA Shutdown Current
- Internal Voltage Reference Accuracy of 1%
- Peak Current-Mode, PWM Operation
- Thermal Shutdown
- LM27341-Q1 and LM27342-Q1 are AEC-Q100 Grade 1 Qualified and Manufactured on an Automotive Grade Flow

2 Applications

- Local 12-V to Vcore Step-Down Converters
- Radio Power Supply
- Core Power in HDDs
- Set-Top Boxes
- Automotive
- USB Powered Devices
- DSL Modems

3 Description

The LM2734x and LM2734x-Q1 regulators are monolithic, high-frequency, PWM step-down DC-DC converters in 10-pin WSON and 10-pin MSOP-PowerPAD packages. They contain all the active functions to provide local DC-DC conversion with fast transient response and accurate regulation in the smallest possible PCB area.

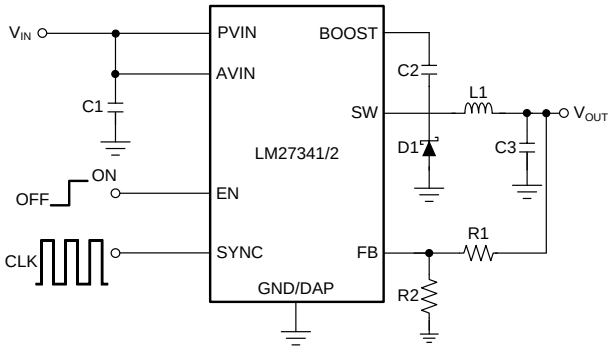
With a minimum of external components, the LM2734x and LM2734x-Q1 are easy to use. The ability to drive 1.5-A or 2-A loads respectively, with an internal 150-mΩ NMOS switch results in the best power density available. The world-class control circuitry allows for on-times as low as 65 ns, thus supporting exceptionally high frequency conversion. Switching frequency is internally set to 2 MHz and synchronizable from 1 to 2.35 MHz, which allows the use of extremely small surface mount inductors and chip capacitors. Even though the operating frequency is very high, efficiencies up to 90% are easy to achieve. External shutdown is included, which features an ultra-low shutdown current of 70 nA. The LM2734x and LM2734x-Q1 use peak current-mode control and internal compensation to provide high-performance regulation over a wide range of operating conditions. Additional features include internal soft-start circuitry to reduce inrush current, pulse-by-pulse current limit, thermal shutdown, and output overvoltage protection.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2734x LM2734x-Q1	MSOP-PowerPAD (10)	4.90 mm × 3.00 mm
	WSON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2013) to Revision F **Page**

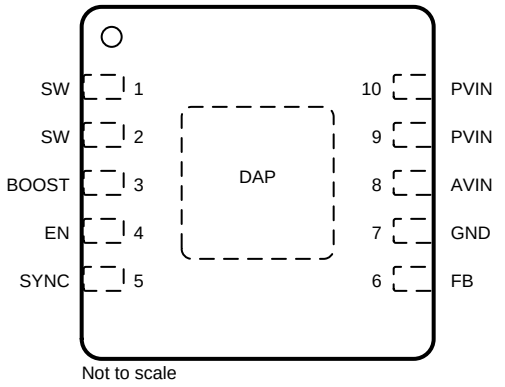
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed values in the *Thermal Information* table to align with JEDEC standards ... 5

Changes from Revision D (April 2013) to Revision E **Page**

- Changed layout of National Semiconductor Data Sheet to TI format ... 1

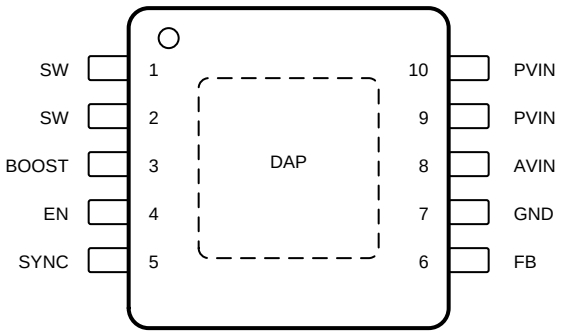
5 Pin Configuration and Functions

DSC Package
10-Pin WSON
Top View



Not to scale

DGQ Package
10-Pin MSOP-PowerPAD
Top View



Not to scale

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1, 2	SW	O	Output switch. Connects to the inductor, catch diode, and bootstrap capacitor.
3	BOOST	I	Boost voltage that drives the internal NMOS control switch. A bootstrap capacitor is connected between the BOOST and SW pins.
4	EN	I	Enable control input. Logic high enables operation. Do not allow this pin to float or be greater than V_{IN} + 0.3 V.
5	SYNC	I	Frequency synchronization input. Drive this pin with an external clock or pulse train. Ground it to use the internal clock.
6	FB	I	Feedback pin. Connect FB to the external resistor divider to set output voltage.
7	GND	G	Signal and power ground pin. Place the bottom resistor of the feedback network as close as possible to this pin for accurate regulation.
8	AVIN	I	Supply voltage for the control circuitry.
9, 10	PVIN	I	Supply voltage for output power stage. Connect a bypass capacitor to this pin.
DAP	DAP	G	Signal or power ground and thermal connection. Tie this directly to GND (pin 7). See *Application Information* regarding optimum thermal layout.

(1) G = Ground, I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
AVIN, PVIN	–0.5	24	V
SW voltage	–0.5	24	V
Boost voltage	–0.5	28	V
Boost to SW voltage	–0.5	6	V
FB voltage	–0.5	3	V
SYNC voltage	–0.5	6	V
EN voltage	–0.5	V_{IN} + 0.3	V
Soldering, infrared reflow (5 s)		260	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human body model, 1.5 kΩ in series with 100 pF.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
AVIN, PVIN	3	20	V
SW voltage	–0.5	20	V
Boost voltage	–0.5	24	V
Boost to SW voltage	3	5.5	V
Junction temperature	–40	125	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the recommended Operating Ratings is not implied. The recommended Operating Ratings indicate conditions at which the device is functional and should not be operated beyond such conditions.

6.4 Thermal Information

THERMAL METRIC[1]		LM2734x, LM2734x-Q1		UNIT
		DSC (WSON)	DGQ (MSOP-PowerPAD)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	47.6	49.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.5	53.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.5	33.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	3.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.7	33.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.7	3.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Thermal shutdown will occur if the junction temperature exceeds 165°C. The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$ and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a 3" × 3" PCB with 2 oz. copper on 4 layers in still air.

6.5 Electrical Characteristics

T_J = 25°C, V_{IN} = 12 V, and $V_{BOOST} – V_{SW}$ = 4.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SYSTEM PARAMETERS							
V_{FB}	Feedback voltage	T_J = 0°C to 85°C		0.99	1	1.01	V
		T_J = –40°C to 125°C		0.984	1	1.014	
$\Delta V_{FB}/\Delta V_{IN}$	Feedback voltage line regulation	V_{IN} = 3 V to 20 V			0.003%		V
I_{FB}	Feedback input bias current	T_J = 25°C			20		nA
		T_J = –40°C to 125°C				100	
OVP	Overvoltage protection	V_{FB} at which PWM halts			1.13		V
UVLO	Undervoltage lockout	V_{IN} rising until V_{SW} is switching	T_J = 25°C		2.75		V
			T_J = –40°C to 125°C	2.6		2.9	
	Undervoltage hysteresis	V_{IN} falling from UVLO	T_J = 25°C		0.47		
			T_J = –40°C to 125°C	0.3		0.6	
SS	Soft-start time			0.5	1	1.5	ms
I_Q	Quiescent current	$I_Q = I_{Q\_AVIN} + I_{Q\_PVIN}$	V_{FB} = 1.1 (not switching)		2.4		mA
			V_{EN} = 0 V (shutdown)		70		nA
I_{BOOST}	Boost pin current	f_{SW}= 2 MHz	T_J = 25°C		8.2		mA
			T_J = –40°C to 125°C			10	
		f_{SW}= 1 MHz			4.4	6	
OSCILLATOR							
f_{SW}	Switching frequency	SYNC = GND	T_J = 25°C		2		MHz
			T_J = –40°C to 125°C	1.75		2.3	
V_{FB_FOLD}	FB pin voltage	SYNC input is overridden			0.53		V
f_{FOLD_MIN}	Frequency foldback minimum	V_{FB} = 0 V			220	250	kHz
LOGIC INPUTS (EN, SYNC)							
f_{SYNC}	SYNC frequency range			1		2.35	MHz
V_{IL}	EN, SYNC logic low threshold	Logic falling edge				0.4	V
V_{IH}	EN, SYNC logic high threshold	Logic rising edge		1.8			
t_{SYNC_HIGH}	SYNC, time required above V_{IH} to ensure a logical high					100	ns

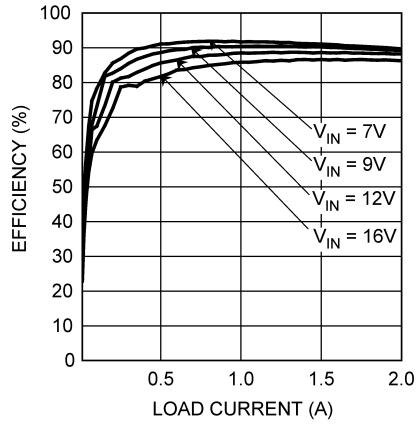
Electrical Characteristics (continued)

T_J = 25°C, V_{IN} = 12 V, and $V_{BOOST} – V_{SW}$ = 4.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{SYNC_LOW}	SYNC, time required below V_{IL} to ensure a logical low					100	ns
I_{SYNC}	SYNC pin current	V_{SYNC} < 5 V			20		nA
I_{EN}	Enable pin current	V_{EN} = 3 V			6	15	µA
		V_{IN} = V_{EN} = 20 V			50	100	
INTERNAL MOSFET							
$R_{DS(ON)}$	Switch ON-resistance	T_J = 25°C			150		mΩ
		T_J = –40°C to 125°C				320	
I_{CL}	Switch current limit	T_J = –40°C to 125°C	LM27342	2.5		4	A
			LM27341	2		3.7	
D_{MAX}	Maximum duty cycle	SYNC = GND	T_J = 25°C		93%		
			T_J = –40°C to 125°C	85%			
t_{MIN}	Minimum ON-time				65		ns
I_{SW}	Switch leakage current				40		nA
BOOST LDO							
V_{LDO}	Boost LDO output voltage				3.9		V
THERMAL							
T_{SHDN}	Thermal shutdown temperature	Junction temperature rising			165		°C
	Thermal shutdown hysteresis	Junction temperature falling			15		

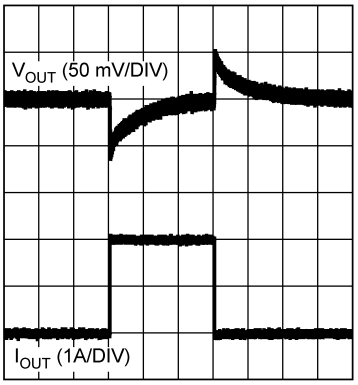
6.6 Typical Characteristics

T_A = 25°C, V_{IN} = 12 V, and $V_{BOOST} – V_{SW}$ = 4.3 V (unless otherwise noted)



V_{OUT} = 5 V f_{SW} = 2 MHz

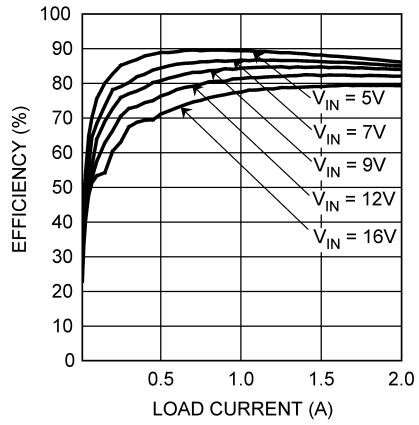
Figure 1. Efficiency vs Load Current
See Figure 34



100 µs/DIV

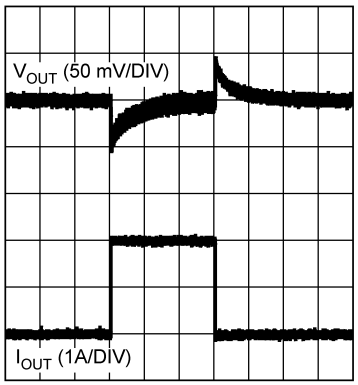
V_{OUT} = 5 V I_{OUT} = 100 mA – 2 A at Slewrate = 2 A / µs

Figure 2. Load Transient
See Figure 34



V_{OUT} = 3.3 V f_{SW} = 2 MHz

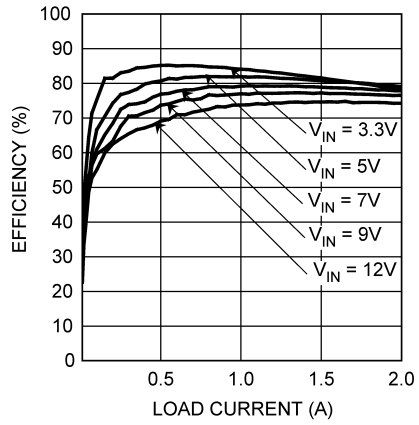
Figure 3. Efficiency vs Load Current
See Figure 40



100 µs/DIV

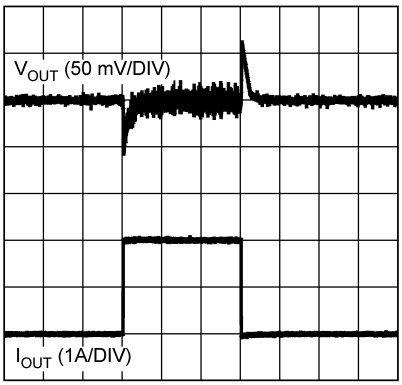
V_{OUT} = 3.3 V I_{OUT} = 100 mA – 2 A at Slewrate = 2 A / µs

Figure 4. Load Transient
See Figure 40



V_{OUT} = 1.8 V f_{SW} = 2 MHz

Figure 5. Efficiency vs Load Current
See Figure 49



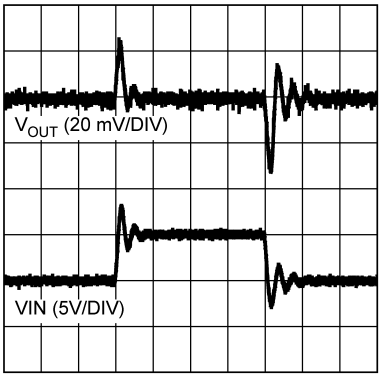
100 µs/DIV

V_{OUT} = 1.8 V I_{OUT} = 100 mA – 2 A at Slewrate = 2 A / µs

Figure 6. Load Transient
See Figure 49

Typical Characteristics (continued)

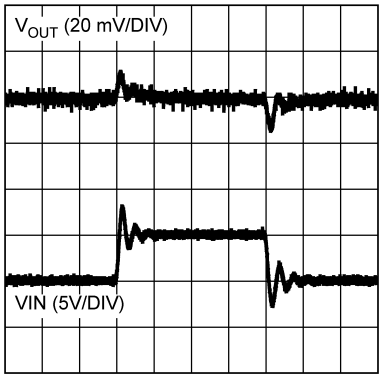
T_A = 25°C, V_{IN} = 12 V, and $V_{BOOST} – V_{SW}$ = 4.3 V (unless otherwise noted)



100 µs/DIV

V_{IN} = 10 V to 15 V V_{OUT} = 3.3 V No C_{FF}

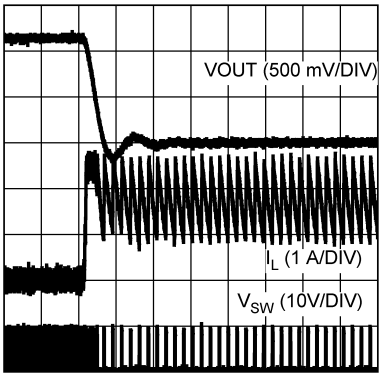
Figure 7. Line Transient
See Figure 43



100 µs/DIV

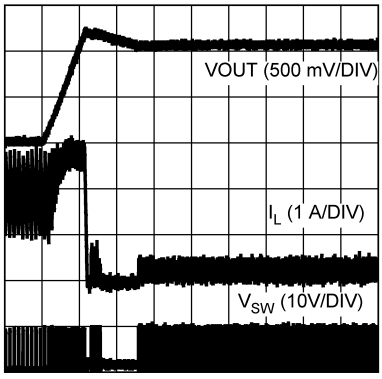
V_{IN} = 10 V to 15 V V_{OUT} = 3.3 V

Figure 8. Line Transient
See Figure 40



20 µs/DIV

Figure 9. Short Circuit



40 µs/DIV

Figure 10. Short-Circuit Release

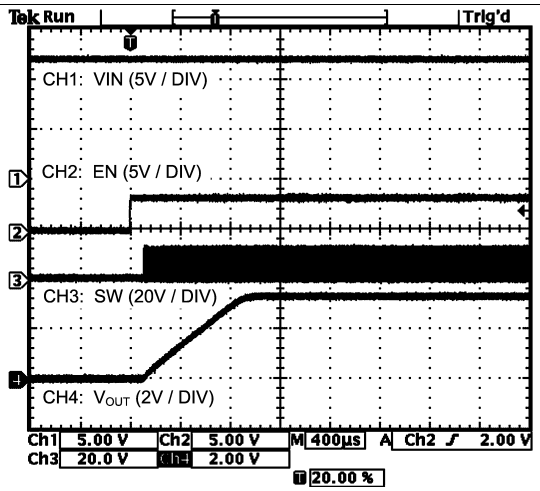


Figure 11. Soft Start With EN Tied to V_{IN}

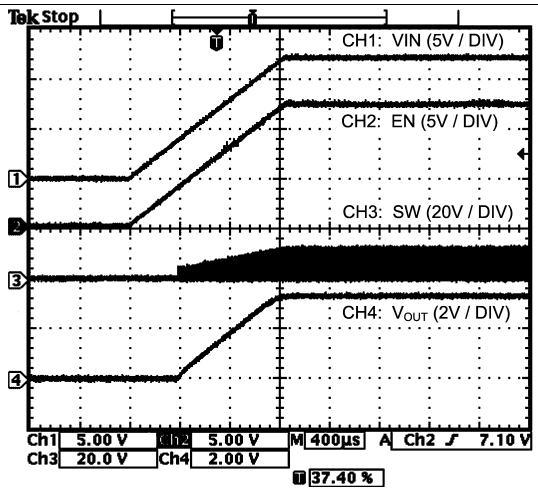
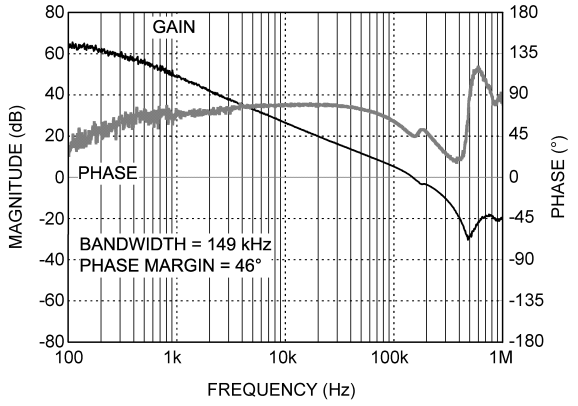


Figure 12. Soft Start With EN Tied to V_{IN}

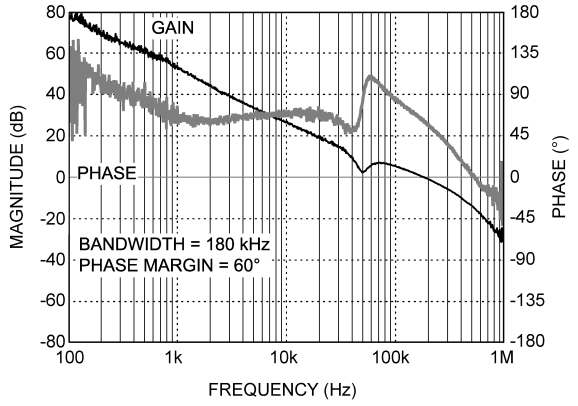
Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 12 V, and $V_{BOOST} – V_{SW}$ = 4.3 V (unless otherwise noted)



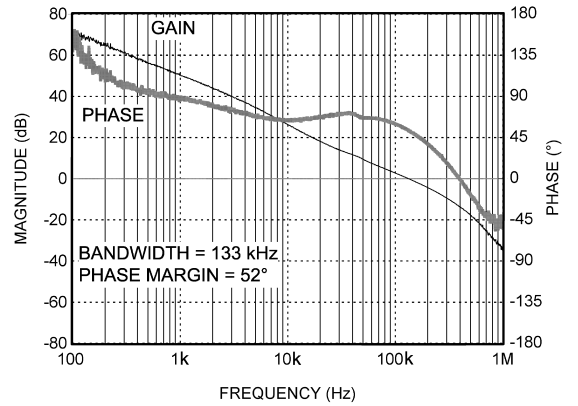
V_{IN} = 12 V L = 2.2 µH Iout =1 A
V_{OUT} = 5 V C_{OUT} = 44 µF

Figure 13. Bode Plot
See Figure 34



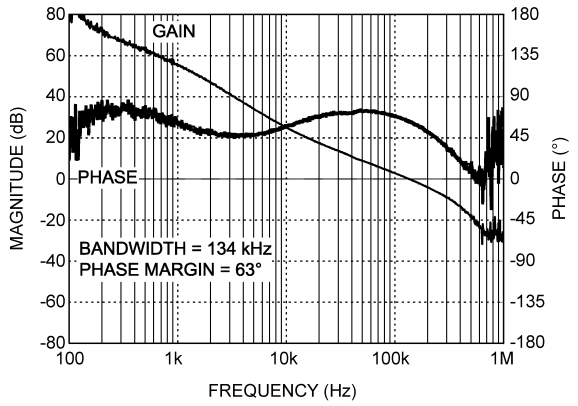
V_{IN} = 12 V L = 1.5 µH Iout =1 A
V_{OUT} = 3.3 V C_{OUT} = 44 µF

Figure 14. Bode Plot
See Figure 40



V_{IN} = 5 V L = 1.0 µH Iout =1 A
V_{OUT} = 1.8 V C_{OUT} = 44 µF

Figure 15. Bode Plot
See Figure 49



V_{IN} = 5 V L = 0.56 µH Iout =1 A
V_{OUT} = 1.2 V C_{OUT} = 68 µF

Figure 16. Bode Plot
See Figure 55

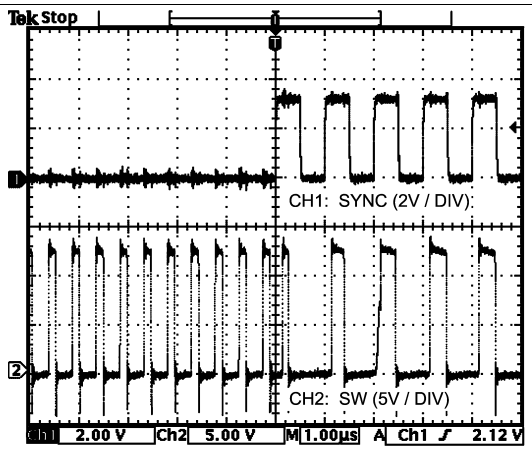


Figure 17. Sync Functionality

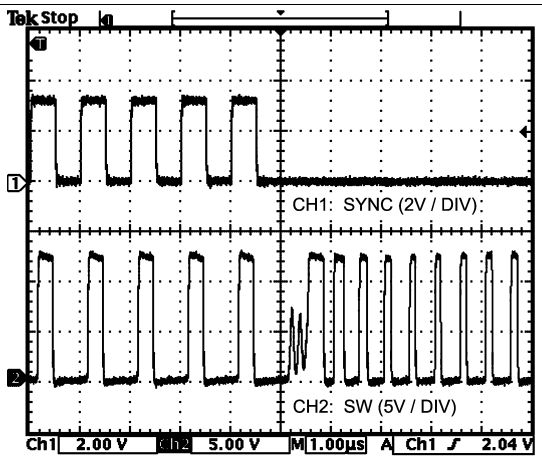
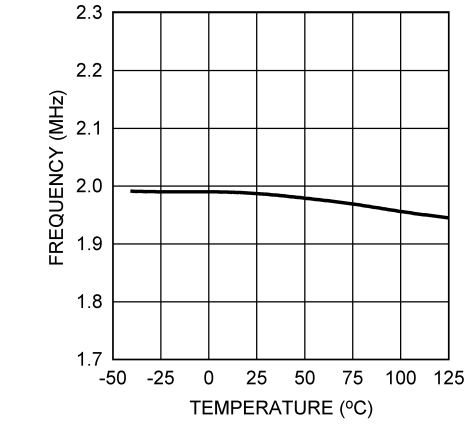


Figure 18. Loss of Synchronization

Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 12 V, and $V_{BOOST} – V_{SW}$ = 4.3 V (unless otherwise noted)



V_{SYNC} = GND f_{SW} = 2 MHz

Figure 19. Oscillator Frequency vs Temperature

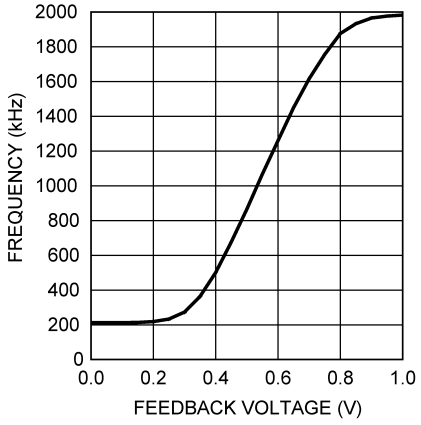


Figure 20. Oscillator Frequency vs V_{FB}

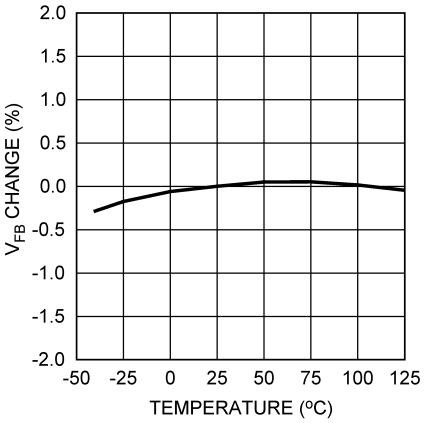


Figure 21. V_{FB} vs Temperature

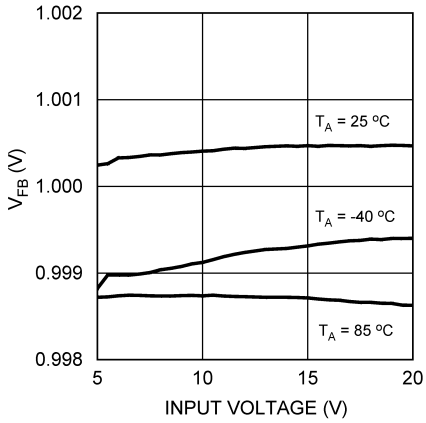
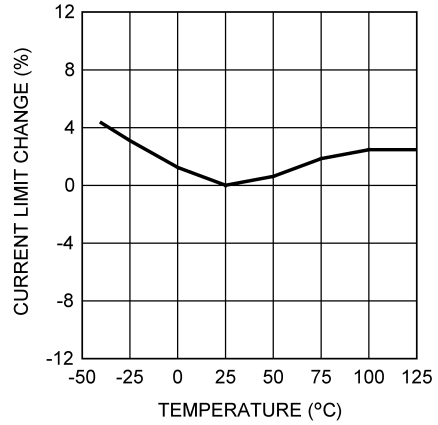


Figure 22. V_{FB} vs V_{IN}



V_{IN} = 12 V

Figure 23. Current Limit vs Temperature

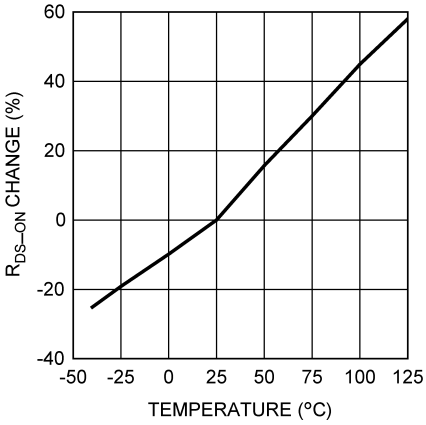
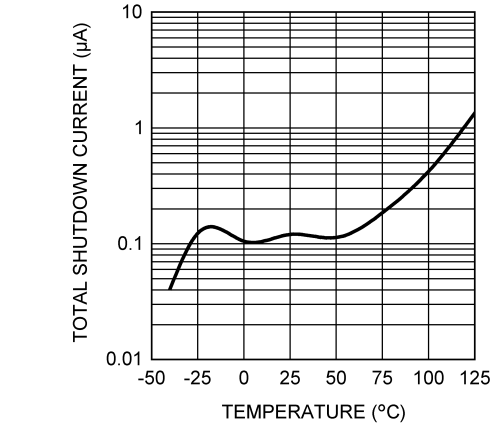


Figure 24. R_{DSON} vs Temperature

Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 12 V, and $V_{BOOST} – V_{SW}$ = 4.3 V (unless otherwise noted)



$I_Q = I_{AVIN} + I_{PVIN}$

Figure 25. I_Q (Shutdown) vs Temperature

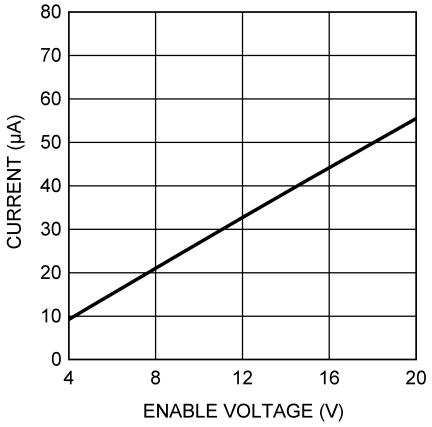


Figure 26. I_{EN} vs V_{EN}

7 Detailed Description

7.1 Overview

The LM2734x and LM2734x-Q1 are a constant-frequency, peak current-mode PWM buck regulator IC that delivers a 1.5-A or 2-A load current. The regulator has a preset switching frequency of 2 MHz. This high frequency allows the LM2734x and LM2734x-Q1 to operate with small surface-mount capacitors and inductors, resulting in a DC-DC converter that requires a minimum amount of board space. The LM2734x and LM2734x-Q1 are internally compensated, which reduces design time, and requires few external components.

The following operating description of the LM2734x and LM2734x-Q1 refers to *Functional Block Diagram* and to the waveforms in Figure 27. The LM2734x and LM2734x-Q1 supply a regulated output voltage by switching the internal NMOS switch at a constant frequency and varying the duty cycle. A switching cycle begins at the falling edge of the reset pulse generated by the internal oscillator. When this pulse goes low, the output control logic turns on the internal NMOS switch. During this on-time, the SW pin voltage (V_{SW}) swings up to approximately V_{IN}, and the inductor current (i_L) increases with a linear slope. The current-sense amplifier measures i_L, which generates an output proportional to the switch current typically called the sense signal. The sense signal is summed with the regulator's corrective ramp and compared to the error amplifier's output, which is proportional to the difference between the feedback voltage (V_{FB}) and V_{REF}. When the output of the PWM comparator goes high, the switch turns off until the next switching cycle begins. During the switch off-time (t_{OFF}), inductor current discharges through the catch diode D1, which forces the SW pin (V_{SW}) to swing below ground by the forward voltage (V_{D1}) of the catch diode. The regulator loop adjusts the duty cycle (D) to maintain a constant output voltage.

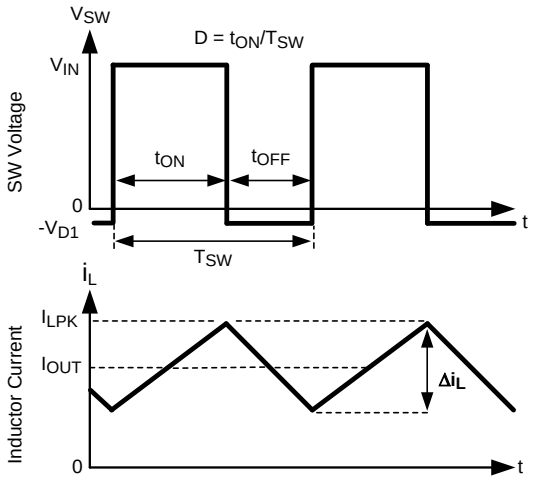
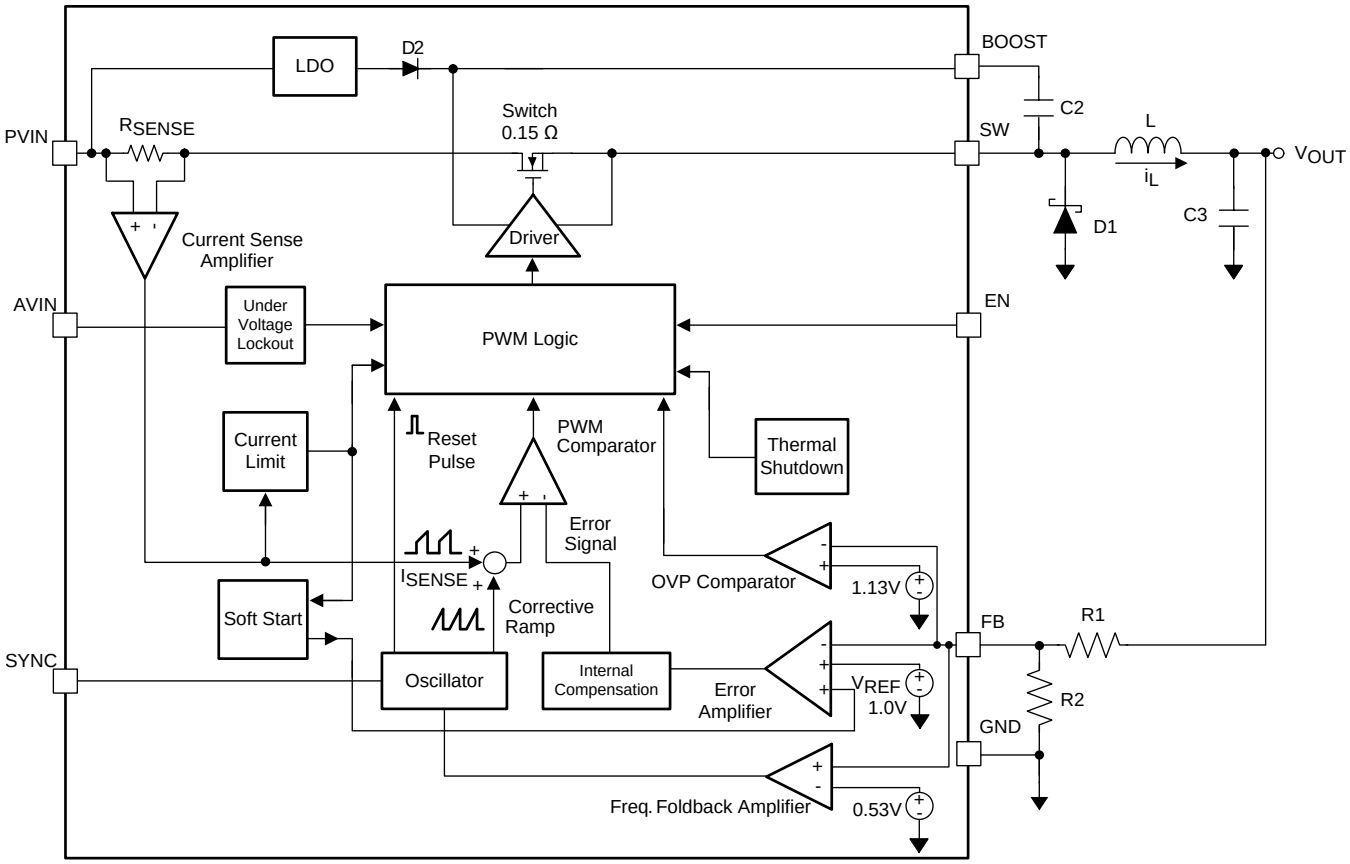


Figure 27. LM2734x Waveforms of SW Pin Voltage and Inductor Current

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Boost Function

Capacitor C_2 in *Functional Block Diagram*, commonly referred to as C_{BOOST}, is used to store a voltage V_{BOOST}. When LM2734x and LM2734x-Q1 start up, an internal LDO charges C_{BOOST} through an internal diode, to a voltage sufficient to turn the internal NMOS switch on. The gate drive voltage supplied to the internal NMOS switch is $V_{BOOST} – V_{SW}$.

During a normal switching cycle, when the internal NMOS control switch is off (t_{OFF}) (see Figure 27), V_{BOOST} equals V_{LDO} minus the forward voltage of the internal diode (V_{D2}). At the same time the inductor current (i_L) forward biases the catch diode D1 forcing the SW pin to swing below ground by the forward voltage drop of the catch diode (V_{D1}). Therefore, the voltage stored across C_{BOOST} is calculated with Equation 1 and Equation 2.

$$V_{BOOST} – V_{SW} = V_{LDO} – V_{D2} + V_{D1} \quad (1)$$

$$V_{BOOST} = V_{SW} + V_{LDO} – V_{D2} + V_{D1} \quad (2)$$

When the NMOS switch turns on (t_{ON}), the switch pin rises to Equation 3.

$$V_{SW} = V_{IN} – (R_{DSON} \times I_L) \quad (3)$$

Then the D1 undergoes reverse biasing, and forces V_{BOOST} to rise. The voltage at V_{BOOST} is then calculated with Equation 4.

$$V_{BOOST} = V_{IN} – (R_{DSON} \times I_L) + V_{LDO} – V_{D2} + V_{D1} \quad (4)$$

Which is approximately calculated with Equation 5.

$$V_{IN} + V_{LDO} – 0.4\ V \quad (5)$$

V_{BOOST} has pulled itself up by its bootstraps, or boosted to a higher voltage.

Feature Description (continued)

7.3.2 Low Input Voltage Considerations

When the input voltage is below 5 V and the duty cycle is greater than 75%, the gate drive voltage developed across C_{BOOST} might not be sufficient for proper operation of the NMOS switch. In this case, C_{BOOST} must be charged through an external Schottky diode attached to a 5-V voltage rail (see Figure 28). This ensures that the gate drive voltage is high enough for proper operation of the NMOS switch in the triode region. Maintain $V_{BOOST} - V_{SW}$ less than the 6-V absolute maximum rating.

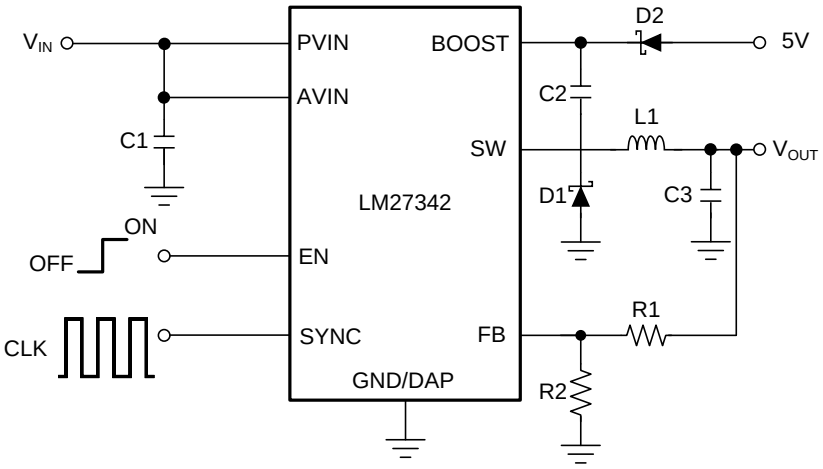


Figure 28. External Diode Charges C_{BOOST}

7.3.3 High Output Voltage Considerations

When the output voltage is greater than 3.3 V, a minimum load current is required to charge C_{BOOST} (see Figure 29). The minimum load current forward biases the catch diode D1 forcing the SW pin to swing below ground. This allows C_{BOOST} to charge, ensuring that the gate drive voltage is high enough for proper operation. The minimum load current depends on many factors including the inductor value.

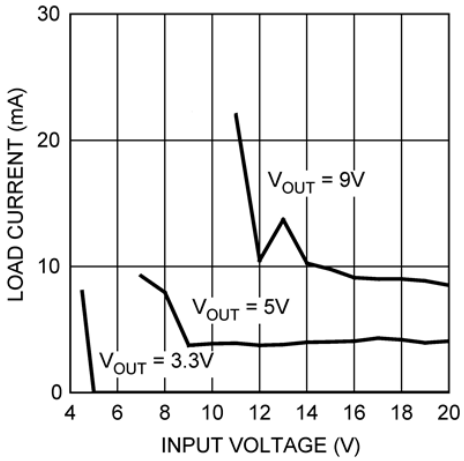


Figure 29. Minimum Load Current for L = 1.5 µH

Feature Description (continued)

7.3.4 Frequency Synchronization

The LM2734x and LM2734x-Q1 switching frequency can be synchronized to an external clock, between 1 MHz and 2.35 MHz, applied at the SYNC pin. At the first rising edge applied to the SYNC pin, the internal oscillator is overridden and subsequent positive edges initiate switching cycles. If the external SYNC signal is lost during operation, the LM2734x and LM2734x-Q1 revert to its internal 2-MHz oscillator within 1.5 µs. To disable frequency synchronization and use the internal 2-MHz oscillator, connect the SYNC pin to GND.

The SYNC pin gives the designer the flexibility to optimize their design. A lower switching frequency can be chosen for higher efficiency. A higher switching frequency can be chosen to keep EMI out of sensitive ranges such as the AM radio band. Synchronization can also be used to eliminate beat frequencies generated by the interaction of multiple switching power converters. Synchronizing multiple switching power converters result in cleaner power rails.

The selected switching frequency (f_{SYNC}) and the minimum on-time (t_{MIN}) limit the minimum duty cycle (D_{MIN}) of the device as calculated with Equation 6.

$$D_{MIN} = t_{MIN} \times f_{SYNC} \quad (6)$$

Operation below D_{MIN} is not recommended. The LM2734x and LM2734x-Q1 skip pulses to keep the output voltage in regulation, and the current limit is not ensured. The switching is in phase but no longer at the same switching frequency as the SYNC signal.

7.3.5 Current Limit

The LM2734x and LM2734x-Q1 use cycle-by-cycle current limiting to protect the output switch. During each switching cycle, a current limit comparator detects if the output switch current exceeds 2 A minimum (LM27341) or 2.5 A minimum (LM27342), and turns off the switch until the next switching cycle begins.

7.3.6 Frequency Foldback

The LM2734x and LM2734x-Q1 employ frequency foldback to protect the device from current run-away during output short-circuit. Once the FB pin voltage falls below regulation, the switch frequency smoothly reduce with the falling FB voltage until the switch frequency reaches 220 kHz (typical). If the device is synchronized to an external clock, synchronization is disabled until the FB pin voltage exceeds 0.53 V.

7.3.7 Output Overvoltage Protection

The overvoltage comparator turns off the internal power NFET when the FB pin voltage exceeds the internal reference voltage by 13% ($V_{FB} > 1.13 \times V_{REF}$). With the power NFET turned off the output voltage decreases toward the regulation level.

7.3.8 Undervoltage Lockout

Undervoltage lockout (UVLO) prevents the LM2734x and LM2734x-Q1 from operating until the input voltage exceeds 2.75 V (typical).

The UVLO threshold has approximately 470 mV of hysteresis, so the part operates until V_{IN} drops below 2.28 V (typical). Hysteresis prevents the part from turning off during power up if V_{IN} has finite impedance.

7.3.9 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the internal NMOS switch when the IC junction temperature exceeds 165°C (typical). After thermal shutdown occurs, hysteresis prevents the internal NMOS switch from turning on until the junction temperature drops to approximately 150°C.

7.4 Device Functional Modes

7.4.1 Enable Pin and Shutdown Mode

Connect the EN pin to a voltage source greater than 1.8 V to enable operation of the LM2734x and LM2734x-Q1. Apply a voltage less than 0.4 V to put the part into shutdown mode. In shutdown mode, the quiescent current drops to typically 70 nA. Switch leakage adds another 40 nA from the input supply. For proper operation, the LM2734x and LM2734x-Q1 EN pin must never be left floating, and the voltage must never exceed V_{IN} + 0.3 V.

The simplest way to enable the operation of LM2734x and LM2734x-Q1 is to connect the EN pin to AVIN which allows self start-up of the LM2734x and LM2734x-Q1 when the input voltage is applied.

When the rise time of V_{IN} is longer than the soft-start time of the LM2734x and LM2734x-Q1, this method may result in an overshoot in output voltage. In such applications, the EN pin voltage can be controlled by a separate logic signal, or tied to a resistor divider, which reaches 1.8 V after V_{IN} is fully established (see Figure 30). This minimizes the potential for output voltage overshoot during a slow V_{IN} ramp condition. Use the lowest value of V_{IN}, seen in your application when calculating the resistor network using Equation 7, to ensure that the 1.8 V minimum EN threshold is reached.

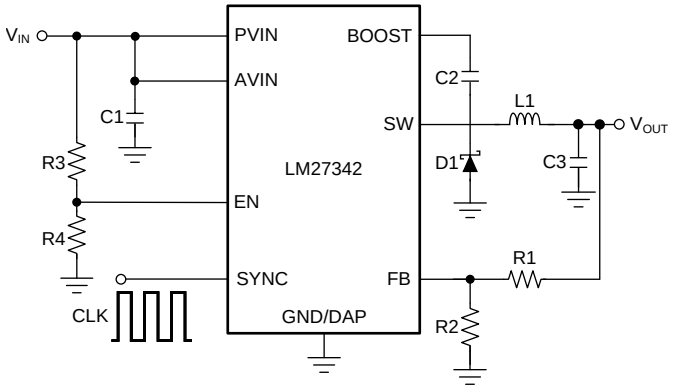


Figure 30. Resistor Divider on EN

$$R3 = \left(\frac{V_{IN}}{1.8} - 1 \right) \times R4 \quad (7)$$

7.4.2 Soft-Start Mode

The LM2734x and LM2734x-Q1 have a fixed internal soft-start of 1 ms (typical). During soft start, the error amplifier's reference voltage ramps from 0 V to its nominal value of 1 V in approximately 1 ms. This forces the regulator output to ramp in a controlled fashion, which helps reduce inrush current. Upon soft start, the part is initially in frequency foldback and the frequency rises as FB rises. The regulator rises gradually to 2 MHz. The LM2734x and LM2734x-Q1 allows synchronization to an external clock at FB > 0.53 V.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Inductor Selection

Inductor selection is critical to the performance of the LM2734x and LM2734x-Q1. The selection of the inductor affects stability, transient response and efficiency. A key factor in inductor selection is determining the ripple current (Δi_L) (see Figure 27). The ripple current (Δi_L) is important in many ways.

First, by allowing more ripple current, lower inductance values can be used with a corresponding decrease in physical dimensions and improved transient response. On the other hand, allowing less ripple current increases the maximum achievable load current and reduce the output voltage ripple (see *Output Capacitor* for more details on calculating output voltage ripple). Increasing the maximum load current is achieved by ensuring that the peak inductor current (I_{LPK}) never exceeds the minimum current limit of 2 A for the LM27341 or 2.5 A for the LM27342 in Equation 8.

$$I_{LPK} = I_{OUT} + \Delta i_L / 2 \quad (8)$$

Secondly, the slope of the ripple current affects the current control loop. The LM2734x and LM2734x-Q1 have a fixed slope corrective ramp. When the slope of the current ripple becomes significantly less than the converter's corrective ramp, the inductor pole moves from high frequencies to lower frequencies. This negates one advantage that peak current-mode control has overvoltage-mode control, which is, a single low-frequency pole in the power stage of the converter. This can reduce the phase margin, crossover frequency and potentially cause instability in the converter. Contrarily, when the slope of the ripple current becomes significantly greater than the converter's corrective ramp, resonant peaking can occur in the control loop. This can also cause instability (subharmonic oscillation) in the converter. For the power supply designer, this means that for lower switching frequencies the current ripple must be increased to keep the inductor pole well above crossover. It also means that for higher switching frequencies the current ripple must be decreased to avoid resonant peaking.

With all these factors, the desired ripple current is selected with Equation 9. The ripple ratio (r) is defined as the ratio of inductor ripple current (Δi_L) to output current (I_{OUT}), evaluated at maximum load.

$$r = \frac{\Delta iL}{IOUT} \quad (9)$$

A good compromise between physical size, transient response and efficiency is achieved when we set the ripple ratio between 0.2 and 0.4. The recommended ripple ratio versus duty cycle shown in Figure 31 is based upon this compromise and control loop optimizations. Note that this is just a guideline. See *AN-1197 Selecting Inductors for Buck Converters* for further considerations.

Application Information (continued)

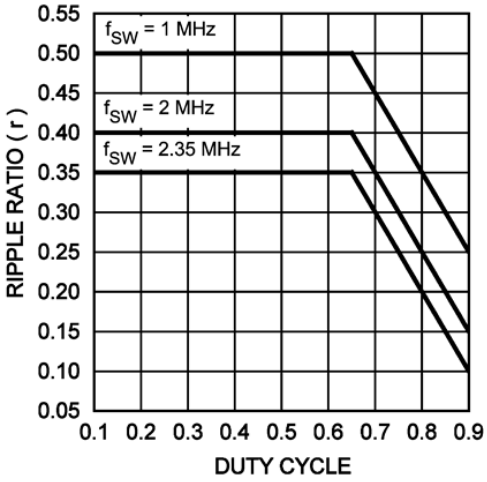


Figure 31. Recommended Ripple Ratio vs Duty Cycle

The duty cycle (D) can be approximated quickly using the ratio of output voltage (V_{OUT}) to input voltage (V_{IN}) in Equation 10.

$$D = \frac{V_{OUT}}{V_{IN}} \tag{10}$$

The application's lowest input voltage must be used to calculate the ripple ratio. The catch diode forward voltage drop (V_{D1}) and the voltage drop across the internal NFET (V_{DS}) must be included to calculate a more accurate duty cycle. Calculate D by using Equation 11.

$$D = \frac{V_{OUT} + V_{D1}}{V_{IN} + V_{D1} - V_{DS}} \tag{11}$$

V_{DS} can be approximated with Equation 12.

$$V_{DS} = I_{OUT} \times R_{DS(ON)} \tag{12}$$

The diode forward drop (V_{D1}) can range from 0.3 V to 0.5 V depending on the quality of the diode. The lower V_{D1} is, the higher the operating efficiency of the converter.

Now that the ripple current or ripple ratio is determined, the required inductance is calculated with Equation 13.

$$L = \frac{V_{OUT} + V_{D1}}{I_{OUT} \times r \times f_{sw}} \times (1 - D_{MIN}) \tag{13}$$

where

- D_{MIN} is the duty cycle calculated with the maximum input voltage
- f_{sw} is the switching frequency
- I_{OUT} is the maximum output current of 2 A

Using I_{OUT} = 2 A minimizes the inductor's physical size.

Application Information (continued)

8.1.1.1 Inductor Calculation Example

Operating conditions for the LM27342 are listed in Table 1.

Table 1. Operating Conditions for Inductor Example

OPERATING PARAMETERS		
V_{IN} = 7 – 16 V	V_{OUT} = 3.3 V	I_{OUT} = 2 A
fSW = 2 MHz	V_{D1} = 0.5 V	

First the maximum duty cycle is calculated with Equation 14.

$$D_{MAX} = (V_{OUT} + V_{D1}) / (V_{IN} + V_{D1} – V_{DS})$$
$$= (3.3 V + 0.5 V) / (7 V + 0.5 V – 0.3 V)$$
$$= 0.528 \quad (14)$$

Using Figure 31 gives us a recommended ripple ratio = 0.4.

Now the minimum duty cycle is calculated with Equation 15.

$$D_{MIN} = (V_{OUT} + V_{D1}) / (V_{IN} + V_{D1} – V_{DS})$$
$$= (3.3 V + 0.5 V) / (16 V + 0.5 V – 0.3 V)$$
$$= 0.235 \quad (15)$$

The inductance can now be calculated with Equation 16.

$$L = (1 – D_{MIN}) × (V_{OUT} + V_{D1}) / (I_{OUT} × r × f_{sw})$$
$$= (1 – 0.235) × (3.3 V + .5 V) / (2 A × 0.4 × 2 MHz)$$
$$= 1.817 µH \quad (16)$$

This is close to the standard inductance value of 1.8 µH. This leads to a 1% deviation from the recommended ripple ratio, which is now 0.4038.

Finally, we check that the peak current does not reach the minimum current limit of 2.5 A with Equation 17.

$$I_{LPK} = I_{OUT} × (1 + r / 2)$$
$$= 2 A × (1 + .4038 / 2)$$
$$= 2.404 A \quad (17)$$

The peak current is less than 2.5 A, so the DC load specification can be met with this ripple ratio. To design for the LM27341 simply replace I_{OUT} = 1.5 A in the equations for I_{LPK} and see that I_{LPK} does not exceed the LM27341's current limit of 2 A (minimum).

8.1.2 Inductor Material Selection

When selecting an inductor, make sure that it is capable of supporting the peak output current without saturating. Inductor saturation results in a sudden reduction in inductance and prevent the regulator from operating correctly. To prevent the inductor from saturating over the entire –40 °C to 125 °C range, pick an inductor with a saturation current higher than the upper limit of I_{CL} listed in *Electrical Characteristics*.

Ferrite core inductors are recommended to reduce AC loss and fringing magnetic flux. The drawback of ferrite core inductors is their quick saturation characteristic. The current limit circuit has a propagation delay and so is oftentimes not fast enough to stop a saturated inductor from going above the current limit. This has the potential to damage the internal switch. To prevent a ferrite core inductor from getting into saturation, the inductor saturation current rating must be higher than the switch current limit I_{CL}. The LM2734x and LM2734x-Q1 are quite robust in handling short pulses of current that are a few amps above the current limit. Saturation protection is provided by a second current limit which is 30% higher than the cycle by cycle current limit. When the saturation protection is triggered the part turns off the output switch and attempt to soft start. When a compromise must be made, pick an inductor with a saturation current just above the lower limit of the I_{CL}. Be sure to validate the short-circuit protection over the intended temperature range.

An inductor's saturation current is usually lower when hot. So consult the inductor vendor if the saturation current rating is only specified at room temperature.

Soft saturation inductors such as the iron powder types can also be used. Such inductors do not saturate suddenly and therefore are safer when there is a severe overload or even shorted output. Their physical sizes are usually smaller than the Ferrite core inductors. The downside is their fringing flux and higher power dissipation due to relatively high AC loss, especially at high frequencies.

8.1.3 Input Capacitor

An input capacitor is necessary to ensure that V_{IN} does not drop excessively during switching transients. The primary specifications of the input capacitor are capacitance, voltage, RMS current rating, and Equivalent Series Inductance (ESL). The recommended input capacitance is 10 µF, although 4.7 µF works well for input voltages below 6 V. The input voltage rating is specifically stated by the capacitor manufacturer. Make sure to check any recommended deratings and also verify if there is any significant change in capacitance at the operating input voltage and the operating temperature. The input capacitor maximum RMS input current rating (I_{RMS-IN}) must be greater than Equation 18.

$$I_{RMS-IN} = I_{OUT} \times \sqrt{D \times \left(1 - D + \frac{r^2}{12}\right)} \tag{18}$$

where

- r is the ripple ratio defined earlier
- I_{OUT} is the output current
- D is the duty cycle

Equation 18 shows that maximum RMS capacitor current occurs when D = 0.5. Always calculate the RMS at the point where the duty cycle, D, is closest to 0.5. The ESL of an input capacitor is usually determined by the effective cross sectional area of the current path. A large leaded capacitor has high ESL and a 0805 ceramic chip capacitor has very low ESL. At the operating frequencies of the LM2734x and LM2734x-Q1, certain capacitors may have an ESL so large that the resulting impedance ($2\pi fL$) is higher than that required to provide stable operation. As a result, TI strongly recommends surface-mount capacitors. Sanyo POSCAP, Tantalum or Niobium, Panasonic SP or Cornell Dubilier Low ESR are all good choices for input capacitors and have acceptable ESL. Multilayer ceramic capacitors (MLCC) have very low ESL. For MLCCs, TI recommends using X7R or X5R dielectrics. Consult the capacitor manufacturer's data sheet to see how rated capacitance varies over operating conditions.

8.1.4 Output Capacitor

The output capacitor is selected based upon the desired output ripple and transient response. The LM2734x and LM2734x-Q1 loop compensation is designed for ceramic capacitors. A minimum of 22 µF is required at 2 MHz (33 µF at 1 MHz) while 47 µF to 100 µF is recommended for improved transient response and higher phase margin. The output voltage ripple of the converter is calculated with Equation 19.

$$\Delta V_{OUT} = \Delta i_L \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \tag{19}$$

When using MLCCs, the ESR is typically so low that the capacitive ripple may dominate. When this occurs, the output ripple is approximately sinusoidal and 90° phase shifted from the switching action. Another benefit of ceramic capacitors is their ability to bypass high-frequency noise. A certain amount of switching edge noise couples through parasitic capacitances in the inductor to the output. A ceramic capacitor bypasses this noise while a tantalum does not.

The transient response is determined by the speed of the control loop and the ability of the output capacitor to provide the initial current of a load transient. Capacitance can be increased significantly with little detriment to the regulator stability. However, increasing the capacitance provides dimininshing improvement over 100 µF in most applications, because the bandwidth of the control loop decreases as output capacitance increases. If improved transient performance is required, add a feedforward capacitor. This becomes especially important for higher output voltages where the bandwidth of the LM2734x and LM2734x-Q1 is lower (see *Feedforward Capacitor (Optional)* and *Frequency Synchronization* for more information).

Check the RMS current rating of the capacitor. The RMS current rating of the capacitor chosen must also meet the following condition with Equation 20.

$$I_{RMS-OUT} = I_{OUT} \times \frac{r}{\sqrt{12}}$$

where

- I_{OUT} is the output current
- r is the ripple ratio

(20)

8.1.5 Catch Diode

The catch diode (D1) conducts during the switch off-time. A Schottky diode is recommended for its fast switching times and low forward voltage drop. The catch diode must be chosen so that its current rating is greater than Equation 21.

$$I_{D1} = I_{OUT} \times (1 - D) \quad (21)$$

The reverse breakdown rating of the diode must be at least the maximum input voltage plus appropriate margin. To improve efficiency, choose a Schottky diode with a low forward voltage drop.

8.1.6 Boost Diode (Optional)

For circuits with input voltages V_{IN} < 5 V and duty cycles (D) > 0.75 V, TI recommends a small-signal Schottky diode. A good choice is the BAT54 small signal diode. The cathode of the diode is connected to the BOOST pin and the anode to a 5-V voltage rail.

8.1.7 Boost Capacitor

A ceramic 0.1-µF capacitor with a voltage rating of at least 6.3 V is sufficient. The X7R and X5R MLCCs provide the best performance.

8.1.8 Output Voltage

The output voltage is set using the following equation where R2 is connected between the FB pin and GND, and R1 is connected between V_{OUT} and the FB pin in Equation 22. A good starting value for R2 is 1 kΩ.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R2 \quad (22)$$

8.1.9 Feedforward Capacitor (Optional)

A feedforward capacitor (C_{FF}) can improve the transient response of the converter. Place C_{FF} in parallel with R1. The value of C_{FF} must place a zero in the loop response at, or above, the pole of the output capacitor and R_{LOAD} as calculated in Equation 23. The C_{FF} capacitor increases the crossover frequency of the design, thus a larger minimum output capacitance is required for designs using C_{FF}. C_{FF} must only be used with an output capacitance greater than or equal to 44 µF.

$$CFF <= \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R1} \quad (23)$$

8.1.10 Calculating Efficiency and Junction Temperature

The complete LM2734x and LM2734x-Q1 DC-DC converter efficiency can be calculated with Equation 24 or Equation 25.

$$\eta = \frac{P_{OUT}}{P_{IN}} \quad (24)$$

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \quad (25)$$

To determine the most significant power losses, see the following equations. Other losses totaling less than 2% are not discussed.

Power loss (P_{LOSS}) is the sum of two basic types of losses in the converter, switching and conduction. Conduction losses usually dominate at higher output loads, where as switching losses remain relatively fixed and dominate at lower output loads. The first step in determining the losses is to calculate the duty cycle (D) with Equation 26.

$$D = \frac{V_{OUT} + V_{D1}}{V_{IN} + V_{D1} - V_{DS}} \quad (26)$$

V_{DS} is the voltage drop across the internal NFET when it is on, and is equal to Equation 27.

$$V_{DS} = I_{OUT} \times R_{DSON} \quad (27)$$

V_D is the forward voltage drop across the Schottky diode. It can be obtained from the *Electrical Characteristics* section of the Schottky diode data sheet. If the voltage drop across the inductor (V_{DCR}) is accounted for, the equation changes to Equation 28.

$$D = \frac{V_{OUT} + V_{D1} + V_{DCR}}{V_{IN} + V_{D1} - V_{DS}} \quad (28)$$

V_{DCR} usually gives only a minor duty cycle change, and has been omitted in the examples for simplicity.

8.1.10.1 Schottky Diode Conduction Losses

The conduction losses in the free-wheeling Schottky diode are calculated with Equation 29.

$$P_{DIODE} = V_{D1} \times I_{OUT} (1 - D) \quad (29)$$

Often this is the single most significant power loss in the circuit. Care must be taken to choose a Schottky diode that has a low forward voltage drop.

8.1.10.2 Inductor Conduction Losses

Another significant external power loss is the conduction loss in the output inductor. The equation can be simplified to Equation 30.

$$P_{IND} = I_{OUT}^2 \times R_{DCR} \quad (30)$$

8.1.10.3 MOSFET Conduction Losses

The LM2734x and LM2734x-Q1 conduction loss is mainly associated with the internal NFET calculated with Equation 31.

$$P_{COND} = I_{OUT}^2 \times R_{DSON} \times D \quad (31)$$

8.1.10.4 MOSFET Switching Losses

Switching losses are also associated with the internal NFET. They occur during the switch on and off transition periods, where voltages and currents overlap resulting in power loss. The simplest means to determine this loss is to empirically measuring the rise and fall times (10% to 90%) of the switch at the switch node with Equation 32, Equation 33, and Equation 34. Typical values are listed in Table 2.

$$P_{SWF} = 1 / 2 (V_{IN} \times I_{OUT} \times f_{SW} \times t_{FALL}) \quad (32)$$

$$P_{SWR} = 1 / 2 (V_{IN} \times I_{OUT} \times f_{SW} \times t_{RISE}) \quad (33)$$

$$P_{SW} = P_{SWF} + P_{SWR} \quad (34)$$

Table 2. Typical Rise and Fall Times vs Input Voltage

V_{IN}	t_{RISE}	t_{FALL}
5 V	8 ns	8 ns
10 V	9 ns	9 ns
15 V	10 ns	10 ns

8.1.10.5 IC Quiescent Losses

Another loss is the power required for operation of the internal circuitry calculated with Equation 35.

$$P_Q = I_Q \times V_{IN} \quad (35)$$

I_Q is the quiescent operating current, and is typically around 2.4 mA.

8.1.10.6 MOSFET Driver Losses

The other operating power that needs calculation is that required to drive the internal NFET with Equation 36.

$$P_{BOOST} = I_{BOOST} \times V_{BOOST} \quad (36)$$

V_{BOOST} is normally between 3 VDC and 5 VDC. The I_{BOOST} rms current is dependant on switching frequency f_{SW}. I_{BOOST} is approximately 8.2 mA at 2 MHz and 4.4 mA at 1 MHz.

8.1.10.7 Total Power Losses

Total power losses is calculated with Equation 37.

$$P_{LOSS} = P_{COND} + P_{SWR} + P_{SWF} + P_Q + P_{BOOST} + P_{DIODE} + P_{IND} \quad (37)$$

Losses internal to the LM2734x and LM2734x-Q1 is calculated with Equation 38.

$$P_{INTERNAL} = P_{COND} + P_{SWR} + P_{SWF} + P_Q + P_{BOOST} \quad (38)$$

8.1.10.8 Efficiency Calculation Example

Operating conditions are listed in Table 3.

Table 3. Operating Conditions for Efficiency Calculation

OPERATING PARAMETERS		
V_{IN} = 12 V	V_{OUT} = 3.3 V	I_{OUT} = 2 A
f_{SW} = 2 MHZ	V_{D1} = 0.5 V	R_{DCR} = 20 mΩ

Internal power losses are calculated with Equation 39 through Equation 43.

$$P_{COND} = I_{OUT}^2 \times R_{DSON} \times D$$
$$= 2^2 \times 0.15\ \Omega \times 0.314$$
$$= 188\ mW \quad (39)$$

$$P_{SW} = (V_{IN} \times I_{OUT} \times f_{SW} \times t_{FALL})$$
$$= (12\ V \times 2A \times 2\ MHz \times 10\ ns)$$
$$= 480\ mW \quad (40)$$

$$P_Q = I_Q \times V_{IN}$$
$$= 2.4\ mA \times 12\ V$$
$$= 29\ mW \quad (41)$$

$$P_{BOOST} = I_{BOOST} \times V_{BOOST}$$
$$= 8.2\ mA \times 4.5\ V$$
$$= 37\ mW \quad (42)$$

$$P_{INTERNAL} = P_{COND} + P_{SW} + P_Q + P_{BOOST} = 733\ mW \quad (43)$$

Total power losses are calculated with Equation 44 through Equation 46.

$$P_{DIODE} = V_{D1} \times I_{OUT} (1 - D)$$
$$= 0.5\ V \times 2 \times (1 - 0.314)$$
$$= 686\ mW \quad (44)$$

$$P_{IND} = I_{OUT}^2 \times R_{DCR}$$

$= 2^2 \times 20\ m\Omega$

$= 80\ mW$ (45)

$P_{LOSS} = P_{INTERNAL} + P_{DIODE} + P_{IND} = 1.499\ W$ (46)

The efficiency can now be estimated with Equation 47.

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} = \frac{6.6W}{6.6W + 1.499W} = 81\% \quad (47)$$

With this information, we can estimate the junction temperature of the LM2734x and LM2734x-Q1.

8.1.10.9 Calculating Junction Temperature

The thermal definitions are:

- T_J = IC junction temperature
- T_A = Ambient temperature
- $R_{\theta JC}$ = Thermal resistance from IC junction to device case
- $R_{\theta JA}$ = Thermal resistance from IC junction to ambient air

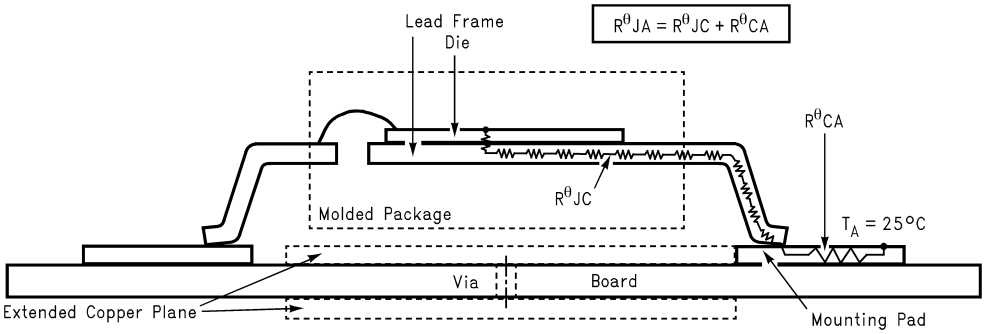


Figure 32. Cross-Sectional View of Integrated Circuit Mounted on a Printed Circuit Board

Heat in the LM2734x and LM2734x-Q1 due to internal power dissipation is removed through conduction and/or convection.

8.1.10.9.1 Conduction

Heat transfer occurs through cross sectional areas of material. Depending on the material, the transfer of heat can be considered to have poor-to-good thermal conductivity properties (insulator versus conductor).

Heat transfer goes from Silicon → Lead Frame → PCB.

8.1.10.9.2 Convection

Heat transfer is by means of airflow. This could be from a fan or natural convection. Natural convection occurs when air currents rise from the hot device to cooler air.

Thermal impedance is defined with Equation 48.

$$R\theta = \frac{\Delta T}{Power} \quad (48)$$

Thermal impedance from the silicon junction to the ambient air is defined with Equation 49.

$$R_{\theta JA} = \frac{T_J - T_A}{Power} \quad (49)$$

This impedance can vary depending on the thermal properties of the PCB. This includes PCB size, weight of copper used to route traces , the ground plane, and the number of layers within the PCB. The type and number of thermal vias can also make a large difference in the thermal impedance. Thermal vias are necessary in most applications. They conduct heat from the surface of the PCB to the ground plane. Six to nine thermal vias must be placed under the exposed pad to the ground plane. Placing more than nine thermal vias results in only a small reduction to $R_{\theta JA}$ for the same copper area. These vias must have 8-mil holes to avoid wicking solder away from the DAP. See *AN-1187 Leadless Leadframe Package* (SNOA401) and *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Packages* (SNVA183) for more information on package thermal performance. If a compromise for cost needs to be made, the thermal vias for the MSOP-PowerPAD package can range from 8 mils to 14 mils, increasing the possibility of solder wicking.

To predict the silicon junction temperature for a given application, three methods can be used. The first is useful before prototyping and the other two can more accurately predict the junction temperature within the application.

8.1.10.9.3 Method 1

The first method predicts the junction temperature by extrapolating a best guess $R_{\theta JA}$ from the table or graph. The tables and graph are for natural convection. The internal dissipation can be calculated using the efficiency calculations. This allows the user to make a rough prediction of the junction temperature in their application. Methods two and three can later be used to determine the junction temperature more accurately.

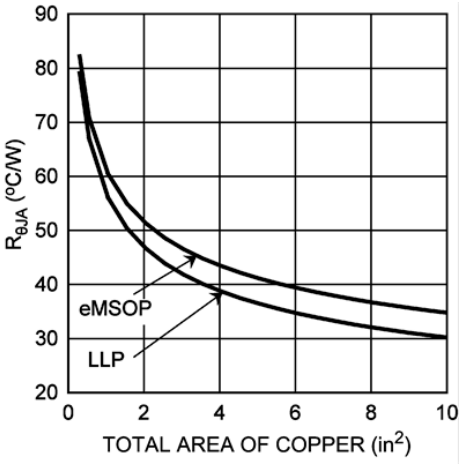
Table 4 and Table 5 have values of $R_{\theta JA}$ for the WSON and the MSOP-PowerPAD packages.

Table 4. $R_{\theta JA}$ Values for the MSOP-PowerPAD at 1-W Dissipation

NUMBER OF BOARD LAYERS	SIZE OF BOTTOM LAYER COPPER CONNECTED TO DAP	SIZE OF TOP LAYER COPPER CONNECTED TO DAP	NUMBER OF 10 MIL THERMAL VIAS	$R_{\theta JA}$
2	0.25 in^2	0.05 in^2	8	80.6°C/W
2	0.5625 in^2	0.05 in^2	8	70.9°C/W
2	1 in^2	0.05 in^2	8	62.1°C/W
2	1.3225 in^2	0.05 in^2	8	54.6°C/W
4 (eval board)	3.25 in^2	2.25 in^2	14	35.3°C/W

Table 5. $R_{\theta JA}$ Values for the WSON at 1-W Dissipation

NUMBER OF BOARD LAYERS	SIZE OF BOTTOM LAYER COPPER CONNECTED TO DAP	SIZE OF TOP LAYER COPPER CONNECTED TO DAP	NUMBER OF 8 MIL THERMAL VIAS	$R_{\theta JA}$
2	0.25 in^2	0.05 in^2	8	78°C/W
2	0.5625 in^2	0.05 in^2	8	65.6°C/W
2	1 in^2	0.05 in^2	8	58.6°C/W
2	1.3225 in^2	0.05 in^2	8	50°C/W
4 (eval board)	3.25 in^2	2.25 in^2	15	30.7°C/W



Eight thermal vias and natural convection

Figure 33. Estimate of Thermal Resistance vs Ground Copper Area

8.1.10.9.4 Method 2

The second method requires the user to know the thermal impedance of the silicon junction to case. $R_{\theta JC}$ is approximately 9.5°C/W for the MSOP-PowerPAD package or 9.1°C/W for the WSON. The case temperature must be measured on the bottom of the PCB at a thermal through directly under the DAP of the LM2734x and LM2734x-Q1. The solder resist must be removed from this area for temperature testing. The reading is more accurate if it is taken midway between pins 2 and 9, where the NMOS switch is placed. Knowing the internal dissipation from *Method 1*, calculate the case temperature (T_C) with Equation 50 and Equation 51.

$$R_{\theta JC} = \frac{T_J - T_C}{Power} \tag{50}$$

$$T_J = (R_{\theta JC} \times P_{LOSS}) + T_C \tag{51}$$

8.1.10.9.4.1 Method 2 Example

The operating conditions are the same as the previous efficiency calculation listed in Table 6.

Table 6. Operating Conditions for Efficiency Calculation

OPERATING PARAMETERS		
V_{IN} = 12 V	V_{OUT} = 3.3 V	I_{OUT} = 2 A
f_{SW} = 2 MHz	V_{D1} = 0.5 V	R_{DCR} = 20 mΩ

Internal power losses are calculated with Equation 52 through Equation 56.

$$P_{COND} = I_{OUT}^2 \times R_{DSON} \times D$$
$$= 2^2 \times 0.15\ \Omega \times 0.314$$
$$= 188\ mW \tag{52}$$

$$P_{SW} = (V_{IN} \times I_{OUT} \times f_{SW} \times t_{FALL})$$
$$= (12\ V \times 2\ A \times 2\ MHz \times 10\ ns)$$
$$= 480\ mW \tag{53}$$

$$P_Q = I_Q \times V_{IN}$$
$$= 1.5\ mA \times 12\ V$$
$$= 29\ mW \tag{54}$$

$$P_{BOOST} = I_{BOOST} \times V_{BOOST}$$
$$= 7\ mA \times 4.5\ V$$
$$= 37\ mW \tag{55}$$

$$P_{INTERNAL} = P_{COND} + P_{SW} + P_Q + P_{BOOST} = 733\ mW \tag{56}$$

The junction temperature can now be estimated with Equation 57.

$$T_J = (R_{\theta JC} \times P_{INTERNAL}) + T_C \quad (57)$$

A TI MSOP-PowerPAD evaluation board was used to determine the T_J of the LM2734x and LM2734x-Q1. The four layer PCB is constructed using FR4 with 2-oz copper traces. There is a ground plane on the internal layer directly beneath the device, and a ground plane on the bottom layer. The ground plane is accessed by fourteen 10-mil vias. The board measures 2 in × 2 in (50.8 mm × 50.8 mm). It was placed in a container with no airflow. The case temperature measured on this LM27342MY Demo Board was 48.7°C. Therefore, T_J is calculated with Equation 58 and Equation 59.

$$T_J = (9.5°C/W \times 733\ mW) + 48.7°C \quad (58)$$

$$T_J = 55.66°C \quad (59)$$

To keep the junction temperature below 125°C for this layout, the ambient temperature must stay below 94.33°C as in Equation 60, Equation 61, and Equation 62.

$$T_{A\_MAX} = T_{J\_MAX} – T_J + T_A \quad (60)$$

$$T_{A\_MAX} = 125°C – 55.66°C + 25°C \quad (61)$$

$$T_{A\_MAX} = 94.33°C \quad (62)$$

8.1.10.9.5 Method 3

The third method can also give a very accurate estimate of silicon junction temperature. The first step is to determine $R_{\theta JA}$ of the application. The LM2734x and LM2734x-Q1 has overtemperature protection circuitry. When the silicon temperature reaches 165°C, the device stops switching. The protection circuitry has a hysteresis of 15°C. Once the silicon temperature has decreased to approximately 150°C, the device starts switching again. Knowing this, the $R_{\theta JA}$ for any PCB can be characterized during the early stages of the design by raising the ambient temperature in the given application until the circuit enters thermal shutdown. If the SW-pin is monitored, it is obvious when the internal NFET stops switching indicating a junction temperature of 165°C. We can calculate the internal power dissipation from the above methods. All that is required for calculation is the estimate of R_{DSON} at 165°C. The value is approximately 0.267 Ω. With this, the junction temperature, and the ambient temperature, $R_{\theta JA}$, can be determined with Equation 63.

$$R_{\theta JA} = \frac{165°C – T_A}{P_{INTERNAL}} \quad (63)$$

Once this is determined, the maximum ambient temperature allowed for a desired junction temperature can be found.

8.1.10.9.5.1 Method 3 Example

The operating conditions are the same as the previous efficiency calculation listed in Table 7.

Table 7. Operating Conditions for Efficiency Calculation

OPERATING PARAMETERS		
V_{IN} = 12 V	V_{OUT} = 3.3 V	I_{OUT} = 2A
f_{SW} = 2 MHz	V_{D1} = 0.5 V	R_{DCR} = 20 mΩ

Internal power losses are calculated with Equation 64 through Equation 68.

$$P_{COND} = I_{OUT}^2 \times R_{DSON} \times D$$
$$= 2^2 \times 0.267\ \Omega \times .314$$
$$= 335\ mW \quad (64)$$

$$P_{SW} = (V_{IN} \times I_{OUT} \times f_{SW} \times t_{FALL})$$
$$= (12\ V \times 2\ A \times 2\ MHz \times 10\ nS)$$
$$= 480\ mW \quad (65)$$

$$P_Q = I_Q \times V_{IN}$$
$$= 1.5\ mA \times 12\ V$$
$$= 29\ mW \quad (66)$$

$$P_{BOOST} = I_{BOOST} \times V_{BOOST}$$
$$= 7\ mA \times 4.5\ V$$

= 37 mW (67)

$P_{INTERNAL} = P_{COND} + P_{SW} + P_Q + P_{BOOST}$ = 881 mW (68)

A TI MSOP-PowerPAD evaluation board was used to determine the $R_{\theta JA}$ of the board. The four-layer PCB is constructed using FR4 with 2oz copper traces. There is a ground plane on the internal layer directly beneath the device, and a ground plane on the bottom layer. The ground plane is accessed by fourteen 10-mil vias. The board measures 2 in × 2 in (50.8 mm × 50.8 mm). It was placed in an oven with no forced airflow.

The ambient temperature was raised to 132°C, and at that temperature, the device went into thermal shutdown. $R_{\theta JA}$ can be calculated with Equation 69.

$$R\theta JA = \frac{165°C - 132°C}{0.881\,W} = 37.46\ °C/W \quad (69)$$

To keep the junction temperature below 125°C for this layout, the ambient temperature must stay below 92°C as in Equation 70, Equation 71, and Equation 72.

$T_{A\_MAX} = T_{J\_MAX} – (R_{\theta JA} \times P_{INTERNAL})$ (70)

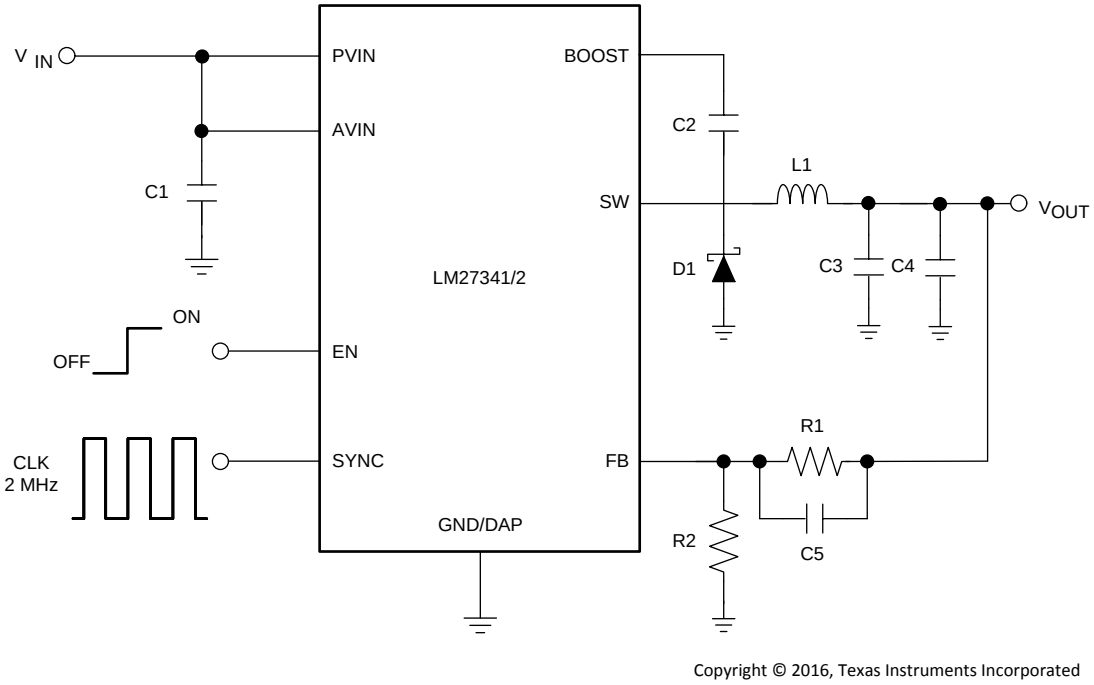
T_{A_MAX} = 125°C – (37.46°C/W × 0.881 W) (71)

T_{A_MAX} = 92°C (72)

This calculation of the maximum ambient temperature is only 2.3°C different from the calculation using method 2. The methods described above to find the junction temperature in the MSOP-PowerPAD package can also be used to calculate the junction temperature in the WSON package. The 10-pin WSON package has a $R_{\theta JC}$ = 9.1°C/W, while $R_{\theta JA}$ can vary depending on the layout. $R_{\theta JA}$ can be calculated in the same manner as described in method 3.

8.2 Typical Applications

8.2.1 LM2734x Configuration From V_{IN} = 7 V to 16 V, V_{OUT} = 5 V For Full Load at 2 MHz



V_{IN} = 7 V to 16 V, V_{OUT} = 5 V f_{SW} = 2 MHz I_{OUT} = Full load

Figure 34. LM2734x Configuration From V_{IN} = 7 V to 16 V, V_{OUT} = 5 V For Full Load at 2-MHz Schematic

Typical Applications (continued)

8.2.1.1 Design Requirements

Create 5-V output at full-rated load for V_{IN} range of 7 V to 16 V with switching frequency F_{SW} = 2 MHz using external synchronization.

8.2.1.2 Detailed Design Procedure

The device must be able to operate at any voltage within the recommended operating range. The load current must be defined to properly size the inductor, input, and output capacitors. The inductor must be able to handle the full expected load current as well as the peak current generated during load transients and start-up. The inrush current at start-up depends on the output capacitor selection.

Table 8 lists the bill of materials for V_{IN} = 7 V to 16 V, V_{OUT} = 5 V for full load at 2 MHz. See Figure 34.

Table 8. Bill of Materials

PART NAME	PART ID	PART VALUE	PART NUMBER	MANUFACTURER
Buck regulator	U1	1.5-A or 2-A Buck regulator	LM2734x and LM2734x-Q1	TI
C_{PVIN}	C1	10 µF	GRM32DR71E106KA12L	Murata
C_{BOOST}	C2	0.1 µF	GRM188R71C104KA01D	Murata
C_{OUT}	C3	22 µF	C3225X7R1C226K	TDK
C_{OUT}	C4	22 µF	C3225X7R1C226K	TDK
C_{FF}	C5	0.18 µF	0603ZC184KAT2A	AVX
Catch diode	D1	Schottky diode, Vf = 0.32 V	CMS06	Toshiba
Inductor	L1	2.2 µH	CDRHD5D28RHPNP	Sumida
Feedback resistor	R1	560 Ω	CRCW0603560RFKEA	Vishay
Feedback resistor	R2	140 Ω	CRCW0603140RFKEA	Vishay

8.2.1.3 Application Curves

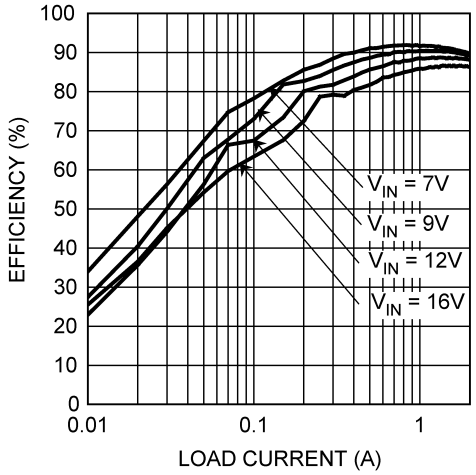
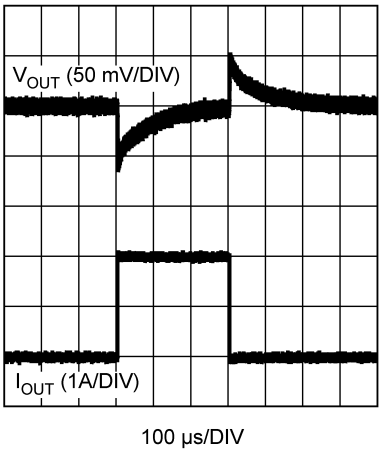


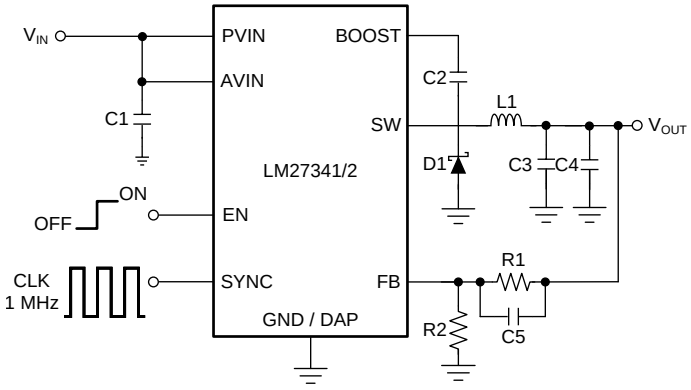
Figure 35. LM27342 Efficiency vs Load Current



I_{OUT} = 100 mA – 2 A at Slewrate = 2 A / µs

Figure 36. Transient Response

8.2.2 LM2734x Configuration From V_{IN} = 7 V to 16 V, V_{OUT} = 5 V For Full Load at 1 MHz



V_{IN} = 7 V to 16 V, V_{OUT} = 5 V f_{SW} = 1 MHz I_{OUT} = Full load

Figure 37. LM2734x Configuration From V_{IN} = 7 V to 16 V, V_{OUT} = 5 V For Full Load at 1-MHz Schematic

8.2.2.1 Design Requirements

Create 5-V output at full-rated load for V_{IN} range of 7 V to 16 V with switching frequency F_{SW} = 1 MHz using external synchronization.

8.2.2.2 Detailed Design Procedure

The device must be able to operate at any voltage within the recommended operating range. The load current must be defined to properly size the inductor, input, and output capacitors. The inductor must be able to handle the full expected load current as well as the peak current generated during load transients and start-up. The inrush current at start-up depends on the output capacitor selection.

Table 9 lists the bill of materials for V_{IN} = 7 V to 16 V, V_{OUT} = 5 V for full load at 1 MHz. See Figure 37.

Table 9. Bill of Materials

PART NAME	PART ID	PART VALUE	PART NUMBER	MANUFACTURER
Buck regulator	U1	1.5-A or 2-A Buck regulator	LM2734x and LM2734x-Q1	TI
C_{PVIN}	C1	10 µF	GRM32DR71E106KA12L	Murata
C_{BOOST}	C2	0.1 µF	GRM188R71C104KA01D	Murata
C_{OUT}	C3	47 µF	GRM32ER61A476KE20L	Murata
C_{OUT}	C4	22 µF	C3225X7R1C226K	TDK
C_{FF}	C5	0.27 µF	C0603C274K4RACTU	Kemet
Catch diode	D1	Schottky diode, Vf = 0.32 V	CMS06	Toshiba
Inductor	L1	3.3 µH	CDRH6D26HPNP	Sumida
Feedback resistor	R1	560 Ω	CRCW0603560RFKEA	Vishay
Feedback resistor	R2	140 Ω	CRCW0603140RFKEA	Vishay

8.2.2.3 Application Curves

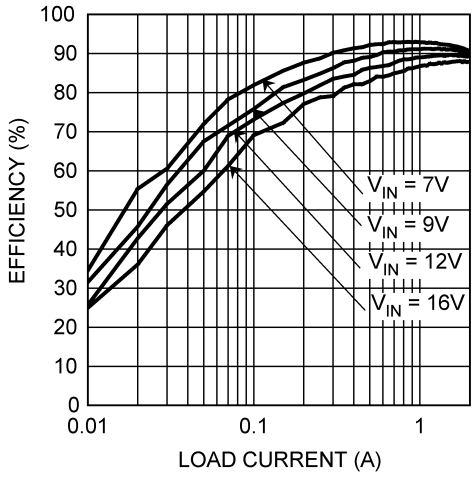
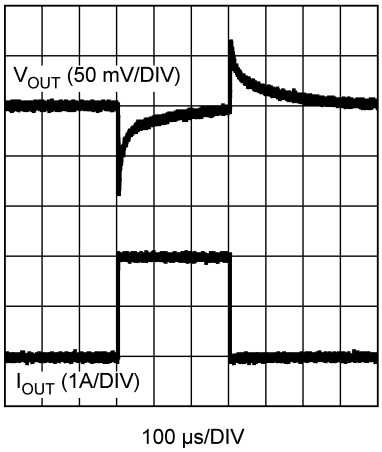


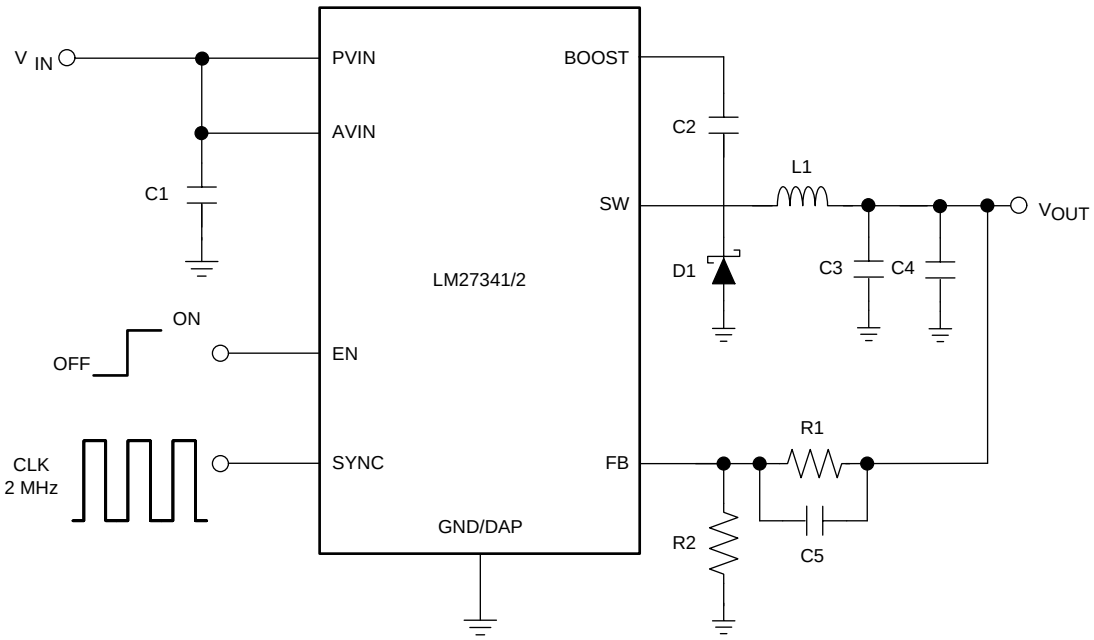
Figure 38. LM27342 Efficiency vs Load Current



I_{OUT} = 100 mA – 2 A at Slewrate = 2 A / µs

Figure 39. Transient Response

8.2.3 LM2734x Configuration From V_{IN} = 5 V to 16 V, V_{OUT} = 3.3 V For Full Load at 2 MHz



V_{IN} = 5 V to 16 V, V_{OUT} = 3.3 V f_{SW} = 2 MHz I_{OUT} = Full load

Figure 40. LM2734x Configuration From V_{IN} = 5 V to 16 V, V_{OUT} = 3.3 V For Full Load at 2-MHz Schematic

8.2.3.1 Design Requirements

Create 3.3-V output at full-rated load for V_{IN} range of 5 V to 16 V with switching frequency F_{SW} = 2 MHz using external synchronization.

8.2.3.2 Detailed Design Procedure

The device must be able to operate at any voltage within the recommended operating range. The load current must be defined to properly size the inductor, input, and output capacitors. The inductor must be able to handle the full expected load current as well as the peak current generated during load transients and start-up. The inrush current at start-up depends on the output capacitor selection.

Table 10 lists the bill of materials for V_{IN} = 5 V to 16 V, V_{OUT} = 3.3 V for full load at 2 MHz. See Figure 40.

Table 10. Bill of Materials

PART NAME	PART ID	PART VALUE	PART NUMBER	MANUFACTURER
Buck regulator	U1	1.5-A or 2-A Buck regulator	LM2734x and LM2734x-Q1	TI
C_{PVIN}	C1	10 µF	GRM32DR71E106KA12L	Murata
C_{BOOST}	C2	0.1 µF	GRM188R71C104KA01D	Murata
C_{OUT}	C3	22 µF	C3225X7R1C226K	TDK
C_{OUT}	C4	22 µF	C3225X7R1C226K	TDK
C_{FF}	C5	0.18 µF	0603ZC184KAT2A	AVX
Catch diode	D1	Schottky diode, Vf = 0.32 V	CMS06	Toshiba
Inductor	L1	1.5 µH	CDRH5D18BHPNP	Sumida
Feedback resistor	R1	430 Ω	CRCW0603430RFKEA	Vishay
Feedback resistor	R2	187 Ω	CRCW0603187RFKEA	Vishay

8.2.3.3 Application Curves

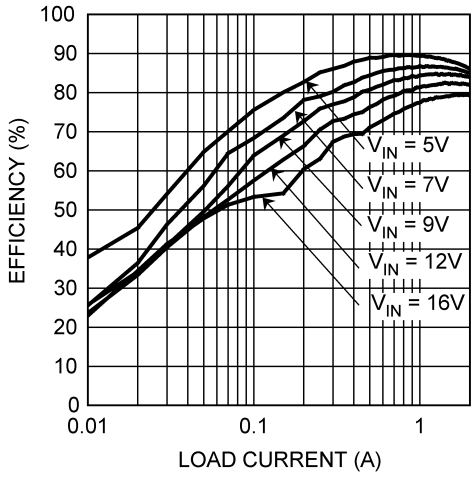
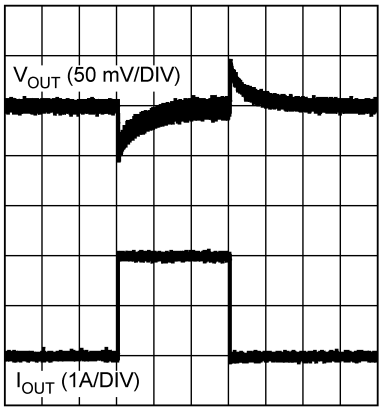


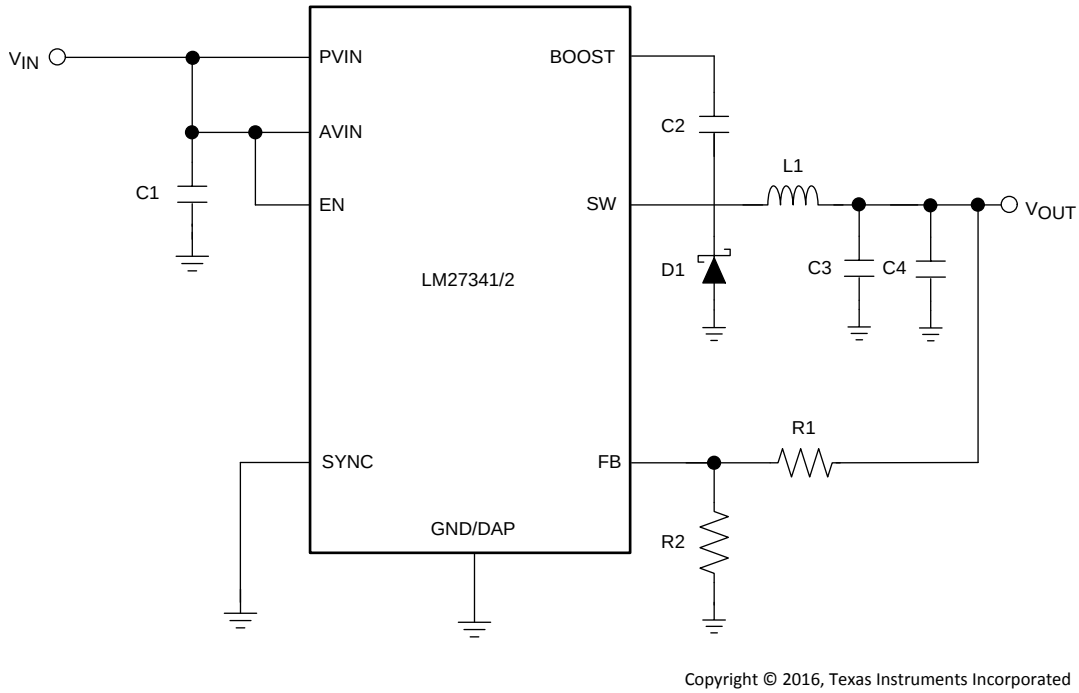
Figure 41. LM27342 Efficiency vs Load Current



I_{OUT} = 100 mA – 2 A at Slewrate = 2 A / µs

Figure 42. Transient Response

8.2.4 LM2734x Configuration From V_{IN} = 5 V to 16 V, V_{OUT} = 3.3 V For Full Load at 2 MHz With SYNC = GND



V_{IN} = 5 V to 16 V, V_{OUT} = 3.3 V f_{SW} = 2 MHz I_{OUT} = Full load

Figure 43. LM2734x Configuration From V_{IN} = 5 V to 16 V, V_{OUT} = 3.3 V For Full Load at 2 MHz With SYNC = GND Schematic

8.2.4.1 Design Requirements

Create 3.3-V output at full-rated load for V_{IN} range of 5 V to 16 V with switching frequency F_{SW} = 2 MHz using internal oscillator.

8.2.4.2 Detailed Design Procedure

The device must be able to operate at any voltage within the recommended operating range. The load current must be defined to properly size the inductor, input, and output capacitors. The inductor must be able to handle the full expected load current as well as the peak current generated during load transients and start-up. The inrush current at start-up depends on the output capacitor selection.

Table 11 lists the bill of materials for V_{IN} = 5 V to 16 V, V_{OUT} = 3.3 V for full load at 2 MHz with SYNC = GND. See Figure 43.

Table 11. Bill of Materials

PART NAME	PART ID	PART VALUE	PART NUMBER	MANUFACTURER
Buck regulator	U1	1.5-A or 2-A Buck regulator	LM2734x and LM2734x-Q1	TI
C_{PVIN}	C1	10 µF	GRM32DR71E106KA12L	Murata
C_{BOOST}	C2	0.1 µF	GRM188R71C104KA01D	Murata
C_{OUT}	C3	22 µF	C3225X7R1C226K	TDK
C_{OUT}	C4	22 µF	C3225X7R1C226K	TDK
Catch diode	D1	Schottky diode, Vf = 0.32 V	CMS06	Toshiba
Inductor	L1	1.5 µH	CDRH5D18BHPNP	Sumida
Feedback resistor	R1	430 Ω	CRCW0603430RFKEA	Vishay
Feedback resistor	R2	187 Ω	CRCW0603187RFKEA	Vishay

8.2.4.3 Application Curves

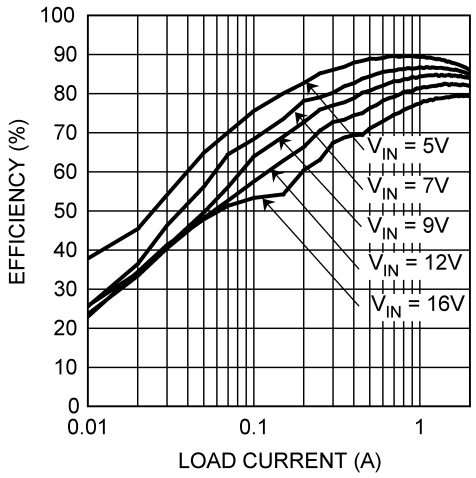
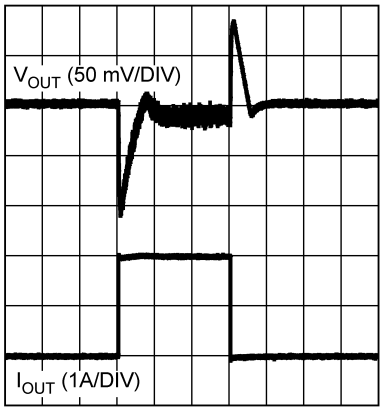


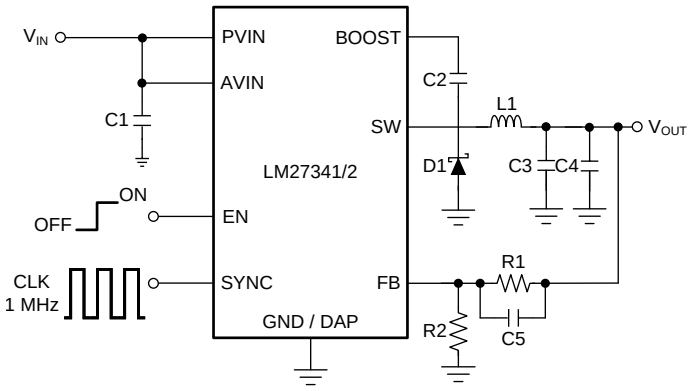
Figure 44. LM27342 Efficiency vs Load Current



I_{OUT} = 100 mA – 2 A at Slewrate = 2 A / µs

Figure 45. Transient Response

8.2.5 LM2734x Configuration From V_{IN} = 5 V to 16 V, V_{OUT} = 3.3 V For Full Load at 2 MHz With SYNC = 1 MHz



V_{IN} = 5 V to 16 V, V_{OUT} = 3.3 V f_{SW} = 1 MHz I_{OUT} = Full load

Figure 46. LM2734x Configuration From V_{IN} = 5 V to 16 V, V_{OUT} = 3.3 V For Full Load at 2 MHz With SYNC = 1-MHz Schematic

8.2.5.1 Design Requirements

Create 1.8-V output at full-rated load for V_{IN} range of 5 V to 16 V with switching frequency F_{SW} = 1 MHz using external synchronization.

8.2.5.2 Detailed Design Procedure

The device must be able to operate at any voltage within the recommended operating range. The load current must be defined to properly size the inductor, input, and output capacitors. The inductor must be able to handle the full expected load current as well as the peak current generated during load transients and start-up. The inrush current at start-up depends on the output capacitor selection.

Table 12 lists the bill of materials for V_{IN} = 5 V to 16 V, V_{OUT} = 3.3 V for full load at 2 MHz with SYNC = 1 MHz. See Figure 46.

Table 12. Bill of Materials

PART NAME	PART ID	PART VALUE	PART NUMBER	MANUFACTURER
Buck regulator	U1	1.5-A or 2-A Buck regulator	LM2734x and LM2734x-Q1	TI
C_{PVIN}	C1	10 µF	GRM32DR71E106KA12L	Murata
C_{BOOST}	C2	0.1 µF	GRM188R71C104KA01D	Murata
C_{OUT}	C3	47 µF	GRM32ER61A476KE20L	Murata
C_{OUT}	C4	22 µF	C3225X7R1C226K	TDK
C_{FF}	C5	0.27 µF	C0603C274K4RACTU	Kemet
Catch diode	D1	Schottky diode, Vf = 0.32 V	CMS06	Toshiba
Inductor	L1	2.7 µH	CDRH5D18BHPNP	Sumida
Feedback resistor	R1	430 Ω	CRCW0603430RFKEA	Vishay
Feedback resistor	R2	187 Ω	CRCW0603187RFKEA	Vishay

8.2.5.3 Application Curves

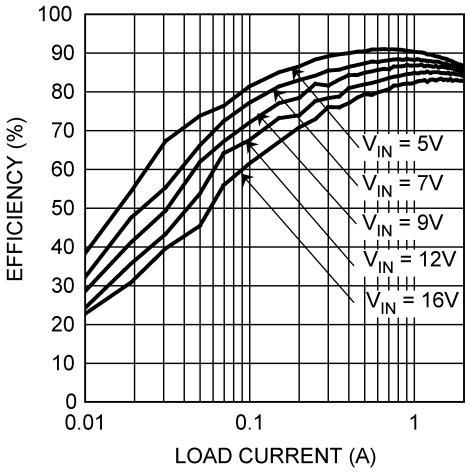
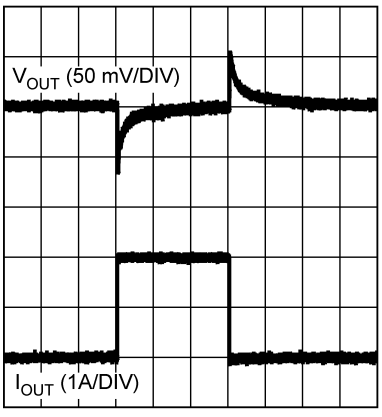


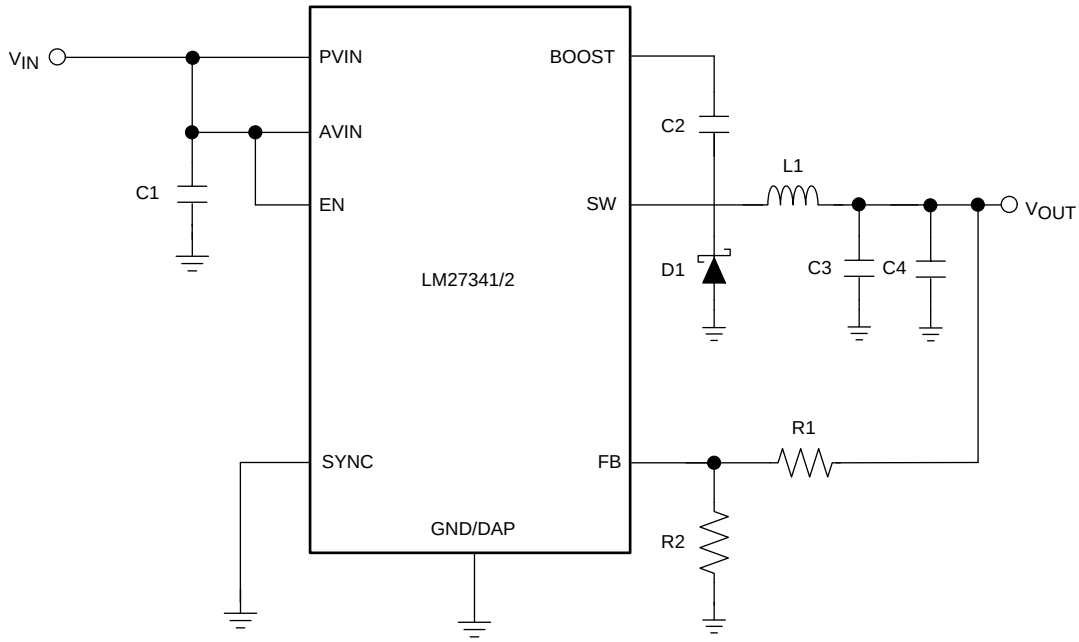
Figure 47. LM27342 Efficiency vs Load Current



I_{OUT} = 100 mA – 2 A at Slewrate = 2 A / µs

Figure 48. Transient Response

8.2.6 LM2734x Configuration From V_{IN} = 3.3 V to 16 V, V_{OUT} = 1.8 V For Full Load at 2 MHz With SYNC = 1 GND



V_{IN} = 3.3 V to 16 V, V_{OUT} = 1.8 V f_{SW} = 2 MHz I_{OUT} = Full load

Figure 49. LM2734x Configuration From V_{IN} = 3.3 V to 16 V, V_{OUT} = 1.8 V For Full Load at 2 MHz With SYNC = GND Schematic

8.2.6.1 Design Requirements

Create 1.8-V output at full-rated load for V_{IN} range of 3.3 V to 16 V with switching frequency F_{SW} = 2 MHz using internal oscillator.

8.2.6.2 Detailed Design Procedure

The device must be able to operate at any voltage within the recommended operating range. The load current must be defined to properly size the inductor, input, and output capacitors. The inductor must be able to handle the full expected load current as well as the peak current generated during load transients and start-up. The inrush current at start-up depends on the output capacitor selection.

Table 13 lists the bill of materials for V_{IN} = 3.3 V to 16 V, V_{OUT} = 1.8 V for full load at 2 MHz with SYNC = GND. See Figure 49.

Table 13. Bill of Materials

PART NAME	PART ID	PART VALUE	PART NUMBER	MANUFACTURER
Buck regulator	U1	1.5-A or 2-A Buck regulator	LM2734x and LM2734x-Q1	TI
C_{PVIN}	C1	10 µF	GRM32DR71E106KA12L	Murata
C_{BOOST}	C2	0.1 µF	GRM188R71C104KA01D	Murata
C_{OUT}	C3	22 µF	C3225X7R1C226K	TDK
C_{OUT}	C4	22 µF	C3225X7R1C226K	TDK
Catch diode	D1	Schottky diode, Vf = 0.32 V	CMS06	Toshiba
Inductor	L1	1 µH	CDRH5D18BHPNP	Sumida
Feedback resistor	R1	12 kΩ	CRCW060312K0FKEA	Vishay
Feedback resistor	R2	15 kΩ	CRCW060315K0FKEA	Vishay

8.2.6.3 Application Curves

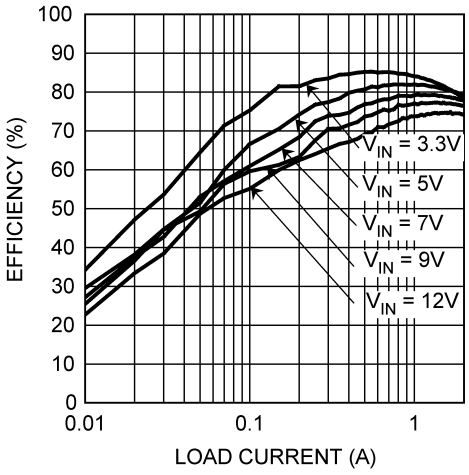
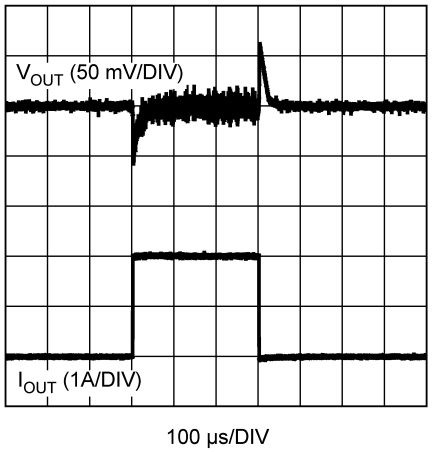


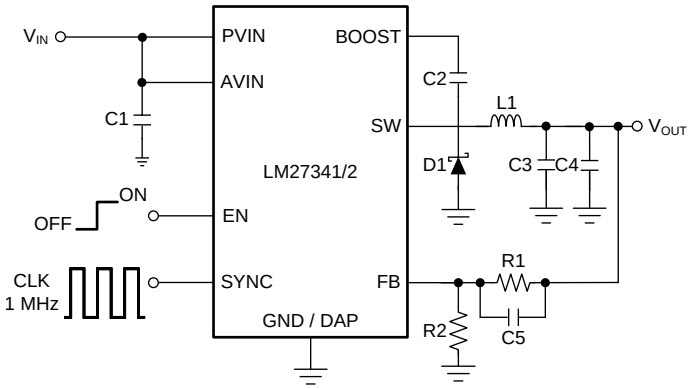
Figure 50. LM27342 Efficiency vs Load Current



I_{OUT} = 100 mA – 2 A at Slewrate = 2 A / µs

Figure 51. Transient Response

8.2.7 LM2734x Configuration From V_{IN} = 3.3 V to 16 V, V_{OUT} = 1.8 V For Full Load at 2 MHz With SYNC = 1 MHz



V_{IN} = 3.3 V to 16 V, V_{OUT} = 1.8 V f_{SW} = 1 MHz I_{OUT} = Full load

Figure 52. LM2734x Configuration From V_{IN} = 3.3 V to 16 V, V_{OUT} = 1.8 V For Full Load at 2 MHz With SYNC = 1-MHz Schematic

8.2.7.1 Design Requirements

Create 1.8-V output at full-rated load for V_{IN} range of 3.3 V to 16 V with switching frequency F_{SW} = 1 MHz using external synchronization.

8.2.7.2 Detailed Design Procedure

The device must be able to operate at any voltage within the recommended operating range. The load current must be defined to properly size the inductor, input, and output capacitors. The inductor must be able to handle the full expected load current as well as the peak current generated during load transients and start-up. The inrush current at start-up depends on the output capacitor selection.

Table 14 lists the bill of materials for V_{IN} = 3.3 V to 16 V, V_{OUT} = 1.8 V for full load at 2 MHz with SYNC = 1 MHz. See Figure 52.

Table 14. Bill of Materials

PART NAME	PART ID	PART VALUE	PART NUMBER	MANUFACTURER
Buck regulator	U1	1.5-A or 2-A Buck regulator	LM2734x and LM2734x-Q1	TI
C_{PVIN}	C1	10 µF	GRM32DR71E106KA12L	Murata
C_{BOOST}	C2	0.1 µF	GRM188R71C104KA01D	Murata
C_{OUT}	C3	22 µF	C3225X7R1C226K	TDK
C_{OUT}	C4	22 µF	C3225X7R1C226K	TDK
C_{FF}	C5	3.9 nF	GRM188R71H392KA01D	Murata
Catch diode	D1	Schottky diode, Vf = 0.32 V	CMS06	Toshiba
Inductor	L1	1.8 µH	CDRH5D18BHPNP	Sumida
Feedback resistor	R1	12 kΩ	CRCW060312K0FKEA	Vishay
Feedback resistor	R2	15 kΩ	CRCW060315K0FKEA	Vishay

8.2.7.3 Application Curves

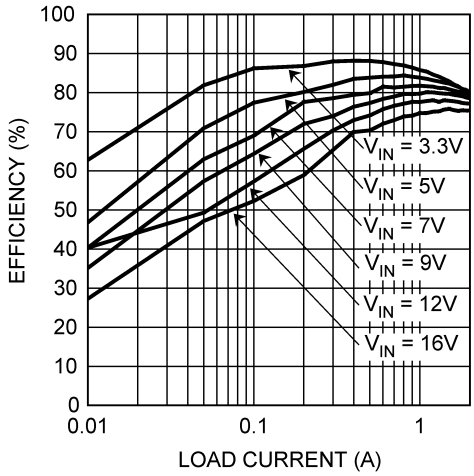
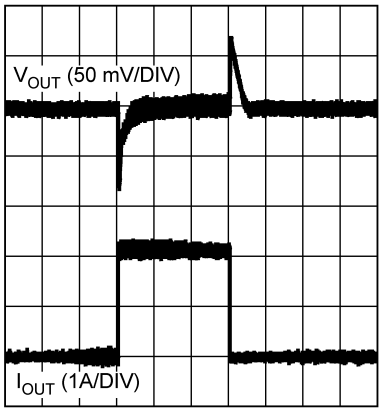


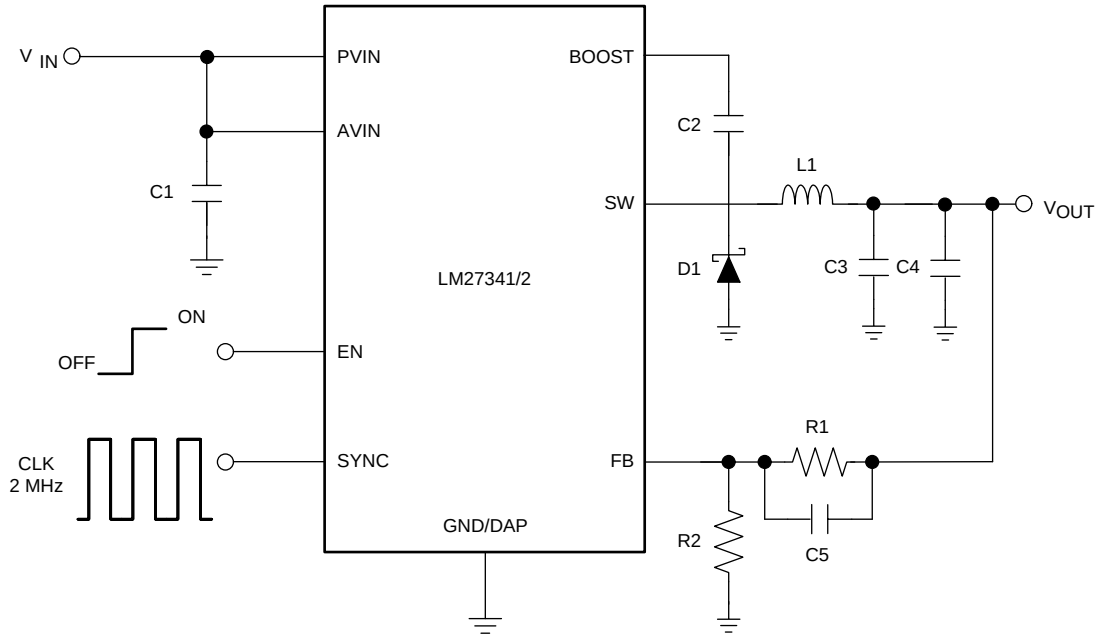
Figure 53. LM27342 Efficiency vs Load Current



I_{OUT} = 100 mA – 2 A at Slewrate = 2 A / µs

Figure 54. Transient Response

8.2.8 LM2734x Configuration From V_{IN} = 3.3 V to 9 V, V_{OUT} = 1.2 V For Full Load at 2 MHz With SYNC = 2 MHz



V_{IN} = 3.3 V to 9 V, V_{OUT} = 1.2 V f_{SW} = 2 MHz I_{OUT} = Full load

Figure 55. LM2734x Configuration From V_{IN} = 3.3 V to 9 V, V_{OUT} = 1.2 V For Full Load at 2 MHz With SYNC = 2-MHz Schematic

8.2.8.1 Design Requirements

Create 1.2-V output at full-rated load for V_{IN} range of 3.3 V to 9 V with switching frequency F_{SW} = 2 MHz using external synchronization.

8.2.8.2 Detailed Design Procedure

The device must be able to operate at any voltage within the recommended operating range. The load current must be defined to properly size the inductor, input, and output capacitors. The inductor must be able to handle the full expected load current as well as the peak current generated during load transients and start-up. The inrush current at start-up depends on the output capacitor selection.

Table 15 lists the bill of materials for V_{IN} = 3.3 V to 9 V, V_{OUT} = 1.2 V for full load at 2 MHz with SYNC = 2 MHz. See Figure 55.

Table 15. Bill of Materials

PART NAME	PART ID	PART VALUE	PART NUMBER	MANUFACTURER
Buck regulator	U1	1.5-A or 2-A Buck regulator	LM2734x and LM2734x-Q1	TI
C_{PVIN}	C1	10 µF	GRM32DR71E106KA12L	Murata
C_{BOOST}	C2	0.1 µF	GRM188R71C104KA01D	Murata
C_{OUT}	C3	47 µF	GRM32ER61A476KE20L	Murata
C_{OUT}	C4	22 µF	C3225X7R1C226K	TDK
C_{FF}	C5	Not mounted		
Catch diode	D1	Schottky diode, Vf = 0.32 V	CMS06	Toshiba
Inductor	L1	0.56 µH	CDRH2D18/HPNP	Sumida
Feedback resistor	R1	1.02 kΩ	CRCW06031K02FKEA	Vishay

Table 15. Bill of Materials (continued)

PART NAME	PART ID	PART VALUE	PART NUMBER	MANUFACTURER
Feedback resistor	R2	5.1 kΩ	CRCW06035K10FKEA	Vishay

8.2.8.3 Application Curves

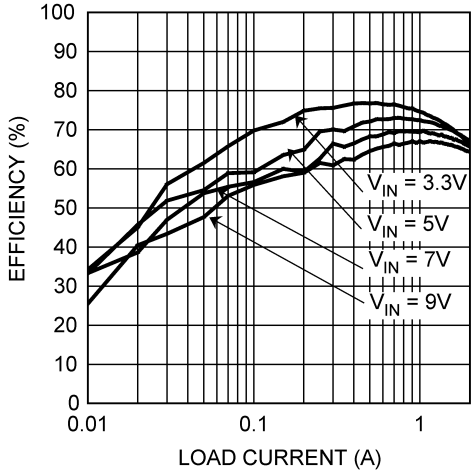
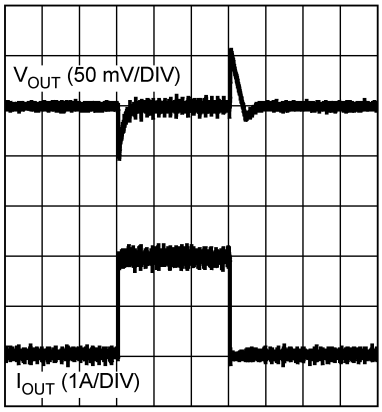


Figure 56. LM27342 Efficiency vs Load Current



100 µs/DIV

I_{OUT} = 100 mA – 2 A at Slewrate = 2 A / µs

Figure 57. Transient Response

9 Power Supply Recommendations

The input voltage is rated as 3 V to 18 V; however, take care in certain circuit configurations (for example, V_{BOOST} derived from V_{IN} where the requirement that $V_{BOOST} - V_{SW} < 5.5$ V must be observed). Also, for the best efficiency, V_{BOOST} must be at least 2.5 V above V_{SW}. The voltage on the enable pin must not exceed V_{IN} by more than 0.3 V.

10 Layout

10.1 Layout Guidelines

10.1.1 Compact Layout

The performance of any switching converter depends as much upon the layout of the PCB as the component selection. The following guidelines help the user design a circuit with maximum rejection of outside EMI and minimum generation of unwanted EMI.

Parasitic inductance can be reduced by keeping the power path components close together and keeping the area of the loops small, on which high currents travel. Short, thick traces or copper pours (shapes) are best. In particular, the switch node (where L1, D1, and the SW pin connect) must be just large enough to connect all three components without excessive heating from the current it carries. The LM2734x and LM2734x-Q1 operate in two distinct cycles (see Figure 27) whose high current paths are shown in Figure 58.

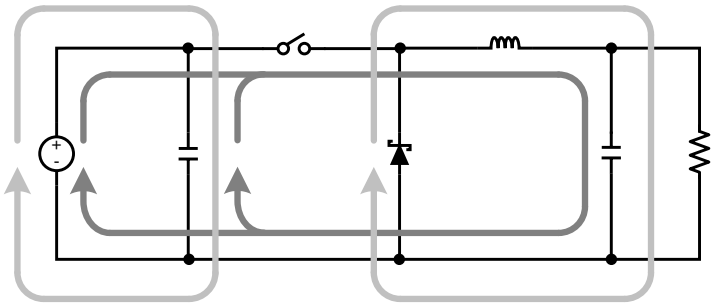


Figure 58. Buck Converter Current Loops

The dark grey, inner loop represents the high current path during the MOSFET on-time. The light grey, outer loop represents the high current path during the off-time.

10.1.2 Ground Plane and Shape Routing

The diagram of Figure 58 is also useful for analyzing the flow of continuous current versus the flow of pulsating currents. The circuit paths with current flow during both the on-time and off-time are considered to be continuous current, while those that carry current during the on-time or off-time only are pulsating currents. Preference in routing must be given to the pulsating current paths, as these are the portions of the circuit most likely to emit EMI. The ground plane of a PCB is a conductor and return path, and it is susceptible to noise injection just like any other circuit path. The path between the input source and the input capacitor and the path between the catch diode and the load are examples of continuous current paths. In contrast, the path between the catch diode and the input capacitor carries a large pulsating current. This path must be routed with a short, thick shape, preferably on the component side of the PCB. Multiple vias in parallel must be used right at the pad of the input capacitor to connect the component side shapes to the ground plane. A second pulsating current loop that is often ignored is the gate drive loop formed by the SW and BOOST pins and boost capacitor C_{BOOST}. To minimize this loop and the EMI it generates, keep C_{BOOST} close to the SW and BOOST pins.

10.1.3 FB Loop

The FB pin is a high-impedance input, and the loop created by R2, the FB pin and ground must be made as small as possible to maximize noise rejection. R2 must therefore be placed as close as possible to the FB and GND pins of the IC.

Layout Guidelines (continued)

10.1.4 PCB Summary

1. Minimize the parasitic inductance by keeping the power path components close together and keeping the area of the high-current loops small.
2. The most important consideration when completing the layout is the close coupling of the GND connections of the C_{IN} capacitor and the catch diode D1. These ground connections must be immediately adjacent, with multiple vias in parallel at the pad of the input capacitor connected to GND. Place C_{IN} and D1 as close to the IC as possible.
3. Next in importance is the location of the GND connection of the C_{OUT} capacitor, which must be near the GND connections of C_{IN} and D1.
4. There must be a continuous ground plane on the copper layer directly beneath the converter. This reduces parasitic inductance and EMI.
5. The FB pin is a high impedance node and care must be taken to make the FB trace short to avoid noise pickup and inaccurate regulation. The feedback resistors must be placed as close as possible to the IC, with the GND of R2 placed as close as possible to the GND of the IC. The V_{OUT} trace to R1 must be routed away from the inductor and any other traces that are switching.
6. High AC currents flow through the V_{IN}, SW and V_{OUT} traces, so they must be as short and wide as possible. However, making the traces wide increases radiated noise, so the layout designer must make this trade-off. Radiated noise can be decreased by choosing a shielded inductor.

The remaining components must also be placed as close as possible to the IC. See *AN-1229 SIMPLE SWITCHER® PCB Layout Guidelines* (SNVA054) for further considerations and the LM27342 demo board as an example of a four-layer layout.

10.2 Layout Example

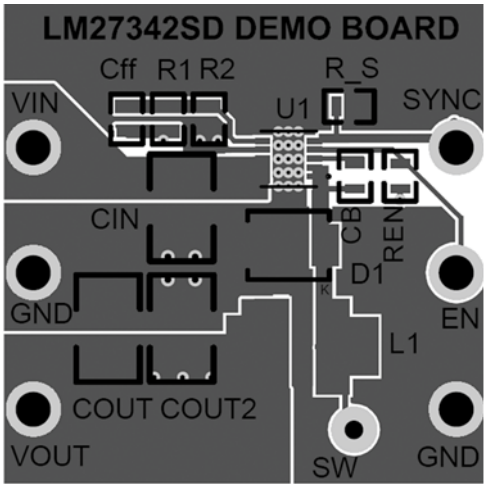


Figure 59. Top Layer and Overlay

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *AN-1197 Selecting Inductors for Buck Converters* (SNVA038)
- *AN-1187 Leadless Leadframe Package* (SNOA401)
- *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Packages* (SNVA183)
- *AN-1229 SIMPLE SWITCHER® PCB Layout Guidelines* (SNVA054)

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 16. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM27341	Click here	Click here	Click here	Click here	Click here
LM27342	Click here	Click here	Click here	Click here	Click here
LM27341-Q1	Click here	Click here	Click here	Click here	Click here
LM27342-Q1	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM27341MY/NOPB	ACTIVE	HVSSOP	DGQ	10	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	SSCB	Samples
LM27341QMY/NOPB	ACTIVE	HVSSOP	DGQ	10	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	SSJB	Samples
LM27341QMYX/NOPB	ACTIVE	HVSSOP	DGQ	10	3500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	SSJB	Samples
LM27341SD/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L231B	Samples
LM27342MY/NOPB	ACTIVE	HVSSOP	DGQ	10	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	SSCA	Samples
LM27342MYX/NOPB	ACTIVE	HVSSOP	DGQ	10	3500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	SSCA	Samples
LM27342QMY/NOPB	ACTIVE	HVSSOP	DGQ	10	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	SSJA	Samples
LM27342QMYX/NOPB	ACTIVE	HVSSOP	DGQ	10	3500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	SSJA	Samples
LM27342SD/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L231A	Samples
LM27342SDX/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L231A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LM27341, LM27341-Q1, LM27342, LM27342-Q1 :

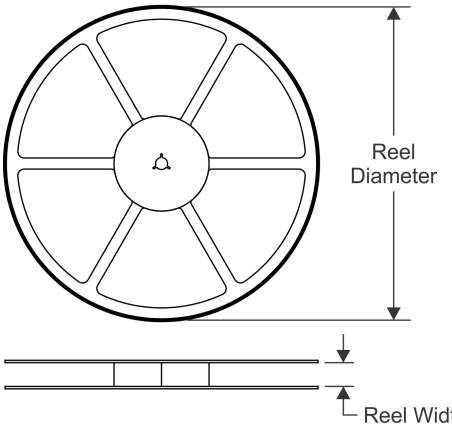
- Catalog: LM27341, LM27342
- Automotive: LM27341-Q1, LM27342-Q1

NOTE: Qualified Version Definitions:

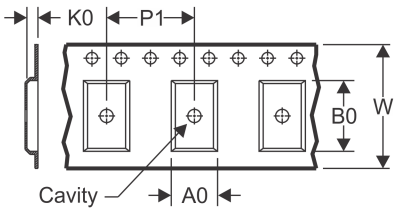
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

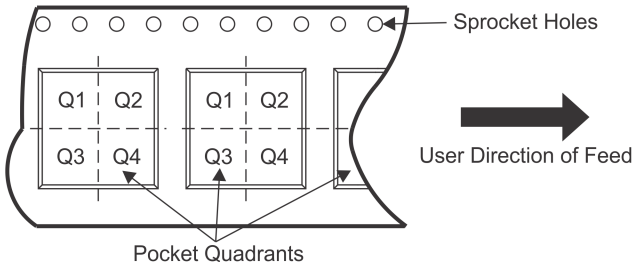


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

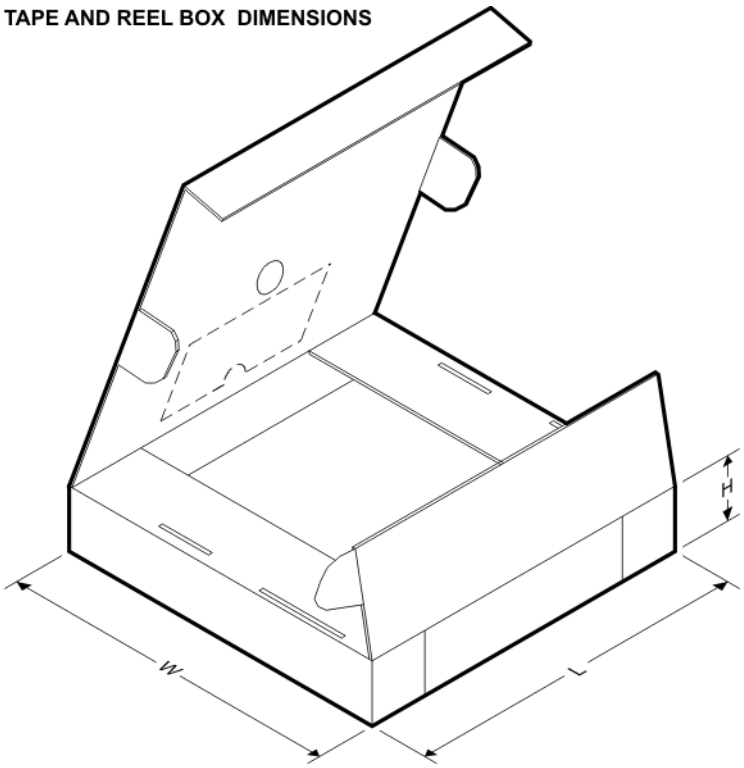
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM27341MY/NOPB	HVSSOP	DGQ	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM27341QMY/NOPB	HVSSOP	DGQ	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM27341QMYX/NOPB	HVSSOP	DGQ	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM27341SD/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM27342MY/NOPB	HVSSOP	DGQ	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM27342MYX/NOPB	HVSSOP	DGQ	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM27342QMY/NOPB	HVSSOP	DGQ	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM27342QMYX/NOPB	HVSSOP	DGQ	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM27342SD/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM27342SDX/NOPB	WSON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

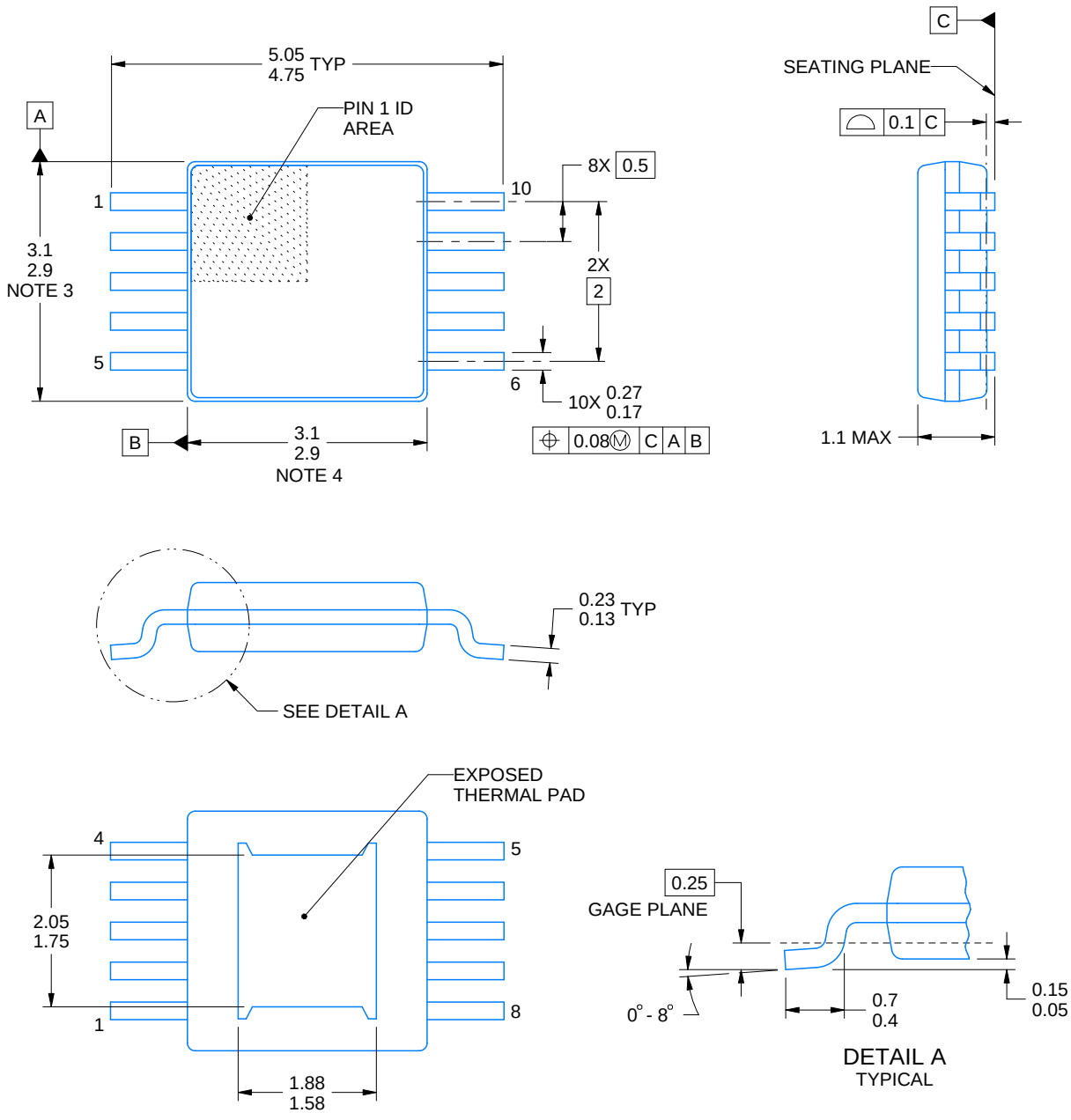
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM27341MY/NOPB	HVSSOP	DGQ	10	1000	210.0	185.0	35.0
LM27341QMY/NOPB	HVSSOP	DGQ	10	1000	210.0	185.0	35.0
LM27341QMYX/NOPB	HVSSOP	DGQ	10	3500	367.0	367.0	35.0
LM27341SD/NOPB	WSON	DSC	10	1000	210.0	185.0	35.0
LM27342MY/NOPB	HVSSOP	DGQ	10	1000	210.0	185.0	35.0
LM27342MYX/NOPB	HVSSOP	DGQ	10	3500	367.0	367.0	35.0
LM27342QMY/NOPB	HVSSOP	DGQ	10	1000	210.0	185.0	35.0
LM27342QMYX/NOPB	HVSSOP	DGQ	10	3500	367.0	367.0	35.0
LM27342SD/NOPB	WSON	DSC	10	1000	210.0	185.0	35.0
LM27342SDX/NOPB	WSON	DSC	10	4500	367.0	367.0	35.0

PACKAGE OUTLINE

DGQ0010A

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE

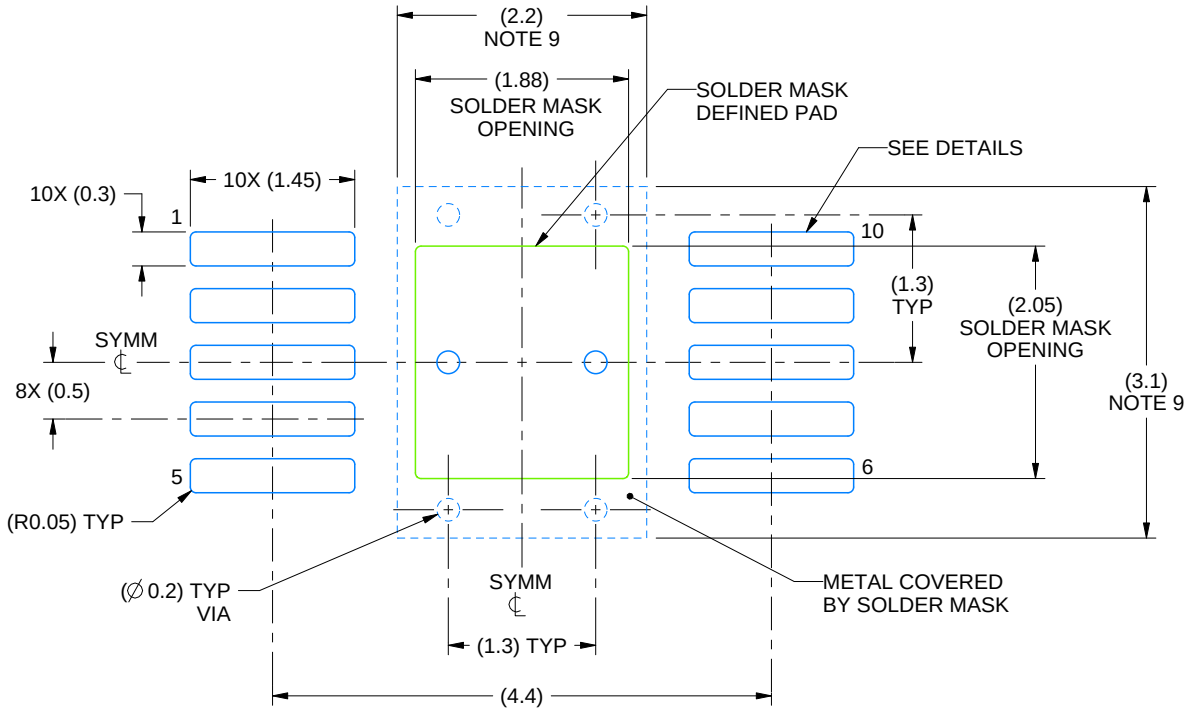


4214864/A 05/2020

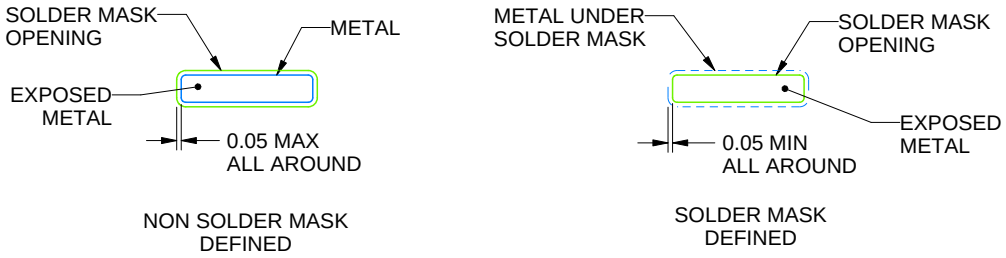
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

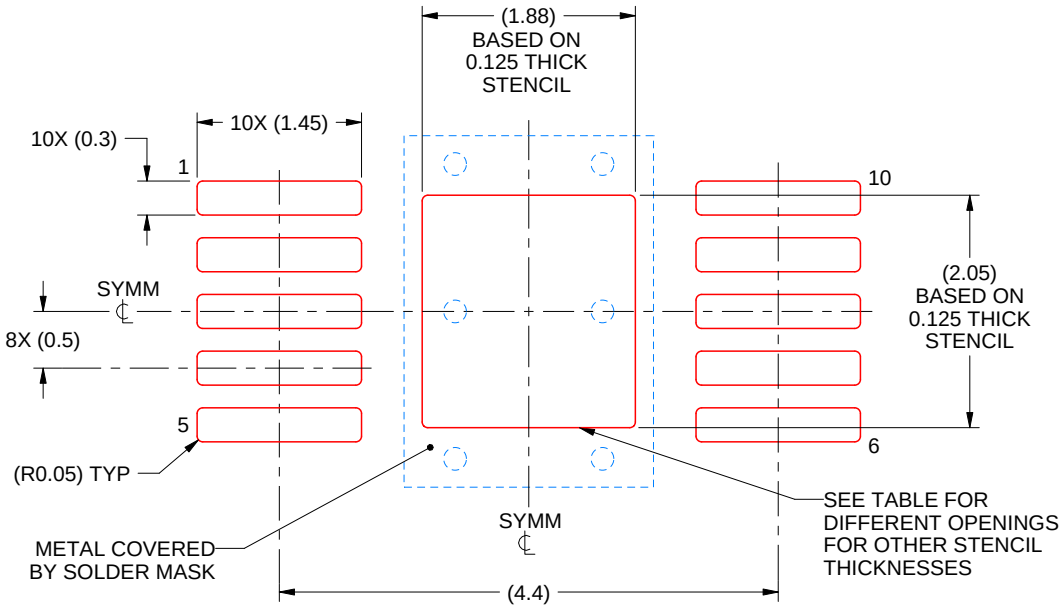


SOLDER MASK DETAILS

4214864/A 05/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.10 X 2.29
0.125	1.88 X 2.05 (SHOWN)
0.150	1.72 X 1.87
0.175	1.59 X 1.73

4214864/A 05/2020

NOTES: (continued)

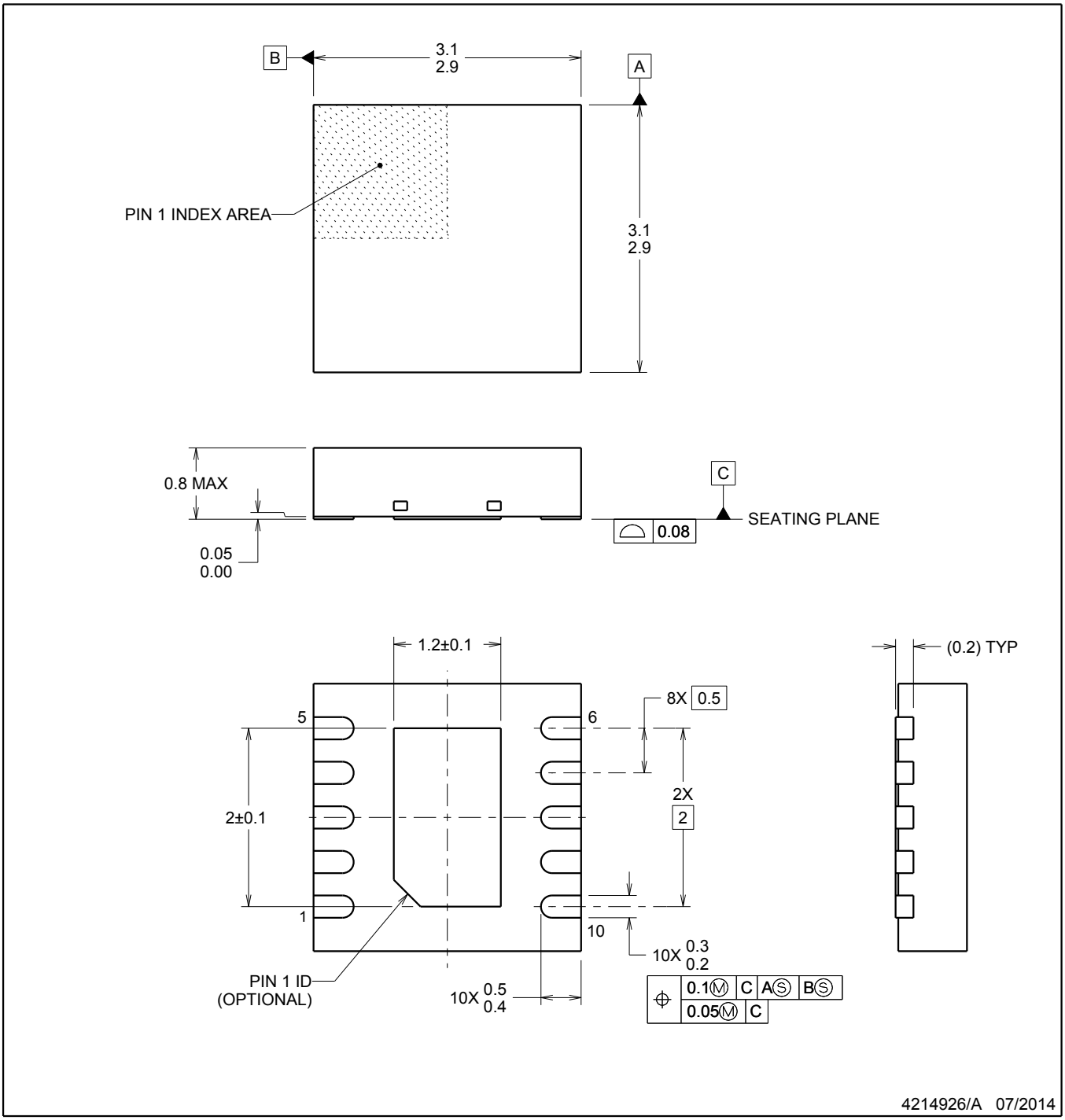
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DSC0010B

WSON - 0.8 mm max height

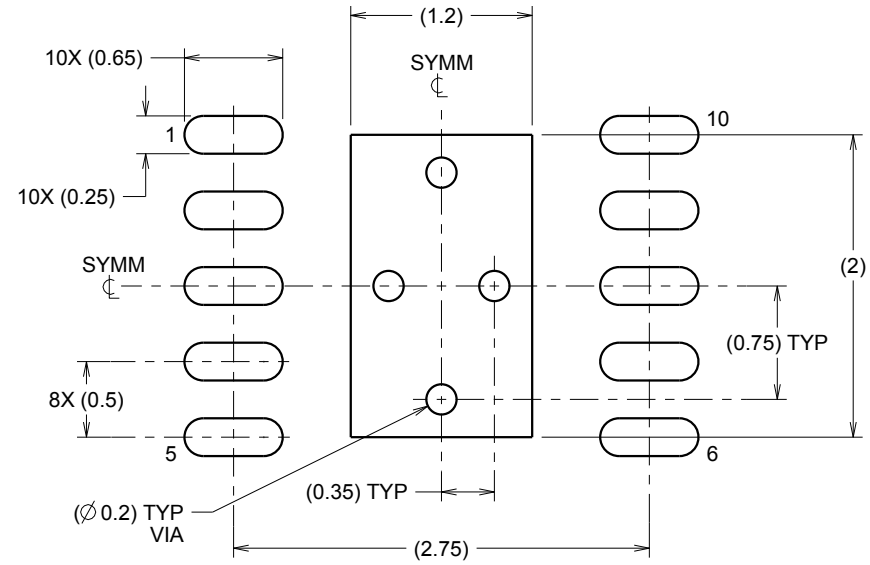
PLASTIC SMALL OUTLINE - NO LEAD



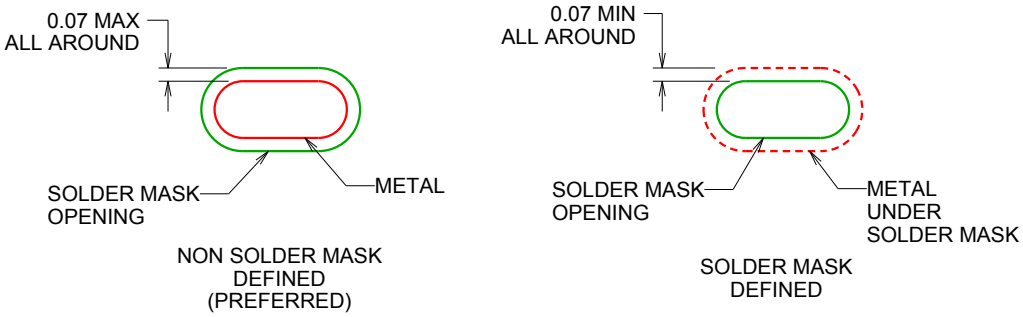
4214926/A 07/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4214926/A 07/2014

NOTES: (continued)

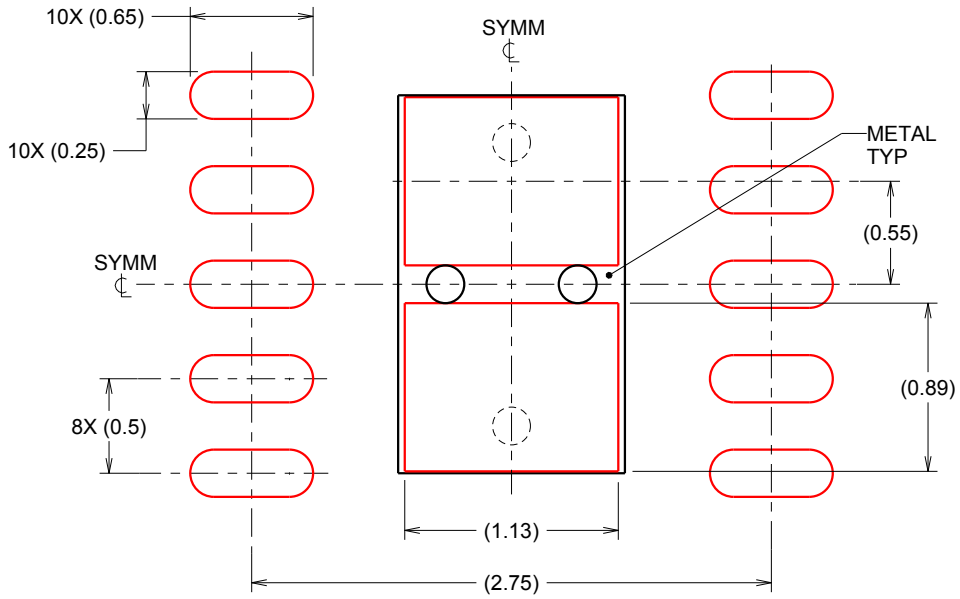
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSC0010B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4214926/A 07/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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