

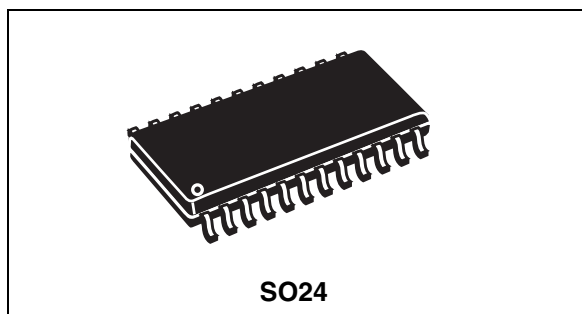
### Features

- Drives both windings of a bipolar stepper motor
- Output current up to 750 mA for each winding
- Wide voltage range: 10 V to 46 V
- Half-step, full-step and microstepping mode
- Built-in protection diodes
- Internal PWM current control
- Low output saturation voltage
- Designed for unstabilized motor supply voltage
- Internal thermal shutdown

### Description

The L6219DSA is a bipolar monolithic integrated circuit intended to control and drive both windings of a bipolar stepper motor or bidirectionally control two DC motors.

With only a few external components, the L6219DSA controls and drives the circuit for LS-TTL or microprocessor-controlled stepper motor systems. The power stage is a dual full bridge sustaining 46 V and including four diodes for current recirculation.



Cross conduction protection is provided to avoid simultaneous cross conduction during switching current direction.

An internal pulse-width modulation (PWM) controls the output current to 750 mA with peak startup current up to 1 A.

A wide range of current control from 750 mA (each bridge) is permitted by two logic inputs and an external voltage reference. A phase input to each bridge determines the load current direction. Thermal protection circuitry disables the outputs if the chip temperature exceeds safe operating limits.

**Table 1. Device summary**

| Order code   | Package | Packing       |
|--------------|---------|---------------|
| E-L6219DSA   | SO24    | Tube          |
| E-L6219DSATR | SO24    | Tape and reel |

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# 1 Block diagram

Figure 1. Block diagram

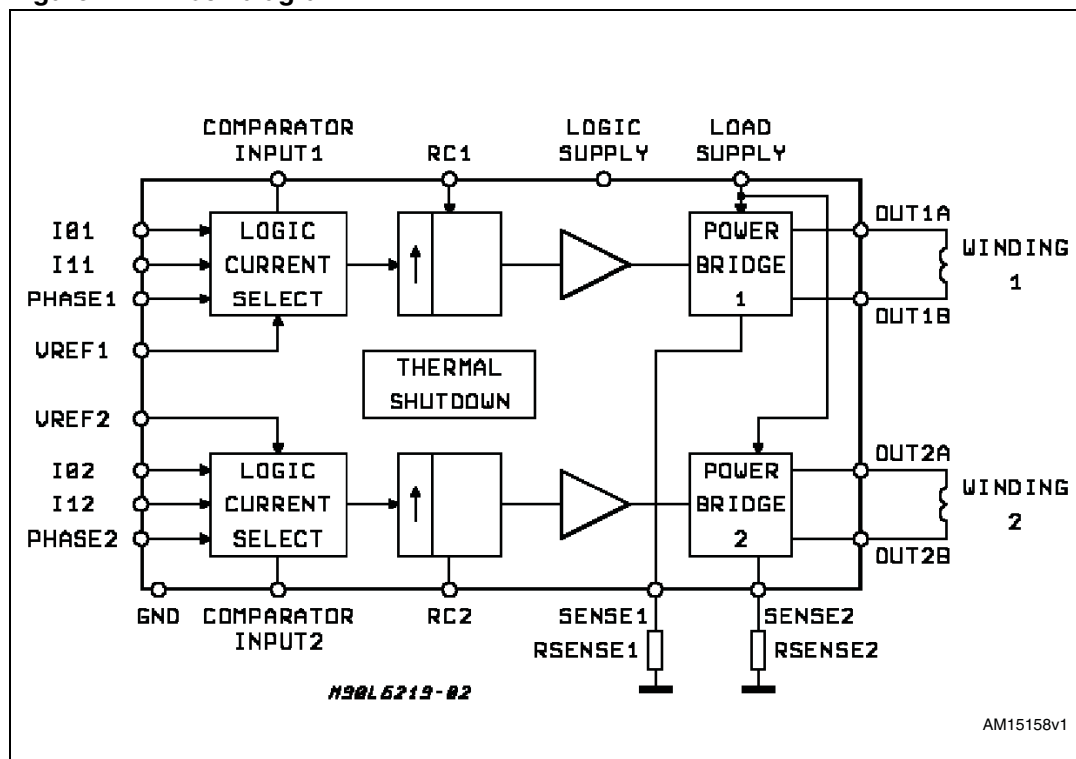


Table 2. Absolute maximum ratings

| Parameter   | Description                 | Value       | Unit |
|-------------|-----------------------------|-------------|------|
| $V_s$       | Supply voltage              | 50          | V    |
| $I_O$       | Output current (peak)       | $\pm 1$     | A    |
| $I_O$       | Output current (continuous) | $\pm 0.75$  | A    |
| $V_{ss}$    | Logic supply voltage        | 7           | V    |
| $V_{in}$    | Logic input voltage range   | -0.3 to +7  | V    |
| $V_{sense}$ | Sense output voltage        | 1.5         | V    |
| $T_j$       | Junction temperature        | +150        | °C   |
| $T_{op}$    | Operating temperature range | -40 to +125 | °C   |
| $T_{stg}$   | Storage temperature range   | -55 to +150 | °C   |

Figure 2. SO24 pin connection (top view)

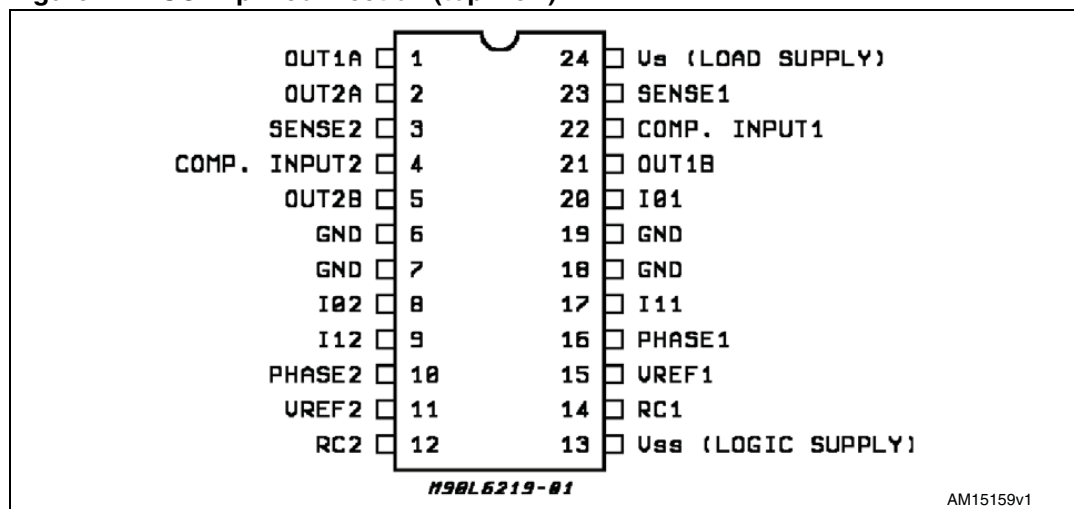


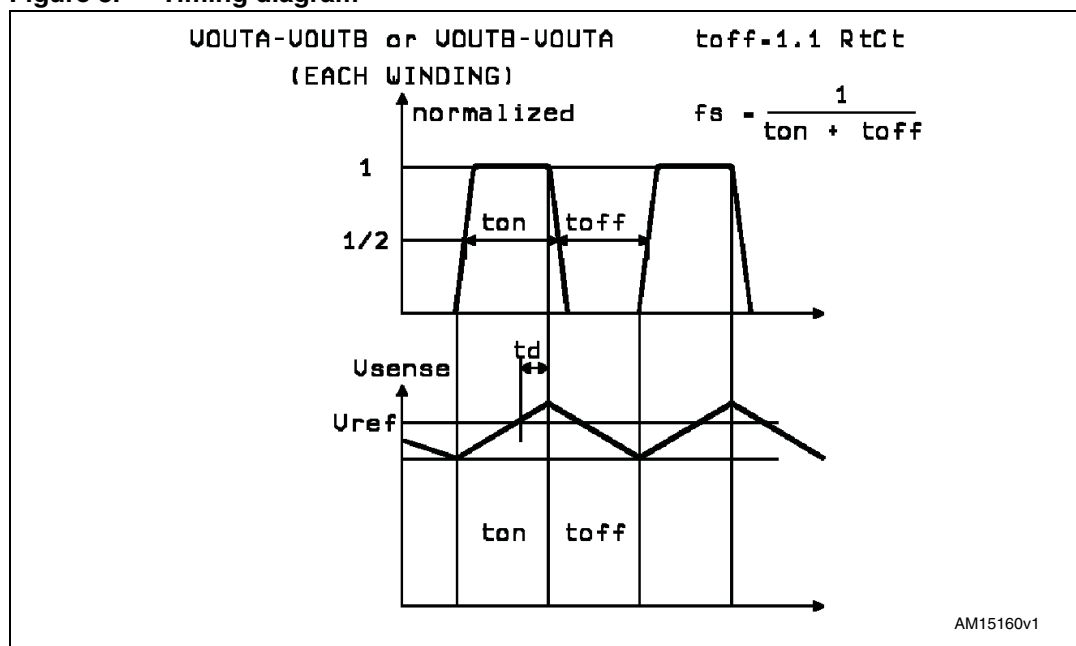
Table 3. Pin functions

| Pin #        | Name               | Description                                                                                                                                                                                                                                                                                                                                                                                   |
|--------------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 21        | Output of bridge 1 | See pins 2, 5                                                                                                                                                                                                                                                                                                                                                                                 |
| 3, 23        | Sense resistor     | Connection to lower emitters of output stage for insertion of current sense resistor                                                                                                                                                                                                                                                                                                          |
| 4, 22        | Comparator input   | Input connected to the comparators. The voltage across the sense resistor is feedback to this input through the low pass filter RC CC. The higher power transistors are disabled when the sense voltage exceeds the reference voltage of the selected comparator. When this occurs the current decays for a time set by $R_T C_T$ ( $t_{off} = 1.1 R_T C_T$ ). See <a href="#">Figure 3</a> . |
| 2, 5         | Output of bridge 2 | Output connection. The output stage is a H bridge formed by four transistors and four diodes suitable for switching applications.                                                                                                                                                                                                                                                             |
| 6, 7, 18, 19 | Ground             | Ground connection. They also conduct heat from die to printed circuit copper                                                                                                                                                                                                                                                                                                                  |
| 8, 20        | Input 0            | See input 1 (pins 9, 17)                                                                                                                                                                                                                                                                                                                                                                      |
| 9, 17        | Input 1            | These pins and pins 8, 20 (input 0) are logic inputs which select the outputs of the comparators to set the current level. Current also depends on the sensing resistor and reference voltage. See <a href="#">Section 2: Functional description</a> .                                                                                                                                        |
| 10, 16       | Phase              | These TTL-compatible logic inputs set the direction of current flow through the load. A high level causes current to flow from output A (source) to output B (sink). A Schmitt trigger on this input provides a good noise immunity and a delay circuit prevents output stage short-circuits during switching.                                                                                |
| 11, 15       | Reference voltage  | A voltage applied to this pin sets the reference voltage of the comparators, this determining the output current (also thus depending on Rs and the two inputs input 0 and input 1)                                                                                                                                                                                                           |

**Table 3. Pin functions (continued)**

| Pin #  | Name                           | Description                                                                                                                                                                                               |
|--------|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12, 14 | RC                             | A parallel RC network connected to this pin sets the off time of the higher power transistors. The pulse generator is a monostable triggered by the output of the comparators ( $t_{off} = 1.1 R_T C_T$ ) |
| 13     | V <sub>SS</sub> - Logic supply | Supply voltage input for logic circuitry                                                                                                                                                                  |
| 24     | V <sub>S</sub> - Load supply   | Supply voltage input for the output stages                                                                                                                                                                |

*Note:* ESD on GND, VS, VSS, OUT 1 A and OUT 2 A is guaranteed up to 1.5 kV (human body model, 1500 W, 100 pF).

**Figure 3. Timing diagram****Table 4. Thermal data**

| Parameter      | Description                              | PDIP              | Unit |
|----------------|------------------------------------------|-------------------|------|
| $R_{thj-case}$ | Thermal resistance junction-case max.    | 18                | °C/W |
| $R_{thj-amb}$  | Thermal resistance junction-ambient max. | 75 <sup>(1)</sup> | °C/W |

1. With minimized copper area.

**Table 5. Electrical characteristics**

( $T_j = -40\text{ }^{\circ}\text{C}$  to  $-125\text{ }^{\circ}\text{C}$ ,  $V_S = 46\text{ V}$ ,  $V_{SS} = 4.75\text{ V}$  to  $5.25\text{ V}$ ,  $V_{REF} = 5\text{ V}$ , unless otherwise specified)  
See [Figure 5](#).

| Parameter                                                  | Description                             | Test condition                                                                            | Min. | Typ. | Max. | Unit                           |
|------------------------------------------------------------|-----------------------------------------|-------------------------------------------------------------------------------------------|------|------|------|--------------------------------|
| <b>Output drivers (OUT<sub>A</sub> or OUT<sub>B</sub>)</b> |                                         |                                                                                           |      |      |      |                                |
| $V_S$                                                      | Motor supply range                      |                                                                                           | 10   | -    | 46   | V                              |
| $I_{CEX}$                                                  | Output leakage current                  | $V_S = 52\text{ V}$ $V_{OUT} = 50\text{ V}$<br>$V_S = 52\text{ V}$ $V_{OUT} = 1\text{ V}$ | -200 | -    | 200  | $\mu\text{A}$<br>$\mu\text{A}$ |
| $V_{CE(sat)}$                                              | Output saturation voltage               | Sink driver, $I_{OUT} = +500\text{ mA}$                                                   | -    | -    | 0.75 | V                              |
|                                                            |                                         | Sink driver, $I_{OUT} = +750\text{ mA}$                                                   | -    | -    | 1.15 | V                              |
|                                                            |                                         | Source driver, $I_{OUT} = -500\text{ mA}$                                                 | -    | -    | 1.6  | V                              |
|                                                            |                                         | Source driver, $I_{OUT} = -750\text{ mA}$                                                 | -    | -    | 1.8  | V                              |
| $V_F$                                                      | Clamp diode forward voltage             | High stage $I_F = 750\text{ mA}$                                                          | -    | -    | 1.7  | V                              |
|                                                            |                                         | Low stage $I_F = 750\text{ mA}$                                                           | -    | -    | 1.6  | V                              |
| $I_{S(on)}$                                                | Driver supply current                   | Both bridges ON, no load                                                                  | -    | -    | 17   | mA                             |
| $I_{S(off)}$                                               | Driver supply current                   | Both bridges OFF                                                                          | -    | -    | 12   | mA                             |
| <b>Control logic</b>                                       |                                         |                                                                                           |      |      |      |                                |
| $V_{IN(H)}$                                                | Input voltage                           | All inputs                                                                                | 2.4  | -    | -    | V                              |
| $V_{IN(L)}$                                                | Input voltage                           | All inputs                                                                                | -    | -    | 0.8  | V                              |
| $I_{IN(H)}$                                                | Input current                           | $V_{IN} = 2.4\text{ V}$                                                                   | -    | <1   | 20   | $\mu\text{A}$                  |
| $I_{IN(L)}$                                                | Input current                           | $V_{IN} = 0.84\text{ V}$                                                                  | -    | -3   | -200 | $\mu\text{A}$                  |
| $V_{REF}$                                                  | Reference voltage                       | Operating <sup>(1)</sup>                                                                  | 1.5  | -    | 7.5  | V                              |
| $I_{SS(ON)}$                                               | Total logic supply current              | $I_0 = I_1 = 0.8\text{ V}$ , no load                                                      | -    | -    | 76   | mA                             |
| $I_{SS(OFF)}$                                              | Total logic supply current              | $I_0 = I_1 = 2.4\text{ V}$ , no load                                                      | -    | -    | 15   | mA                             |
| <b>Comparators</b>                                         |                                         |                                                                                           |      |      |      |                                |
| $V_{REF}/V_{sense}$                                        | Current limit threshold (at trip point) | $I_0 = I_1 = 0.8\text{ V}$                                                                | 9.5  | 10   | 10.5 | -                              |
|                                                            |                                         | $I_0 = 2.4\text{ V}$ , $I_1 = 0.8\text{ V}$                                               | 13.5 | 15   | 16.5 | -                              |
|                                                            |                                         | $I_0 = 0.8\text{ V}$ , $I_1 = 2.4\text{ V}$                                               | 25.5 | 30   | 34.5 | -                              |
| $t_{off}$                                                  | Cut off time                            | $R_t = 56\text{ K}\Omega$ , $C_t = 820\text{ pF}$                                         | -    | 50   | -    | $\mu\text{s}$                  |
| $t_d$                                                      | Turn off delay                          | <a href="#">Figure 3</a>                                                                  | -    | 1    | -    | $\mu\text{s}$                  |
| <b>Protection</b>                                          |                                         |                                                                                           |      |      |      |                                |
| $T_J$                                                      | Thermal shutdown temperature            |                                                                                           | -    | 170  | -    | $^{\circ}\text{C}$             |

1. To reduce the switching losses the base bias of the bridge's low side NPN transistor is proportional to the DAC output, then the output current driving capability is also proportional to the DAC output voltage, having as reference 750 mA with  $V_{REF} = 5\text{ V}$  and DAC = 100%. For example using  $V_{REF} = 2\text{ V}$  and DAC = 67% the output maximum current driving capability will become  $750\text{ mA} \cdot (2\text{ V} \cdot 0.67) / (5\text{ V} \cdot 1) = 200\text{ mA}$ .

## 2 Functional description

The circuit is intended to drive both windings of a bipolar stepper motor.

The peak current control is generated through switch mode regulation. There is a choice of three different current levels with the two logic inputs  $I_{01}$  -  $I_{11}$  for winding 1 and  $I_{02}$  -  $I_{12}$  for winding 2.

The current can also be switched off completely.

### 2.1 Input logic ( $I_0$ and $I_1$ )

The current level in the motor winding is selected by these inputs. (See [Figure 4](#)). If any of the logic inputs is left open, the circuit treats it as a high level input.

**Table 6. Current levels**

| $I_0$ | $I_1$ | Current level                |
|-------|-------|------------------------------|
| H     | H     | No current                   |
| L     | H     | Low current $1/3 I_0$ max    |
| H     | L     | Medium current $2/3 I_0$ max |
| L     | L     | Maximum current $I_0$ max    |

### 2.2 Phase

This input determines the direction of current flow in the windings, depending on the motor connections. The signal is fed through a Schmidt trigger for noise immunity, and through a time delay in order to guarantee that no short-circuit occurs in the output stage during phase-shift. A high level on the Phase input causes the motor current flow from out A through the winding to out B.

### 2.3 Current sensor

This part contains a current sensing resistor ( $R_S$ ), a low pass filter ( $R_C$ ,  $C_C$ ) and three comparators. Only one comparator is active at a time. It is activated by the input logic according to the current level chosen with signals  $I_0$  and  $I_1$ . The motor current flows through the sensing resistor  $R_S$ . When the current has increased so that the voltage across  $R_S$  becomes higher than the reference voltage on the other comparator input, the comparator goes high, triggering the pulse generator.

The max peak current  $I_{max}$  can be defined by:

**Equation 1**

$$I_{max} = \frac{V_{ref}}{10R_S}$$

## 2.4 Single-pulse generator

The pulse generator is a monostable triggered on the positive going edge of the comparator output. The monostable output is high during the pulse time,  $t_{off}$ , which is determined by the time components  $R_t$  and  $C_t$ .

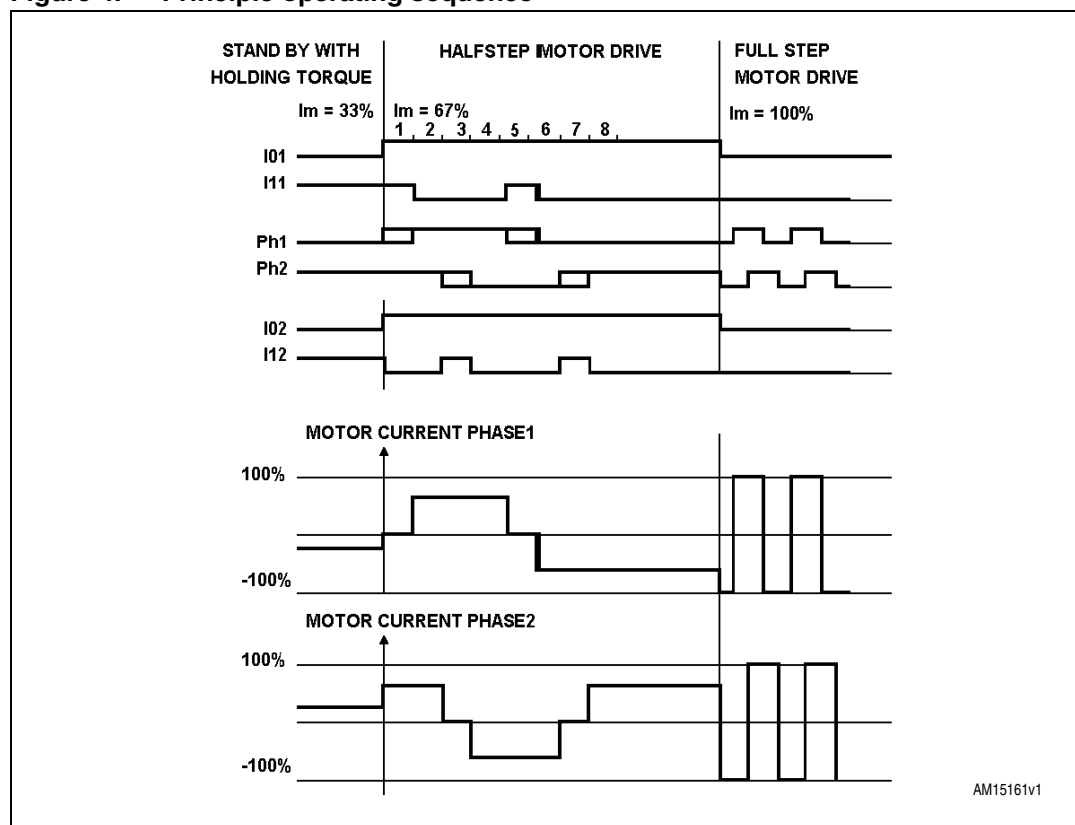
$$t_{off} = 1.1 \cdot R_t C_t$$

The single pulse switches off the power feed to the motor winding, causing the winding current to decrease during  $t_{off}$ . If a new trigger signal should occur during  $t_{off}$ , it is ignored.

## 2.5 Output stage

The output stage contains four Darlington transistors (source drivers) four saturated transistors (sink drivers) and eight diodes, connected in two H bridge.

**Figure 4. Principle operating sequence**



The source transistors are used to switch the power supplied to the motor winding, thus driving a constant current through the winding. It should be noted however, that is not permitted to short-circuit the outputs.

Internal circuitry is added in order to increase the accuracy of the motor current particularly with low current levels.

## 2.6 $V_S$ , $V_{SS}$ , $V_{Ref}$

The circuit withstands any order of turn-on or turn-off of the supply voltages  $V_S$  and  $V_{SS}$ . Normal  $dV/dt$  values are then assumed.

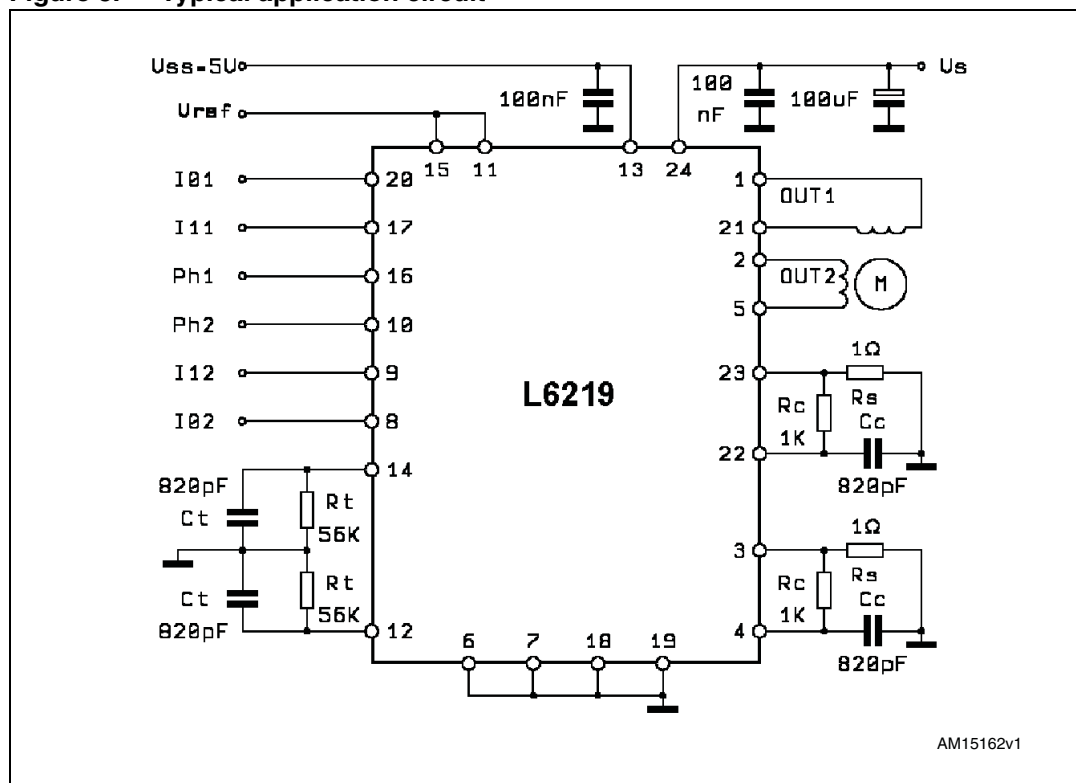
Preferably,  $V_{Ref}$  should be tracking  $V_{SS}$  during power-on and power-off if  $V_S$  is established.

### 3 Application information

Some stepper motors are not designed for continuous operation at maximum current. As the circuit drives a constant current through the motor, its temperature might increase exceedingly both at low and high speed operation. Also, some stepper motors have such high core losses that they are not suited for switch mode current regulation.

Unused inputs should be connected to proper voltage levels in order to get the highest noise immunity. As the circuit operates with switch mode current regulation, interference generation problems might arise in some applications. A good measure might then be to decouple the circuit with a 100 nF capacitor, located near the package between power line and ground. The ground lead between  $R_s$ , and circuit GND should be kept as short as possible. A typical application circuit is shown in [Figure 5](#). Note that  $C_t$  must be NPO type or similar else. To sense the winding current, paralleled metal film resistors are recommended ( $R_s$ ).

**Figure 5. Typical application circuit**



## 4 Package mechanical data

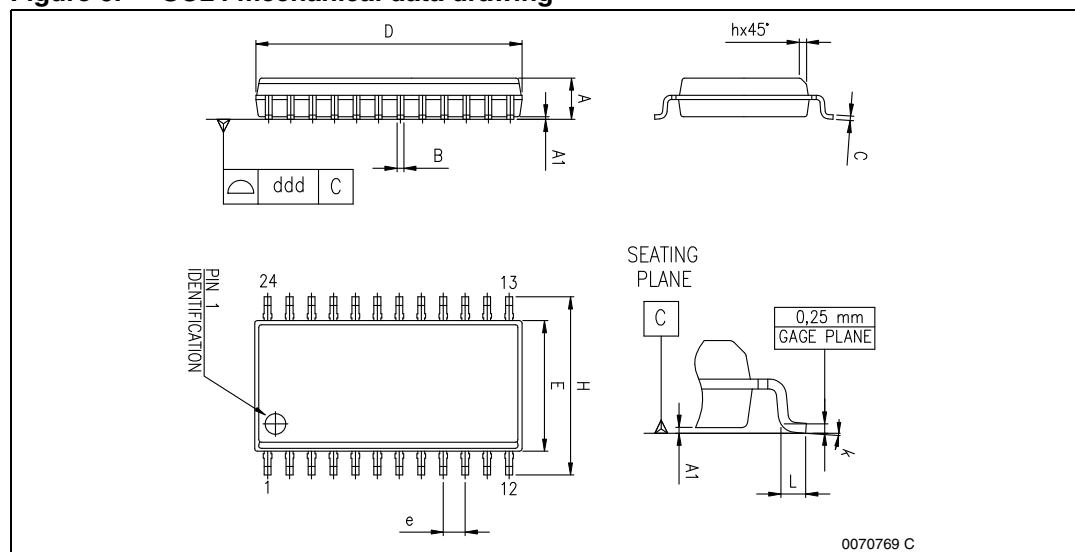
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**Table 7. SO24 mechanical data dimensions**

| Dim. | mm    |      |       |
|------|-------|------|-------|
|      | Min.  | Typ. | Max.  |
| A    | 2.35  |      | 2.65  |
| A1   | 0.10  |      | 0.30  |
| B    | 0.33  |      | 0.51  |
| C    | 0.23  |      | 0.32  |
| D    | 15.20 |      | 15.60 |
| E    | 7.40  |      | 7.60  |
| e    |       | 1.27 |       |
| H    | 10.00 |      | 10.65 |
| h    | 0.25  |      | 0.75  |
| L    | 0.40  |      | 1.27  |
| k    | 0     |      | 8     |
| ddd  |       |      | 0.10  |

**Note:** Dimension "D" does not include mold flash, protrusions or gate burrs.  
Mold flash, protrusions or gate burrs do not exceed 0.15 mm per side.

**Figure 6. SO24 mechanical data drawing**



## 5 Revision history

**Table 8. Document revision history**

| Date        | Revision | Changes                                                                                                                            |
|-------------|----------|------------------------------------------------------------------------------------------------------------------------------------|
| 12-Nov-1998 | 1        | Initial release.                                                                                                                   |
| 29-Apr-2008 | 2        | Document reformatted                                                                                                               |
| 05-Sep-2008 | 3        | Added note <a href="#">1.</a> to <a href="#">Table 5.</a>                                                                          |
| 24-Oct-2012 | 4        | Changed the title of the document.<br>Reformatted document to current standards.<br>Minor text changes to improve the readability. |

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