TWO-PHASE, SYNCHRONOUS BUCK CONTROLLER WITH INTEGRATED MOSFET DRIVERS

FEATURES

- **Two-Phase Interleaved Operation**
- **3-V to 40-V Power Stage Operation Range**
- **Supports Up to 6-V V_{OUT} With External Divider**
- **Requires VIN5 @ 50 mA, Typical, Depending on External MOSFETs and Switching Frequency**
- **1-µA Shutdown Current**
- **Programmable Switching Frequency up to 1 MHz/Phase**
- **Current Mode Control with Forced Current Sharing**
- **Better than 1% Internal 0.7-V Reference**
- **Resistive Divider Sets Direct Output Over Voltage Threshold and Sets Input Undervoltage Lockout**
- **True Remote Sensing Differential Amplifier**
- **Resistive or Inductor's DCR Current Sensing**
- **30-pin TSSOP or 32-Pin QFN Packages**
- **Can Be Used with TPS40120 to Provide a 6-Bit Digitally Controlled Output**

APPLICATIONS

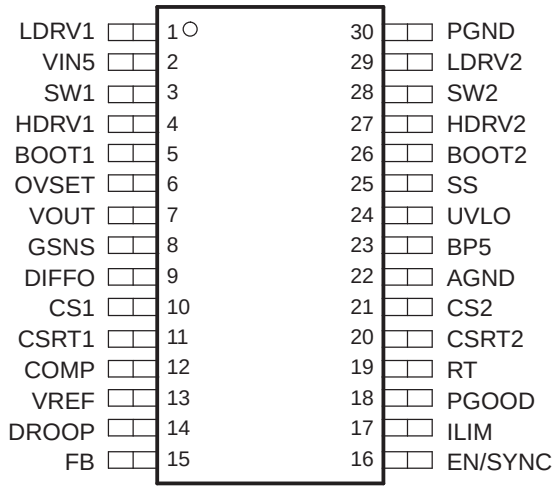
- **Graphic Cards**
- **Internet Servers**
- **Networking Equipment**
- **Telecommunications Equipment**
- **DC Power Distributed Systems**

DESCRIPTION

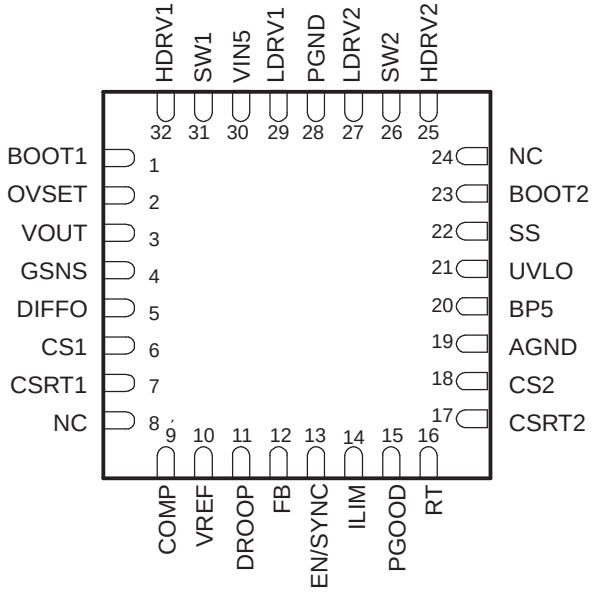
The TPS40130 is a two-phase synchronous buck controller that is optimized for low-output voltage, high-output current applications powered from a supply between 3 V and 40 V. A multi-phase converter offers several advantages over a single power stage including lower current ripple on the input and output capacitors, faster transient response to load steps, improved power handling capabilities, and higher system efficiency.

Each phase can be operated at a switching frequency up to 1 MHz, resulting in an effective ripple frequency of up to 2 MHz at the input and the output. The two phases operates 180 degrees out-of-phase.

DBT PACKAGE
(TOP VIEW)



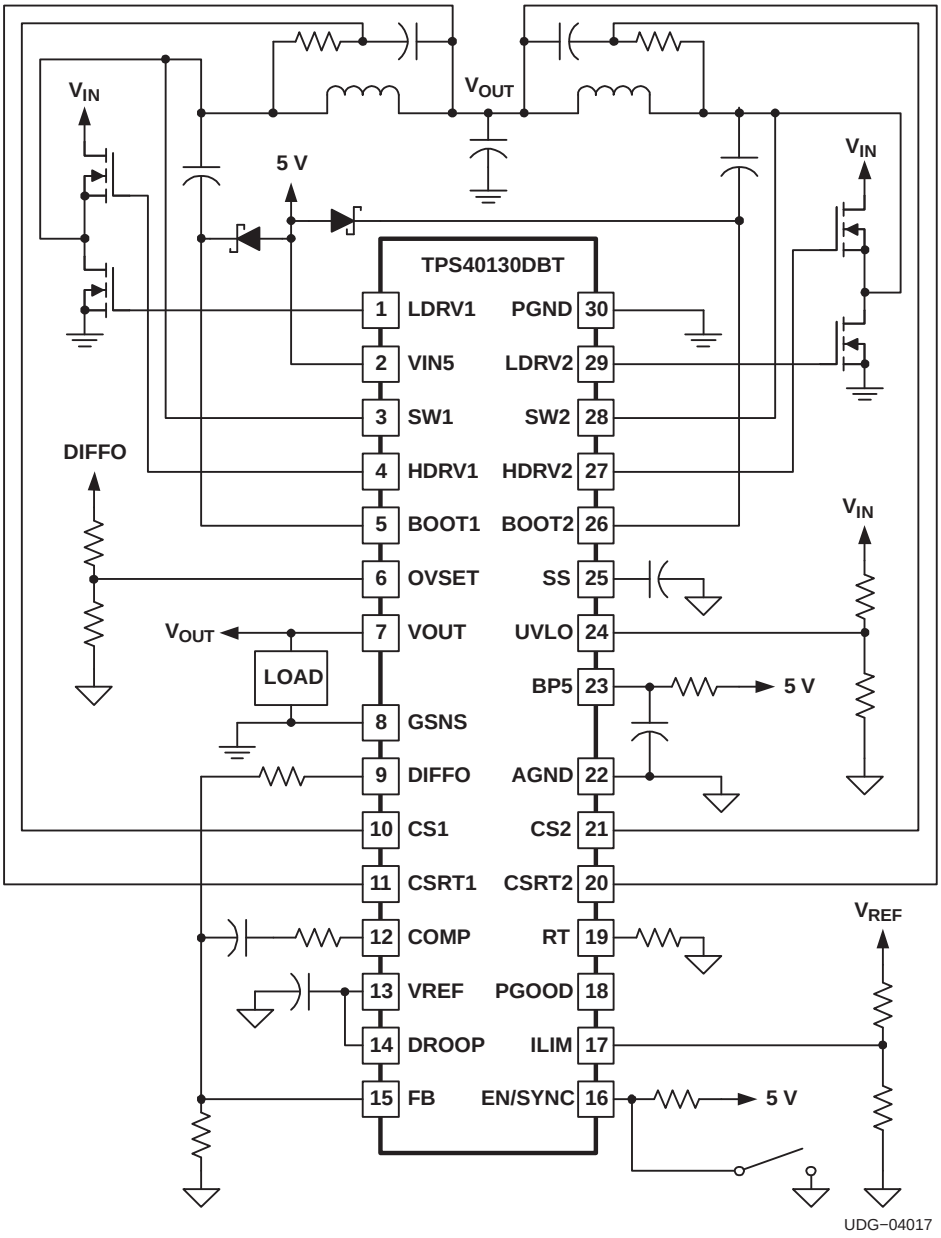
RHB PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SIMPLIFIED APPLICATION DIAGRAM



ORDERING INFORMATION

T_A	PACKAGE	PART NUMBER
-40°C to 85°C	Plastic TSSOP(DBT)(1)	TPS40130DBT(2)(3)
	Plastic QFN (RHB)	TPS40130RHB

(1) The DBTpackage is also available taped and reeled. Add an R suffix to the device type (i.e., TPS40130DBTR).
(2) The TPS40130DBTRG4 is a lead (Pb) free product, which means that it is compatible with current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous material. In addition, this part has NiPdAu plated copper lead frame and is rated at MSL level 2 at 260°C according to JEDEC 020C Standards.
(3) Release date for the TPS40130DBTRG4 TBD.

ABSOLUTE MAXIMUM RATING

over operating free-air temperature range unless otherwise noted(1)

			TPS40130	UNITS
	Input voltage range	SW1, SW2	-1 to 44	V
		BOOT1, BOOT2	-0.3 to V_{SW} + 6.0	
		All other pins	-0.3 to 6.0	
	Sourcing current	RT	200	µA
T_J	Operating junction temperature range		-40 to 125	°C
T_{stg}	Storage temperature		-55 to 150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	3.0		40	V
T_A	Operating free-air temperature	-40		85	°C

ELECTRICAL CHARACTERISTICS

T_A = -40°C to 85°C, V_{IN} = 12 V, R_{RT} = 64.9 kΩ, T_J = T_A (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN5 INPUT SUPPLY						
V_{IN}	Operating voltage range, VIN5		4.5	5.0	5.5	V
I_{IN}	Shutdown current, VIN5	EN/SYNC = GND		1	5	µA
	Operating current	Outputs switching, No load	0.5	1.0	1.5	mA
BP5 INPUT SUPPLY						
	Operating voltage range		4.3	5.0	5.5	V
I_{BP5}	Operating current	V_{FB} < V_{REF}, Outputs switching, no external FETs	2	3	5	mA
	Turn-on BP5 rising		4.00	4.25	4.45	V
	Turn-off hysteresis(1)			150		mV
OSCILLATOR/SYNCHRONIZATION						
	Phase frequency accuracy	R_T = 64.9 kΩ	360	415	455	kHz
	Phase frequency set range(1)		100		1200	
	Synchronization frequency range(1)		800		9600	
	Synchronization input threshold(1)			V_{BP5}/2		V
EN/SYNC						
	Enable threshold	Pulse width > 50 ns	0.8	1.0	1.5	V
	Voltage capability(1)			V_{BP5}		
PWM						
	Maximum duty cycle per channel(1)			87.5%		
	Minimum duty cycle per channel(1)			0		
VREF						
	Voltage reference	I_{LOAD} = 100 µA	0.687	0.700	0.709	V
ERROR AMPLIFIER						
V_{FB}	Voltage feedback, trimmed (including differential amplifier)		0.691	0.700	0.705	V
CMRR	Input common mode range(1)		0.0	0.7	2.0	
	Input bias current	V_{FB} = 0.7 V		55	150	nA
	Input offset voltage	Value trimmed to zero		0		V
I_{SRC}	Output source current(1)	V_{COMP} = 1.1 V, V_{FB} = 0.6 V	1	2		mA
I_{SINK}	Output sink current(1)	V_{COMP} = 1.1 V, V_{FB} =V_{BP5}	1	2		
V_{OH}	High-level output voltage	I_{COMP} = -1 mA	2.5	2.9		V
V_{OL}	low-level output voltage	I_{COMP} = 1 mA		0.5	0.8	
G_{BW}	Gain bandwidth(1)		3	5		MHz
A_{VOL}	Open loop gain(1)		60	90		dB

(1) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

T_A = -40°C to 85°C, V_{IN} = 12 V, R_{RT} = 64.9 kΩ, T_J = T_A (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT START						
I_{SS}	Soft-start source current	32 clocks after EN/SYNC before SS current begins	3.5	5.0	6.5	µA
V_{SS}	Fault enable threshold voltage		0.95	1.00	1.05	V
CURRENT SENSE AMPLIFIER						
	Input offset voltage	CS1, CS2	-5	4	10	mV
	Gain transfer to PWM comparator	-100 mV ≤ V_{CS}≤ 100 mV, V_{CSRT} = 1.5 V	5.1	5.6	6.1	V/V
	Transconductance to DROOP	V_{CS} - V_{CSRTn} = 100 mV		40		µA
	Gain variance between phases	V_{CS} - V_{CSRTn} = 100 mV	-4%	0	4%	
	Input offset variance	V_{CS} = 0 V	-3.5	0	3.5	mV
	Offset current at DROOP	V_{CS} - V_{CSRTn} = 0 V			6	µA
	Input common mode (2)		0		V_{BP5}-0.7	V
	Bandwidth(2)		18			MHz
DIFFERENTIAL AMPLIFIER						
	Gain			1		V/V
	Gain tolerance	V_{OUT} = 4 V vs V_{OUT} = 0.7 V, V_{GSNS} = 0 V	-0.5%		0.5%	
CMRR	Common mode rejection ratio(2)	0.7 V≤ V_{OUT} ≤ 4.0 V	60			dB
	Output source current	V_{OUT} - V_{GSNS} = 2.0 V, V_{DIFFO}≥ 1.98 V	2	4		mA
	Output sink current	V_{OUT} - V_{GSNS} = 2.0 V, V_{DIFFO}≥ 2.02 V	2	4		
	Input offset voltage(2)	0.7 V≤ V_{OUT} ≤ 4.0 V			5	mV
	Bandwidth(2)		5			MHz
	Input impedance, non-inverting(2)	V_{OUT} to GND		40		kΩ
	Input impedance, inverting(2)	V_{GSNS} to V_{DIFFO}		40		
GATE DRIVERS						
	Source on-resistance, HDRV1, HDRV2	V_{BOOT1} = 5 V, V_{BOOT2} = 5 V, V_{SW1} = 0 V, V_{SW2} = 0 V, Sourcing 100 mA	1.0	2.0	3.5	Ω
	Sink on-resistance, HDRV1, HDRV2	V_{BOOT1} = 5 V, V_{BOOT2} = 5 V, V_{VIN5} = 5 V, V_{SW1} = 0 V, V_{SW2} = 0 V, Sinking 100 mA	0.5	1.0	2.0	
	Source on-resistance, LDRV1, LDRV2	V_{VIN5} = 5 V, V_{SW1} = 0 V, V_{SW2} = 0 V, Sourcing 100 mA	1	2	3.5	Ω
	Sink on-resistance, LDRV1, LDRV2	V_{VIN5} = 5 V, V_{SW1} = 0 V, V_{SW2} = 0 V, Sinking 100 mA	0.30	0.75	1.50	
t_{RISE}	Rise time, HDRV(2)	C_{LOAD} = 3.3 nF		25	75	ns
t_{FALL}	Fall time, HDRV(2)	C_{LOAD} = 3.3 nF		25	75	
t_{RISE}	Rise time, LDRV(2)	C_{LOAD} = 3.3 nF		25	75	
t_{FALL}	Fall time, LDRV(2)	C_{LOAD} = 3.3 nF		25	60	
t_{DEAD}	Dead time(2)	SW falling to LDRV rising		50		
		LDRV falling to SW rising		30		
t_{ON}	Minimum controllable on-time(2)	C_{LOAD} = 3.3 nF		150		
OUTPUT UNDERVOLTAGE FAULT						
	Undervoltage fault threshold	V_{FB} relative to GND	560	588	610	mV
		V_{FB} relative to V_{VREF}	-20%	-16%	-13%	
OUTPUT OVERVOLTAGE SET						
	Overvoltage threshold	V_{OVSET} relative to GND	796	817	832	mV
		V_{OVSET} relative to V_{VREF}	14%	16%	19%	

(2) Ensured by design. Not production tested.

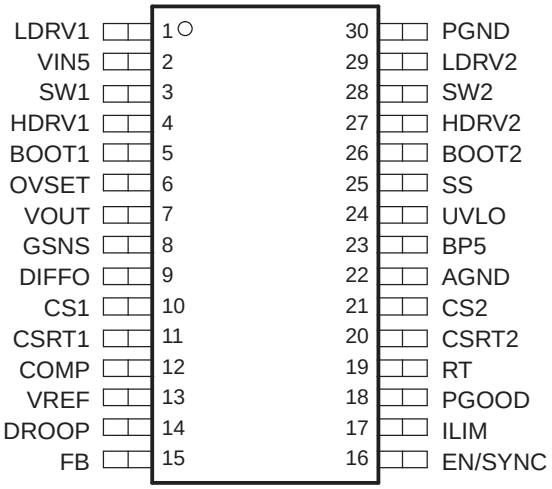
ELECTRICAL CHARACTERISTICS (continued)

T_A = -40°C to 85°C, V_{IN} = 12 V, R_{RT} = 64.9 kΩ, T_J = T_A (unless otherwise noted)

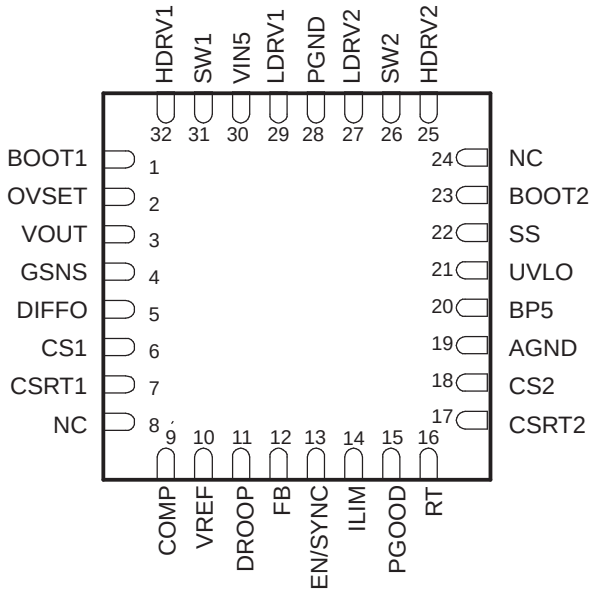
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RAMP						
	Ramp amplitude (3)		0.4	0.5	0.6	V
	Ramp valley(3)			1.4		
POWER GOOD						
	PGOOD high threshold	V_{FB} relative to V_{REF}	10%		14%	
	PGOOD low threshold	V_{FB} relative to V_{REF}	-14%		-10%	
V_{OL}	Low-level output voltage	I_{PGOOD} = 4 mA		0.35	0.60	V
I_{LEAK}	PGOOD bias current	V_{PGOOD} = 5.0 V		50	80	µA
	Current sense fault (3)	Current from CS1, CS2		5		
INPUT UVLO PROGRAMMABLE						
	Input threshold voltage, turn-on		0.9	1.0	1.1	V
	Input threshold voltage, turn-off			0.810		
LOAD LINE PROGRAMMING						
I_{DROOP}	Pull-down current	V_{CS} = 100 mV	30	40	50	µA

(3) Ensured by design. Not production tested.

DBT PACKAGE
(TOP VIEW)



RHB PACKAGE
(TOP VIEW)



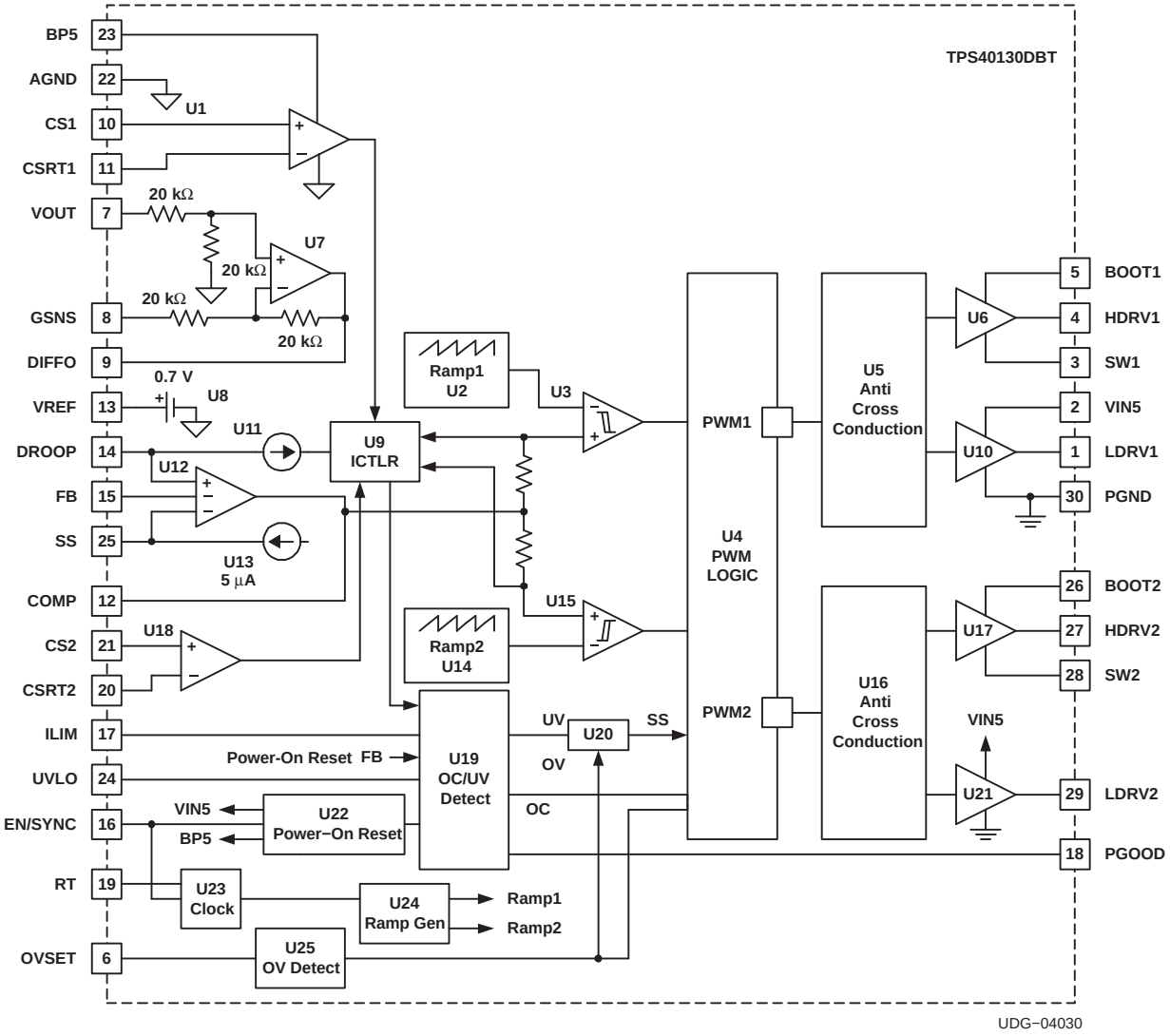
Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	RHB	DBT		
AGND	19	22	-	Low noise ground connection to the device.
BOOT1	1	5	I	Provides a bootstrapped supply for the high-side FET driver for PWM1, enabling the gate of the high-side FET to be driven above the input supply rail. Connect a capacitor from this pin to SW1 pin and a Schottky diode from this pin to VIN5.
BOOT2	23	26	I	Provides a bootstrapped supply for the high-side FET driver for PWM2, enabling the gate of the high-side FET to be driven above the input supply rail. Connect a capacitor from this pin to SW2 pin and a Schottky diode from this pin to VIN5.
BP5	20	23	O	Filtered input from the VIN5 pin. A 10-Ω resistor should be connected between VIN5 and BP5 and a 1.0-µF ceramic capacitor should be connected from this pin to ground.
COMP	9	12	O	Output of the error amplifier. The voltage at this pin determines the duty cycle for the PWM.
CS1	6	10	I	These pins are used to sense the inductor phase current. Inductor current can be sensed with an external current sense resistor or by using an external R-C circuit and the inductor's DC resistance. The traces for these signals must be connected directly at the current sense element. See Layout Guidelines for more information. After the device is enabled and prior to the device starting (during the first 32 clock cycles), a 5-µA current flows out of these pins. The current flows through the external components: current sense resistor, R_{CS}, the output inductor and the output capacitor(s) to ground. If the voltage on the CS1, and CS2 pins exceed 0.2 V (resistance greater than 40 kΩ), a fault is declared and the device does not start. This is a fault detection feature that insures the output inductor, current sense resistor and output capacitors are installed properly on the board.
CS2	18	21	I	
CSRT1	7	11	O	Return point of current sense voltage. The traces for these signals must be connected directly at the current sense element. See Layout Guidelines for more information.
CSRT2	17	20	O	
DIFFO	5	9	O	Output of the differential amplifier. The voltage at this pin represents the true output voltage without IR drops that result from high-current in the PCB traces. The VOUT and GSNS pins must be connected directly at the point of load where regulation is required. See Layout Guidelines for more information.
DROOP	11	14	I	This is the input to the non-inverting input of the Error Amplifier. This pin is normally connected to the VREF pin and is the voltage that the feedback loop regulates to. This pin is also used to program droop function. A resistor between this pin and the VREF pin sets the desired droop value. The value of the DROOP resistor is described in Equation 22.
EN/SYNC	13	16	I	A logic high signal on this input enables the controller operation. A pulsing signal to this pin synchronizes the rising edge of SW to the falling edge of an external clock source. These pulses must be greater than 8.2 times the free running frequency of the main oscillator set by the RT resistor.

Terminal Functions (continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	RHB	DBT		
FB	12	15	I	Inverting input of the error amplifier. In closed loop operation, the voltage at this pin is the internal reference level of 700 mV. This pin is also used for the PGOOD and undervoltage comparators.
GSNS	4	8	I	Inverting input of the differential amplifier. This pin should be connected to ground at the point of load.
HDRV1	32	4	O	Gate drive output for the high-side N-channel MOSFET switch for PWM1. Output is referenced to SW1 and is bootstrapped for enhancement of the high-side switch.
HDRV2	25	27	O	Gate drive output for the high-side N-channel MOSFET switch for PWM2. Output is referenced to SW2 and is bootstrapped for enhancement of the high-side switch
ILIM	14	17	I	Used to set the cycle-by-cycle current limit threshold. If ILIM threshold is reached, the PWM cycle is terminated and the converter delivers limited current to the output. Under these conditions the undervoltage threshold eventually is reached and the controller enters the hiccup mode. The controller stays in the hiccup mode for seven (7) consecutive cycles of SS voltage rising from zero to 1.0 V. At the eighth cycle the controller attempts a full start-up sequence. The relationship between ILIM and the maximum phase current is described in Equation 4 and Equation 5. See the Overcurrent Protection section for more details.
LDRV1	29	1	O	Gate drive output for the low-side synchronous rectifier (SR) N-channel MOSFET for PWM1. See *Layout Considerations* section.
LDRV2	27	29	O	Gate drive output for the low-side synchronous rectifier (SR) N-channel MOSFET for PWM2. See *Layout Considerations* section.
NC	8	-	-	No connect. This pin is mechanical only.
NC	24			
OVSET	2	6	I	A resistor divider, on this pin connected to the output voltage sets the overvoltage sense point.
PGOOD	15	18	O	Power good indicator of the output voltage. This open-drain output connects to a voltage via an external resistor. When the FB pin voltage is between 0.616 V to 0.784 V (88% to 112% of VREF), the PGOOD output is in a high impedance state. If the DROOP function is implemented, the programmed droop voltage must be within this window.
PGND	28	30	-	Power ground reference for the controller lower gate drivers. There should be a high-current return path from the sources of the lower MOSFETs to this pin.
RT	16	19	I	Connecting a resistor from this pin to ground sets the oscillator frequency.
SS	22	25	I	Provides user programmable soft-start by means of a capacitor connected to the pin. If an undervoltage fault is detected the soft-start capacitor cycles 7 times with no switching before a normal soft-start sequence allowed.
SW1	31	3	I	Connect to the switched node on converter 1. Power return for the channel 1 upper gate driver. There should be a high-current return path from the source of the upper MOSFET to this pin. It is also used by the adaptive gate drive circuits to minimize the dead time between upper and lower MOSFET conduction.
SW2	26	28	I	Connect to the switched node on converter 2. Power return for the channel 2 upper gate driver. There should be a high-current return path from the source of the upper MOSFET to this pin. It is also used by the adaptive gate drive circuits to minimize the dead time between upper and lower MOSFET conduction.
UVLO	21	24	O	A voltage divider from VIN to this pin, set to 1V, determines the input voltage that starts the controller.
VOUT	3	7	O	Non-inverting input of the differential amplifier. This pin should be connected to VOUT at the point of load.
VREF	10	13	O	Output of an internal reference voltage. The load may be up to 100 µA DC.
VIN5	30	2	I	Power input for the device. A 1.0-µF ceramic capacitor should be connected from this pin to ground.

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The TPS40130 uses programmable fixed-frequency, peak current mode control with forced phase current balancing. When compared to voltage-mode control, current mode results in a simplified feedback network and reduced input line sensitivity. Phase current is sensed by using either the DCR (direct current resistance) of the filter inductors or current sense resistors installed in series with output. The first method involves generation of a current signal with an R-C circuit (shown in the applications diagram). The R-C values are selected by matching time constants of the RC circuit and the inductor time constant, R×C = L/DCR. With either current sense method, the current signal is amplified and superimposed on the amplified voltage error signal to provide current mode PWM control.

Output voltage droop can be programmed to improve the transient window and reduce size of the output filter.

Other features include: a true differential output sense amplifier, programmable current limit, programmable output over-voltage set-point, capacitor set soft-start, power good indicator, programmable input undervoltage lockout (UVLO), user programmable operation frequency for design flexibility, external synchronization capability, programmable pulse-by-pulse overcurrent protection, output undervoltage shutdown and restart.

FUNCTIONAL DESCRIPTION (continued)

Startup Sequence

Figure 1 shows a typical start up with the VIN5 and BP5 applied to the controller and then the EN/SYNC being enabled. Shut down occurs when the VIN5 is removed

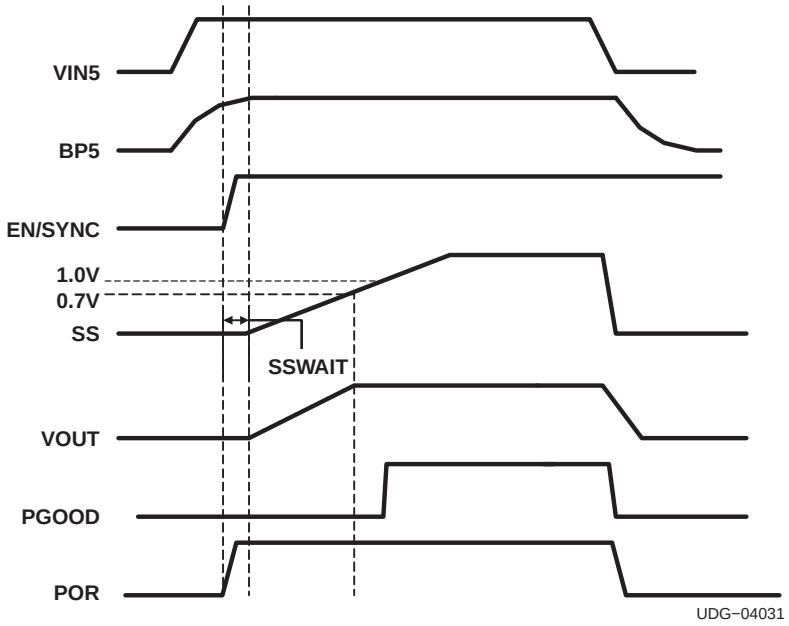


Figure 1. Startup and Shutdown Sequence

Differential Amplifier (U7)

The unity gain differential amplifier with high bandwidth allows improved regulation at a user-defined point and eases layout constraints. The output voltage is sensed between the VOUT and GSNS pins. The output voltage programming divider is connected to the output of the amplifier (DIFFO). The differential amplifier input voltage must be lower than (V_{BP5} - 0.7 V).

If there is no need for a differential amplifer, the differential amplifier can be disabled by connecting the GSNS pin to the BP5 pin and leaving VOUT and DIFFO open. The voltage programming divider in this case should be connected directly to the output of the converter.

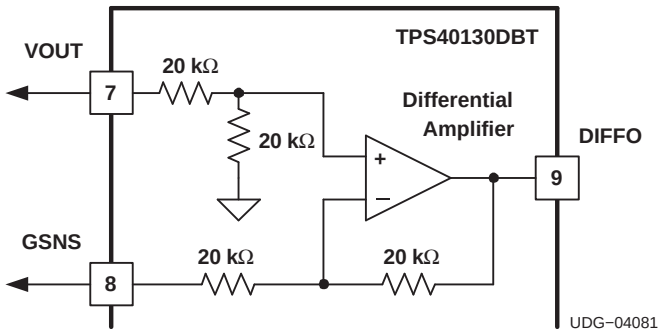


Figure 2. Differential Amplifier Configuration

Because of the resistor configuration of the differential amplifier, the input impedance must be kept very low or there will be error in setting the output voltage.

FUNCTIONAL DESCRIPTION (continued)

Current Sensing and Balancing (U1, U9 and U18)

The controller employs peak current mode control scheme, thus naturally provides certain degree of current balancing. With current mode, the level of current feedback should comply with certain guidelines depending on duty factor known as “slope compensation” to avoid the sub-harmonic instability. This requirement can prohibit achieving a higher degree of phase current balance. To avoid the controversy, a separate current loop that forces phase currents to match is added to the proprietary control scheme. This effectively provides high degree of current sharing independent of the controller’s small signal response and is implemented in U9, ICTLR.

High bandwidth current amplifiers, U1 and U18 can accept as an input voltage either the voltage drop across dedicated precise current sense resistors, or inductor’s DCR voltage derived by an RC network, or thermally compensated voltage derived from the inductor’s DCR. The wide range of current sense arrangements ease the cost/complexity constrains and provides superior performance compared to controllers utilizing the low-side MOSFET current sensing. The current sense amplifier inputs must not exceed 4 V. See the *Inductor DCR Current Sense* section for more information on selecting component values for the R-C network.

PowerGood

The PGOOD pin indicates when the inputs and output are within their specified ranges of operation. Also monitored are the EN/SYNC and SS pins. PGOOD has high impedance when indicating inputs and outputs are within specified limits and is pulled low to indicate an out-of-limits condition. Some applications may require hysteresis on the PGOOD signal to avoid a PGOOD signal bounce. A simple method to achieve this (and thereby eliminate any PGOOD signal bounce) is to add a small resistor (R_A) and capacitor (C_A) between the FB pin and the PGOOD pin. See Figure 3 for implementation.

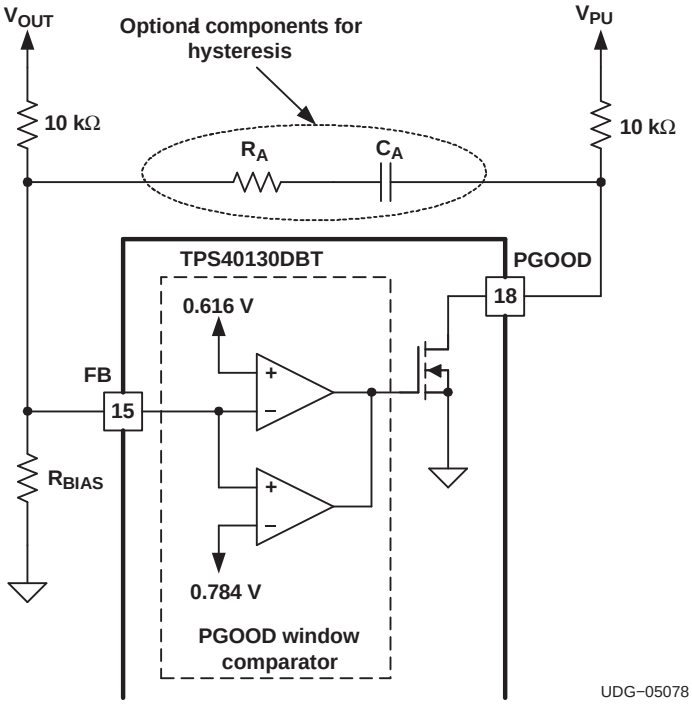


Figure 3. Adding Hysteresis to the PGOOD Signal

To select R_A and C_A, the following criteria can be used.

$$R_A = R_{BIAS} \times \left[\left(\frac{V_{PU} - V_{FB}}{1.3 \times 0.16 \times V_{FB}} \right) - 1 \right] \quad (1)$$

V_{PU} and the PGOOD pull-up voltage and V_{FB} is the TPS40130 internal reference voltage. The factor 1.3 in Equation 1 provides a margin for robustness.

FUNCTIONAL DESCRIPTION (continued)

$$C_A = \frac{100\ ns}{R_A} \quad (2)$$

Even though C_A may calculate to less than 1 pF, a capacitance of no more than 4.7 pF is recommended.

Soft-Start

A capacitor connected to the soft start pin (SS) sets the power-up time. When EN is high and POR is cleared, the calibrated current source, U13, starts charging the external soft start capacitor. The PGOOD pin is held low during the start up. The rising voltage across the capacitor serves as a reference for the error amplifier, U12. When the soft-start voltage reaches the level of the reference voltage, U8 (V_{VREF}=0.7V), the converter's output reaches the regulation point and further voltage rise of the soft start voltage has no effect on the output. When the soft start voltage reaches 1.0 V, the power good (PGOOD) function is cleared to be reported on the PGOOD pin. Normally the PGOOD pin goes high at this time. Equation 3 is used to calculate the value of the soft-start capacitor.

$$t_{SS} = \frac{0.7 \times C_{SS}}{5 \times 10^{-6}} \quad (3)$$

Overcurrent Protection

The overcurrent function, U19, monitors the output of current sense amplifiers U1 and U18. These currents are converted to voltages and compared to the voltage on the ILIM pin. The relationship between the maximum phase current and the current sense resistance is given in the following equation. In case a threshold of V_{ILIM}/2.7 is exceeded the PWM cycle on the associated phase is terminated. The overcurrent threshold, $I_{PH(max)}$, and the voltage to set on the ILIM pin is determined by Equation 4 and Equation 5.

$$V_{ILIM} = 2.7 \times I_{PH(max)} \times R_{CS} \quad (4)$$

$$I_{PH(max)} = \frac{I_{OUT}}{2} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L_{OUT} \times f_{SW} \times V_{IN}} \quad (5)$$

where

- $I_{PH(max)}$ is a maximum value of the phase current allowed
- I_{OUT} is the total maximum DC output current
- R_{CS} is a value of the current sense resistor used or the DCR value of the output inductor, L_{OUT}

If the overcurrent condition persists, both phases have PWM cycles terminated by the overcurrent signals. This puts a converter in a constant current mode with the output current programmed by the ILIM voltage. Eventually the supply-and-demand equilibrium on the converter output is not satisfied and the output voltage starts to decline. When the undervoltage threshold is reached, the converter enters a hiccup mode. The controller is stopped and the output is not regulated any more, the soft-start pin function changes.

It now serves as a hiccup timing capacitor controlled by U20, the fault control circuit. The soft-start pin is periodically charged and discharged by U20. After seven hiccup cycles, the controller attempts another soft-start cycle to restore normal operation. If the overload condition persists, the controller returns to the hiccup mode. This condition may continue indefinitely. In such conditions the average current delivered to the load is approximately 1/8 of the set overcurrent value.

Current Sense Fault Protection

Multiphase controllers with forced current sharing are inherently sensitive to a failure of the current sense component or a defect in the assembly process. In case of such failure the entire load current can be steered with catastrophic consequences into a single channel where the fault has occurred. A dedicated circuit in the TPS40130 controller detects this defect and prevents the controller from starting up. This fault detection circuit is active only during chip initialization and does not protect should current sense failure happen during normal operation.

FUNCTIONAL DESCRIPTION (continued)

After the device is enabled and prior to the IC starting (during the first 32 clock cycles), a 5-µA current flows out of the CS1 and CS2 pins. The current flows through the external components: current sense resistor, R_{CS}, the output inductor and the output capacitor(s) to ground. If the voltage on the CS1 and CS2 pins exceed 0.2 V (resistance greater than 40 kΩ), a fault is declared and the device does not start. This is a fault detection feature that insures the output inductor, current sense resistor and output capacitors are installed properly on the board.

Overvoltage Protection

The voltage on OVSET is compared with 0.817 V, 16% higher than VREF, in U25 to determine the output overvoltage point. When an overvoltage is detected, the output drivers command the upper MOSFETs off and the lower MOSFETs on. If the overvoltage is caused by a shorted upper MOSFET, latching on the lower MOSFET should blow the input fuse and protect the output. Hiccup mode consisting of seven (7) soft-start timing cycles is initiated and then attempts to restart. If the overvoltage condition has been cleared and the input fuse has not opened, the output comes up and normal operation continues. If the overvoltage condition persists, the controller restarts to allow the output to rise to the overvoltage level and return to the hiccup mode. Using a voltage divider with the same ratio, that sets the output voltage, an output overvoltage is declared when the output rises 16% above nominal.

Output Undervoltage Protection

If the output voltage, as sensed by U19 on the FB pin becomes less than 0.588 V, the undervoltage protection threshold (84% of VREF), the controller enters the hiccup mode as it is described in the Overcurrent Protection section.

Programmable Input Undervoltage Lockout Protection

A voltage divider that sets 1V on the UVLO pin determines when the controller starts operating. Operation commences when the voltage on the UVLO pin exceeds 1.0 V.

Power-On Reset (POR)

The power-on reset (POR) function, U22, insures the VIN5 and BP5 voltages are within their regulation windows before the controller is allowed to start.

Fault Masking Operation

If the SS pin voltage is externally limited below the 1-V threshold, the controller does not respond to most faults and the PGOOD output is always low. Only the overcurrent function and current sense fault remain active. The overcurrent protection still continues to terminate PWM cycle every time when the threshold is exceeded but the hiccup mode is not entered.

Fault Conditions and MOSFET Control

Table 1 shows a summary of the fault conditions and the state of the MOSFETs.

Table 1. Fault Condifions

FAULT MODE	UPPER MOSFET	LOWER MOSFET
EN/SYNC = LOW	OFF	OFF
FIXED UVLO, V_{BP5} < 4.25 V	OFF	OFF
Programmable UVLO, < 1.0 V	OFF	ON
Output undervoltage	OFF, Hiccup mode	ON, Hiccup mode
Output overvoltage	OFF, Hiccup mode	ON, Hiccup mode
ISF, current sense fault	OFF	ON

Setting the Switching Frequency

The clock frequency is programmed by the value of the timing resistor connected from the RT pin to ground. See Equation 6.

$$R_T = 0.8 \times \left[\left(\frac{36 \times 10^3}{f_{PH}} \right) - 9 \right] \quad (6)$$

f_{PH} is a single phase frequency, kHz. The RT resistor value is expressed in kΩ. See Figure 4.

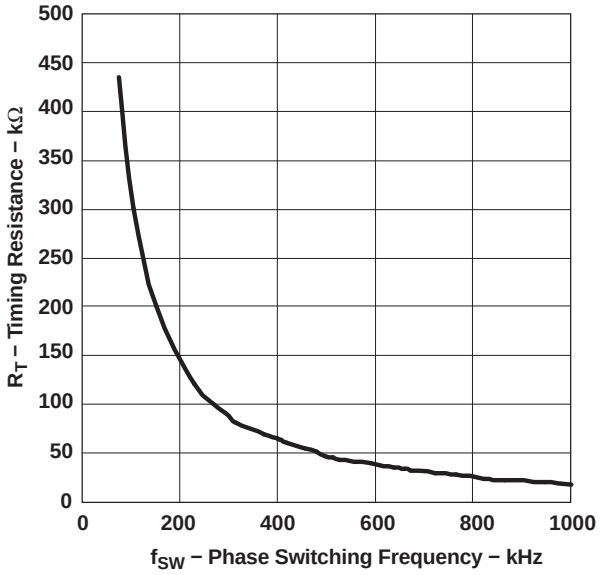


Figure 4. Phase Switching Frequency vs. Timing Resistance

EN/SYNC Function

The output ripple frequency is twice that of the single phase frequency. The switching frequency of the controller can be synchronized to an external clock applied to the EN/SYNC pin. The external clock synchronizes the rising edge of HDRV and the falling edge of an external clock source. The external clock pulses must be at a frequency at least 8.2 times higher than the switching frequency set by the RT resistor.

Setting Overcurrent Protection

Setting the overcurrent protection is given in the following equations. Care must be taken when calculating V_{ILIM} to include the increase in R_{CS} caused by the output current as it approaches the overcurrent trip point. The DCR (R_{CS} in the equation) of the inductor increases approximately 0.39% per degree Centigrade.

$$V_{ILIM} = 2.7 \times I_{PH(max)} \times R_{CS} \tag{7}$$

$$I_{PH(max)} = \frac{I_{OUT}}{2} + \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{2 \times L_{OUT} \times f_{SW} \times V_{IN}} \tag{8}$$

where

- $I_{PH(max)}$ is a maximum value of the phase current allowed
- I_{OUT} is the total maximum DC output current
- L_{OUT} is the output inductor value
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage
- R_{CS} is a value of the current sense resistor used or the DCR value of the output inductor, L_{OUT}

Resistor Divider Calculation for VOUT, ILIM, OVSET and UVLO

Use Figure 9 for setting the output voltage, current limit voltage and overvoltage setting voltage. Select R_{BIAS} using Equation 9. With a voltage divider from V_{REF}, select R6 using Equation 10. WIth a voltage from DIFFO select R4 using Equation 11. With a voltage divider from V_{IN}, select R8 using Equation 12.

$$R_{BIAS} = 0.7 \times \frac{R1}{\left(V_{OUT} - 0.7\right)} \tag{9}$$

$$R6 = R5 \times \frac{V_{ILIM}}{\left(0.7 - V_{ILIM}\right)} \tag{10}$$

$$R4 = 0.812 \times \frac{R3}{\left(V_{OUT(ov)} - 0.812\right)} \tag{11}$$

$$R8 = 1.0 \times \frac{R7}{\left(V_{IN} - 1.0\right)} \tag{12}$$

Feedback Loop Compensation

The TPS40130 operates in a peak-current mode and the converter exhibits a single pole response with ESR zero for which Type II compensation network is usually adequate as shown in Figure 5.

The load pole is situated at a value calculated using Equation 13.

$$f_{OP} = \frac{1}{2\pi \times R_{OUT} \times C_{OUT}} \tag{13}$$

and the ESR zero is situated at a value calculated using Equation 14.

$$f_{ESRZ} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \tag{14}$$

To achieve the desired bandwidth the error amplifier has to compensate for modulator gain loss at the crossover frequency. A zero placed at the load pole frequency facilitates that. The ESR zero alters the modulator -1 slope at higher frequencies. To compensate for the ESR zero, a pole in the error amplifier transfer function should be placed at the ESR zero frequency.

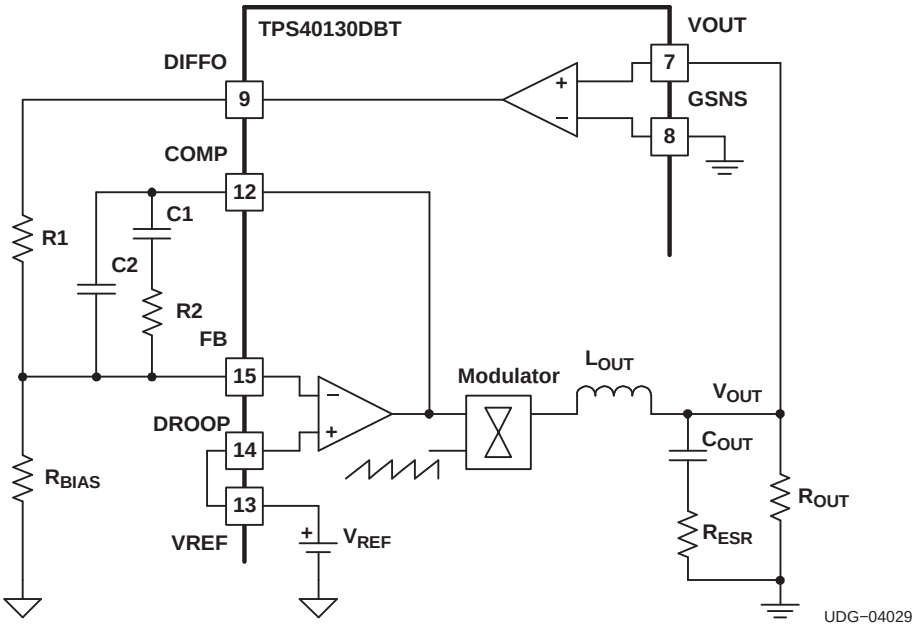


Figure 5. Compensation Components

The following expressions help in choosing components of the EA compensation network. It is recommended to fix value of the resistor R1 first as it further simplifies adjustments of the output voltage without altering the compensation network.

$$R2 = \frac{R1}{AMOD(f)} \tag{15}$$

$$AMOD = \frac{V_{VIN}}{0.4} \tag{16}$$

where AMOD is the modulator gain at DC

$$AMOD(f) = AMOD \times \frac{f_{OP}}{f_C} \tag{17}$$

where AMOD(f) is the modulator gain at the crossover frequency

$$C1 = \frac{1}{\left(2\pi \times f_{OP} \times R2\right)} \tag{18}$$

$$C2 = \frac{1}{\left(2\pi \times f_{ESRZ} \times R2\right)} \tag{19}$$

Introduction of output voltage droop as a measure to reduce amount of filter capacitors changes the transfer function of the modulator as it is shown in Figure 6 and Figure 7. The droop function introduces another zero in the modulator gain function.

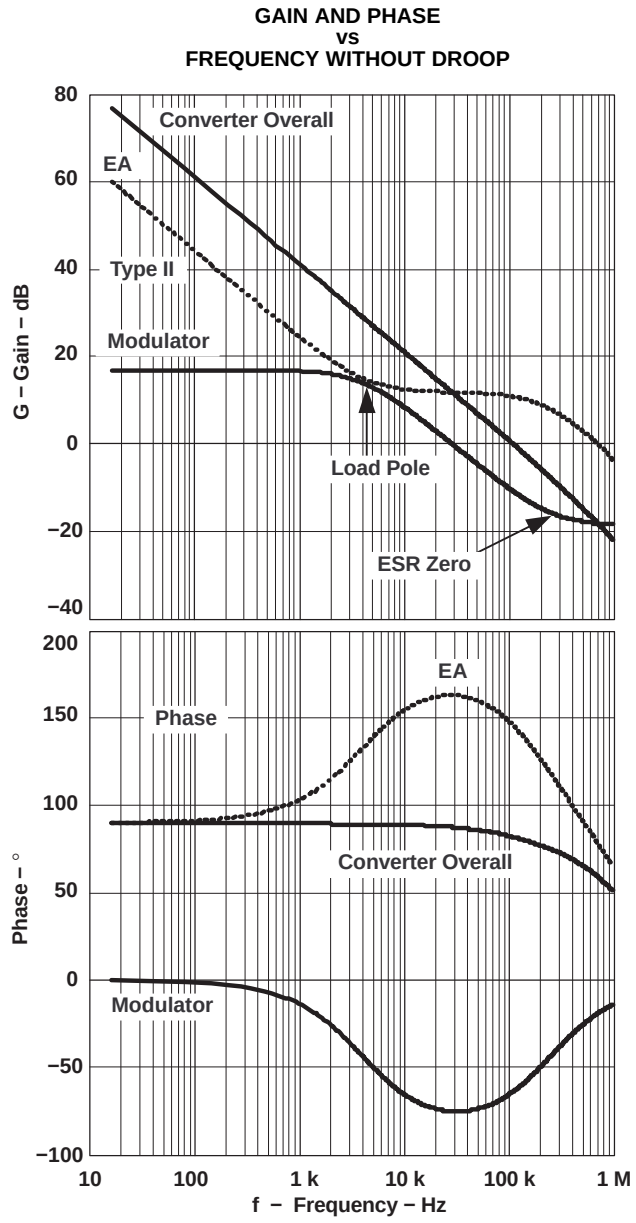


Figure 6.

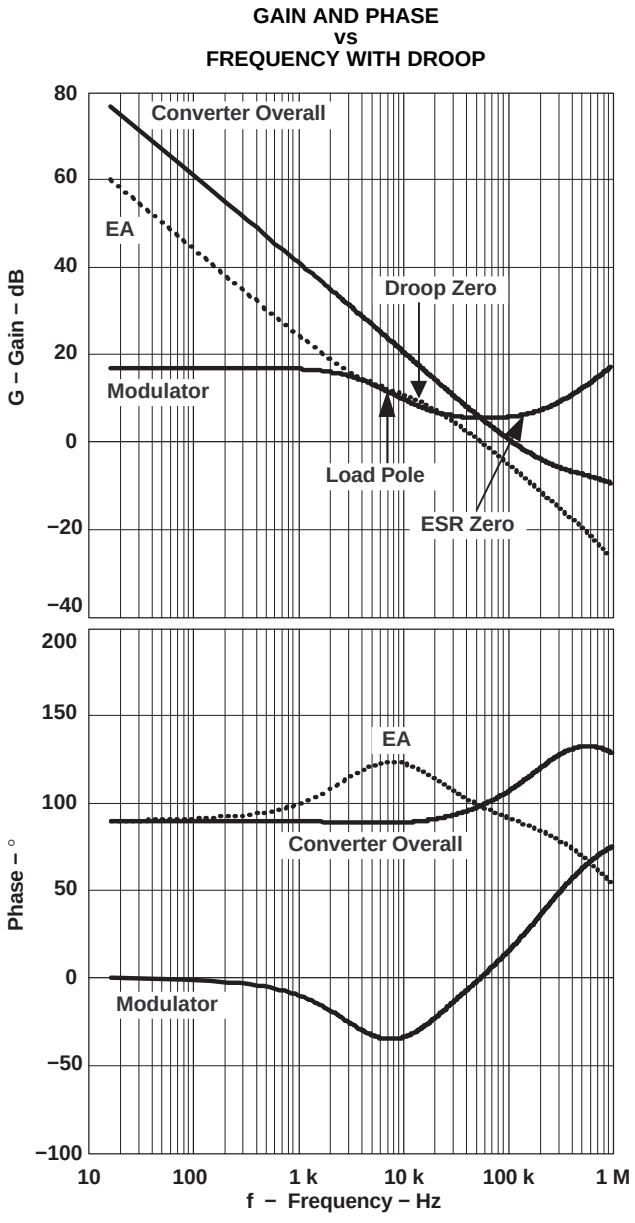


Figure 7.

The droop function, as well as the the output capacitor ESR, introduce a zero on some frequency left from the crossover point. See Equation 20

$$f_{DROOPZ} = \frac{1}{2\pi \left(\frac{V_{DROOP}}{I_{OUT(max)}} \right) \times C_{OUT}} \quad (20)$$

To compensate for this zero, pole on the same frequency should be added to the error amplifier transfer function. With Type II compensation network a new value for the capacitor C2 is required compared to the case without droop.

$$C2 = \frac{C1}{2\pi \times R2 \times C1 \times \left(f_{DROOPZ} - 1\right)} \quad (21)$$

When attempting closing the feedback loop at frequency that is close to the theoretical limit, use the above considerations as a first approximation and perform on bench measurements of closed loop parameters as effects of switching frequency proximity and finite bandwidth of voltage and current amplifiers may substantially alter them as it is shown in Figure 8.

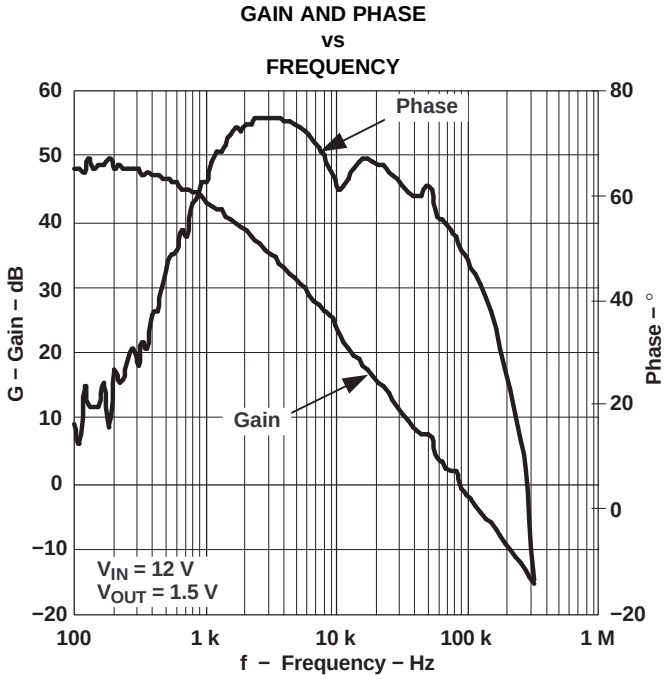


Figure 8.

Setting the Output Voltage Droop

In many applications the output voltage of the converter intentionally allowed to droop as load current increases. This approach also called active load line programming and allows for better use of regulation window and reduces the amount of the output capacitors required to handle a load current step. A resistor from the VREF pin to the DROOP pin sets the desired value of the output voltage droop. See Equation 22.

$$R_{DROOP} = \frac{5000 \times V_{DROOP}}{I_{OUT} \times R_{CS}} \times \frac{R_{BIAS}}{R1 + R_{BIAS}} \quad (22)$$

where

- V_{DROOP} is the value of droop at maximum load current (I_{LOAD})
- R_{CS} is a value of the current sense resistor used or the DCR value of the output inductor

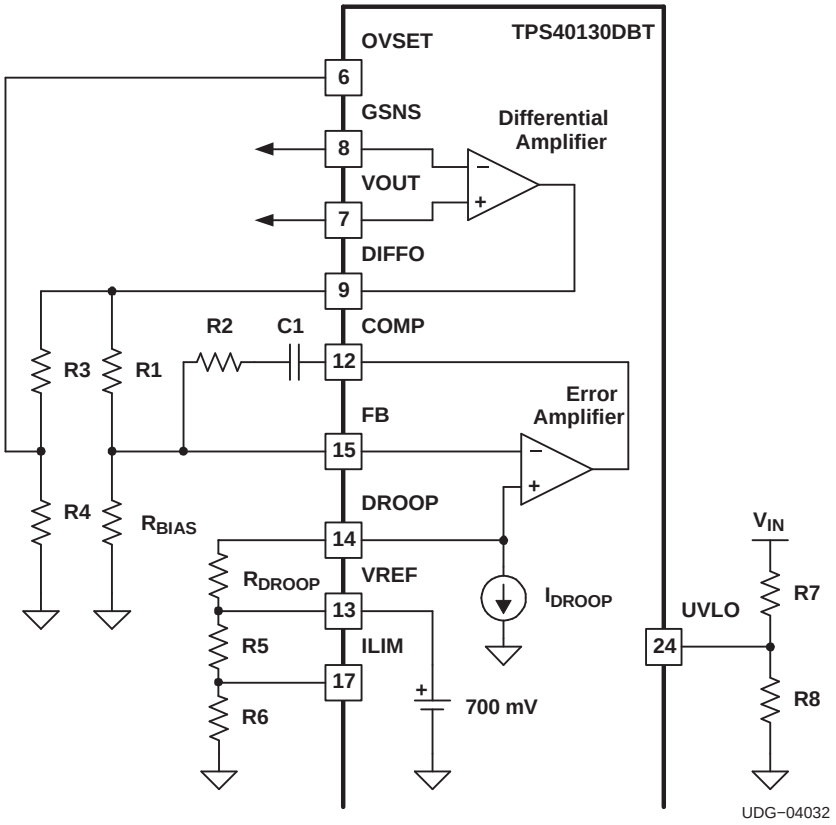


Figure 9. Implementing the Droop Function, Resistor Between DROOP and VREF.

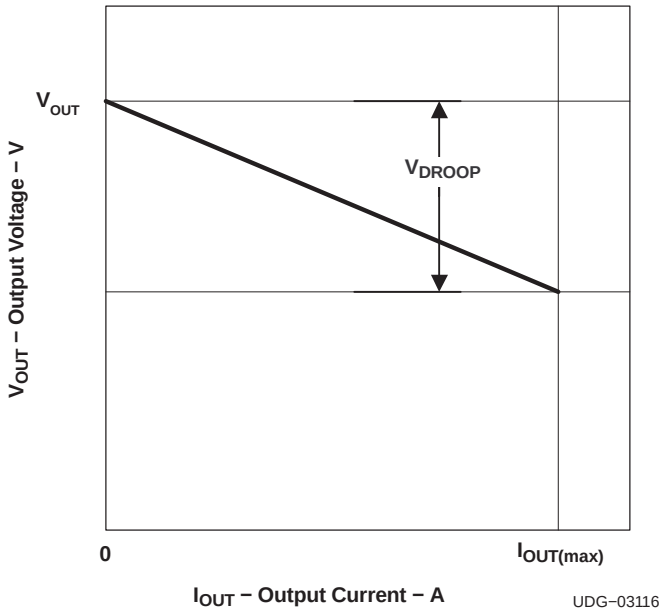


Figure 10. Output Voltage Droop Characteristic as Output Current Varies.

Inductor DCR Current Sense

Inductor DCR current sensing is a known lossless technique to retrieve current proportional signal. Referring to Figure 11.

At any given frequency the DCR voltage can be calculated using Equation 23 and Equation 24.

$$V_{DCR} = \left(V_{IN} - V_{OUT}\right) \times \frac{DCR}{DCR + \omega \times L} \tag{23}$$

$$V_C = \left(V_{IN} - V_{OUT}\right) \times \frac{1}{\omega \times C \times \left(R_{CS} + \frac{1}{\omega \times C}\right)} \tag{24}$$

Voltage across the capacitor is equal to voltage drop across the inductor DCR, V_C=V_{DCR} when time constant of the inductor and the time constant of the RC network are equal, see Equation 25. Setting the value of the capacitor to 0.1 µF or 0.01 µF provides for reasonable resistor values.

$$V_C = \frac{1}{\omega \times C \times \left(R_{CS} + \frac{1}{\omega \times C}\right)} = \frac{DCR}{DCR + \omega \times L}; \quad \frac{L}{DCR} = R_{CS} \times C; \quad \tau_{DCRL} = \tau_{RC} \tag{25}$$

The output signal generated by the network shown in Figure 11 is temperature dependent due to positive thermal coefficient of copper specific resistance K_T=1+0.0039 ×(T-25). The temperature variation of the inductor coil can easily exceed 100°C in a practical application leading to approximately 40% variation in the output signal and, in turn, respectively moving the overcurrent threshold and the load line.

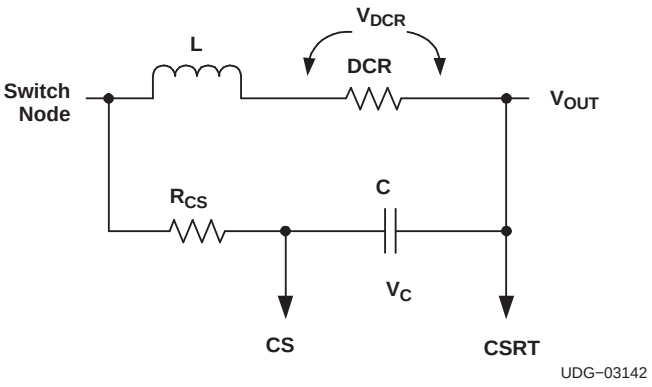


Figure 11. Inductor Current Sense Configuration for 1.2-V Output

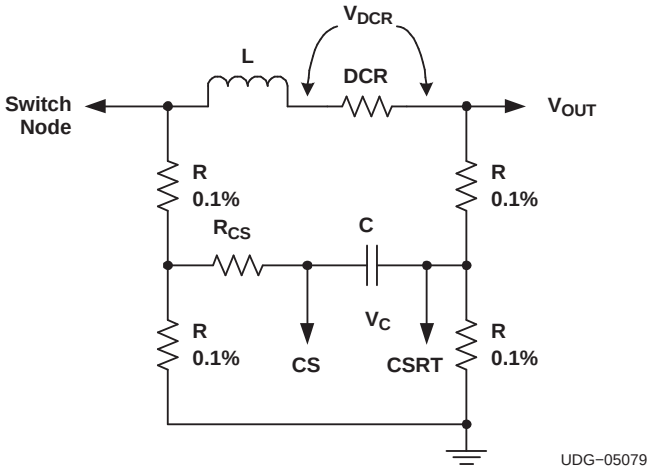


Figure 12. Inductor Current Sense Configuration for 5-V Output

Inductor DCR Current Sensing with 5-V Outputs

Due to the current sense operational amplifier input common mode voltage range, it is necessary to divide the current sense information before connecting to the TPS40130 current sense pins (CS1, CSRT1, CS2 and CSRT2). Figure 12 shows how this is achieved. R_{CS} and C are selected as normal using the method described in Equation 24 and Equation 25. The divider resistors (R) are chosen to be much smaller than R_{CS}. They are typically 100 times smaller. However, if these resitors are too small, they may dissipate too much power. In that case, choose a smaller capacitance value, and select a new R_{CS}. The resistors used in the divider should be precision resistors each having the same value.

APPLICATION INFORMATION

Applications Circuit

Figure 13 shows a typical applications circuit providing 1.5 V_{OUT} at 40 A.

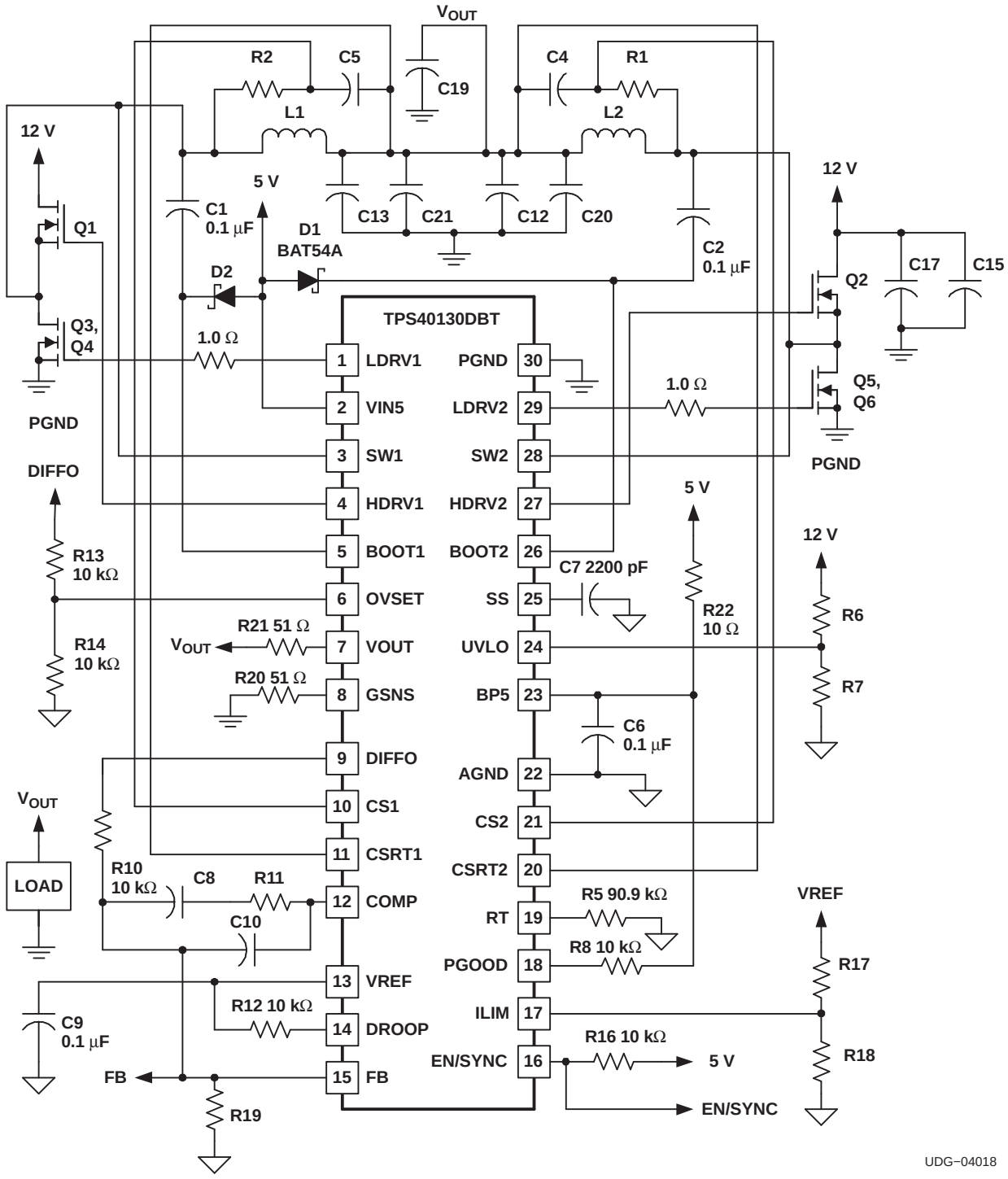


Figure 13. Typical Application Circuit

APPLICATION INFORMATION (continued)

Additional Application Circuits

Figure 14 shows a VRM10.x compliant solution where the output voltage is controlled by the VID code of the TPS40120. The six-bit controller provides outputs from 0.8375 V to 1.600 V in 12.5 mV steps for VRM 10.x or provides five-bit control for other Intel processors. When the TPS40120 receives a VID of x11111, indicating the no CPU state, output NCPU1# pulls the soft-start (SS) pin low insuring the output voltage soft-starts with a valid VID code.

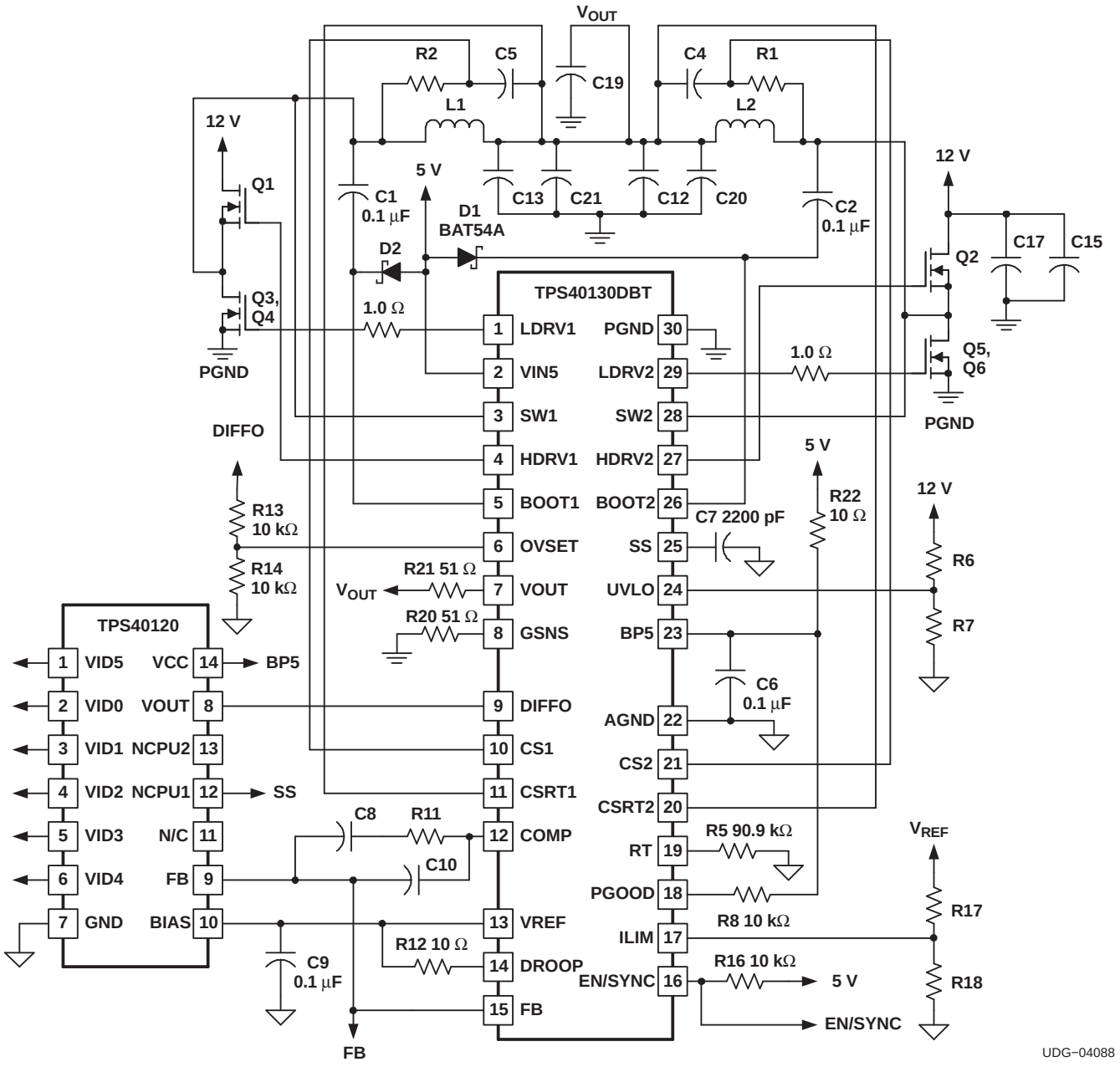


Figure 14. Application Circuit with VID Control

Figure 15 shows the configuration with the TPS40130 processing power from two different input power sources, 12 V and 5 V is shown. This is useful when there is not sufficient power from a single input source to provide the required output power. The inductor currents are not equal and the difference in the peak currents are approximately:

APPLICATION INFORMATION (continued)

$$\Delta I_{PEAK} \cong 0.067 \frac{(D1 - D2)}{DCR \times \eta} \quad (26)$$

where

- D1 is the duty cycle for V_{IN1}
- D2 is the duty cycle for V_{IN2}
- DCR is the resistance of the output inductor
- η is the efficiency of the converter

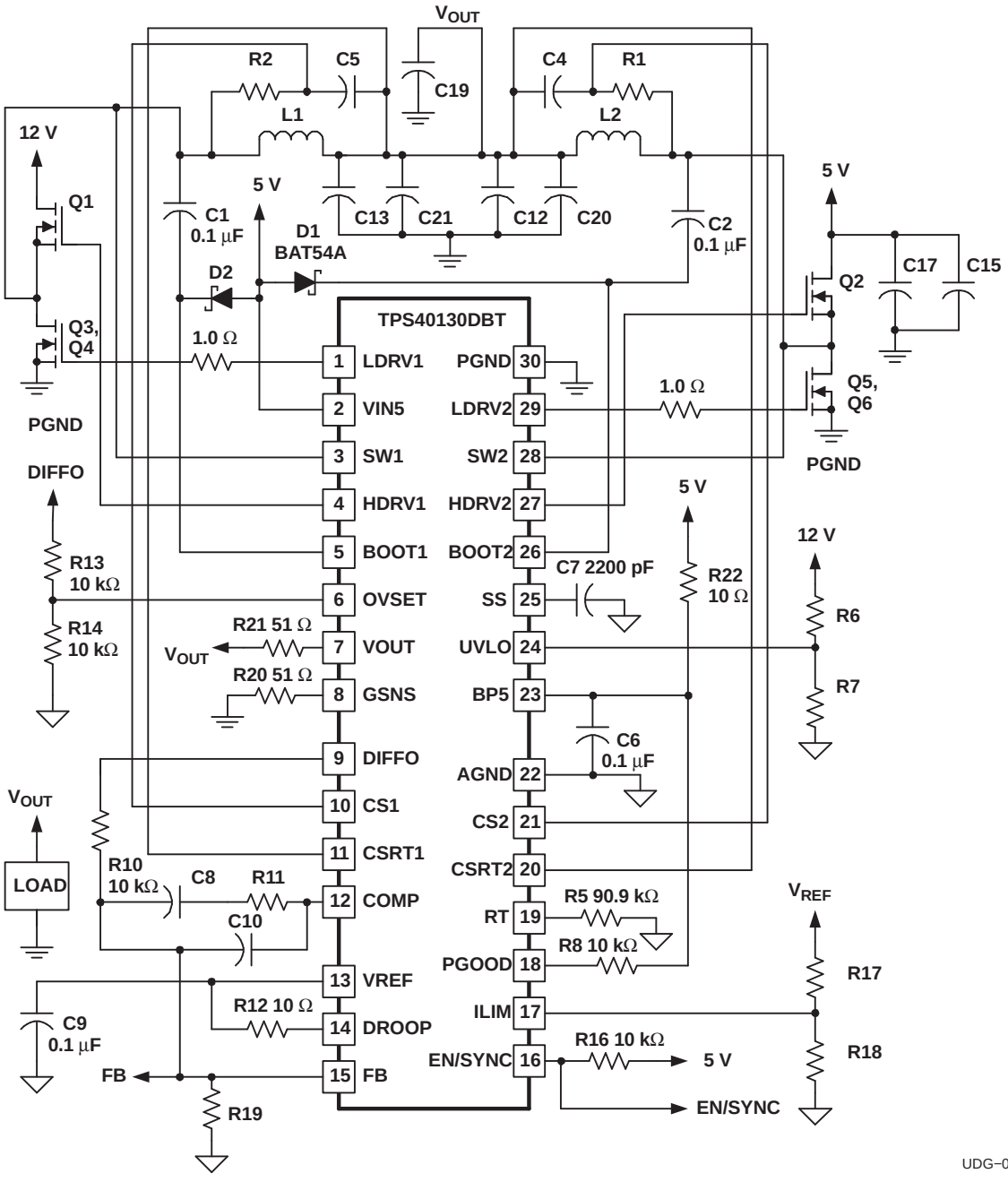


Figure 15. Application Circuit with Input Voltage Power Sharing from Two Separate Voltage Sources

APPLICATION INFORMATION (continued)

Figure 16 shows the required 5-V input being generated with an external linear regulator. The regulator shown is the TL431 shunt regulator which is a very cost effective solution. Depending on the required current to the MOSFET gates, the 115 Ω resistor may need to be a ¼ W or ½ W resistor.

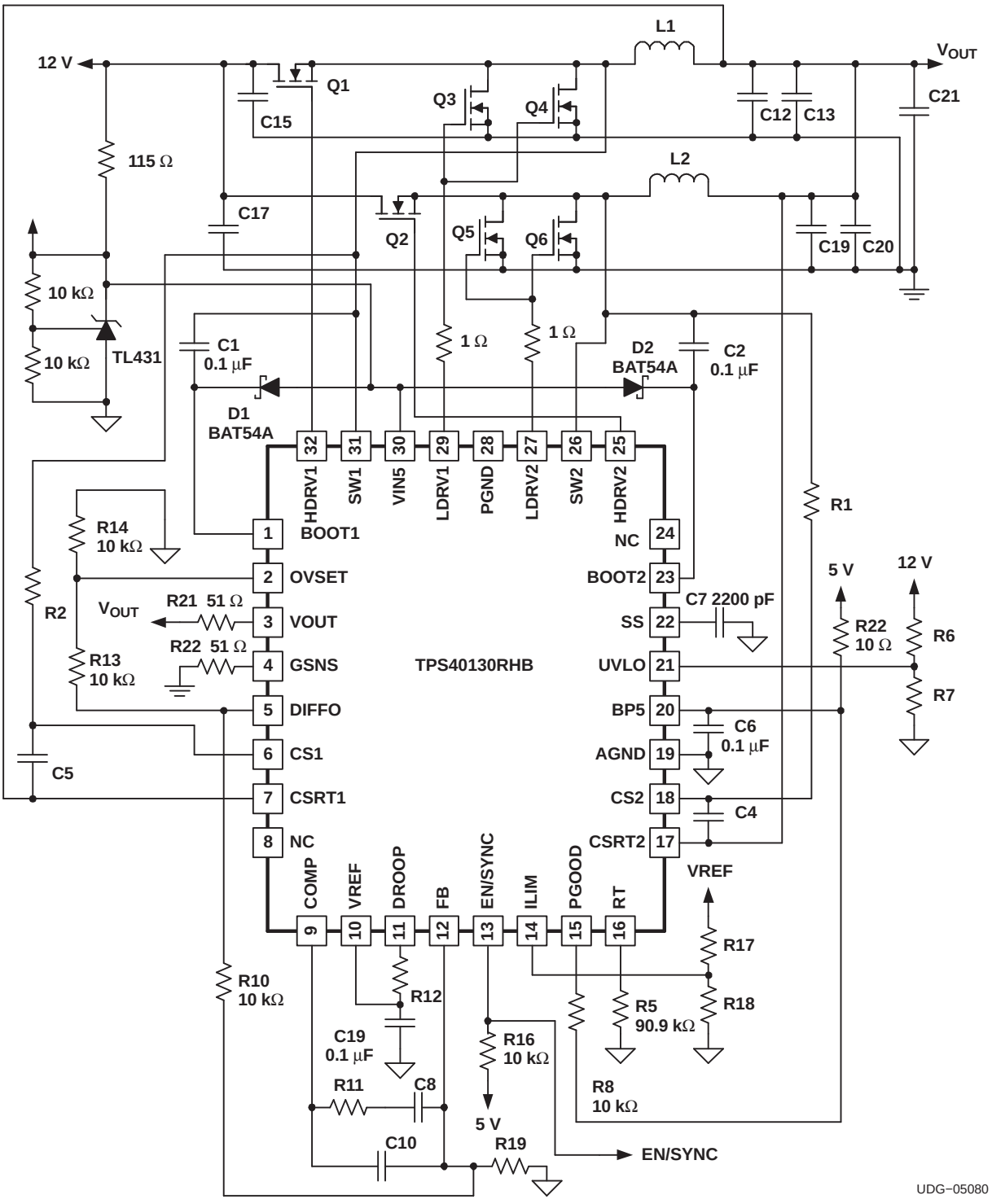


Figure 16. Application Circuit with an External Linear Regulator Providing VIN5

APPLICATION INFORMATION (continued)

Figure 17 shows the configuration for efficiently operating at high frequencies. With the power stages input at 5 V, the switching losses in the upper MOSFET are significantly reduced. The upper MOSFET should be selected for lower $R_{DS(on)}$ because the conduction losses are somewhat higher at the higher duty cycle.

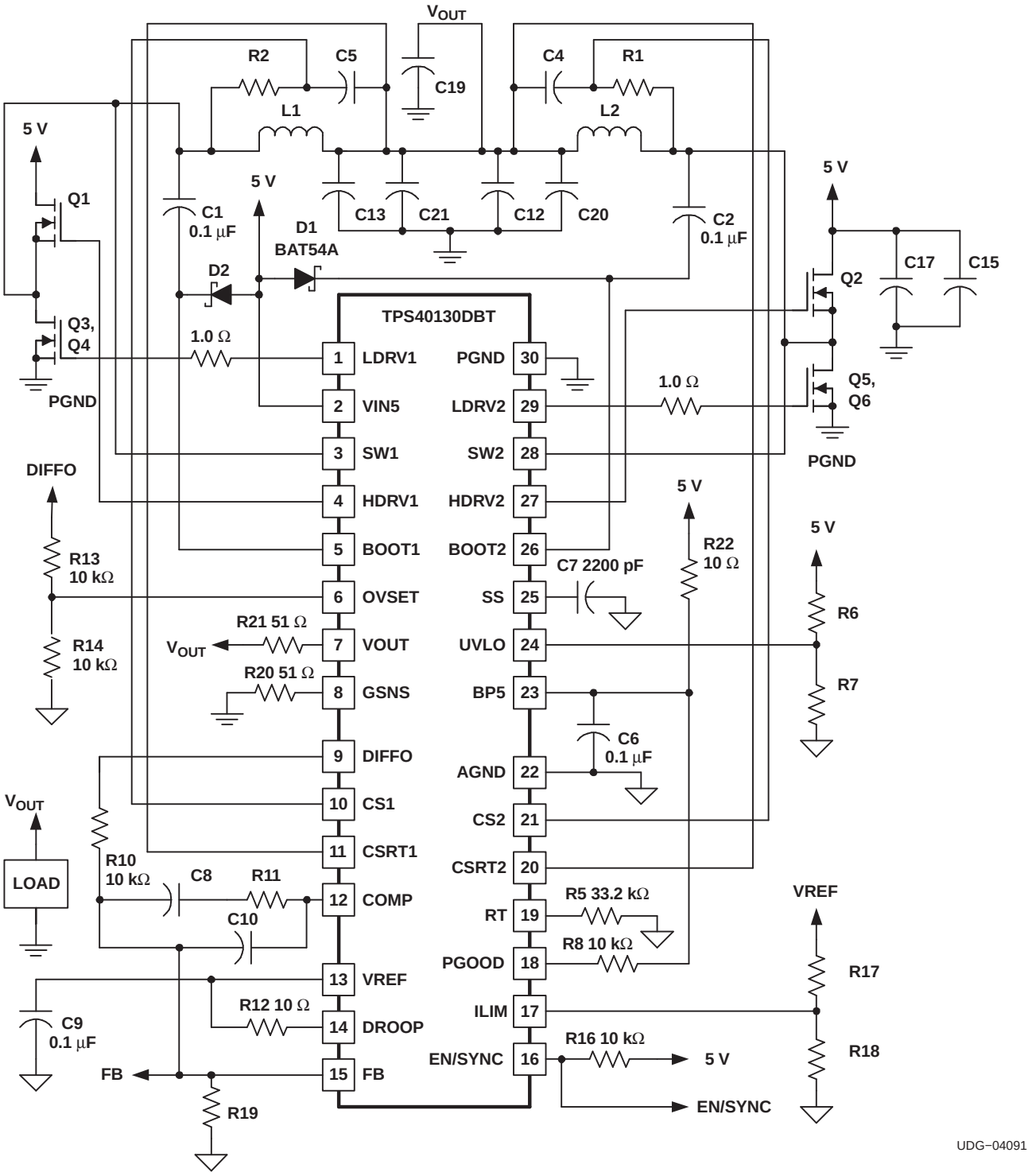


Figure 17. Application Circuit For High-Frequency Operation With Input Voltage of 5 V

APPLICATION INFORMATION (continued)

Figure 18 shows how to configure for a 5-V output. The resistor dividers on the CSx and CSRTx inputs are necessary to reduce the common mode voltage into the current sense amplifiers. The differential amplifier is not used because with a 5-V output, remote sensing is not generally necessary. If the differential Amplifier is necessary, a voltage divider of 2/3 should be used and the magnitude of the resistors should be about 500 Ω and 1 kΩ.

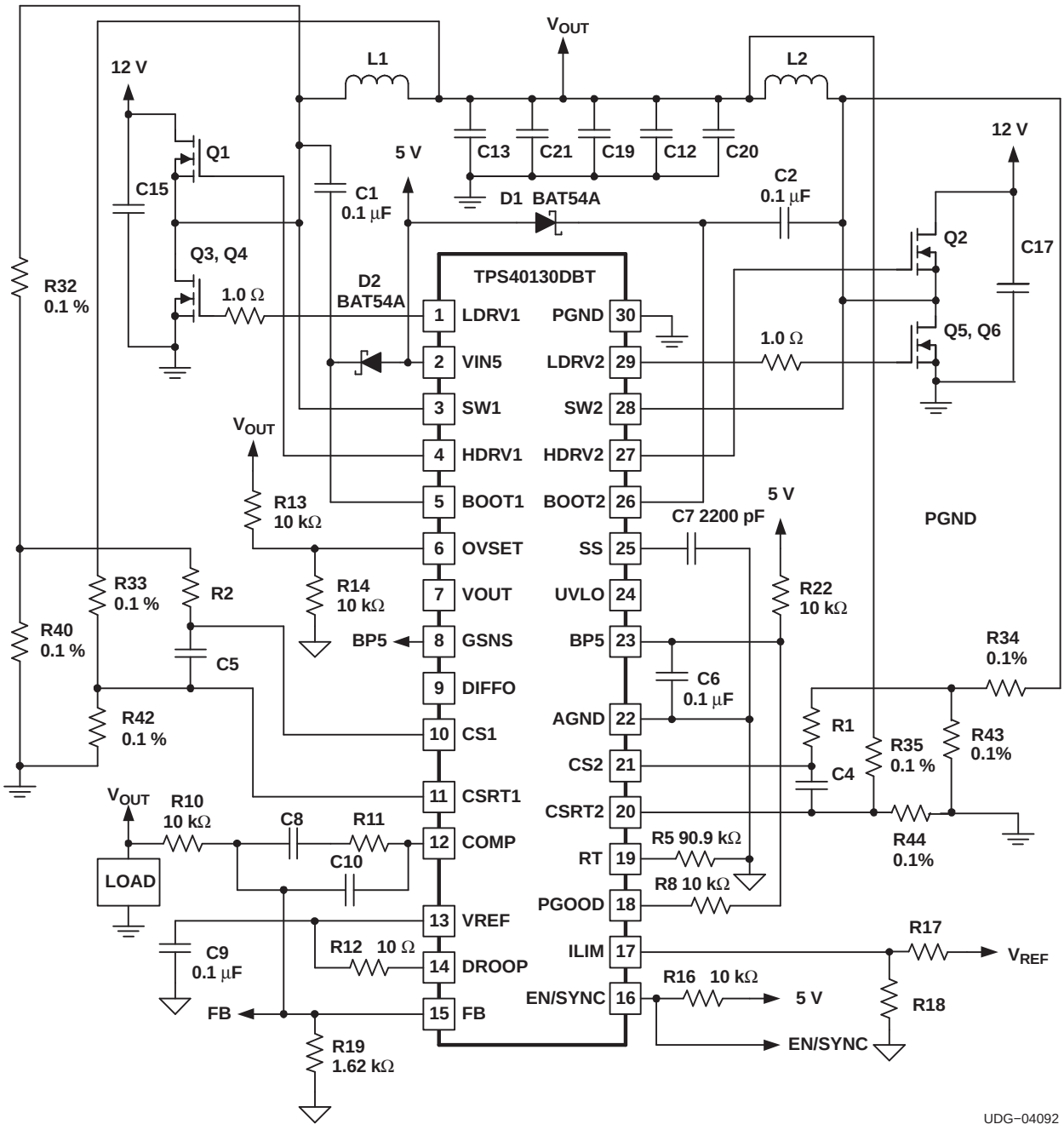


Figure 18. Application Circuit for Providing 5-V Output

TYPICAL CHARACTERISTICS

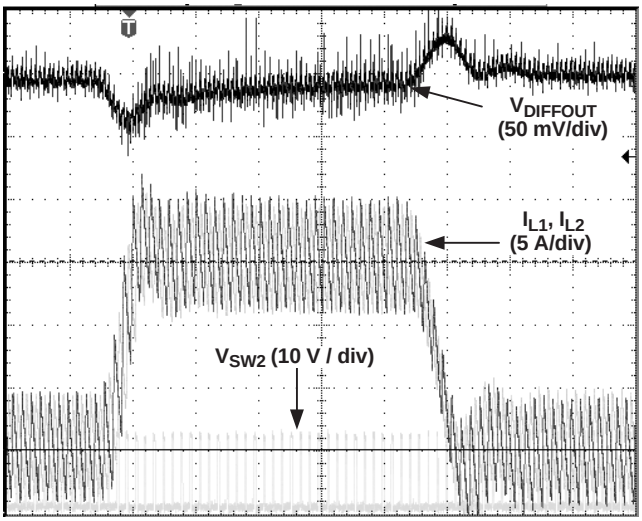


Figure 19. Load Transient

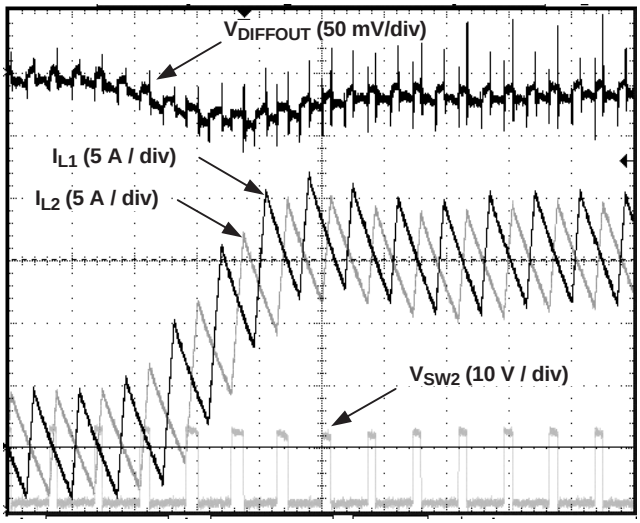


Figure 20. Load Transient Rising Edge

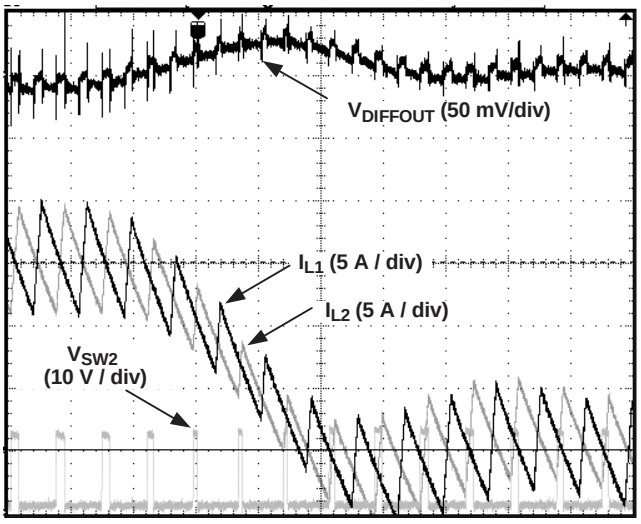


Figure 21. Load Transient Falling Edge

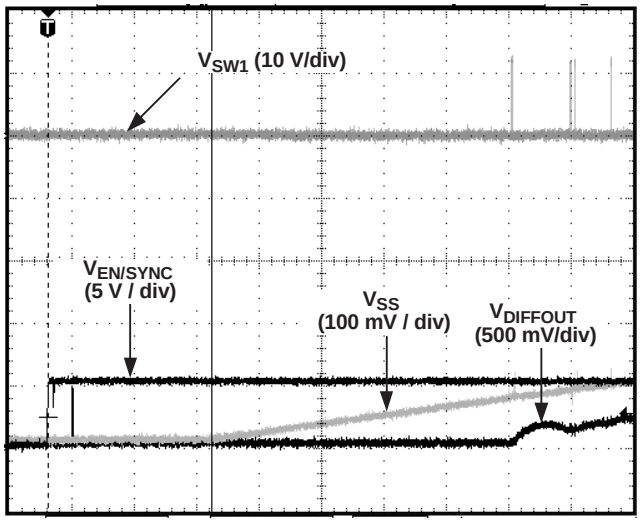


Figure 22. Start-Up with EN/SYNC and Showing Soft-Wait Time

TYPICAL CHARACTERISTICS (continued)

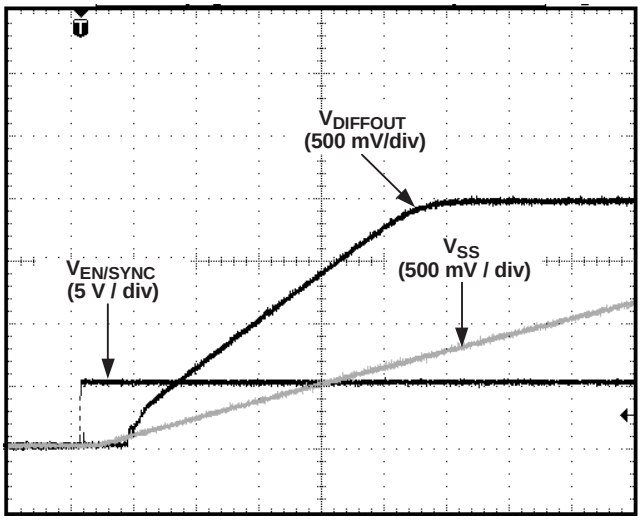


Figure 23. Start-Up with EN/SYNC

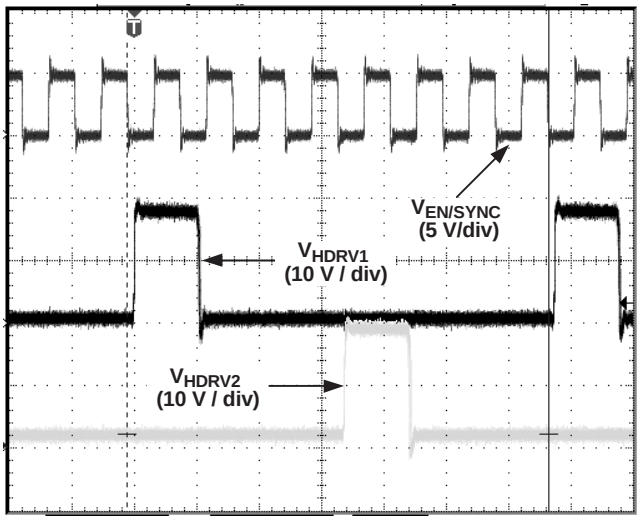


Figure 24. External Clock on EN/SYNC

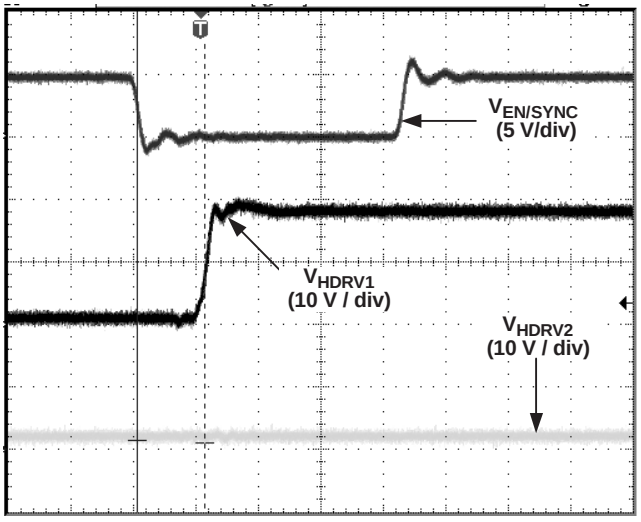


Figure 25. External Clock on EN/SYN and Delay to HDRV

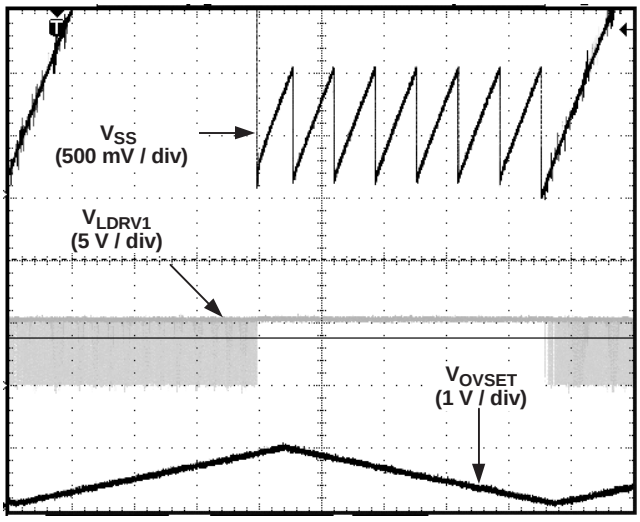


Figure 26. Overvoltage, Latch and Re-Start

TYPICAL CHARACTERISTICS (continued)

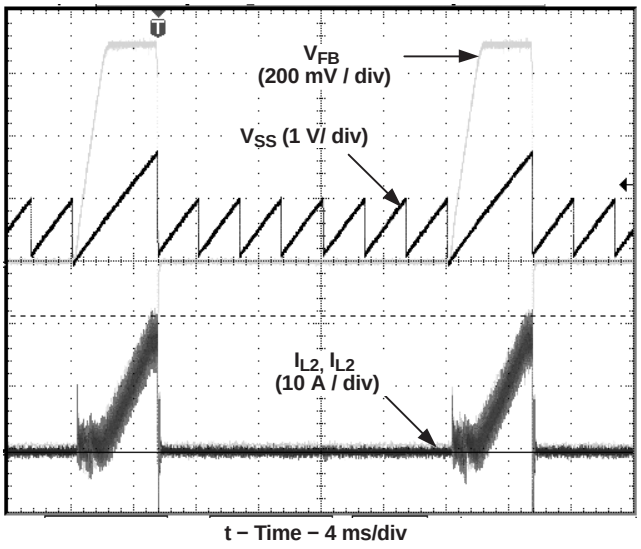


Figure 27. Overcurrent, Hiccup Mode

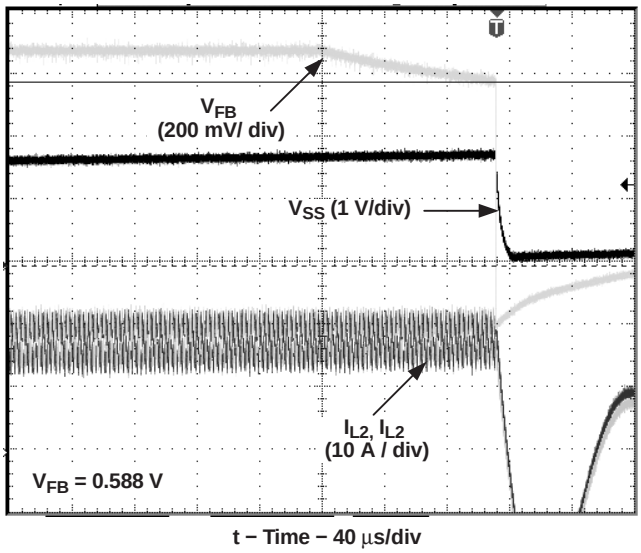


Figure 28. Overcurrent

LAYOUT CONSIDERATIONS

Introduction

Any pin number references are for the DBT, TSSOP package. There are two general classes of signals to consider for proper layout, high-current switching and low-level analog. Refer to Figure 13 for references to components. A printed wiring board (PWB) with a minimum of four layers should be used.

Two Ground Planes

A basic requirement is two separate ground planes that ultimately get connected together at a point where no switching currents are present, the power ground (PGND) and the analog ground (AGND). They should be implemented as split planes on the top and bottom layers. The PGND is used for all high-current signals including LDRV1, LDRV2, lower MOSFETs and input and output decoupling capacitors. PGND should be used on the top layer around the high current components and on the bottom layer as a minimum. The AGND is used for low level signals such as: soft-start, R_T, VREF, FB, BP5 decoupling to AGND. AGND should be used on the top layer around the device and low level components and on the bottom layer as a minimum. The signals which connect to the two different ground planes are shown in Figure 13 using different symbols for each ground.

Low-Level Signal Connections and Routing

Current Sense Signals

Using inductor current sense has advantages over using a low-value, high-power current-sense resistor, but attention must be paid to how the current sense signals are generated and routed.

Connection

Resistor R2 and capacitor C5 generate the current sense signal for phase 1 and resister R1 and capacitor C4 generate the current sense signal for phase 2. The R2-C5 and R1-C4 components must be connected directly to the pads for L1 and L2, respectively.

LAYOUT CONSIDERATIONS (continued)

Routing

The traces that connect to C5 and C4 should be made directly at the capacitor(s) and routed on an internal signal plane to CS1, CSRT1 and CS2, CSRT2, respectively. In addition, a small value of R-C filter may be used on the CSx and CSRTx lines, with these components placed close to the device. A 5.1-Ω resistor in series with the CSx and CSRTx lines and a 100-pF capacitor between the CSx and CSRTx lines, provides additional filtering, a prudent measure since the level of switching noise in a given layout is not fully known until the board is being tested for the first time.

Differential Amplifier Signals

The differential amplifier provides optimum regulation at the load point.

Connection

The signal connections for VOUT and GSNS should be made across the closest capacitor to the load point. This ensures the most accurate DC sensing and most noise free connection also.

Routing

Since the load point may be physically several inches, or more, from the device, it is very likely that the VOUT and GSNS inputs to the differential amplifier are corrupted by switching noise. The signals should be routed on an internal layer, and the R-C filter approach recommended for the CSx and CSRTx lines is applicable for these lines as well.

High-Current Connections and Routing

Device Decoupling for VIN5 and BP5

The 1.0-µF decoupling capacitor for VIN5 should be placed close to pins 1 and 30 of the device. The decoupling capacitor for BP5 should be placed close to pins 22 and 23 of the device.

Symmetry

Symmetry is especially important in the power processing components when considering the device placement between the two phases. Input ceramic decoupling capacitors should be placed close to the upper MOSFETs and the current path from the upper MOSFET drain to the lower MOSFET source should be on the PGND with maximum copper area. Output capacitors should be placed symmetrically between the output inductor and lower MOSFET for each phase.

SW Node

The SW node consists of the source of the upper MOSFET, the drain of the lower MOSFET,and the output inductor. These components should be placed to minimize the area of the SW node. The area of the SW node determines the amount of stray capacitance and inductance that causes ringing during switching transitions.

Lower MOSFET Gate Drive, LDRV1 and LDRV2

A resistor, with a value of between approximately 1.0 Ω and 2.2 Ω should be placed between LDRVx and the gate of the respective MOSFET. The resistors are necessary if the falling SW node pulls the gate voltage below GND. This can occur if the MOSFET Q_{GD} is larger than Q_{GS}. The traces for LDRVx should be wide, (0.05 to 0.1 inches) and routed on the top layer if possible. If routing must go to another layer, use multiple vias for interconnect. The return signal from the MOSFET drain to PGND on the device should be as wide as the return for LDRVx.

Upper MOSFET Gate Drive, HDRV1 and HDRV2

The traces for HDRVx and SWx should be wide, (0.05 to 0.1inches), and routed on the top layer if possible. If routing must go to another layer, use multiple vias for interconnect.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS40130DBT	NRND	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS40130	
TPS40130DBTR	NRND	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS40130	
TPS40130RHBR	NRND	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 40130	
TPS40130RHBT	NRND	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 40130	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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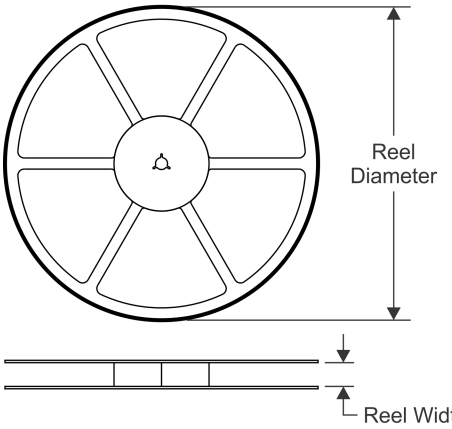
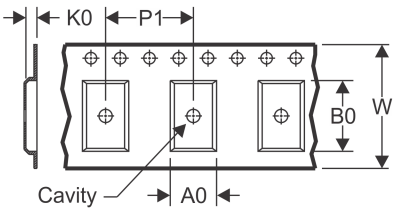
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

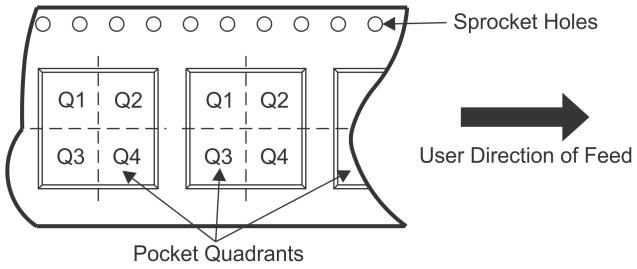


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

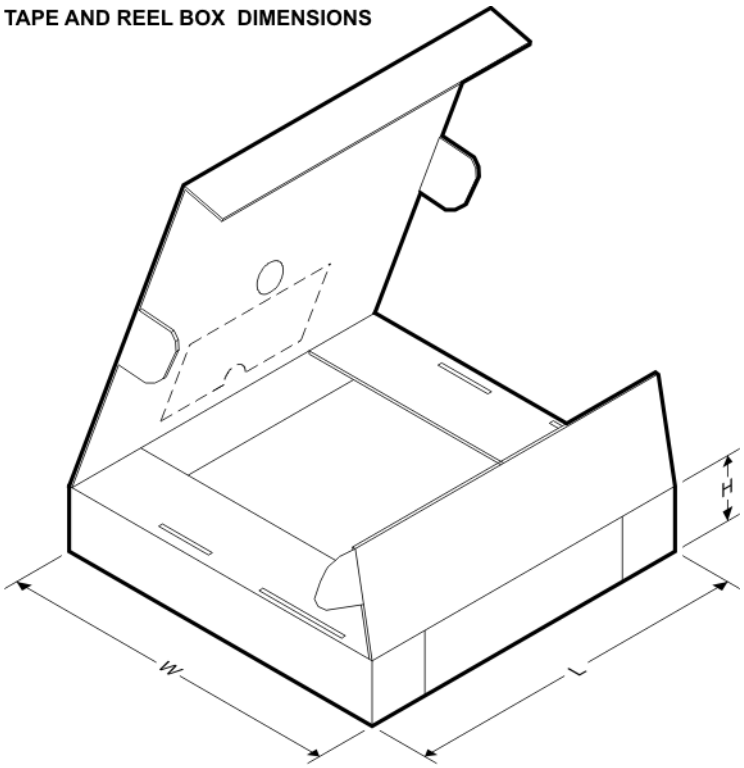
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40130DBTR	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TPS40130RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS40130RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

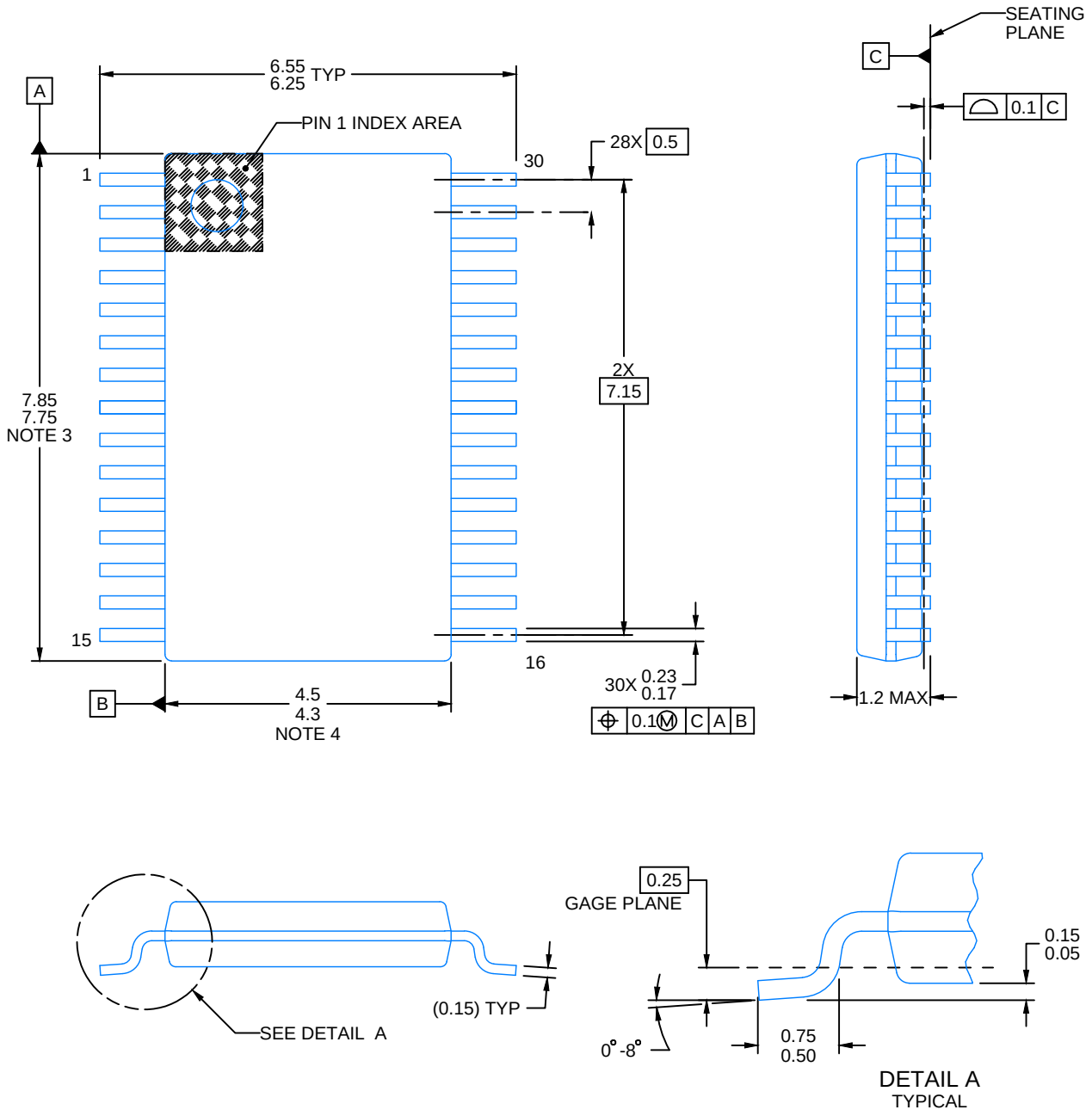
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40130DBTR	TSSOP	DBT	30	2000	367.0	367.0	38.0
TPS40130RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
TPS40130RHBT	VQFN	RHB	32	250	210.0	185.0	35.0

PACKAGE OUTLINE

DBT0030A

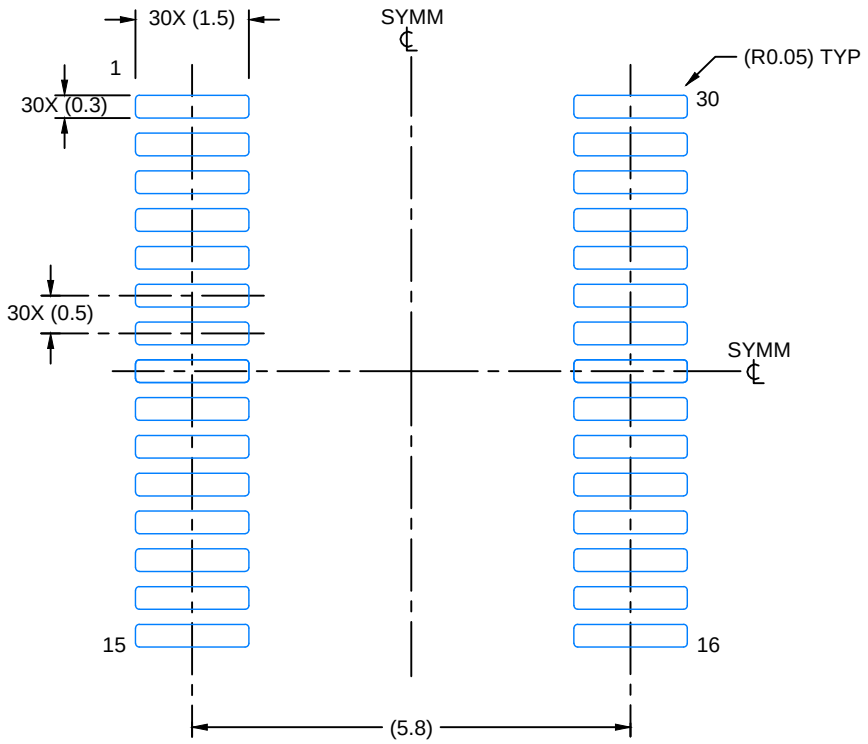
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

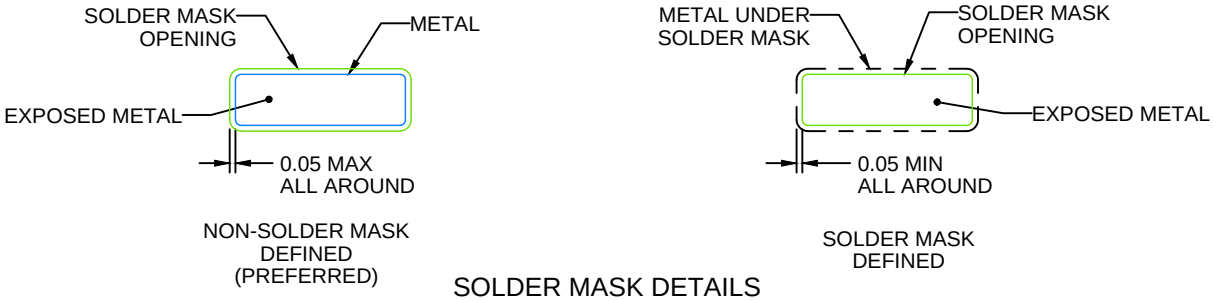


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

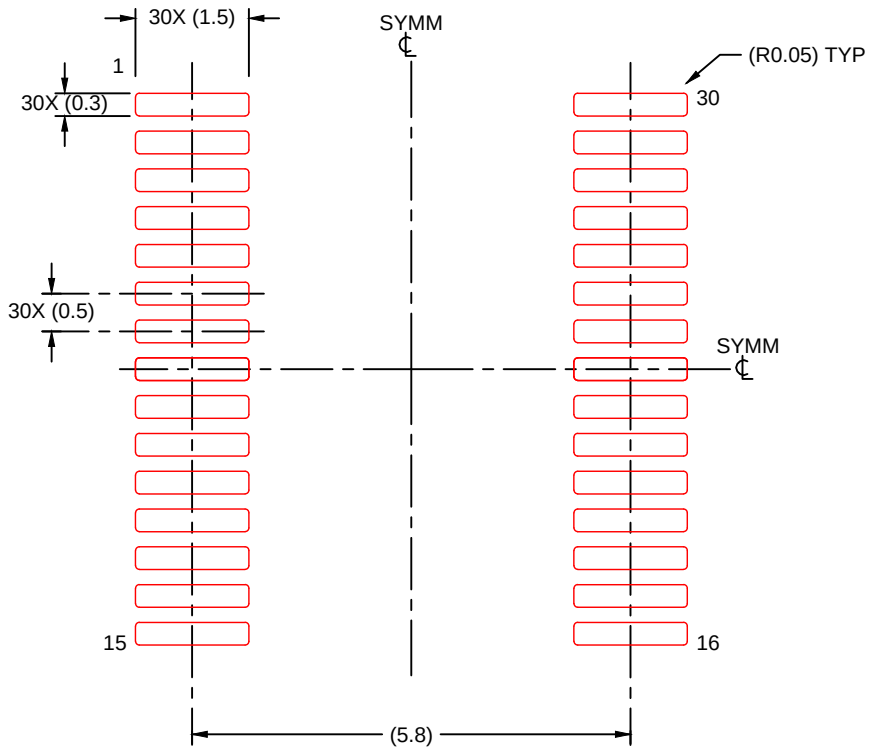


SOLDER MASK DETAILS

4220214/A 05/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220214/A 05/2020

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

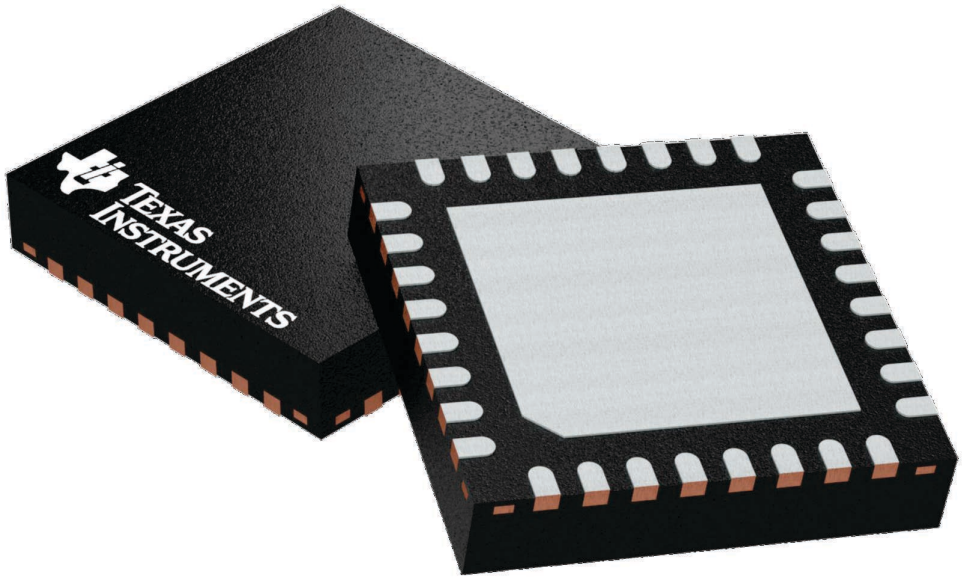
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

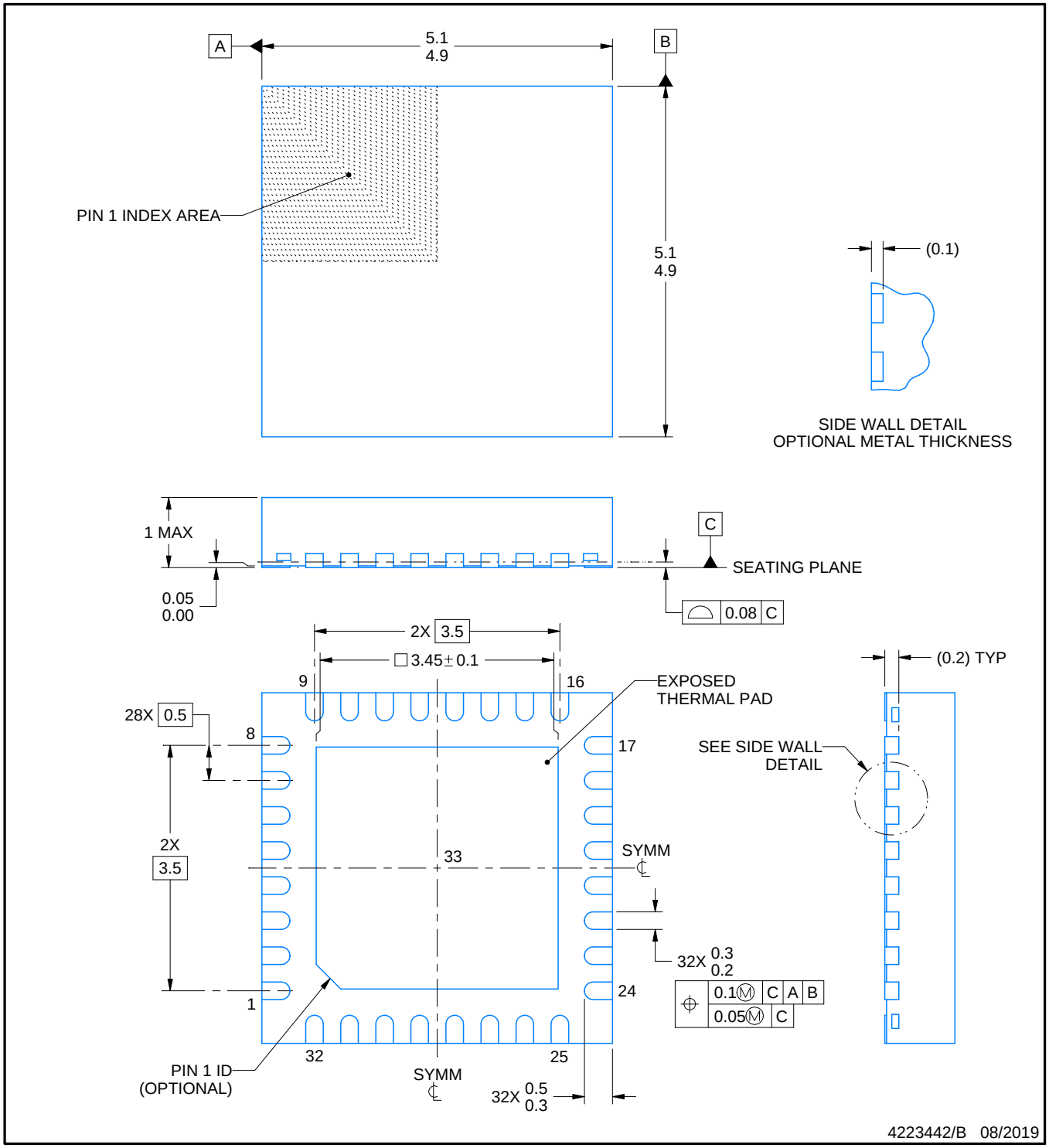
4224745/A

RHB0032E

PACKAGE OUTLINE

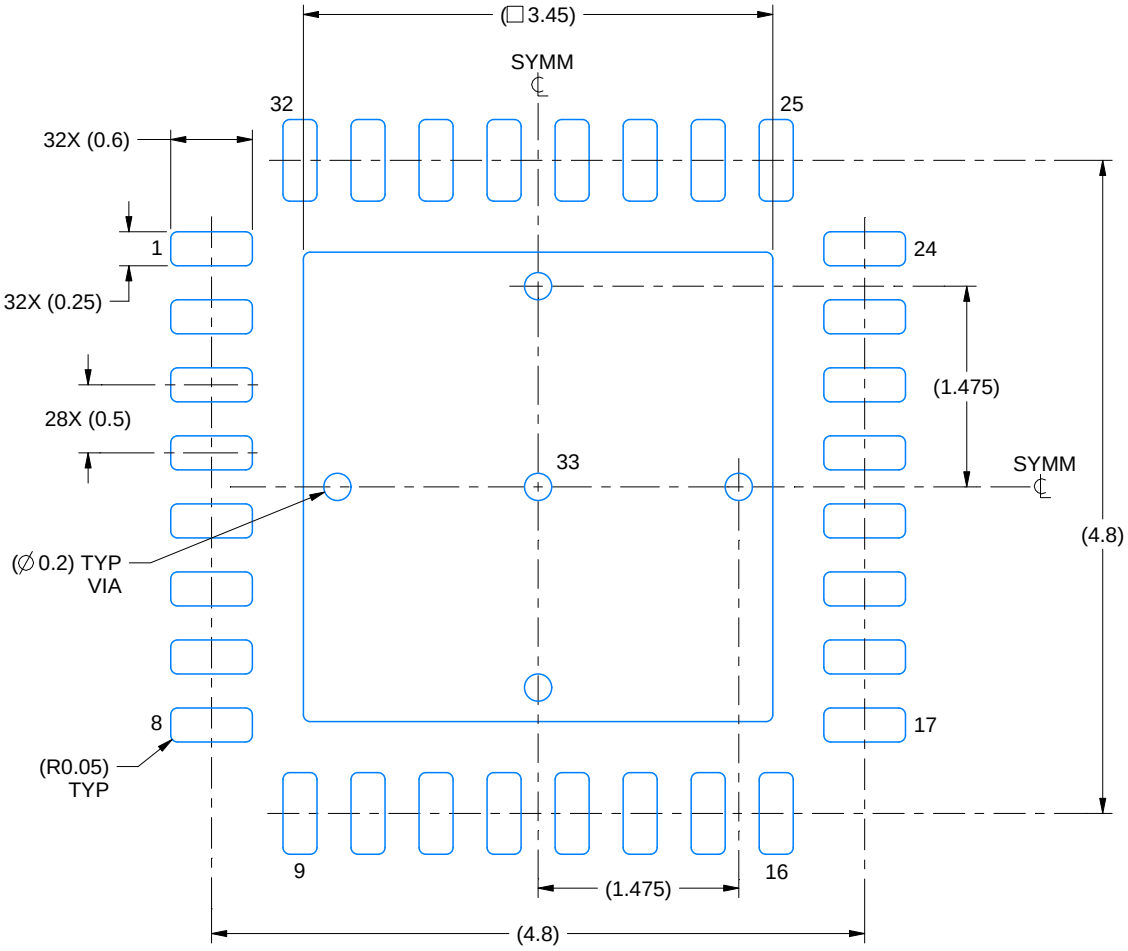
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

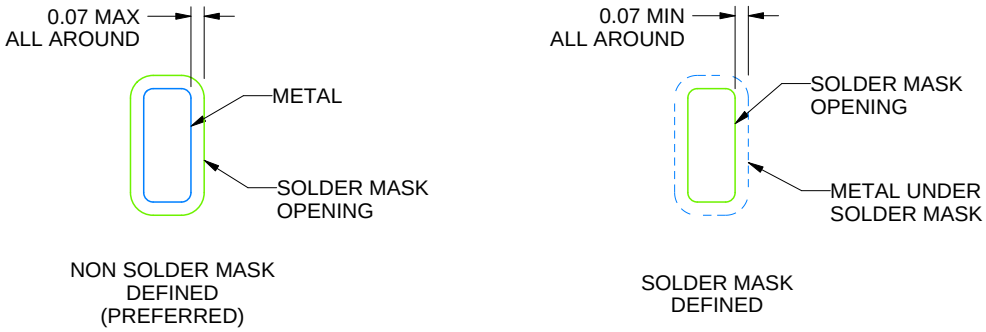


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

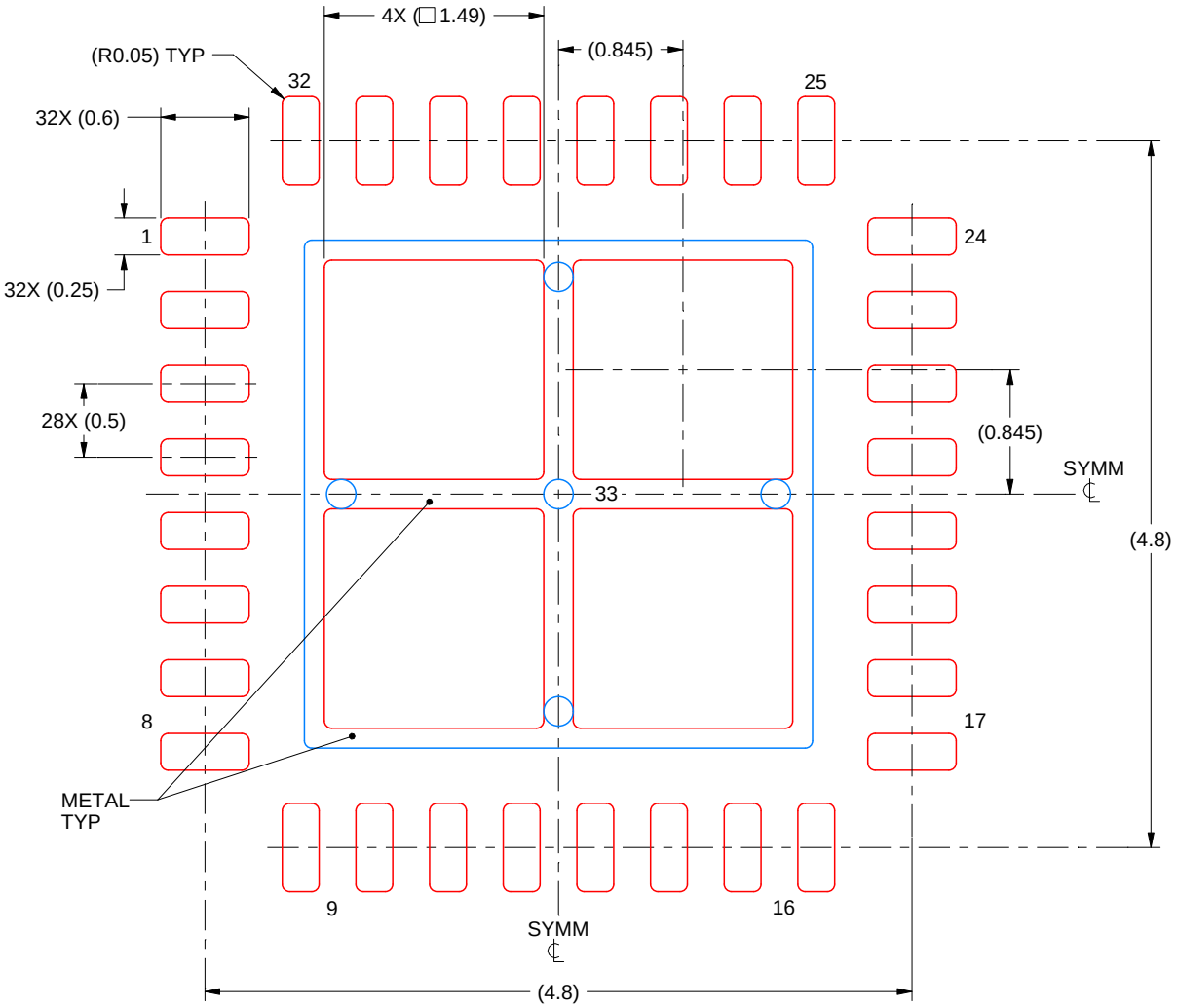


SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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