

# CC1352P SimpleLink™ High-Performance Multi-Band Wireless MCU With Integrated Power Amplifier

## 1 Device Overview

### 1.1 Features

- Microcontroller
  - Powerful 48-MHz Arm® Cortex®-M4F processor
  - EEMBC CoreMark® score: 148
  - 352KB of in-system Programmable Flash
  - 256KB of ROM for protocols and library functions
  - 8KB of Cache SRAM (Alternatively available as general-purpose RAM)
  - 80KB of ultra-low leakage SRAM. The SRAM is protected by parity to ensure high reliability of operation.
  - 2-Pin cJTAG and JTAG debugging
  - Supports Over-the-Air upgrade (OTA)
- Ultra-low power sensor controller with 4KB of SRAM
  - Sample, store, and process sensor data
  - Operation independent from system CPU
  - Fast wake-up for low-power operation
- TI-RTOS, drivers, Bootloader, *Bluetooth*® 5.1 Low Energy Controller, and IEEE 802.15.4 MAC in ROM for optimized application size
- RoHS-compliant package
  - 7-mm × 7-mm RGZ VQFN48 (26 GPIOs)
- Peripherals
  - Digital peripherals can be routed to any GPIO
  - 4× 32-bit or 8× 16-bit general-purpose timers
  - 12-Bit ADC, 200 kSamples/s, 8 channels
  - 2× comparators with internal reference DAC (1× continuous time, 1× ultra-low power)
  - Programmable current source
  - 2× UART
  - 2× SSI (SPI, MICROWIRE, TI)
  - I<sup>2</sup>C
  - I<sup>2</sup>S
  - Real-Time Clock (RTC)
  - AES 128- and 256-bit Crypto Accelerator
  - ECC and RSA Public Key Hardware Accelerator
  - SHA2 Accelerator (Full suite up to SHA-512)
  - True Random Number Generator (TRNG)
  - Capacitive sensing, up to 8 channels
  - Integrated temperature and battery monitor
- External system
  - On-chip Buck DC/DC converter
- Low power
  - Wide supply voltage range: 1.8 V to 3.8 V
  - Active-mode RX: 5.8 mA (3.6 V, 868 MHz), 6.9 mA (3.0 V, 2.4 GHz)
  - Active-Mode TX at +20 dBm: 63 mA (3.3 V, 915 MHz), 85 mA (3.0 V, 2.4 GHz)
  - Active-Mode TX at +10 dBm: 22 mA (2.4 GHz)
  - Active-Mode MCU 48 MHz (CoreMark): 2.9 mA (60 μA/MHz)
  - Sensor Controller, Low Power-Mode, 2 MHz, running infinite loop: 30.1 μA
  - Sensor Controller, Active-Mode, 24 MHz, running infinite loop: 808 μA
  - Standby: 0.85 μA (RTC on, 80KB RAM and CPU retention)
  - Shutdown: 150 nA (wakeup on external events)
- Radio section
  - Multi-band sub-1 GHz and 2.4 GHz RF transceiver compatible with Bluetooth 5.1 Low Energy and earlier LE specifications, and IEEE 802.15.4 PHY and MAC
  - Excellent receiver sensitivity:
    - 121 dBm for SimpleLink long-range mode
    - 110 dBm at 50 kbps, -105 dBm for Bluetooth 125-kbps (LE Coded PHY)
  - Output power up to +20 dBm with temperature compensation
  - Suitable for systems targeting compliance with worldwide radio frequency regulations
    - ETSI EN 300 220 Receiver Category 1.5 and 2, EN 300 328, EN 303 131, EN 303 204 (Europe)
    - EN 300 440 Category 2
    - FCC CFR47 Part 15
    - ARIB STD-T108 and STD-T66
  - Wide standard support
- Wireless protocols
  - [Thread](#), [Zigbee](#)®, [Bluetooth](#)® 5.1 Low Energy, IEEE 802.15.4g, IPv6-enabled smart objects (6LoWPAN), MIOTY®, Wireless M-Bus, Wi-SUN®, KNX RF, proprietary systems, SimpleLink™ TI 15.4-Stack (Sub-1 GHz), and Dynamic Multiprotocol Manager (DMM) driver.



- Development *Tools and Software*
  - [LAUNCHXL-CC1352P1](#) and [LAUNCHXL-CC1352P-2](#) Development Kits
  - [SimpleLink™ CC13x2 and CC26x2 Software](#)
- Development Kit (SDK)
  - [SmartRF™ Studio](#) for simple radio configuration
  - [Sensor Controller Studio](#) for building low-power sensing applications

## 1.2 Applications

- 433, 470 to 510, 868, 902 to 928, and 2400 to 2480 MHz ISM and SRD systems <sup>(1)</sup> with down to 4 kHz of receive bandwidth
- **Building automation**
  - Building security systems – [motion detector](#), [electronic smart lock](#), [door and window sensor](#), [garage door system](#), [gateway](#)
  - HVAC – [thermostat](#), [wireless environmental sensor](#), [HVAC system controller](#), [gateway](#)
  - Fire safety system – [smoke and heat detector](#), [fire alarm control panel \(FACP\)](#)
  - Video surveillance – [IP network camera](#)
  - Elevators and escalators – [elevator main control panel for elevators and escalators](#)
- **Grid infrastructure**
  - Smart meters – [water meter](#), [gas meter](#), [electricity meter](#), and [heat cost allocators](#)
  - Grid communications – [wireless communications](#) – Long-range sensor applications
  - Other alternative energy – [energy harvesting](#)
- **Industrial transport – asset tracking**
- **Factory automation and control**
- **Medical**
- **Electronic point of sale (EPOS) – Electronic Shelf Label (ESL)**
- **Communication equipment**
  - **Wired networking – wireless LAN or Wi-Fi access points, edge router**
- **Personal electronics**
  - **Portable electronics – RF smart remote control**
  - **Home theater & entertainment – smart speakers, smart display, set-top box**
  - **Connected peripherals – consumer wireless module, pointing devices, keyboards and keypads**
  - **Gaming – electronic and robotic toys**
  - **Wearables (non-medical) – smart trackers, smart clothing**

(1) See [RF Core](#) for additional details on supported protocol standards, modulation formats, and data rates.

## 1.3 Description

The SimpleLink™ CC1352P device is a multiprotocol and multi-band Sub-1 GHz and 2.4-GHz wireless microcontroller (MCU) supporting [Thread](#), [Zigbee®](#), [Bluetooth® 5.1 Low Energy](#), IEEE 802.15.4g, IPv6-enabled smart objects (6LoWPAN), MIOTY®, proprietary systems, including the TI 15.4-Stack (Sub-1 GHz and 2.4 GHz), and [concurrent multiprotocol](#) through a Dynamic Multiprotocol Manager (DMM) driver. The device is optimized for low-power wireless communication and advanced sensing in [building security systems](#), [HVAC](#), [smart meters](#), [medical](#), [wired networking](#), [portable electronics](#), [home theater & entertainment](#), and [connected peripherals](#) markets. The highlighted features of this device include:

- Multi-band device supporting concurrent multiprotocol for both Sub-1 GHz and 2.4 GHz through a DMM driver.
- Wide flexibility of protocol stack support in the [SimpleLink™ CC13x2 and CC26x2 Software Development Kit \(SDK\)](#).
- Enablement of long-range and low-power applications using the integrated +20 dBm high-power amplifier with best-in-class transmit current consumption at 63 mA for Sub-1 GHz and 85 mA for 2.4 GHz operation.
- Optimized for coin-cell operation at +10 dBm with 22 mA current consumption.
- Longer battery life wireless applications with low standby current of 0.85 µA and full RAM retention.
- Industrial temperature ready with lowest standby current of 5 µA at 85 °C.
- Advanced sensing with a programmable, autonomous ultra-low power [Sensor Controller CPU](#) with fast wake-up capability. As an example, the sensor controller is capable of 1-Hz ADC sampling at 1 µA system current.

- Low **SER (Soft Error Rate)** FIT (Failure-in-time) for long operation lifetime with no disruption for industrial markets with always-on SRAM parity against corruption due to potential radiation events.
- Dedicated software controlled radio controller (Arm® Cortex®-M0) providing flexible low-power RF transceiver capability to support multiple physical layers and RF standards.
- Excellent radio sensitivity (-121 dBm) and robustness (selectivity and blocking) performance for SimpleLink™ long-range mode.

The CC1352P device is part of the SimpleLink™ MCU platform, which consists of Wi-Fi®, Bluetooth Low Energy, Thread, Zigbee, Sub-1 GHz MCUs, and host MCUs that all share a common, easy-to-use development environment with a single core software development kit (SDK) and rich tool set. A one-time integration of the SimpleLink™ platform enables you to add any combination of the portfolio's devices into your design, allowing 100 percent code reuse when your design requirements change. For more information, visit [SimpleLink™ MCU platform](#).

#### Device Information<sup>(1)</sup>

| PART NUMBER   | PACKAGE   | BODY SIZE (NOM)   |
|---------------|-----------|-------------------|
| CC1352P1F3RGZ | VQFN (48) | 7.00 mm × 7.00 mm |

(1) For the most current part, package, and ordering information for all available devices, see the Package Option Addendum in [Section 9](#), or see the [TI website](#).

### 1.4 Functional Block Diagram

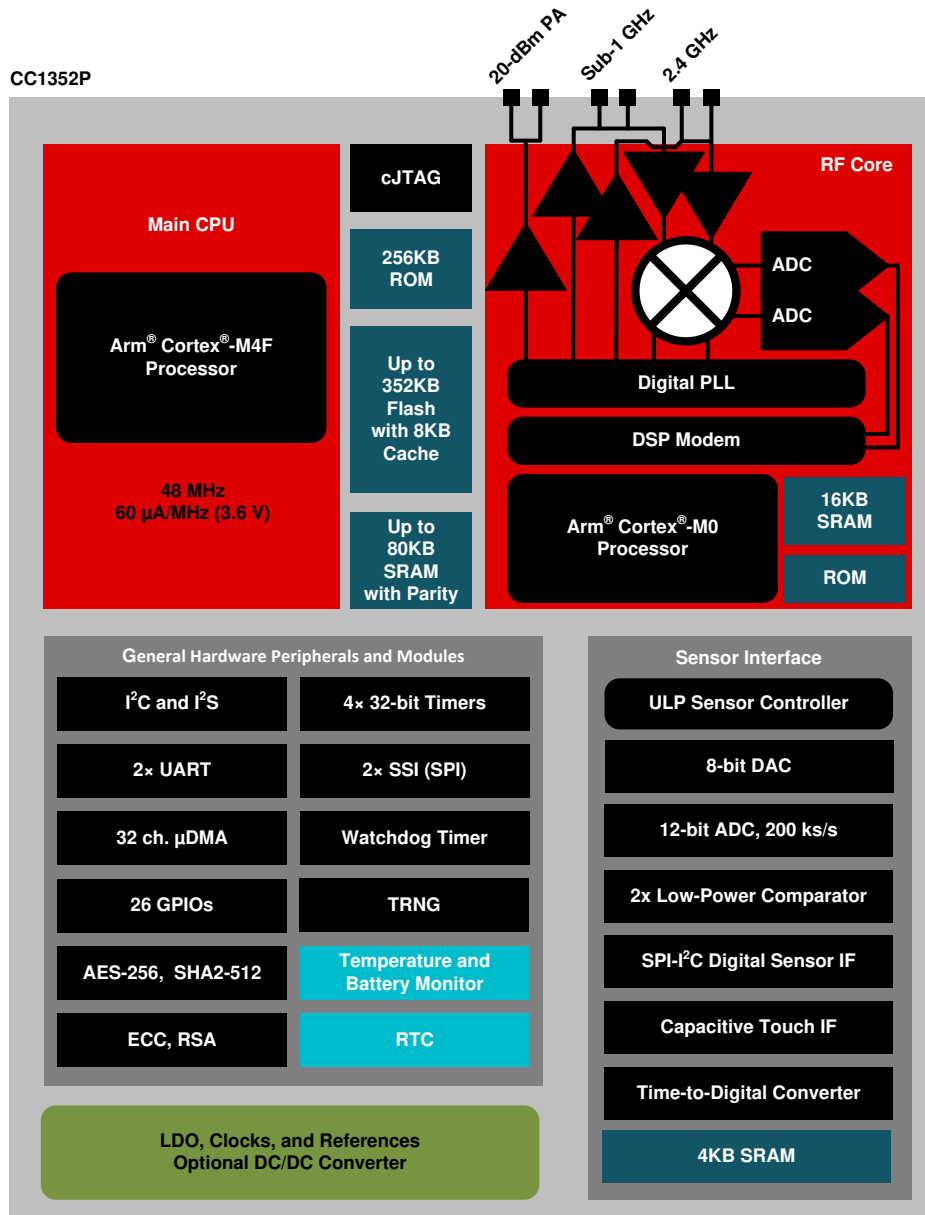


Figure 1-1. CC1352P Block Diagram

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## 2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (July 2019) to Revision D   | Page |
|---|------|
| • Changed Sensor Controller, Low Power-Mode current value in <a href="#">Section 1.1</a> .....  | 1    |
| • Added Wireless protocols to <a href="#">Section 1.1</a> .....   | 1    |
| • Changed <a href="#">Section 1.2</a> .....   | 2    |
| • Added Personal electronics to <a href="#">Section 1.2</a> .....   | 2    |
| • Changed <a href="#">Section 1.3</a> .....   | 2    |
| • Added CC2642R-Q1 to <a href="#">Table 3-1</a> .....   | 7    |
| • Added 359 MHz to 527 MHz - Receive (RX) table in <a href="#">Section 5</a> .....  | 19   |
| • Added 359 MHz to 527 MHz - Transmit (TX) table in <a href="#">Section 5</a> .....   | 19   |
| • Added 359 MHz to 527 MHz - PLL Phase Noise table in <a href="#">Section 5</a> .....   | 19   |
| • Changed TEST CONDITIONS for 2 Mbps Intermodulation in Bluetooth Low Energy - Receive (RX) table in <a href="#">Section 5.17</a> ..... | 23   |
| • Changed Motional inductance TYP value in 48 MHz Crystal Oscillator (XOSC_HF) table in <a href="#">Section 5.21.1</a> .....            | 31   |
| • Added performance numbers for 10 dBm configuration in <a href="#">Section 5.23</a> .....  | 42   |
| • Added <a href="#">Figure 5-17</a> .....   | 49   |

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|  |                    |
|--|--------------------|
| • Added <a href="#">Figure 5-22</a> .....                                    | <a href="#">52</a> |
| • Added <a href="#">Figure 5-35</a> .....                                    | <a href="#">60</a> |
| • Added <a href="#">Figure 5-41</a> .....                                    | <a href="#">63</a> |
| • Added <a href="#">Figure 5-47</a> .....                                    | <a href="#">66</a> |
| • Added <a href="#">Figure 5-54</a> .....                                    | <a href="#">70</a> |
| • Added LAUNCHXL-CC1352P-4 Design Files to <a href="#">Section 7.1</a> ..... | <a href="#">86</a> |

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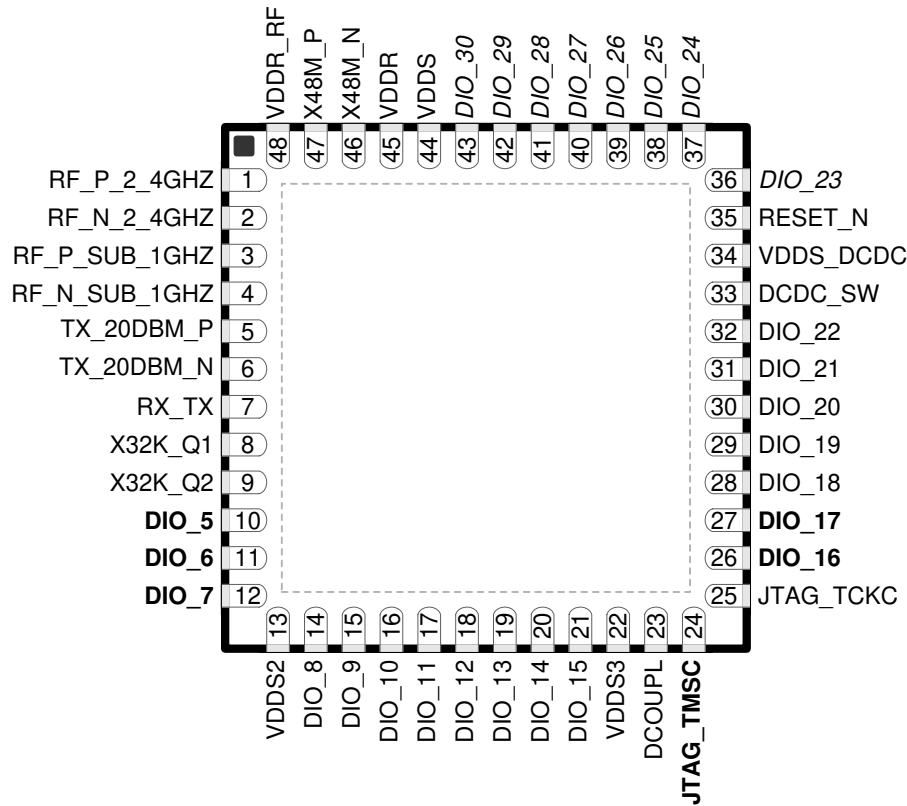
### 3 Device Comparison

**Table 3-1. Device Family Overview**

| DEVICE       | RADIO SUPPORT   | FLASH (KB) | RAM (KB) | GPIO  | PACKAGE SIZE  |
|--------------|---|------------|----------|-------|---|
| CC1312R      | Sub-1 GHz   | 352        | 80       | 30    | RGZ (7-mm × 7-mm VQFN48)  |
| CC1352P      | Multiprotocol<br>Sub-1 GHz<br>Bluetooth 5.1 Low Energy<br>Zigbee<br>Thread<br>2.4 GHz proprietary FSK-based formats<br>+20-dBm high-power amplifier | 352        | 80       | 26    | RGZ (7-mm × 7-mm VQFN48)  |
| CC1352R      | Multiprotocol<br>Sub-1 GHz<br>Bluetooth 5.1 Low Energy<br>Zigbee<br>Thread<br>2.4 GHz proprietary FSK-based formats                                 | 352        | 80       | 28    | RGZ (7-mm × 7-mm VQFN48)  |
| CC2642R      | Bluetooth 5.1 Low Energy<br>2.4 GHz proprietary FSK-based formats   | 352        | 80       | 31    | RGZ (7-mm × 7-mm VQFN48)  |
| CC2642R-Q1   | Bluetooth 5.1 Low Energy  | 352        | 80       | 31    | RTC (7-mm × 7-mm VQFN48)  |
| CC2652R      | Multiprotocol<br>Bluetooth 5.1 Low Energy<br>Zigbee<br>Thread<br>2.4 GHz proprietary FSK-based formats  | 352        | 80       | 31    | RGZ (7-mm × 7-mm VQFN48)  |
| CC2652RB     | Multiprotocol<br>Bluetooth 5.1 Low Energy<br>Zigbee<br>Thread<br>2.4 GHz proprietary FSK-based formats  | 352        | 80       | 31    | RGZ (7-mm × 7-mm VQFN48)  |
| CC2652P      | Multiprotocol<br>Bluetooth 5.1 Low Energy<br>Zigbee<br>Thread<br>2.4 GHz proprietary FSK-based formats<br>+19.5-dBm high-power amplifier            | 352        | 80       | 26    | RGZ (7-mm × 7-mm VQFN48)  |
| CC1310       | Sub-1 GHz   | 32–128     | 16–20    | 10–31 | RGZ (7-mm × 7-mm VQFN48)<br>RHB (5-mm × 5-mm VQFN32)<br>RSM (4-mm × 4-mm VQFN32)                                  |
| CC1350       | Sub-1 GHz<br>Bluetooth 4.2 Low Energy   | 128        | 20       | 10–31 | RGZ (7-mm × 7-mm VQFN48)<br>RHB (5-mm × 5-mm VQFN32)<br>RSM (4-mm × 4-mm VQFN32)                                  |
| CC2640R2F    | Bluetooth 5.1 Low Energy<br>2.4 GHz proprietary FSK-based formats   | 128        | 20       | 10–31 | RGZ (7-mm × 7-mm VQFN48)<br>RHB (5-mm × 5-mm VQFN32)<br>RSM (4-mm × 4-mm VQFN32)<br>YFV (2.7-mm × 2.7-mm DSBGA34) |
| CC2640R2F-Q1 | Bluetooth 5.1 Low Energy<br>2.4 GHz proprietary FSK-based formats   | 128        | 20       | 31    | RGZ (7-mm × 7-mm VQFN48)  |

## 4 Terminal Configuration and Functions

### 4.1 Pin Diagram – RGZ Package (Top View)



**Figure 4-1. RGZ (7-mm x 7-mm) Pinout, 0.5-mm Pitch (Top View)**

The following I/O pins marked in [Figure 4-1](#) in **bold** have high-drive capabilities:

- Pin 10, DIO\_5
- Pin 11, DIO\_6
- Pin 12, DIO\_7
- Pin 24, JTAG\_TMSC
- Pin 26, DIO\_16
- Pin 27, DIO\_17

The following I/O pins marked in [Figure 4-1](#) in *italics* have analog capabilities:

- Pin 36, DIO\_23
- Pin 37, DIO\_24
- Pin 38, DIO\_25
- Pin 39, DIO\_26
- Pin 40, DIO\_27
- Pin 41, DIO\_28
- Pin 42, DIO\_29
- Pin 43, DIO\_30



## 4.2 Signal Descriptions – RGZ Package

**Table 4-1. Signal Descriptions – RGZ Package**

| PIN           |     | I/O | TYPE              | DESCRIPTION  |
|---------------|-----|-----|-------------------|--|
| NAME          | NO. |     |                   |  |
| DCDC_SW       | 33  | —   | Power             | Output from internal DC/DC converter <sup>(1)</sup>  |
| DCOUP_L       | 23  | —   | Power             | For decoupling of internal 1.27 V regulated digital-supply <sup>(2)</sup>                                    |
| DIO_5         | 10  | I/O | Digital           | GPIO, high-drive capability  |
| DIO_6         | 11  | I/O | Digital           | GPIO, high-drive capability  |
| DIO_7         | 12  | I/O | Digital           | GPIO, high-drive capability  |
| DIO_8         | 14  | I/O | Digital           | GPIO   |
| DIO_9         | 15  | I/O | Digital           | GPIO   |
| DIO_10        | 16  | I/O | Digital           | GPIO   |
| DIO_11        | 17  | I/O | Digital           | GPIO   |
| DIO_12        | 18  | I/O | Digital           | GPIO   |
| DIO_13        | 19  | I/O | Digital           | GPIO   |
| DIO_14        | 20  | I/O | Digital           | GPIO   |
| DIO_15        | 21  | I/O | Digital           | GPIO   |
| DIO_16        | 26  | I/O | Digital           | GPIO, JTAG_TDO, high-drive capability  |
| DIO_17        | 27  | I/O | Digital           | GPIO, JTAG_TDI, high-drive capability  |
| DIO_18        | 28  | I/O | Digital           | GPIO   |
| DIO_19        | 29  | I/O | Digital           | GPIO   |
| DIO_20        | 30  | I/O | Digital           | GPIO   |
| DIO_21        | 31  | I/O | Digital           | GPIO   |
| DIO_22        | 32  | I/O | Digital           | GPIO   |
| DIO_23        | 36  | I/O | Digital or Analog | GPIO, analog capability  |
| DIO_24        | 37  | I/O | Digital or Analog | GPIO, analog capability  |
| DIO_25        | 38  | I/O | Digital or Analog | GPIO, analog capability  |
| DIO_26        | 39  | I/O | Digital or Analog | GPIO, analog capability  |
| DIO_27        | 40  | I/O | Digital or Analog | GPIO, analog capability  |
| DIO_28        | 41  | I/O | Digital or Analog | GPIO, analog capability  |
| DIO_29        | 42  | I/O | Digital or Analog | GPIO, analog capability  |
| DIO_30        | 43  | I/O | Digital or Analog | GPIO, analog capability  |
| EGP           | —   | —   | GND               | Ground – exposed ground pad <sup>(3)</sup>   |
| JTAG_TMSC     | 24  | I/O | Digital           | JTAG TMSC, high-drive capability   |
| JTAG_TCKC     | 25  | I   | Digital           | JTAG TCKC  |
| RESET_N       | 35  | I   | Digital           | Reset, active low. No internal pullup resistor   |
| RF_P_2_4GHZ   | 1   | —   | RF                | Positive 2.4-GHz RF input signal to LNA during RX<br>Positive 2.4-GHz RF output signal from PA during TX     |
| RF_N_2_4GHZ   | 2   | —   | RF                | Negative 2.4-GHz RF input signal to LNA during RX<br>Negative 2.4-GHz RF output signal from PA during TX     |
| RF_P_SUB_1GHZ | 3   | —   | RF                | Positive Sub-1 GHz RF input signal to LNA during RX<br>Positive Sub-1 GHz RF output signal from PA during TX |
| RF_N_SUB_1GHZ | 4   | —   | RF                | Negative Sub-1 GHz RF input signal to LNA during RX<br>Negative Sub-1 GHz RF output signal from PA during TX |
| RX_TX         | 7   | —   | RF                | Optional bias pin for the RF LNA   |
| TX_20DBM_P    | 5   | —   | RF                | Positive Sub-1 GHz or 2.4-GHz high-power TX signal   |
| TX_20DBM_N    | 6   | —   | RF                | Negative Sub-1 GHz or 2.4-GHz high-power TX signal   |

(1) For more details, see technical reference manual listed in [Section 8.3](#).

(2) Do not supply external circuitry from this pin.

(3) EGP is the only ground connection for the device. Good electrical connection to device ground on printed circuit board (PCB) is imperative for proper device operation.

**Table 4-1. Signal Descriptions – RGZ Package (continued)**

| PIN       |     | I/O | TYPE   | DESCRIPTION   |
|-----------|-----|-----|--------|---|
| NAME      | NO. |     |        |   |
| VDDR      | 45  | —   | Power  | Internal supply, must be powered from the internal DC/DC converter or the internal LDO <sup>(4)(2)(5)</sup> |
| VDDR_RF   | 48  | —   | Power  | Internal supply, must be powered from the internal DC/DC converter or the internal LDO <sup>(6)(2)(5)</sup> |
| VDDS      | 44  | —   | Power  | 1.8-V to 3.8-V main chip supply <sup>(1)</sup>  |
| VDDS2     | 13  | —   | Power  | 1.8-V to 3.8-V DIO supply <sup>(1)</sup>  |
| VDDS3     | 22  | —   | Power  | 1.8-V to 3.8-V DIO supply <sup>(1)</sup>  |
| VDDS_DCDC | 34  | —   | Power  | 1.8-V to 3.8-V DC/DC converter supply   |
| X48M_N    | 46  | —   | Analog | 48-MHz crystal oscillator pin 1   |
| X48M_P    | 47  | —   | Analog | 48-MHz crystal oscillator pin 2   |
| X32K_Q1   | 8   | —   | Analog | 32-kHz crystal oscillator pin 1   |
| X32K_Q2   | 9   | —   | Analog | 32-kHz crystal oscillator pin 2   |

(4) If internal DC/DC converter is not used, this pin is supplied internally from the main LDO.

(5) Output from internal DC/DC and LDO is trimmed to 1.68 V.

(6) If internal DC/DC converter is not used, this pin must be connected to VDDR for supply from the main LDO.

### 4.3 Connections for Unused Pins and Modules

**Table 4-2. Connections for Unused Pins**

| FUNCTION                       | SIGNAL NAME | PIN NUMBER              | ACCEPTABLE PRACTICE <sup>(1)</sup> | PREFERRED PRACTICE <sup>(1)</sup> |
|--------------------------------|-------------|-------------------------|------------------------------------|-----------------------------------|
| GPIO                           | DIO_n       | 10–12                   | NC or GND                          | NC                                |
|                                |             | 14–21<br>26–32<br>36–43 |                                    |                                   |
| 32.768-kHz crystal             | X32K_Q1     | 8                       | NC or GND                          | NC                                |
|                                | X32K_Q2     | 9                       |                                    |                                   |
| DC/DC converter <sup>(2)</sup> | DCDC_SW     | 33                      | NC                                 | NC                                |
|                                | VDDS_DCDC   | 34                      | VDDS                               | VDDS                              |

(1) NC = No connect

(2) When the DC/DC converter is not used, the inductor between DCDC\_SW and VDDR can be removed. VDDR and VDDR\_RF must still be connected and the 22 uF DCDC capacitor must be kept on the VDDR net.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

|                                 |   | MIN   | MAX                              | UNIT |
|---------------------------------|---|---|----------------------------------|------|
| V <sub>DDS</sub> <sup>(3)</sup> | Supply voltage  | -0.3  | 4.1                              | V    |
|                                 | Voltage on any digital pin <sup>(4)</sup>                               | -0.3  | V <sub>DDS</sub> + 0.3, max 4.1  | V    |
|                                 | Voltage on crystal oscillator pins, X32K_Q1, X32K_Q2, X48M_N and X48M_P | -0.3  | V <sub>DDR</sub> + 0.3, max 2.25 | V    |
| V <sub>in</sub>                 | Voltage on ADC input  | Voltage scaling enabled                                 | V <sub>DDS</sub>                 | V    |
|                                 |   | Voltage scaling disabled, internal reference            | 1.49                             |      |
|                                 |   | Voltage scaling disabled, V <sub>DDS</sub> as reference | V <sub>DDS</sub> / 2.9           |      |
|                                 | Input level, Sub-1 GHz RF pins  |   | 10                               | dBm  |
|                                 | Input level, 2.4 GHz RF pins  |   | 5                                | dBm  |
| T <sub>stg</sub>                | Storage temperature   | -40   | 150                              | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to ground, unless otherwise noted.
- (3) V<sub>DDS\_DCDC</sub>, V<sub>DDS2</sub> and V<sub>DDS3</sub> must be at the same potential as V<sub>DDS</sub>.
- (4) Including analog capable DIOs.

### 5.2 ESD Ratings

|                  |                         |  | VALUE    | UNIT  |   |
|------------------|-------------------------|--|----------|-------|---|
| V <sub>ESD</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS001 <sup>(1)</sup> | All pins | ±2000 | V |
|                  |                         | Charged device model (CDM), per JESD22-C101 <sup>(2)</sup>       | All pins | ±500  | V |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|  |  | MIN | MAX | UNIT  |
|--|--|-----|-----|-------|
| Operating ambient temperature                            |  | -40 | 85  | °C    |
| Operating supply voltage (V <sub>DDS</sub> )             |  | 1.8 | 3.8 | V     |
| Operating supply voltage (V <sub>DDS</sub> ), boost mode | V <sub>DDR</sub> = 1.95 V<br>+14 dBm RF output sub-1 GHz power amplifier | 2.1 | 3.8 | V     |
| Rising supply voltage slew rate                          |  | 0   | 100 | mV/μs |
| Falling supply voltage slew rate <sup>(1)</sup>          |  | 0   | 20  | mV/μs |

- (1) For small coin-cell batteries, with high worst-case end-of-life equivalent source resistance, a 22-μF V<sub>DDS</sub> input capacitor must be used to ensure compliance with this slew rate.

### 5.4 Power Supply and Modules

over operating free-air temperature range (unless otherwise noted)

| PARAMETER   |                   | TYP        | UNIT |
|---|-------------------|------------|------|
| V <sub>DDS</sub> Power-on-Reset (POR) threshold                               |                   | 1.1 - 1.55 | V    |
| V <sub>DDS</sub> Brown-out Detector (BOD) <sup>(1)</sup>                      | Rising threshold  | 1.77       | V    |
| V <sub>DDS</sub> Brown-out Detector (BOD), before initial boot <sup>(2)</sup> | Rising threshold  | 1.70       | V    |
| V <sub>DDS</sub> Brown-out Detector (BOD) <sup>(1)</sup>                      | Falling threshold | 1.75       | V    |

- (1) For boost mode (V<sub>DDR</sub> = 1.95 V), TI drivers software initialization will trim V<sub>DDS</sub> BOD limits to maximum (approximately 2.0 V)
- (2) Brown-out Detector is trimmed at initial boot, value is kept until device is reset by a POR reset or the RESET\_N pin

## 5.5 Power Consumption - Power Modes

When measured on the CC1352PEM-XD7793-XD24-PA9093 reference design with  $T_c = 25\text{ }^\circ\text{C}$ ,  $V_{DD5} = 3.6\text{ V}$  with DC/DC enabled unless otherwise noted.

| PARAMETER   |  | TEST CONDITIONS   | TYP   | UNIT          |
|---|--|---|-------|---------------|
| <b>Core Current Consumption</b>                         |  |   |       |               |
| $I_{core}$  | Reset and Shutdown                               | Reset. RESET_N pin asserted or VDD5 below power-on-reset threshold    | 150   | nA            |
|   |  | Shutdown. No clocks running, no retention                             | 150   |               |
|   | Standby without cache retention                  | RTC running, CPU, 80KB RAM and (partial) register retention. RCOSC_LF | 0.85  | $\mu\text{A}$ |
|   |  | RTC running, CPU, 80KB RAM and (partial) register retention. XOSC_LF  | 0.99  | $\mu\text{A}$ |
|   | Standby with cache retention                     | RTC running, CPU, 80KB RAM and (partial) register retention. RCOSC_LF | 2.78  | $\mu\text{A}$ |
|   |  | RTC running, CPU, 80KB RAM and (partial) register retention. XOSC_LF  | 2.92  | $\mu\text{A}$ |
|   | Idle   | Supply Systems and RAM powered. RCOSC_HF                              | 590   | $\mu\text{A}$ |
| Active  | MCU running CoreMark at 48 MHz. RCOSC_HF         | 2.89  | mA    |               |
| <b>Peripheral Current Consumption<sup>(1) (2)</sup></b> |  |   |       |               |
| $I_{peri}$  | Peripheral power domain                          | Delta current with domain enabled                                     | 82.3  | $\mu\text{A}$ |
|   | Serial power domain                              | Delta current with domain enabled                                     | 5.5   |               |
|   | RF Core  | Delta current with power domain enabled, clock enabled, RF core idle  | 178.9 |               |
|   | $\mu\text{DMA}$                                  | Delta current with clock enabled, module is idle                      | 53.6  |               |
|   | Timers   | Delta current with clock enabled, module is idle <sup>(3)</sup>       | 67.8  |               |
|   | I2C  | Delta current with clock enabled, module is idle                      | 8.2   |               |
|   | I2S  | Delta current with clock enabled, module is idle                      | 21.7  |               |
|   | SSI  | Delta current with clock enabled, module is idle <sup>(4)</sup>       | 69.4  |               |
|   | UART   | Delta current with clock enabled, module is idle <sup>(5)</sup>       | 140.8 |               |
|   | CRYPTO (AES)                                     | Delta current with clock enabled, module is idle                      | 21.1  |               |
|   | PKA  | Delta current with clock enabled, module is idle                      | 71.1  |               |
| TRNG  | Delta current with clock enabled, module is idle | 29.7  |       |               |
| <b>Sensor Controller Engine Consumption</b>             |  |   |       |               |
| $I_{SCE}$   | Active mode                                      | 24 MHz, infinite loop, $V_{DD5} = 3.0\text{ V}$                       | 808.5 | $\mu\text{A}$ |
|   | Low-power mode                                   | 2 MHz, infinite loop, $V_{DD5} = 3.0\text{ V}$                        | 30.1  |               |

(1) Adds to core current  $I_{core}$  for each peripheral unit activated.

(2)  $I_{peri}$  is not supported in Standby or Shutdown modes.

(3) Only one GPTimer running

(4) Only one SSI running

(5) Only one UART running

## 5.6 Power Consumption - Radio Modes

When measured on the CC1352PEM-XD7793-XD24-PA9093 reference design with  $T_c = 25\text{ }^\circ\text{C}$ ,  $V_{DD5} = 3.6\text{ V}$  with DC/DC enabled unless otherwise noted.

High power PA connected to  $V_{DD5}$  unless otherwise noted.

Using boost mode (increasing VDDR up to 1.95 V), will increase system current by 15% (does not apply to TX +14 dBm setting where this current is already included).

Relevant  $I_{core}$  and  $I_{peri}$  currents are included in below numbers.

| PARAMETER  | TEST CONDITIONS   | TYP  | UNIT |
|--|---|------|------|
| Radio receive current, 868 MHz   |   | 5.8  | mA   |
| Radio receive current, 2.44 GHz (BLE)  | $V_{DD5} = 3.0\text{ V}$  | 6.9  | mA   |
| Radio transmit current<br>Sub-1 GHz PA                                       | 0 dBm output power setting<br>868 MHz   | 8.0  | mA   |
|  | +10 dBm output power setting<br>868 MHz   | 14.3 | mA   |
| Radio transmit current<br>Boost mode, Sub-1 GHz PA                           | +14 dBm output power setting<br>868 MHz   | 24.9 | mA   |
| Radio transmit current<br>2.4 GHz PA (BLE)                                   | 0 dBm output power setting, $V_{DD5} = 3.0\text{ V}$                                    | 7.1  | mA   |
|  | +5 dBm output power setting<br>2440 MHz, $V_{DD5} = 3.0\text{ V}$                       | 9.6  | mA   |
| Radio transmit current<br>High-power PA                                      | Transmit (TX), +20 dBm output power setting<br>915 MHz, $V_{DD5} = 3.3\text{ V}$        | 63   | mA   |
| Radio transmit current<br>High-power PA <sup>(1)</sup>                       | Transmit (TX), +20 dBm output power setting<br>2440 MHz (BLE), $V_{DD5} = 3.0\text{ V}$ | 85   | mA   |
| Radio transmit current<br>High-power PA, 10 dBm configuration <sup>(2)</sup> | Transmit (TX), +10 dBm output power setting<br>2440 MHz (BLE), $V_{DD5} = 3.0\text{ V}$ | 22   | mA   |

(1) Measured on the CC1352PEM-XD7793-XD24-PA24 reference design.

(2) Measured on evaluation board as described in <https://www.ti.com/lit/pdf/swra636>.

## 5.7 Nonvolatile (Flash) Memory Characteristics

Over operating free-air temperature range and  $V_{DD5} = 3.0\text{ V}$  (unless otherwise noted)

| PARAMETER   | TEST CONDITIONS                          | MIN  | TYP  | MAX | UNIT             |
|---|--|------|------|-----|------------------|
| Flash sector size   |  |      | 8    |     | KB               |
| Supported flash erase cycles before failure, full bank <sup>(1)(2)</sup>      |  | 30   |      |     | k Cycles         |
| Supported flash erase cycles before failure, single sector <sup>(3)</sup>     |  | 60   |      |     | k Cycles         |
| Maximum number of write operations per row before sector erase <sup>(4)</sup> |  |      |      | 83  | Write Operations |
| Flash retention   | 105 °C                                   | 11.4 |      |     | Years at 105 °C  |
| Flash sector erase current  | Average delta current                    |      | 10.7 |     | mA               |
| Flash sector erase time <sup>(5)</sup>  |  |      | 10   |     | ms               |
| Flash write current   | Average delta current, 4 bytes at a time |      | 6.2  |     | mA               |
| Flash write time <sup>(5)</sup>   | 4 bytes at a time                        |      | 21.6 |     | µs               |

(1) A full bank erase is counted as a single erase cycle on each sector

(2) Aborting flash during erase or program modes is not a safe operation.

(3) Up to 4 customer-designated sectors can be individually erased an additional 30k times beyond the baseline bank limitation of 30k cycles

(4) Each wordline is 2048 bits (or 256 bytes) wide. This limitation corresponds to sequential memory writes of 4 (3.1) bytes minimum per write over a whole wordline. If additional writes to the same wordline are required, a sector erase is required once the maximum number of write operations per row is reached.

(5) This number is dependent on Flash aging and increases over time and erase cycles

## 5.8 Thermal Resistance Characteristics

| THERMAL METRIC <sup>(1)</sup> |  | PACKAGE       | UNIT                              |
|-------------------------------|--|---------------|-----------------------------------|
|                               |  | RGZ<br>(VQFN) |                                   |
|                               |  | 48 PINS       |                                   |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 23.4          | $^{\circ}\text{C}/\text{W}^{(2)}$ |
| $R_{\theta JC(\text{top})}$   | Junction-to-case (top) thermal resistance    | 13.3          | $^{\circ}\text{C}/\text{W}^{(2)}$ |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 8.0           | $^{\circ}\text{C}/\text{W}^{(2)}$ |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 0.1           | $^{\circ}\text{C}/\text{W}^{(2)}$ |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 7.9           | $^{\circ}\text{C}/\text{W}^{(2)}$ |
| $R_{\theta JC(\text{bot})}$   | Junction-to-case (bottom) thermal resistance | 1.7           | $^{\circ}\text{C}/\text{W}^{(2)}$ |

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

(2)  $^{\circ}\text{C}/\text{W}$  = degrees Celsius per watt.

## 5.9 RF Frequency Bands

Over operating free-air temperature range (unless otherwise noted).

| PARAMETER       | MIN  | TYP | MAX  | UNIT |
|-----------------|------|-----|------|------|
| Frequency bands | 2360 |     | 2500 | MHz  |
|                 | 1076 |     | 1315 |      |
|                 | 861  |     | 1054 |      |
|                 | 431  |     | 527  |      |
|                 | 359  |     | 439  |      |
|                 | 287  |     | 351  |      |

## 5.10 861 MHz to 1054 MHz - Receive (RX)

Measured on the CC1352PEM-XD7793-XD24-PA9093 reference design with  $T_c = 25\text{ }^\circ\text{C}$ ,  $V_{DD5} = 3.6\text{ V}$  with DC/DC enabled and high power PA connected to  $V_{DD5}$  unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER  | TEST CONDITIONS  | MIN | TYP     | MAX  | UNIT |
|--|--|-----|---------|------|------|
| <b>General Parameters</b>  |  |     |         |      |      |
| Digital channel filter programmable receive bandwidth  |  | 4   |         | 4000 | kHz  |
| Data rate step size  |  |     | 1.5     |      | bps  |
| Spurious emissions 25 MHz to 1 GHz   | 868 MHz  |     | < -57   |      | dBm  |
| Spurious emissions 1 GHz to 13 GHz   | Conducted emissions measured according to ETSI EN 300 220          |     | < -47   |      | dBm  |
| <b>802.15.4g Mandatory Mode (50 kbps, 2-GFSK, 100 kHz RX Bandwidth)</b>  |  |     |         |      |      |
| Sensitivity  | BER = $10^{-2}$ , 868 MHz  |     | -110    |      | dBm  |
| Saturation limit   | BER = $10^{-2}$  |     | 10      |      | dBm  |
| Selectivity, $\pm 200\text{ kHz}$  | BER = $10^{-2}$ , 868 MHz <sup>(1)</sup>                           |     | 44      |      | dB   |
| Selectivity, $\pm 400\text{ kHz}$  | BER = $10^{-2}$ , 868 MHz <sup>(1)</sup>                           |     | 48      |      | dB   |
| Blocking, $\pm 1\text{ MHz}$   | BER = $10^{-2}$ , 868 MHz <sup>(1)</sup>                           |     | 57      |      | dB   |
| Blocking, $\pm 2\text{ MHz}$   | BER = $10^{-2}$ , 868 MHz <sup>(1)</sup>                           |     | 61      |      | dB   |
| Blocking, $\pm 5\text{ MHz}$   | BER = $10^{-2}$ , 868 MHz <sup>(1)</sup>                           |     | 67      |      | dB   |
| Blocking, $\pm 10\text{ MHz}$  | BER = $10^{-2}$ , 868 MHz <sup>(1)</sup>                           |     | 76      |      | dB   |
| Image rejection (image compensation enabled)   | BER = $10^{-2}$ , 868 MHz <sup>(1)</sup>                           |     | 39      |      | dB   |
| RSSI dynamic range   | Starting from the sensitivity limit                                |     | 95      |      | dB   |
| RSSI accuracy  | Starting from the sensitivity limit across the given dynamic range |     | $\pm 3$ |      | dB   |
| <b>SimpleLink™ Long Range 2.5 kbps or 5 kbps (20 ksymbols/s, 2-GFSK, 5 kHz Deviation, FEC (Half Rate), DSSS = 1:2 or 1:4, 34 kHz RX Bandwidth)</b> |  |     |         |      |      |
| Sensitivity  | 2.5 kbps, BER = $10^{-2}$ , 868 MHz                                |     | -121    |      | dBm  |
| Sensitivity  | 5 kbps, BER = $10^{-2}$ , 868 MHz                                  |     | -120    |      | dBm  |
| Saturation limit   | 2.5 kbps, BER = $10^{-2}$ , 868 MHz                                |     | 10      |      | dBm  |
| Selectivity, $\pm 100\text{ kHz}$  | 2.5 kbps, BER = $10^{-2}$ , 868 MHz <sup>(1)</sup>                 |     | 49      |      | dB   |
| Selectivity, $\pm 200\text{ kHz}$  | 2.5 kbps, BER = $10^{-2}$ , 868 MHz <sup>(1)</sup>                 |     | 50      |      | dB   |
| Selectivity, $\pm 300\text{ kHz}$  | 2.5 kbps, BER = $10^{-2}$ , 868 MHz <sup>(1)</sup>                 |     | 51      |      | dB   |
| Blocking, $\pm 1\text{ MHz}$   | 2.5 kbps, BER = $10^{-2}$ , 868 MHz <sup>(1)</sup>                 |     | 63      |      | dB   |
| Blocking, $\pm 2\text{ MHz}$   | 2.5 kbps, BER = $10^{-2}$ , 868 MHz <sup>(1)</sup>                 |     | 68      |      | dB   |
| Blocking, $\pm 5\text{ MHz}$   | 2.5 kbps, BER = $10^{-2}$ , 868 MHz <sup>(1)</sup>                 |     | 78      |      | dB   |
| Blocking, $\pm 10\text{ MHz}$  | 2.5 kbps, BER = $10^{-2}$ , 868 MHz <sup>(1)</sup>                 |     | 88      |      | dB   |
| Image rejection (image compensation enabled)   | 2.5 kbps, BER = $10^{-2}$ , 868 MHz <sup>(1)</sup>                 |     | 45      |      | dB   |
| RSSI dynamic range   | Starting from the sensitivity limit                                |     | 97      |      | dB   |
| RSSI accuracy  | Starting from the sensitivity limit across the given dynamic range |     | $\pm 3$ |      | dB   |

(1) Wanted signal 3 dB above usable sensitivity limit according to ETSI EN 300 220 v. 3.1.1.

## 5.11 861 MHz to 1054 MHz - Transmit (TX)

Measured on the CC1352PEM-XD7793-XD24-PA9093 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DD5}} = 3.6\text{ V}$  with DC/DC enabled and high power PA connected to  $V_{\text{DD5}}$  unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted. <sup>(1)</sup>

| PARAMETER   |  | TEST CONDITIONS   | MIN | TYP   | MAX | UNIT |
|---|--|---|-----|-------|-----|------|
| <b>General parameters</b>   |  |   |     |       |     |      |
| Max output power, boost mode<br>Sub-1 GHz PA <sup>(2)</sup>                         |  | VDDR = 1.95 V<br>Minimum supply voltage (VDDS) for boost mode is 2.1 V<br>868 MHz and 915 MHz |     | 14    |     | dBm  |
| Max output power,<br>Sub-1 GHz PA <sup>(2)</sup>                                    |  | 868 MHz and 915 MHz   |     | 12    |     | dBm  |
| Max output power,<br>High power PA  |  | 915 MHz<br>VDDS = 3.3V  |     | 20    |     | dBm  |
| Output power programmable range<br>Sub-1 GHz PA                                     |  | 868 MHz and 915 MHz   |     | 24    |     | dB   |
| Output power programmable range<br>High power PA                                    |  | 868 MHz and 915 MHz<br>VDDS = 3.3V  |     | 6     |     | dB   |
| Output power variation over temperature<br>Sub-1 GHz PA                             |  | +10 dBm setting<br>Over recommended temperature operating range                               |     | ±2    |     | dB   |
| Output power variation over temperature<br>Boost mode, Sub-1 GHz PA                 |  | +14 dBm setting<br>Over recommended temperature operating range                               |     | ±1.5  |     | dB   |
| <b>Spurious emissions and harmonics</b>   |  |   |     |       |     |      |
| Spurious emissions<br>(excluding harmonics)<br>Sub-1 GHz PA, 868 MHz <sup>(3)</sup> | 30 MHz to 1 GHz  | +14 dBm setting<br>ETSI restricted bands  |     | < -54 |     | dBm  |
|   |  | +14 dBm setting<br>ETSI outside restricted bands  |     | < -36 |     | dBm  |
|   | 1 GHz to 12.75 GHz<br>(outside ETSI restricted bands)                    | +14 dBm setting<br>measured in 1 MHz bandwidth (ETSI)   |     | < -30 |     | dBm  |
| Spurious emissions out-of-band<br>Sub-1 GHz PA, 915 MHz <sup>(3)</sup>              | 30 MHz to 88 MHz<br>(within FCC restricted bands)                        | +14 dBm setting   |     | < -56 |     | dBm  |
|   | 88 MHz to 216 MHz<br>(within FCC restricted bands)                       | +14 dBm setting   |     | < -52 |     | dBm  |
|   | 216 MHz to 960 MHz<br>(within FCC restricted bands)                      | +14 dBm setting   |     | < -50 |     | dBm  |
|   | 960 MHz to 2390 MHz and above<br>2483.5 MHz (within FCC restricted band) | +14 dBm setting   |     | < -42 |     | dBm  |
|   | 1 GHz to 12.75 GHz<br>(outside FCC restricted bands)                     | +14 dBm setting   |     | < -40 |     | dBm  |

- (1) Some combinations of frequency, data rate and modulation format requires use of external crystal load capacitors for regulatory compliance. More details can be found in the device errata.
- (2) Output power is dependent on RF match. For dual-band devices in the CC13X2 platform, output power might be slightly reduced depending on RF layout trade-offs.
- (3) Suitable for systems targeting compliance with EN 300 220, EN 303 131, EN 303 204, FCC CFR47 Part 15, ARIB STD-T108.



## 861 MHz to 1054 MHz - Transmit (TX) (continued)

Measured on the CC1352PEM-XD7793-XD24-PA9093 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.6\text{ V}$  with

DC/DC enabled and high power PA connected to  $V_{\text{DDS}}$  unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted. <sup>(1)</sup>

| PARAMETER  |   | TEST CONDITIONS  | MIN  | TYP   | MAX   | UNIT |     |
|--|---|--|--|-------|-------|------|-----|
| Spurious emissions out-of-band<br>High power PA, 915 MHz <sup>(3)(4)</sup>   | 30 MHz to 88 MHz (within FCC restricted bands)                        | +20 dBm setting, $V_{\text{DDS}} = 3.3\text{ V}$           |  | < -55 |       | dBm  |     |
|  | 88 MHz to 216 MHz (within FCC restricted bands)                       | +20 dBm setting, $V_{\text{DDS}} = 3.3\text{ V}$           |  | < -52 |       | dBm  |     |
|  | 216 MHz to 960 MHz (within FCC restricted bands)                      | +20 dBm setting, $V_{\text{DDS}} = 3.3\text{ V}$           |  | < -49 |       | dBm  |     |
|  | 960 MHz to 2390 MHz and above 2483.5 MHz (within FCC restricted band) | +20 dBm setting, $V_{\text{DDS}} = 3.3\text{ V}$           |  | < -41 |       | dBm  |     |
|  | 1 GHz to 12.75 GHz (outside FCC restricted bands)                     | +20 dBm setting, $V_{\text{DDS}} = 3.3\text{ V}$           |  | < -20 |       | dBm  |     |
| Spurious emissions out-of-band<br>Sub-1 GHz PA, 920.6/928 MHz <sup>(3)</sup> | Below 710 MHz (ARIB T-108)  | +14 dBm setting  |  | < -36 |       | dBm  |     |
|  | 710 MHz to 900 MHz (ARIB T-108)                                       | +14 dBm setting  |  | < -55 |       | dBm  |     |
|  | 900 MHz to 915 MHz (ARIB T-108)                                       | +14 dBm setting  |  | < -55 |       | dBm  |     |
|  | 930 MHz to 1000 MHz (ARIB T-108)                                      | +14 dBm setting  |  | < -55 |       | dBm  |     |
|  | 1000 MHz to 1215 MHz (ARIB T-108)                                     | +14 dBm setting  |  | < -45 |       | dBm  |     |
| Above 1215 MHz (ARIB T-108)  | +14 dBm setting   |  | < -30  |       | dBm   |      |     |
| Harmonics<br>Sub-1 GHz PA  | Second harmonic   | +14 dBm setting, 868 MHz                                   |  | < -30 |       | dBm  |     |
|  |   | +14 dBm setting, 915 MHz                                   |  | < -30 |       |      |     |
|  | Third harmonic  | +14 dBm setting, 868 MHz                                   |  | < -30 |       | dBm  |     |
|  |   | +14 dBm setting, 915 MHz                                   |  | < -42 |       |      |     |
|  | Fourth harmonic   | +14 dBm setting, 868 MHz                                   |  | < -30 |       | dBm  |     |
|  |   | +14 dBm setting, 915 MHz                                   |  | < -30 |       |      |     |
|  | Fifth harmonic  | +14 dBm setting, 868 MHz                                   |  | < -30 |       | dBm  |     |
|  |   | +14 dBm setting, 915 MHz                                   |  | < -42 |       |      |     |
|  | Harmonics<br>High power PA  | Second harmonic  | +20 dBm setting, $V_{\text{DDS}} = 3.3\text{ V}$ , 915 MHz |       | < -30 |      | dBm |
|  |   | Third harmonic   | +20 dBm setting, $V_{\text{DDS}} = 3.3\text{ V}$ , 915 MHz |       | < -42 |      | dBm |
| Fourth harmonic  |   | +20 dBm setting, $V_{\text{DDS}} = 3.3\text{ V}$ , 915 MHz |  | < -30 |       | dBm  |     |
| Fifth harmonic   |   | +20 dBm setting, $V_{\text{DDS}} = 3.3\text{ V}$ , 915 MHz |  | < -42 |       | dBm  |     |

(4) Spurious emissions increase for supply voltages below 2.2 V. As such, care must be taken to ensure regulatory requirements are met when operating at low supply voltage levels. An alternative is to use the Sub-1 GHz PA below 2.2 V.

## 5.12 861 MHz to 1054 MHz - PLL Phase Noise Wideband Mode

When measured on the CC1352PEM-XD7793-XD24-PA9093 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{ V}$ .

| PARAMETER  | TEST CONDITIONS               | MIN | TYP  | MAX | UNIT   |
|--|-------------------------------|-----|------|-----|--------|
| Phase noise in the 868- and 915-MHz bands<br>20 kHz PLL loop bandwidth | $\pm 10\text{ kHz}$ offset    |     | -74  |     | dBc/Hz |
|  | $\pm 100\text{ kHz}$ offset   |     | -97  |     | dBc/Hz |
|  | $\pm 200\text{ kHz}$ offset   |     | -107 |     | dBc/Hz |
|  | $\pm 400\text{ kHz}$ offset   |     | -113 |     | dBc/Hz |
|  | $\pm 1000\text{ kHz}$ offset  |     | -120 |     | dBc/Hz |
|  | $\pm 2000\text{ kHz}$ offset  |     | -127 |     | dBc/Hz |
|  | $\pm 10000\text{ kHz}$ offset |     | -141 |     | dBc/Hz |

### 5.13 861 MHz to 1054 MHz - PLL Phase Noise Narrowband Mode

When measured on the CC1352PEM-XD7793-XD24-PA9093 reference design with  $T_c = 25\text{ }^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$ .

| PARAMETER   | TEST CONDITIONS   | MIN | TYP  | MAX | UNIT   |
|---|-------------------|-----|------|-----|--------|
| Phase noise in the 868- and 915-MHz bands<br>150 kHz PLL loop bandwidth | ±10 kHz offset    |     | -93  |     | dBc/Hz |
|   | ±100 kHz offset   |     | -93  |     | dBc/Hz |
|   | ±200 kHz offset   |     | -94  |     | dBc/Hz |
|   | ±400 kHz offset   |     | -104 |     | dBc/Hz |
|   | ±1000 kHz offset  |     | -121 |     | dBc/Hz |
|   | ±2000 kHz offset  |     | -130 |     | dBc/Hz |
|   | ±10000 kHz offset |     | -140 |     | dBc/Hz |

## 5.14 359 MHz to 527 MHz - Receive (RX)

Measured on the LAUNCHXL-CC1352P-4 reference design with  $T_c = 25\text{ }^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$  with DC/DC enabled and high power PA connected to  $V_{DD5}$  unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER  | TEST CONDITIONS  | MIN | TYP     | MAX | UNIT |
|--|--|-----|---------|-----|------|
| <b>General Parameters</b>                                |  |     |         |     |      |
| Spurious emissions 25 MHz to 1 GHz                       | 433.92 MHz   |     | < -57   |     | dBm  |
| Spurious emissions 1 GHz to 13 GHz                       | Conducted emissions measured according to ETSI EN 300 220          |     | < -47   |     | dBm  |
| <b>802.15.4g, 200 kbps, 2-GFSK, 310 kHz RX Bandwidth</b> |  |     |         |     |      |
| Sensitivity  | BER = $10^{-2}$ , 433.92 MHz                                       |     | -104    |     | dBm  |
| Saturation limit   | BER = $10^{-2}$ , 433.92 MHz                                       |     | 10      |     | dBm  |
| Selectivity, $\pm 400\text{ kHz}$                        | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 48      |     | dB   |
| Blocking, $\pm 1\text{ MHz}$                             | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 51      |     | dB   |
| Blocking, $\pm 2\text{ MHz}$                             | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 53      |     | dB   |
| Blocking, $\pm 10\text{ MHz}$                            | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 68      |     | dB   |
| Image rejection (image compensation enabled)             | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 45      |     | dB   |
| RSSI dynamic range                                       | Starting from the sensitivity limit                                |     | 89      |     | dB   |
| RSSI accuracy  | Starting from the sensitivity limit across the given dynamic range |     | $\pm 3$ |     | dB   |
| <b>802.15.4g, 50 kbps, 2-GFSK, 100 kHz RX Bandwidth</b>  |  |     |         |     |      |
| Sensitivity  | BER = $10^{-2}$ , 433.92 MHz                                       |     | -110    |     | dBm  |
| Saturation limit   | BER = $10^{-2}$ , 433.92 MHz                                       |     | 10      |     | dBm  |
| Selectivity, +200 kHz                                    | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 48      |     | dB   |
| Selectivity, -200 kHz                                    | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 43      |     | dB   |
| Selectivity, +400 kHz                                    | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 53      |     | dB   |
| Selectivity, -400 kHz                                    | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 44      |     | dB   |
| Blocking, +1 MHz   | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 60      |     | dB   |
| Blocking, -1 MHz   | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 54      |     | dB   |
| Blocking, +2 MHz   | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 62      |     | dB   |
| Blocking, -2 MHz   | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 61      |     | dB   |
| Blocking, +10 MHz  | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 75      |     | dB   |
| Blocking, -10 MHz  | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 75      |     | dB   |
| Image rejection (image compensation enabled)             | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 44      |     | dB   |
| RSSI dynamic range                                       | Starting from the sensitivity limit                                |     | 95      |     | dB   |
| RSSI accuracy  | Starting from the sensitivity limit across the given dynamic range |     | $\pm 3$ |     | dB   |
| <b>Narrowband, 4.8 kbps 2-GFSK, 12.5 kHz ch.</b>         |  |     |         |     |      |
| Sensitivity  | BER = $10^{-2}$ , 426.1 MHz  |     | -120    |     | dBm  |
| Saturation limit   | BER = $10^{-2}$ , 426.1 MHz  |     | 10      |     | dBm  |
| Selectivity, +12.5 kHz                                   | BER = $10^{-2}$ , 426.1 MHz <sup>(1)</sup>                         |     | 53      |     | dB   |
| Selectivity, -12.5 kHz                                   | BER = $10^{-2}$ , 426.1 MHz <sup>(1)</sup>                         |     | 52      |     | dB   |
| Selectivity, +25 kHz                                     | BER = $10^{-2}$ , 426.1 MHz <sup>(1)</sup>                         |     | 53      |     | dB   |
| Selectivity, -25 kHz                                     | BER = $10^{-2}$ , 426.1 MHz <sup>(1)</sup>                         |     | 52      |     | dB   |
| Blocking, +1 MHz   | BER = $10^{-2}$ , 426.1 MHz <sup>(1)</sup>                         |     | 70      |     | dB   |
| Blocking, -1 MHz   | BER = $10^{-2}$ , 426.1 MHz <sup>(1)</sup>                         |     | 66      |     | dB   |
| Blocking, +2 MHz   | BER = $10^{-2}$ , 426.1 MHz <sup>(1)</sup>                         |     | 72      |     | dB   |
| Blocking, -2 MHz   | BER = $10^{-2}$ , 426.1 MHz <sup>(1)</sup>                         |     | 70      |     | dB   |
| Blocking, +10 MHz  | BER = $10^{-2}$ , 426.1 MHz <sup>(1)</sup>                         |     | 84      |     | dB   |
| Blocking, -10 MHz  | BER = $10^{-2}$ , 426.1 MHz <sup>(1)</sup>                         |     | 84      |     | dB   |

(1) Wanted signal 3 dB above sensitivity limit

### 359 MHz to 527 MHz - Receive (RX) (continued)

Measured on the LAUNCHXL-CC1352P-4 reference design with  $T_c = 25\text{ }^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$  with

DC/DC enabled and high power PA connected to  $V_{DD5}$  unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER   | TEST CONDITIONS  | MIN | TYP     | MAX | UNIT |
|---|--|-----|---------|-----|------|
| Image rejection (image compensation enabled)  | BER = $10^{-2}$ , 426.1 MHz <sup>(1)</sup>                         |     | 44      |     | dB   |
| RSSI dynamic range  | Starting from the sensitivity limit                                |     | 102     |     | dB   |
| RSSI accuracy   | Starting from the sensitivity limit across the given dynamic range |     | $\pm 3$ |     | dB   |
| <b>SimpleLink™ Long Range 5 kbps (20 ksym/s, 2-GFSK, 5 kHz Deviation, FEC (Half Rate), DSSS = 1:4, 34 kHz RX Bandwidth)</b>   |  |     |         |     |      |
| Sensitivity   | BER = $10^{-2}$ , 433.92 MHz                                       |     | -119    |     | dBm  |
| Saturation limit  | BER = $10^{-2}$ , 433.92 MHz                                       |     | 10      |     | dBm  |
| Selectivity, +100 kHz   | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 55      |     | dB   |
| Selectivity, -100 kHz   | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 53      |     | dB   |
| Blocking, +1 MHz  | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 69      |     | dB   |
| Blocking, -1 MHz  | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 65      |     | dB   |
| Blocking, +2 MHz  | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 71      |     | dB   |
| Blocking, -2 MHz  | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 70      |     | dB   |
| Blocking, +10 MHz   | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 84      |     | dB   |
| Blocking, -10 MHz   | BER = $10^{-2}$ , 433.92 MHz <sup>(1)</sup>                        |     | 84      |     | dB   |
| Image rejection (image compensation enabled)  | BER = $10^{-2}$ , 433.92 MHz                                       |     | 49      |     | dB   |
| RSSI dynamic range  | Starting from the sensitivity limit                                |     | 101     |     | dB   |
| RSSI accuracy   | Starting from the sensitivity limit across the given dynamic range |     | $\pm 3$ |     | dB   |
| <b>SimpleLink™ Long Range 2.5 kbps (20 ksym/s, 2-GFSK, 5 kHz Deviation, FEC (Half Rate), DSSS = 1:2, 34 kHz RX Bandwidth)</b> |  |     |         |     |      |
| Sensitivity   | BER = $10^{-2}$ , 433.92 MHz                                       |     | -121    |     | dBm  |

## 5.15 359 MHz to 527 MHz - Transmit (TX)

Measured on the LAUNCHXL-CC1352P-4 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DD5}} = 3.6\text{ V}$  with DC/DC enabled and high power PA connected to  $V_{\text{DD5}}$  unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted. <sup>(1)</sup>

| PARAMETER  | TEST CONDITIONS   | MIN   | TYP   | MAX | UNIT |
|--|---|---|-------|-----|------|
| <b>General parameters</b>  |   |   |       |     |      |
| Max output power, Sub-1 GHz PA <sup>(2)</sup>                                    | 433.92 MHz, without BOOST ( $V_{\text{DDR}} = 1.7\text{ V}$ )               |   | 13    |     | dBm  |
| Output power programmable range Sub-1 GHz PA                                     | 433.92 MHz, without BOOST ( $V_{\text{DDR}} = 1.7\text{ V}$ )               |   | 24    |     | dB   |
| Output power variation over temperature, Sub-1 GHz PA                            | +13 dBm setting, 433.92 MHz<br>Over recommended temperature operating range |   | ±1.5  |     | dB   |
| <b>Spurious emissions and harmonics</b>  |   |   |       |     |      |
| Spurious emissions (excluding harmonics) Sub-1 GHz PA, 433.92 MHz <sup>(3)</sup> | 30 MHz to 1 GHz   | +10 dBm setting<br>ETSI restricted bands              | < -54 |     | dBm  |
|  |   | +10 dBm setting<br>ETSI outside restricted bands      | < -36 |     | dBm  |
|  | 1 GHz to 12.75 GHz (outside ETSI restricted bands)                          | +10 dBm setting<br>measured in 1 MHz bandwidth (ETSI) | < -30 |     | dBm  |
| Spurious emissions out-of-band Sub-1 GHz PA, 429 MHz <sup>(3)</sup>              | Outside the necessary frequency band (ARIB T-67)                            | +10 dBm setting                                       | < -26 |     | dBm  |
|  | 710 MHz to 900 MHz (ARIB T-67)  | +10 dBm setting                                       | < -55 |     | dBm  |
|  | 900 MHz to 915 MHz (ARIB T-67)  | +10 dBm setting                                       | < -55 |     | dBm  |
|  | 930 MHz to 1000 MHz (ARIB T-67)   | +10 dBm setting                                       | < -55 |     | dBm  |
|  | 1000 MHz to 1215 MHz (ARIB T-67)  | +10 dBm setting                                       | < -45 |     | dBm  |
|  | Above 1215 MHz (ARIB T-67)  | +10 dBm setting                                       | < -30 |     | dBm  |
| Harmonics Sub-1 GHz PA   | Second harmonic   | +13 dBm setting, 433 MHz                              | < -36 |     | dBm  |
| Harmonics Sub-1 GHz PA   | Third harmonic  | +13 dBm setting, 433 MHz                              | < -30 |     | dBm  |
| Harmonics Sub-1 GHz PA   | Fourth harmonic   | +13 dBm setting, 433 MHz                              | < -30 |     | dBm  |
| Harmonics Sub-1 GHz PA   | Fifth harmonic  | +13 dBm setting, 433 MHz                              | < -30 |     | dBm  |

- (1) Some combinations of frequency, data rate and modulation format requires use of external crystal load capacitors for regulatory compliance. More details can be found in the device errata.
- (2) Output power is dependent on RF match. For dual-band devices in the CC13X2 platform, output power might be slightly reduced depending on RF layout trade-offs.
- (3) Suitable for systems targeting compliance with EN 300 220, EN 303 131, EN 303 204, FCC CFR47 Part 15, ARIB STD-T108.

## 5.16 359 MHz to 527 MHz - PLL Phase Noise

When measured on the LAUNCHXL-CC1352P-4 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DD5}} = 3.0\text{ V}$ .

| PARAMETER   | TEST CONDITIONS   | MIN | TYP  | MAX | UNIT   |
|---|-------------------|-----|------|-----|--------|
| Phase noise in the 429 MHz band<br>200 kHz PLL loop bandwidth | ±10 kHz offset    |     | -103 |     | dBc/Hz |
|   | ±100 kHz offset   |     | -101 |     | dBc/Hz |
|   | ±200 kHz offset   |     | -101 |     | dBc/Hz |
|   | ±400 kHz offset   |     | -106 |     | dBc/Hz |
|   | ±1000 kHz offset  |     | -122 |     | dBc/Hz |
|   | ±2000 kHz offset  |     | -133 |     | dBc/Hz |
|   | ±10000 kHz offset |     | -143 |     | dBc/Hz |

### 359 MHz to 527 MHz - PLL Phase Noise (*continued*)

When measured on the LAUNCHXL-CC1352P-4 reference design with  $T_c = 25\text{ }^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$ .

| PARAMETER  | TEST CONDITIONS   | MIN | TYP  | MAX | UNIT   |
|--|-------------------|-----|------|-----|--------|
| Phase noise in the 433 MHz band<br>20 kHz PLL loop bandwidth | ±10 kHz offset    |     | -86  |     | dBc/Hz |
|  | ±100 kHz offset   |     | -108 |     | dBc/Hz |
|  | ±200 kHz offset   |     | -115 |     | dBc/Hz |
|  | ±400 kHz offset   |     | -122 |     | dBc/Hz |
|  | ±1000 kHz offset  |     | -130 |     | dBc/Hz |
|  | ±2000 kHz offset  |     | -137 |     | dBc/Hz |
|  | ±10000 kHz offset |     | -145 |     | dBc/Hz |

## 5.17 Bluetooth Low Energy - Receive (RX)

Measured on the CC1352PEM-XD7793-XD24-PA24 reference design with  $T_c = 25\text{ }^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$ ,  $f_{RF} = 2440\text{ MHz}$  with DC/DC enabled and high power PA connected to  $V_{DD5}$  unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER  | TEST CONDITIONS   | MIN | TYP                     | MAX | UNIT |
|--|---|-----|-------------------------|-----|------|
| <b>125 kbps (LE Coded)</b>                                     |   |     |                         |     |      |
| Receiver sensitivity   | Differential mode. BER = $10^{-3}$  |     | -105                    |     | dBm  |
| Receiver saturation  | Differential mode. BER = $10^{-3}$  |     | >5                      |     | dBm  |
| Frequency error tolerance                                      | Difference between the incoming carrier frequency and the internally generated carrier frequency  |     | > (-300 / 300)          |     | kHz  |
| Data rate error tolerance                                      | Difference between incoming data rate and the internally generated data rate (37-byte packets)  |     | > (-320 / 240)          |     | ppm  |
| Data rate error tolerance                                      | Difference between incoming data rate and the internally generated data rate (255-byte packets)   |     | > (-125 / 125)          |     | ppm  |
| Co-channel rejection <sup>(1)</sup>                            | Wanted signal at -79 dBm, modulated interferer in channel, BER = $10^{-3}$  |     | -1.5                    |     | dB   |
| Selectivity, $\pm 1\text{ MHz}$ <sup>(1)</sup>                 | Wanted signal at -79 dBm, modulated interferer at $\pm 1\text{ MHz}$ , BER = $10^{-3}$  |     | 8 / 4.5 <sup>(2)</sup>  |     | dB   |
| Selectivity, $\pm 2\text{ MHz}$ <sup>(1)</sup>                 | Wanted signal at -79 dBm, modulated interferer at $\pm 2\text{ MHz}$ , BER = $10^{-3}$  |     | 44 / 39 <sup>(2)</sup>  |     | dB   |
| Selectivity, $\pm 3\text{ MHz}$ <sup>(1)</sup>                 | Wanted signal at -79 dBm, modulated interferer at $\pm 3\text{ MHz}$ , BER = $10^{-3}$  |     | 46 / 44 <sup>(2)</sup>  |     | dB   |
| Selectivity, $\pm 4\text{ MHz}$ <sup>(1)</sup>                 | Wanted signal at -79 dBm, modulated interferer at $\pm 4\text{ MHz}$ , BER = $10^{-3}$  |     | 44 / 46 <sup>(2)</sup>  |     | dB   |
| Selectivity, $\pm 6\text{ MHz}$ <sup>(1)</sup>                 | Wanted signal at -79 dBm, modulated interferer at $\geq \pm 6\text{ MHz}$ , BER = $10^{-3}$   |     | 48 / 44 <sup>(2)</sup>  |     | dB   |
| Selectivity, $\pm 7\text{ MHz}$                                | Wanted signal at -79 dBm, modulated interferer at $\geq \pm 7\text{ MHz}$ , BER = $10^{-3}$   |     | 51 / 45 <sup>(2)</sup>  |     | dB   |
| Selectivity, Image frequency <sup>(1)</sup>                    | Wanted signal at -79 dBm, modulated interferer at image frequency, BER = $10^{-3}$  |     | 39                      |     | dB   |
| Selectivity, Image frequency $\pm 1\text{ MHz}$ <sup>(1)</sup> | Note that Image frequency + 1 MHz is the Co- channel -1 MHz. Wanted signal at -79 dBm, modulated interferer at $\pm 1\text{ MHz}$ from image frequency, BER = $10^{-3}$ |     | 4.5 / 44 <sup>(2)</sup> |     | dB   |
| <b>500 kbps (LE Coded)</b>                                     |   |     |                         |     |      |
| Receiver sensitivity   | Differential mode. BER = $10^{-3}$  |     | -100                    |     | dBm  |
| Receiver saturation  | Differential mode. BER = $10^{-3}$  |     | > 5                     |     | dBm  |
| Frequency error tolerance                                      | Difference between the incoming carrier frequency and the internally generated carrier frequency  |     | > (-300 / 300)          |     | kHz  |
| Data rate error tolerance                                      | Difference between incoming data rate and the internally generated data rate (37-byte packets)  |     | > (-450 / 450)          |     | ppm  |
| Data rate error tolerance                                      | Difference between incoming data rate and the internally generated data rate (255-byte packets)   |     | > (-175 / 175)          |     | ppm  |
| Co-channel rejection <sup>(1)</sup>                            | Wanted signal at -72 dBm, modulated interferer in channel, BER = $10^{-3}$  |     | -3.5                    |     | dB   |
| Selectivity, $\pm 1\text{ MHz}$ <sup>(1)</sup>                 | Wanted signal at -72 dBm, modulated interferer at $\pm 1\text{ MHz}$ , BER = $10^{-3}$  |     | 8 / 4 <sup>(2)</sup>    |     | dB   |
| Selectivity, $\pm 2\text{ MHz}$ <sup>(1)</sup>                 | Wanted signal at -72 dBm, modulated interferer at $\pm 2\text{ MHz}$ , BER = $10^{-3}$  |     | 44 / 37 <sup>(2)</sup>  |     | dB   |
| Selectivity, $\pm 3\text{ MHz}$ <sup>(1)</sup>                 | Wanted signal at -72 dBm, modulated interferer at $\pm 3\text{ MHz}$ , BER = $10^{-3}$  |     | 46 / 46 <sup>(2)</sup>  |     | dB   |
| Selectivity, $\pm 4\text{ MHz}$ <sup>(1)</sup>                 | Wanted signal at -72 dBm, modulated interferer at $\pm 4\text{ MHz}$ , BER = $10^{-3}$  |     | 45 / 47 <sup>(2)</sup>  |     | dB   |
| Selectivity, $\pm 6\text{ MHz}$ <sup>(1)</sup>                 | Wanted signal at -72 dBm, modulated interferer at $\geq \pm 6\text{ MHz}$ , BER = $10^{-3}$   |     | 46 / 45 <sup>(2)</sup>  |     | dB   |
| Selectivity, $\pm 7\text{ MHz}$                                | Wanted signal at -72 dBm, modulated interferer at $\geq \pm 7\text{ MHz}$ , BER = $10^{-3}$   |     | 49 / 45 <sup>(2)</sup>  |     | dB   |

(1) Numbers given as I/C dB

(2) X / Y, where X is +N MHz and Y is -N MHz

## Bluetooth Low Energy - Receive (RX) (continued)

Measured on the CC1352PEM-XD7793-XD24-PA24 reference design with  $T_c = 25\text{ }^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$ ,  $f_{RF} = 2440\text{ MHz}$  with DC/DC enabled and high power PA connected to  $V_{DD5}$  unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER  | TEST CONDITIONS  | MIN | TYP                    | MAX | UNIT |
|--|--|-----|------------------------|-----|------|
| Selectivity, Image frequency <sup>(1)</sup>                    | Wanted signal at $-72\text{ dBm}$ , modulated interferer at image frequency, $BER = 10^{-3}$   |     | 37                     |     | dB   |
| Selectivity, Image frequency $\pm 1\text{ MHz}$ <sup>(1)</sup> | Note that Image frequency $+ 1\text{ MHz}$ is the Co- channel $-1\text{ MHz}$ . Wanted signal at $-72\text{ dBm}$ , modulated interferer at $\pm 1\text{ MHz}$ from image frequency, $BER = 10^{-3}$ |     | 4 / 46 <sup>(2)</sup>  |     | dB   |
| <b>1 Mbps (LE 1M)</b>  |  |     |                        |     |      |
| Receiver sensitivity   | Differential mode. $BER = 10^{-3}$   |     | $-97$                  |     | dBm  |
| Receiver saturation  | Differential mode. $BER = 10^{-3}$   |     | $> 5$                  |     | dBm  |
| Frequency error tolerance                                      | Difference between the incoming carrier frequency and the internally generated carrier frequency   |     | $> (-350 / 350)$       |     | kHz  |
| Data rate error tolerance                                      | Difference between incoming data rate and the internally generated data rate (37-byte packets)   |     | $> (-750 / 750)$       |     | ppm  |
| Co-channel rejection <sup>(1)</sup>                            | Wanted signal at $-67\text{ dBm}$ , modulated interferer in channel, $BER = 10^{-3}$   |     | $-6$                   |     | dB   |
| Selectivity, $\pm 1\text{ MHz}$ <sup>(1)</sup>                 | Wanted signal at $-67\text{ dBm}$ , modulated interferer at $\pm 1\text{ MHz}$ , $BER = 10^{-3}$   |     | 7 / 4 <sup>(2)</sup>   |     | dB   |
| Selectivity, $\pm 2\text{ MHz}$ <sup>(1)</sup>                 | Wanted signal at $-67\text{ dBm}$ , modulated interferer at $\pm 2\text{ MHz}$ , $BER = 10^{-3}$   |     | 40 / 33 <sup>(2)</sup> |     | dB   |
| Selectivity, $\pm 3\text{ MHz}$ <sup>(1)</sup>                 | Wanted signal at $-67\text{ dBm}$ , modulated interferer at $\pm 3\text{ MHz}$ , $BER = 10^{-3}$   |     | 36 / 41 <sup>(2)</sup> |     | dB   |
| Selectivity, $\pm 4\text{ MHz}$ <sup>(1)</sup>                 | Wanted signal at $-67\text{ dBm}$ , modulated interferer at $\pm 4\text{ MHz}$ , $BER = 10^{-3}$   |     | 36 / 45 <sup>(2)</sup> |     | dB   |
| Selectivity, $\pm 5\text{ MHz}$ or more <sup>(1)</sup>         | Wanted signal at $-67\text{ dBm}$ , modulated interferer at $\geq \pm 5\text{ MHz}$ , $BER = 10^{-3}$  |     | 40                     |     | dB   |
| Selectivity, image frequency <sup>(1)</sup>                    | Wanted signal at $-67\text{ dBm}$ , modulated interferer at image frequency, $BER = 10^{-3}$   |     | 33                     |     | dB   |
| Selectivity, image frequency $\pm 1\text{ MHz}$ <sup>(1)</sup> | Note that Image frequency $+ 1\text{ MHz}$ is the Co- channel $-1\text{ MHz}$ . Wanted signal at $-67\text{ dBm}$ , modulated interferer at $\pm 1\text{ MHz}$ from image frequency, $BER = 10^{-3}$ |     | 4 / 41 <sup>(2)</sup>  |     | dB   |
| Out-of-band blocking <sup>(3)</sup>                            | 30 MHz to 2000 MHz   |     | $-10$                  |     | dBm  |
| Out-of-band blocking   | 2003 MHz to 2399 MHz   |     | $-18$                  |     | dBm  |
| Out-of-band blocking   | 2484 MHz to 2997 MHz   |     | $-12$                  |     | dBm  |
| Out-of-band blocking   | 3000 MHz to 12.75 GHz  |     | $-2$                   |     | dBm  |
| Intermodulation  | Wanted signal at 2402 MHz, $-64\text{ dBm}$ . Two interferers at 2405 and 2408 MHz respectively, at the given power level  |     | $-42$                  |     | dBm  |
| Spurious emissions, 30 to 1000 MHz <sup>(4)</sup>              | Measurement in a $50\text{-}\Omega$ single-ended load.   |     | $< -59$                |     | dBm  |
| Spurious emissions, 1 to 12.75 GHz <sup>(4)</sup>              | Measurement in a $50\text{ }\Omega$ single-ended load.   |     | $< -47$                |     | dBm  |
| RSSI dynamic range   |  |     | 70                     |     | dB   |
| RSSI accuracy  |  |     | $\pm 4$                |     | dB   |
| <b>2 Mbps (LE 2M)</b>  |  |     |                        |     |      |
| Receiver sensitivity   | Differential mode. Measured at SMA connector, $BER = 10^{-3}$  |     | $-92$                  |     | dBm  |
| Receiver saturation  | Differential mode. Measured at SMA connector, $BER = 10^{-3}$  |     | $> 5$                  |     | dBm  |
| Frequency error tolerance                                      | Difference between the incoming carrier frequency and the internally generated carrier frequency   |     | $> (-500 / 500)$       |     | kHz  |

(3) Excluding one exception at  $F_{\text{wanted}} / 2$ , per Bluetooth Specification

(4) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)



## Bluetooth Low Energy - Receive (RX) (continued)

Measured on the CC1352PEM-XD7793-XD24-PA24 reference design with  $T_c = 25\text{ }^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$ ,  $f_{RF} = 2440\text{ MHz}$  with DC/DC enabled and high power PA connected to  $V_{DD5}$  unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER  | TEST CONDITIONS   | MIN | TYP                    | MAX | UNIT |
|--|---|-----|------------------------|-----|------|
| Data rate error tolerance                                      | Difference between incoming data rate and the internally generated data rate (37-byte packets)  |     | > (-700 / 750)         |     | ppm  |
| Co-channel rejection <sup>(1)</sup>                            | Wanted signal at -67 dBm, modulated interferer in channel, BER = $10^{-3}$  |     | -7                     |     | dB   |
| Selectivity, $\pm 2\text{ MHz}$ <sup>(1)</sup>                 | Wanted signal at -67 dBm, modulated interferer at $\pm 2\text{ MHz}$ , Image frequency is at -2 MHz, BER = $10^{-3}$  |     | 8 / 4 <sup>(2)</sup>   |     | dB   |
| Selectivity, $\pm 4\text{ MHz}$ <sup>(1)</sup>                 | Wanted signal at -67 dBm, modulated interferer at $\pm 4\text{ MHz}$ , BER = $10^{-3}$  |     | 36 / 36 <sup>(2)</sup> |     | dB   |
| Selectivity, $\pm 6\text{ MHz}$ <sup>(1)</sup>                 | Wanted signal at -67 dBm, modulated interferer at $\pm 6\text{ MHz}$ , BER = $10^{-3}$  |     | 37 / 36 <sup>(2)</sup> |     | dB   |
| Selectivity, image frequency <sup>(1)</sup>                    | Wanted signal at -67 dBm, modulated interferer at image frequency, BER = $10^{-3}$  |     | 4                      |     | dB   |
| Selectivity, image frequency $\pm 2\text{ MHz}$ <sup>(1)</sup> | Note that Image frequency + 2 MHz is the Co-channel. Wanted signal at -67 dBm, modulated interferer at $\pm 2\text{ MHz}$ from image frequency, BER = $10^{-3}$ |     | -7 / 36 <sup>(2)</sup> |     | dB   |
| Out-of-band blocking <sup>(3)</sup>                            | 30 MHz to 2000 MHz  |     | -16                    |     | dBm  |
| Out-of-band blocking   | 2003 MHz to 2399 MHz  |     | -21                    |     | dBm  |
| Out-of-band blocking   | 2484 MHz to 2997 MHz  |     | -15                    |     | dBm  |
| Out-of-band blocking   | 3000 MHz to 12.75 GHz   |     | -12                    |     | dBm  |
| Intermodulation  | Wanted signal at 2402 MHz, -64 dBm. Two interferers at 2408 and 2414 MHz respectively, at the given power level   |     | -38                    |     | dBm  |

### 5.18 Bluetooth Low Energy - Transmit (TX)

Measured on the CC1352PEM-XD7793-XD24-PA24 reference design with  $T_c = 25\text{ }^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$ ,  $f_{RF} = 2440\text{ MHz}$  with DC/DC enabled and high power PA connected to  $V_{DD5}$  unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER  | TEST CONDITIONS   | MIN             | TYP                            | MAX   | UNIT |     |
|--|---|-----------------|--------------------------------|-------|------|-----|
| <b>General Parameters</b>  |   |                 |                                |       |      |     |
| Max output power, high power PA  | Differential mode, delivered to a single-ended 50 $\Omega$ load through a balun |                 | 19.5                           |       | dBm  |     |
| Output power programmable range high power PA                                      | Differential mode, delivered to a single-ended 50 $\Omega$ load through a balun |                 | 6                              |       | dB   |     |
| Max output power, high power PA, 10 dBm configuration <sup>(1)</sup>               | Differential mode, delivered to a single-ended 50 $\Omega$ load through a balun |                 | 10.5                           |       | dBm  |     |
| Output power programmable range high power PA, 10 dBm configuration <sup>(1)</sup> | Differential mode, delivered to a single-ended 50 $\Omega$ load through a balun |                 | 5                              |       | dB   |     |
| Max output power, 2.4 GHz PA   | Differential mode, delivered to a single-ended 50 $\Omega$ load through a balun |                 | 5                              |       | dBm  |     |
| Output power programmable range, 2.4 GHz PA  | Differential mode, delivered to a single-ended 50 $\Omega$ load through a balun |                 | 26                             |       | dB   |     |
| <b>Spurious emissions and harmonics</b>  |   |                 |                                |       |      |     |
| Spurious emissions, high-power PA <sup>(2)(3)</sup>                                | f < 1 GHz, outside restricted bands   | +20 dBm setting | < -36                          |       | dBm  |     |
|  | f < 1 GHz, restricted bands FCC   |                 | < -55                          |       | dBm  |     |
|  | f > 1 GHz, including harmonics  |                 | -37                            |       | dBm  |     |
| Harmonics, high-power PA <sup>(2)(4)</sup>   | Second harmonic   |                 | -35                            |       | dBm  |     |
|  | Third harmonic  |                 | -42                            |       | dBm  |     |
| Spurious emissions, high-power PA, 10 dBm configuration <sup>(2)(3)(1)</sup>       | f < 1 GHz, outside restricted bands   |                 | +10 dBm setting <sup>(1)</sup> | < -36 |      | dBm |
|  | f < 1 GHz, restricted bands ETSI  | < -54           |                                |       | dBm  |     |
|  | f < 1 GHz, restricted bands FCC   | < -55           |                                |       | dBm  |     |
|  | f > 1 GHz, including harmonics  | -41             |                                |       | dBm  |     |
| Harmonics, high-power PA, 10 dBm configuration <sup>(2)(1)</sup>                   | Second harmonic   | < -42           |                                |       | dBm  |     |
|  | Third harmonic  | < -42           |                                |       | dBm  |     |
| Spurious emissions, 2.4 GHz PA <sup>(2)</sup>                                      | f < 1 GHz, outside restricted bands   | +5 dBm setting  |                                | < -36 |      | dBm |
|  | f < 1 GHz, restricted bands ETSI  |                 |                                | < -54 |      | dBm |
|  | f < 1 GHz, restricted bands FCC   |                 | < -55                          |       | dBm  |     |
|  | f > 1 GHz, including harmonics  |                 | < -42                          |       | dBm  |     |
| Harmonics, 2.4 GHz PA <sup>(2)</sup>   | Second harmonic   |                 | < -42                          |       | dBm  |     |
|  | Third harmonic  |                 | < -42                          |       | dBm  |     |

- (1) Measured on evaluation board as described in [www.ti.com/lit/pdf/swra636](http://www.ti.com/lit/pdf/swra636).
- (2) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).
- (3) To ensure margins for passing FCC band edge requirements at 2483.5 MHz, a lower than maximum output-power setting or less than 100% duty cycle may be used when operating at the upper BLE channel(s).
- (4) To ensure margins for passing FCC requirements for harmonic emission, duty cycling may be required. The CC1352P-2 LaunchPad reference design should also be reviewed as the filter provides higher attenuation of harmonics compared to the CC1352PEM-XD7793-XD24-PA24 reference design.

## 5.19 Zigbee and Thread - IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) - RX

Measured on the CC1352PEM-XD7793-XD24-PA24 reference design with  $T_c = 25\text{ }^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$ ,  $f_{RF} = 2440\text{ MHz}$  with DC/DC enabled and high power PA connected to  $V_{DD5}$  unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER  | TEST CONDITIONS  | MIN | TYP     | MAX | UNIT |
|--|--|-----|---------|-----|------|
| Receiver sensitivity                                       | PER = 1%   |     | -100    |     | dBm  |
| Receiver saturation  | PER = 1%   |     | > 5     |     | dBm  |
| Adjacent channel rejection                                 | Wanted signal at -82 dBm, modulated interferer at $\pm 5\text{ MHz}$ , PER = 1%  |     | 36      |     | dB   |
| Alternate channel rejection                                | Wanted signal at -82 dBm, modulated interferer at $\pm 10\text{ MHz}$ , PER = 1%   |     | 57      |     | dB   |
| Channel rejection, $\pm 15\text{ MHz}$ or more             | Wanted signal at -82 dBm, undesired signal is IEEE 802.15.4 modulated channel, stepped through all channels 2405 to 2480 MHz, PER = 1% |     | 59      |     | dB   |
| Blocking and desensitization, 5 MHz from upper band edge   | Wanted signal at -97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%   |     | 57      |     | dB   |
| Blocking and desensitization, 10 MHz from upper band edge  | Wanted signal at -97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%   |     | 63      |     | dB   |
| Blocking and desensitization, 20 MHz from upper band edge  | Wanted signal at -97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%   |     | 63      |     | dB   |
| Blocking and desensitization, 50 MHz from upper band edge  | Wanted signal at -97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%   |     | 66      |     | dB   |
| Blocking and desensitization, -5 MHz from lower band edge  | Wanted signal at -97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%   |     | 60      |     | dB   |
| Blocking and desensitization, -10 MHz from lower band edge | Wanted signal at -97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%   |     | 60      |     | dB   |
| Blocking and desensitization, -20 MHz from lower band edge | Wanted signal at -97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%   |     | 63      |     | dB   |
| Blocking and desensitization, -50 MHz from lower band edge | Wanted signal at -97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%   |     | 65      |     | dB   |
| Spurious emissions, 30 MHz to 1000 MHz                     | Measurement in a 50- $\Omega$ single-ended load  |     | -66     |     | dBm  |
| Spurious emissions, 1 GHz to 12.75 GHz                     | Measurement in a 50- $\Omega$ single-ended load  |     | -53     |     | dBm  |
| Frequency error tolerance                                  | Difference between the incoming carrier frequency and the internally generated carrier frequency                                       |     | > 350   |     | ppm  |
| Symbol rate error tolerance                                | Difference between incoming symbol rate and the internally generated symbol rate   |     | > 1000  |     | ppm  |
| RSSI dynamic range   |  |     | 95      |     | dB   |
| RSSI accuracy  |  |     | $\pm 4$ |     | dB   |

## 5.20 Zigbee and Thread - IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) - TX

Measured on the CC1352PEM-XD7793-XD24-PA24 reference design with  $T_c = 25\text{ }^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$ ,  $f_{RF} = 2440\text{ MHz}$  with DC/DC enabled and high power PA connected to  $V_{DD5}$  unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER   | TEST CONDITIONS  | MIN                            | TYP   | MAX | UNIT |
|---|--|--------------------------------|-------|-----|------|
| <b>General Parameters</b>   |  |                                |       |     |      |
| Max output power, high power PA   | Differential mode, delivered to a single-ended 50- $\Omega$ load through a balun |                                | 19.5  |     | dBm  |
| Output power programmable range, high power PA                                      | Differential mode, delivered to a single-ended 50- $\Omega$ load through a balun |                                | 6     |     | dB   |
| Max output power, high power PA, 10 dBm configuration <sup>(1)</sup>                | Differential mode, delivered to a single-ended 50- $\Omega$ load through a balun |                                | 10.5  |     | dBm  |
| Output power programmable range, high power PA, 10 dBm configuration <sup>(1)</sup> | Differential mode, delivered to a single-ended 50- $\Omega$ load through a balun |                                | 5     |     | dB   |
| Max output power, 2.4 GHz PA  | Differential mode, delivered to a single-ended 50- $\Omega$ load through a balun |                                | 5     |     | dBm  |
| Output power programmable range, 2.4 GHz PA   | Differential mode, delivered to a single-ended 50- $\Omega$ load through a balun |                                | 26    |     | dB   |
| <b>Spurious emissions and harmonics</b>   |  |                                |       |     |      |
| Spurious emissions, high-power PA <sup>(2)(3)</sup>                                 | f < 1 GHz, outside restricted bands  | +20 dBm setting                | < -39 |     | dBm  |
|   | f < 1 GHz, restricted bands FCC  |                                | < -49 |     | dBm  |
|   | f > 1 GHz, including harmonics   |                                | -40   |     | dBm  |
| Harmonics, high-power PA <sup>(2)(4)</sup>  | Second harmonic  |                                | -35   |     | dBm  |
|   | Third harmonic   |                                | -42   |     | dBm  |
| Spurious emissions, high-power PA, 10 dBm configuration <sup>(2)(3)(1)</sup>        | f < 1 GHz, outside restricted bands  | +10 dBm setting <sup>(1)</sup> | < -36 |     | dBm  |
|   | f < 1 GHz, restricted bands ETSI   |                                | < -47 |     | dBm  |
|   | f < 1 GHz, restricted bands FCC  |                                | < -55 |     | dBm  |
|   | f > 1 GHz, including harmonics   |                                | -42   |     | dBm  |
| Harmonics, high-power PA, 10 dBm configuration <sup>(2)(1)</sup>                    | Second harmonic  |                                | < -42 |     | dBm  |
|   | Third harmonic   |                                | < -42 |     | dBm  |
| Spurious emissions, 2.4 GHz PA <sup>(2)(5)</sup>                                    | f < 1 GHz, outside restricted bands  | +5 dBm setting                 | < -36 |     | dBm  |
|   | f < 1 GHz, restricted bands ETSI   |                                | < -47 |     | dBm  |
|   | f < 1 GHz, restricted bands FCC  |                                | < -55 |     | dBm  |
|   | f > 1 GHz, including harmonics   |                                | < -42 |     | dBm  |
| Harmonics, 2.4 GHz PA <sup>(2)</sup>  | Second harmonic  |                                | < -42 |     | dBm  |
|   | Third harmonic   |                                | < -42 |     | dBm  |
| <b>IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps)</b>                         |  |                                |       |     |      |
| Error vector magnitude, high power PA   | +20 dBm setting  |                                | 2     |     | %    |
| Error vector magnitude, high power PA, 10 dBm configuration <sup>(1)</sup>          | +10 dBm setting  |                                | 2     |     | %    |

(1) Measured on evaluation board as described in <https://www.ti.com/lit/pdf/swra636>.

(2) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

(3) To ensure margins for passing FCC band edge requirements at 2483.5 MHz, a lower than maximum output-power setting or less than 100% duty cycle may be used when operating at the upper 802.15.4 channel(s).

(4) To ensure margins for passing FCC requirements for harmonic emission, duty cycling may be required. The CC1352P-2 LaunchPad reference design should also be reviewed as the filter provides higher attenuation of harmonics compared to the CC1352PEM-XD7793-XD24-PA24 reference design.

(5) To ensure margins for passing FCC band edge requirements at 2483.5 MHz, a lower than maximum output-power setting or less than 100% duty cycle may be used when operating at 2480 MHz.

**Zigbee and Thread - IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) - TX (continued)**

Measured on the CC1352PEM-XD7793-XD24-PA24 reference design with  $T_c = 25\text{ }^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{ V}$ ,  $f_{\text{RF}} = 2440\text{ MHz}$  with DC/DC enabled and high power PA connected to  $V_{\text{DDS}}$  unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER                          | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------|-----------------|-----|-----|-----|------|
| Error vector magnitude, 2.4-GHz PA | +5 dBm setting  |     | 2   |     | %    |

## 5.21 Timing and Switching Characteristics

**Table 5-1. Reset Timing**

| PARAMETER            | MIN | TYP | MAX | UNIT |
|----------------------|-----|-----|-----|------|
| RESET_N low duration | 1   |     |     | μs   |

**Table 5-2. Wakeup Timing**

Measured over operating free-air temperature with  $V_{DD5} = 3.0\text{ V}$  (unless otherwise noted). The times listed here do not include software overhead.

| PARAMETER                              | TEST CONDITIONS | MIN | TYP  | MAX | UNIT |
|--|-----------------|-----|------|-----|------|
| MCU, Reset to Active <sup>(1)</sup>    |                 | 850 | 3000 |     | μs   |
| MCU, Shutdown to Active <sup>(1)</sup> |                 | 850 | 3000 |     | μs   |
| MCU, Standby to Active                 |                 |     | 160  |     | μs   |
| MCU, Active to Standby                 |                 |     | 36   |     | μs   |
| MCU, Idle to Active                    |                 |     | 14   |     | μs   |

- (1) The wakeup time is dependent on remaining charge on VDDR capacitor when starting the device, and thus how long the device has been in Reset or Shutdown before starting up again.

### 5.21.1 Clock Specifications

**Table 5-3. 48 MHz Crystal Oscillator (XOSC\_HF)**

Measured on a Texas Instruments reference design with  $T_c = 25\text{ }^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{ V}$ , unless otherwise noted. <sup>(1)</sup>

|       | PARAMETER   | MIN | TYP                           | MAX | UNIT          |
|-------|---|-----|-------------------------------|-----|---------------|
|       | Crystal frequency   |     | 48                            |     | MHz           |
| ESR   | Equivalent series resistance<br>$6\text{ pF} < C_L \leq 9\text{ pF}$  |     | 20                            | 60  | $\Omega$      |
| ESR   | Equivalent series resistance<br>$5\text{ pF} < C_L \leq 6\text{ pF}$  |     |                               | 80  | $\Omega$      |
| $L_M$ | Motional inductance, relates to the load capacitance that is used for the crystal ( $C_L$ in Farads) <sup>(2)</sup> |     | $< 3 \times 10^{-25} / C_L^2$ |     | H             |
| $C_L$ | Crystal load capacitance <sup>(3)</sup>   | 5   | 7 <sup>(4)</sup>              | 9   | pF            |
|       | Start-up time <sup>(5)</sup>  |     | 200                           |     | $\mu\text{s}$ |

- (1) Probing or otherwise stopping the crystal while the DC/DC converter is enabled may cause permanent damage to the device.
- (2) The crystal manufacturer's specification must satisfy this requirement for proper operation.
- (3) Adjustable load capacitance is integrated into the device. External load capacitors are required for systems targeting compliance with certain regulations. See the device errata for further details.
- (4) On-chip default connected capacitance including reference design parasitic capacitance. Connected internal capacitance is changed through software in the Customer Configuration section (CCFG).
- (5) Start-up time using the TI-provided power driver. Start-up time may increase if driver is not used.

**Table 5-4. 48 MHz RC Oscillator (RCOSC\_HF)**

Measured on a Texas Instruments reference design with  $T_c = 25\text{ }^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{ V}$ , unless otherwise noted.

|  | MIN | TYP        | MAX | UNIT          |
|--|-----|------------|-----|---------------|
| Frequency                                    |     | 48         |     | MHz           |
| Uncalibrated frequency accuracy              |     | $\pm 1$    |     | %             |
| Calibrated frequency accuracy <sup>(1)</sup> |     | $\pm 0.25$ |     | %             |
| Start-up time                                |     | 5          |     | $\mu\text{s}$ |

- (1) Accuracy relative to the calibration source (XOSC\_HF)

**Table 5-5. 2 MHz RC Oscillator (RCOSC\_MF)**

Measured on a Texas Instruments reference design with  $T_c = 25\text{ }^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{ V}$ , unless otherwise noted.

|                      | MIN | TYP | MAX | UNIT          |
|----------------------|-----|-----|-----|---------------|
| Calibrated frequency |     | 2   |     | MHz           |
| Start-up time        |     | 5   |     | $\mu\text{s}$ |

**Table 5-6. 32.768 kHz Crystal Oscillator (XOSC\_LF)**

Measured on a Texas Instruments reference design with  $T_c = 25\text{ }^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{ V}$ , unless otherwise noted.

|       | MIN | TYP              | MAX | UNIT       |
|-------|-----|------------------|-----|------------|
|       |     | 32.768           |     | kHz        |
| ESR   |     | 30               | 100 | k $\Omega$ |
| $C_L$ | 6   | 7 <sup>(1)</sup> | 12  | pF         |

- (1) Default load capacitance using TI reference designs including parasitic capacitance. Crystals with different load capacitance may be used.

**Table 5-7. 32 kHz RC Oscillator (RCOSC\_LF)**

Measured on a Texas Instruments reference design with  $T_c = 25\text{ }^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{ V}$ , unless otherwise noted.

|                         | MIN | TYP                 | MAX | UNIT                  |
|-------------------------|-----|---------------------|-----|-----------------------|
| Calibrated frequency    |     | 32.8 <sup>(1)</sup> |     | kHz                   |
| Temperature coefficient |     | 50                  |     | ppm/ $^\circ\text{C}$ |

- (1) When using RCOSC\_LF as source for the low frequency system clock (SCLK\_LF), the accuracy of the SCLK\_LF-derived Real Time Clock (RTC) can be improved by measuring RCOSC\_LF relative to XOSC\_HF and compensating for the RTC tick speed. This functionality is available through the TI-provided Power driver.

### 5.21.2 Synchronous Serial Interface (SSI) Characteristics

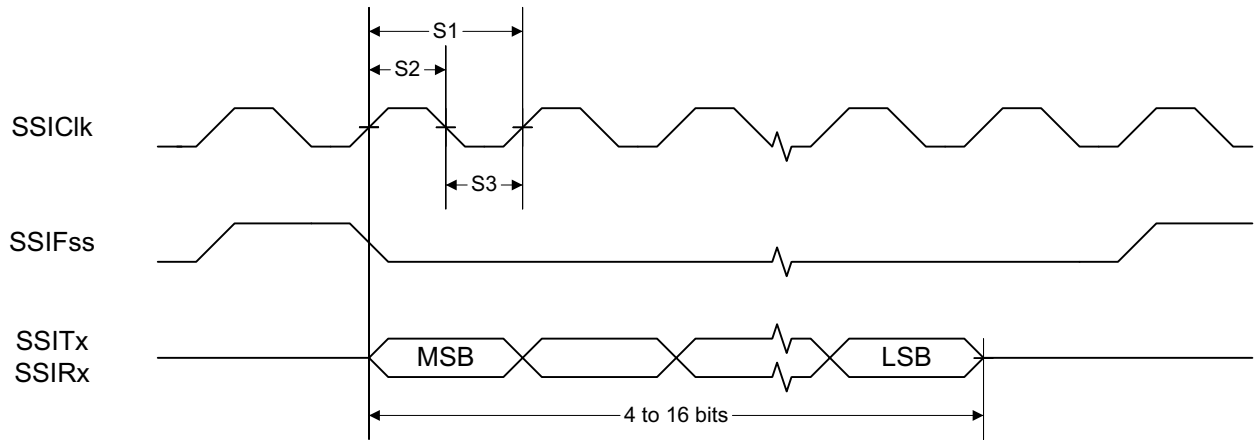
**Table 5-8. Synchronous Serial Interface (SSI) Characteristics**

over operating free-air temperature range (unless otherwise noted)

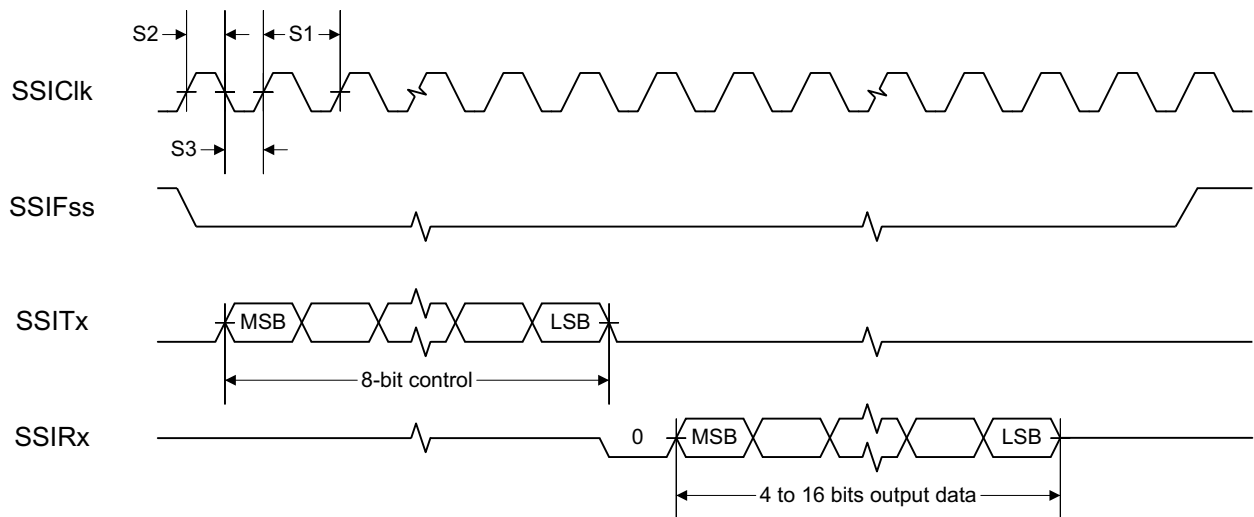
| PARAMETER NO.     | PARAMETER       |                   | MIN | TYP | MAX   | UNIT                         |
|-------------------|-----------------|-------------------|-----|-----|-------|------------------------------|
| S1                | $t_{clk\_per}$  | SSIClk cycle time | 12  |     | 65024 | System Clocks <sup>(1)</sup> |
| S2 <sup>(2)</sup> | $t_{clk\_high}$ | SSIClk high time  |     | 0.5 |       | $t_{clk\_per}$               |
| S3 <sup>(2)</sup> | $t_{clk\_low}$  | SSIClk low time   |     | 0.5 |       | $t_{clk\_per}$               |

(1) When using the TI-provided Power driver, the SSI system clock is always 48 MHz.

(2) Refer to SSI timing diagrams [Figure 5-1](#), [Figure 5-2](#), and [Figure 5-3](#).



**Figure 5-1. SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement**



**Figure 5-2. SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer**



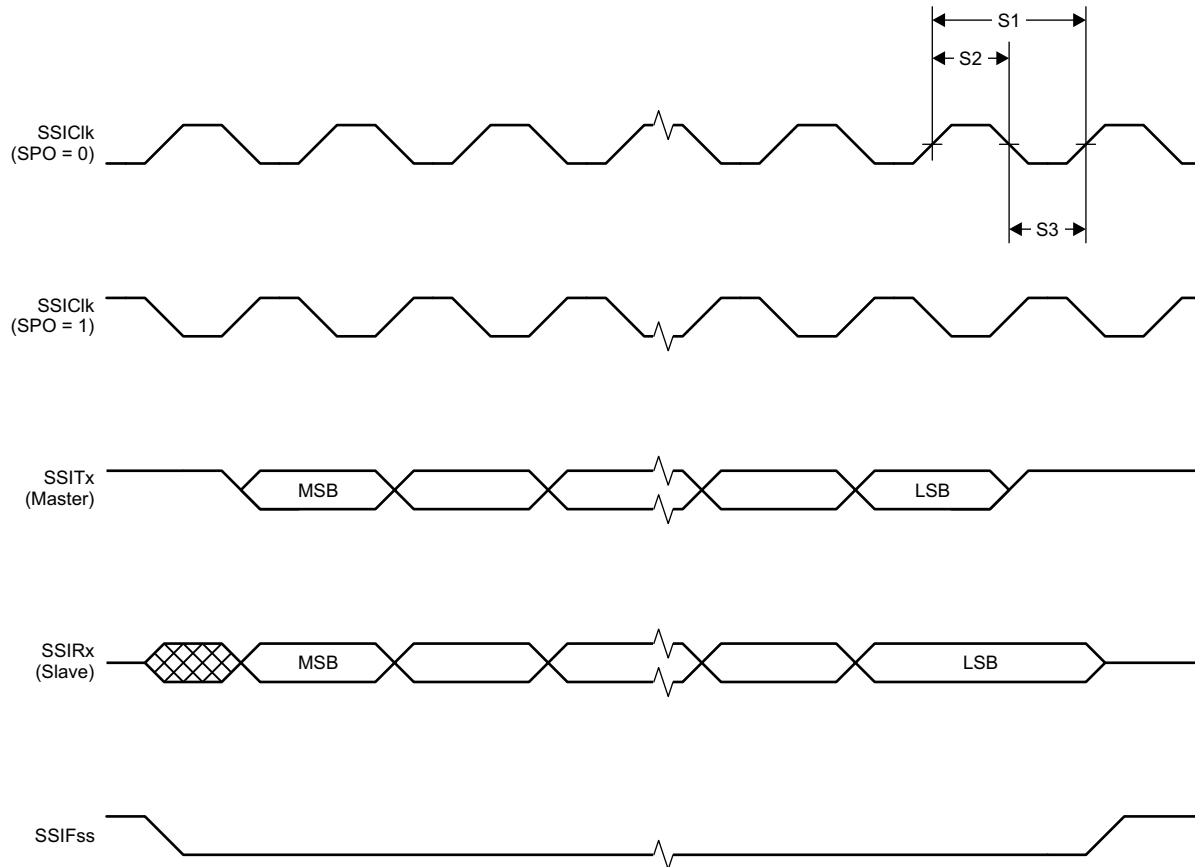


Figure 5-3. SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1

### 5.21.3 UART

Table 5-9. UART Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | MIN | TYP | MAX | UNIT  |
|-----------|-----|-----|-----|-------|
| UART rate |     |     | 3   | MBaud |

## 5.22 Peripheral Characteristics

### 5.22.1 ADC

**Table 5-10. Analog-to-Digital Converter (ADC) Characteristics**

$T_c = 25\text{ }^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$  and voltage scaling enabled, unless otherwise noted.<sup>(1)</sup>

Performance numbers require use of offset and gain adjustments in software by TI-provided ADC drivers.

| PARAMETER          |                                      | TEST CONDITIONS   | MIN | TYP                   | MAX  | UNIT         |
|--------------------|--------------------------------------|---|-----|-----------------------|------|--------------|
|                    | Input voltage range                  |   | 0   |                       | VDDS | V            |
|                    | Resolution                           |   |     | 12                    |      | Bits         |
|                    | Sample Rate                          |   |     |                       | 200  | ksps         |
|                    | Offset                               | Internal 4.3 V equivalent reference <sup>(2)</sup>  |     | -0.24                 |      | LSB          |
|                    | Gain error                           | Internal 4.3 V equivalent reference <sup>(2)</sup>  |     | 7.14                  |      | LSB          |
| DNL <sup>(3)</sup> | Differential nonlinearity            |   |     | >-1                   |      | LSB          |
| INL                | Integral nonlinearity                |   |     | ±4                    |      | LSB          |
| ENOB               | Effective number of bits             | Internal 4.3 V equivalent reference <sup>(2)</sup> , 200 kSamples/s, 9.6 kHz input tone   |     | 9.8                   |      | Bits         |
|                    |                                      | Internal 4.3 V equivalent reference <sup>(2)</sup> , 200 kSamples/s, 9.6 kHz input tone, DC/DC enabled  |     | 9.8                   |      |              |
|                    |                                      | VDDS as reference, 200 kSamples/s, 9.6 kHz input tone   |     | 10.1                  |      |              |
|                    |                                      | Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone   |     | 11.1                  |      |              |
|                    |                                      | Internal reference, voltage scaling disabled, 14-bit mode, 200 kSamples/s, 300 Hz input tone <sup>(4)</sup>   |     | 11.3                  |      |              |
|                    |                                      | Internal reference, voltage scaling disabled, 15-bit mode, 200 kSamples/s, 300 Hz input tone <sup>(4)</sup>   |     | 11.6                  |      |              |
| THD                | Total harmonic distortion            | Internal 4.3 V equivalent reference <sup>(2)</sup> , 200 kSamples/s, 9.6 kHz input tone   |     | -65                   |      | Bits         |
|                    |                                      | VDDS as reference, 200 kSamples/s, 9.6 kHz input tone   |     | -70                   |      |              |
|                    |                                      | Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone   |     | -72                   |      |              |
| SINAD, SNDR        | Signal-to-noise and distortion ratio | Internal 4.3 V equivalent reference <sup>(2)</sup> , 200 kSamples/s, 9.6 kHz input tone   |     | 60                    |      | dB           |
|                    |                                      | VDDS as reference, 200 kSamples/s, 9.6 kHz input tone   |     | 63                    |      |              |
|                    |                                      | Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone   |     | 68                    |      |              |
| SFDR               | Spurious-free dynamic range          | Internal 4.3 V equivalent reference <sup>(2)</sup> , 200 kSamples/s, 9.6 kHz input tone   |     | 70                    |      | dB           |
|                    |                                      | VDDS as reference, 200 kSamples/s, 9.6 kHz input tone   |     | 73                    |      |              |
|                    |                                      | Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone   |     | 75                    |      |              |
|                    | Conversion time                      | Serial conversion, time-to-output, 24 MHz clock   |     | 50                    |      | Clock Cycles |
|                    | Current consumption                  | Internal 4.3 V equivalent reference <sup>(2)</sup>  |     | 0.42                  |      | mA           |
|                    | Current consumption                  | VDDS as reference   |     | 0.6                   |      | mA           |
|                    | Reference voltage                    | Equivalent fixed internal reference (input voltage scaling enabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1   |     | 4.3 <sup>(2)(5)</sup> |      | V            |
|                    | Reference voltage                    | Fixed internal reference (input voltage scaling disabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1. This value is derived from the scaled value (4.3 V) as follows:<br>$V_{ref} = 4.3\text{ V} \times 1408 / 4095$ |     | 1.48                  |      | V            |
|                    | Reference voltage                    | VDDS as reference, input voltage scaling enabled  |     | VDDS                  |      | V            |

(1) Using IEEE Std 1241-2010 for terminology and test methods

(2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V

(3) No missing codes

(4)  $ADC\_output = \Sigma(4^n \text{ samples}) \gg n$ ,  $n$  = desired extra bits

(5) Applied voltage must be within Absolute Maximum Ratings (see Section 5.1) at all times

**Table 5-10. Analog-to-Digital Converter (ADC) Characteristics (continued)**

$T_c = 25\text{ }^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$  and voltage scaling enabled, unless otherwise noted.<sup>(1)</sup>

Performance numbers require use of offset and gain adjustments in software by TI-provided ADC drivers.

| PARAMETER |                   | TEST CONDITIONS  | MIN | TYP                    | MAX | UNIT       |
|-----------|-------------------|--|-----|------------------------|-----|------------|
|           | Reference voltage | VDDS as reference, input voltage scaling disabled  |     | $V_{DD5} / 2.82^{(5)}$ |     | V          |
|           | Input impedance   | 200 kSamples/s, voltage scaling enabled. Capacitive input, Input impedance depends on sampling frequency and sampling time |     | >1                     |     | M $\Omega$ |

## 5.22.2 DAC

**Table 5-11. Digital-to-Analog Converter (DAC) Characteristics**
 $T_c = 25\text{ }^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$ , unless otherwise noted.

| PARAMETER  |   | TEST CONDITIONS   | MIN | TYP        | MAX  | UNIT               |
|--|---|---|-----|------------|------|--------------------|
| <b>General Parameters</b>  |   |   |     |            |      |                    |
|  | Resolution  |   |     | 8          |      | Bits               |
| $V_{DD5}$  | Supply voltage  | Any load, any $V_{REF}$ , pre-charge OFF, DAC charge-pump ON  | 1.8 |            | 3.8  | V                  |
|  |   | External Load <sup>(1)</sup> , any $V_{REF}$ , pre-charge OFF, DAC charge-pump OFF                                    | 2.0 |            | 3.8  |                    |
|  |   | Any load, $V_{REF} = \text{DCOUP}$ L, pre-charge ON   | 2.6 |            | 3.8  |                    |
| $F_{DAC}$  | Clock frequency   | Buffer ON (recommended for external load)   | 16  |            | 250  | kHz                |
|  |   | Buffer OFF (internal load)  | 16  |            | 1000 |                    |
|  | Voltage output settling time  | $V_{REF} = V_{DD5}$ , buffer OFF, internal load   |     | 13         |      | $1 / F_{DAC}$      |
|  |   | $V_{REF} = V_{DD5}$ , buffer ON, external capacitive load = 20 pF <sup>(2)</sup>                                      |     | 13.8       |      |                    |
|  | External capacitive load  |   |     | 20         | 200  | pF                 |
|  | External resistive load   |   | 10  |            |      | M $\Omega$         |
|  | Short circuit current   |   |     |            | 400  | $\mu\text{A}$      |
| $Z_{MAX}$  | Max output impedance $V_{ref} = V_{DD5}$ , buffer ON, CLK 250 kHz                     | $V_{DD5} = 3.8\text{ V}$ , DAC charge-pump OFF  |     | 50.8       |      | k $\Omega$         |
|  |   | $V_{DD5} = 3.0\text{ V}$ , DAC charge-pump ON   |     | 51.7       |      |                    |
|  |   | $V_{DD5} = 3.0\text{ V}$ , DAC charge-pump OFF  |     | 53.2       |      |                    |
|  |   | $V_{DD5} = 2.0\text{ V}$ , DAC charge-pump ON   |     | 48.7       |      |                    |
|  |   | $V_{DD5} = 2.0\text{ V}$ , DAC charge-pump OFF  |     | 70.2       |      |                    |
|  |   | $V_{DD5} = 1.8\text{ V}$ , DAC charge-pump ON   |     | 46.3       |      |                    |
|  |   | $V_{DD5} = 1.8\text{ V}$ , DAC charge-pump OFF  |     | 88.9       |      |                    |
| <b>Internal Load - Continuous Time Comparator / Low Power Clocked Comparator</b> |   |   |     |            |      |                    |
| DNL  | Differential nonlinearity   | $V_{REF} = V_{DD5}$ , load = Continuous Time Comparator or Low Power Clocked Comparator<br>$F_{DAC} = 250\text{ kHz}$ |     | $\pm 1$    |      | LSB <sup>(3)</sup> |
|  | Differential nonlinearity   | $V_{REF} = V_{DD5}$ , load = Continuous Time Comparator or Low Power Clocked Comparator<br>$F_{DAC} = 16\text{ kHz}$  |     | $\pm 1.2$  |      |                    |
|  | Offset error <sup>(4)</sup><br>Load = Continuous Time Comparator                      | $V_{REF} = V_{DD5} = 3.8\text{ V}$  |     | $\pm 0.64$ |      | LSB <sup>(3)</sup> |
|  |   | $V_{REF} = V_{DD5} = 3.0\text{ V}$  |     | $\pm 0.81$ |      |                    |
|  |   | $V_{REF} = V_{DD5} = 1.8\text{ V}$  |     | $\pm 1.27$ |      |                    |
|  |   | $V_{REF} = \text{DCOUP}$ L, pre-charge ON   |     | $\pm 3.43$ |      |                    |
|  |   | $V_{REF} = \text{DCOUP}$ L, pre-charge OFF  |     | $\pm 2.88$ |      |                    |
|  |   | $V_{REF} = \text{ADCREF}$   |     | $\pm 2.37$ |      |                    |
|  | Offset error <sup>(4)</sup><br>Load = Low Power Clocked Comparator                    | $V_{REF} = V_{DD5} = 3.8\text{ V}$  |     | $\pm 0.78$ |      | LSB <sup>(3)</sup> |
|  |   | $V_{REF} = V_{DD5} = 3.0\text{ V}$  |     | $\pm 0.77$ |      |                    |
|  |   | $V_{REF} = V_{DD5} = 1.8\text{ V}$  |     | $\pm 3.46$ |      |                    |
|  |   | $V_{REF} = \text{DCOUP}$ L, pre-charge ON   |     | $\pm 3.44$ |      |                    |
|  |   | $V_{REF} = \text{DCOUP}$ L, pre-charge OFF  |     | $\pm 4.70$ |      |                    |
|  |   | $V_{REF} = \text{ADCREF}$   |     | $\pm 4.11$ |      |                    |
|  | Max code output voltage variation <sup>(4)</sup><br>Load = Continuous Time Comparator | $V_{REF} = V_{DD5} = 3.8\text{ V}$  |     | $\pm 1.53$ |      | LSB <sup>(3)</sup> |
|  |   | $V_{REF} = V_{DD5} = 3.0\text{ V}$  |     | $\pm 1.71$ |      |                    |
|  |   | $V_{REF} = V_{DD5} = 1.8\text{ V}$  |     | $\pm 2.10$ |      |                    |
|  |   | $V_{REF} = \text{DCOUP}$ L, pre-charge ON   |     | $\pm 6.00$ |      |                    |
|  |   | $V_{REF} = \text{DCOUP}$ L, pre-charge OFF  |     | $\pm 3.85$ |      |                    |
|  |   | $V_{REF} = \text{ADCREF}$   |     | $\pm 5.84$ |      |                    |

(1) Keysight 34401A Multimeter

(2) A load &gt; 20 pF will increase the settling time

(3) 1 LSB ( $V_{REF} = 3.8\text{ V}/3.0\text{ V}/1.8\text{ V}/\text{DCOUP}/\text{ADCREF}$ ) = 14.10 mV/11.13 mV/6.68 mV/4.67 mV/5.48 mV

(4) Includes comparator offset

**Table 5-11. Digital-to-Analog Converter (DAC) Characteristics (continued)**
 $T_c = 25\text{ }^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$ , unless otherwise noted.

| PARAMETER   | TEST CONDITIONS  | MIN   | TYP   | MAX   | UNIT               |
|---|--|---|-------|-------|--------------------|
| Max code output voltage variation <sup>(4)</sup><br>Load = Low Power Clocked Comparator | $V_{REF} = V_{DD5} = 3.8\text{ V}$   |   | ±2.92 |       | LSB <sup>(3)</sup> |
|   | $V_{REF} = V_{DD5} = 3.0\text{ V}$   |   | ±3.06 |       |                    |
|   | $V_{REF} = V_{DD5} = 1.8\text{ V}$   |   | ±3.91 |       |                    |
|   | $V_{REF} = \text{DCOUPPL}$ , pre-charge ON                                 |   | ±7.84 |       |                    |
|   | $V_{REF} = \text{DCOUPPL}$ , pre-charge OFF                                |   | ±4.06 |       |                    |
|   | $V_{REF} = \text{ADCREFL}$   |   | ±6.94 |       |                    |
| Output voltage range <sup>(4)</sup><br>Load = Continuous Time Comparator                | $V_{REF} = V_{DD5} = 3.8\text{ V}$ , code 1                                |   | 0.03  |       | V                  |
|   | $V_{REF} = V_{DD5} = 3.8\text{ V}$ , code 255                              |   | 3.62  |       |                    |
|   | $V_{REF} = V_{DD5} = 3.0\text{ V}$ , code 1                                |   | 0.02  |       |                    |
|   | $V_{REF} = V_{DD5} = 3.0\text{ V}$ , code 255                              |   | 2.86  |       |                    |
|   | $V_{REF} = V_{DD5} = 1.8\text{ V}$ , code 1                                |   | 0.01  |       |                    |
|   | $V_{REF} = V_{DD5} = 1.8\text{ V}$ , code 255                              |   | 1.71  |       |                    |
|   | $V_{REF} = \text{DCOUPPL}$ , pre-charge OFF, code 1                        |   | 0.01  |       |                    |
|   | $V_{REF} = \text{DCOUPPL}$ , pre-charge OFF, code 255                      |   | 1.21  |       |                    |
|   | $V_{REF} = \text{DCOUPPL}$ , pre-charge ON, code 1                         |   | 1.27  |       |                    |
|   | $V_{REF} = \text{DCOUPPL}$ , pre-charge ON, code 255                       |   | 2.46  |       |                    |
|   | $V_{REF} = \text{ADCREFL}$ , code 1  |   | 0.01  |       |                    |
|   | $V_{REF} = \text{ADCREFL}$ , code 255                                      |   | 1.41  |       |                    |
|   | Output voltage range <sup>(4)</sup><br>Load = Low Power Clocked Comparator | $V_{REF} = V_{DD5} = 3.8\text{ V}$ , code 1             |       | 0.03  |                    |
| $V_{REF} = V_{DD5} = 3.8\text{ V}$ , code 255   |  |   | 3.61  |       |                    |
| $V_{REF} = V_{DD5} = 3.0\text{ V}$ , code 1   |  |   | 0.02  |       |                    |
| $V_{REF} = V_{DD5} = 3.0\text{ V}$ , code 255   |  |   | 2.85  |       |                    |
| $V_{REF} = V_{DD5} = 1.8\text{ V}$ , code 1   |  |   | 0.01  |       |                    |
| $V_{REF} = V_{DD5} = 1.8\text{ V}$ , code 255   |  |   | 1.71  |       |                    |
| $V_{REF} = \text{DCOUPPL}$ , pre-charge OFF, code 1                                     |  |   | 0.01  |       |                    |
| $V_{REF} = \text{DCOUPPL}$ , pre-charge OFF, code 255                                   |  |   | 1.21  |       |                    |
| $V_{REF} = \text{DCOUPPL}$ , pre-charge ON, code 1                                      |  |   | 1.27  |       |                    |
| $V_{REF} = \text{DCOUPPL}$ , pre-charge ON, code 255                                    |  |   | 2.46  |       |                    |
| $V_{REF} = \text{ADCREFL}$ , code 1   |  |   | 0.01  |       |                    |
| $V_{REF} = \text{ADCREFL}$ , code 255   |  |   | 1.41  |       |                    |
| <b>External Load (Keysight 34401A Multimeter)</b>                                       |  |   |       |       |                    |
| INL   | Integral nonlinearity  | $V_{REF} = V_{DD5}$ , $F_{DAC} = 250\text{ kHz}$        |       | ±1    | LSB <sup>(3)</sup> |
|   |  | $V_{REF} = \text{DCOUPPL}$ , $F_{DAC} = 250\text{ kHz}$ |       | ±1    |                    |
|   |  | $V_{REF} = \text{ADCREFL}$ , $F_{DAC} = 250\text{ kHz}$ |       | ±1    |                    |
| DNL   | Differential nonlinearity  | $V_{REF} = V_{DD5}$ , $F_{DAC} = 250\text{ kHz}$        |       | ±1    | LSB <sup>(3)</sup> |
| Offset error  |  | $V_{REF} = V_{DD5} = 3.8\text{ V}$                      |       | ±0.20 | LSB <sup>(3)</sup> |
|   |  | $V_{REF} = V_{DD5} = 3.0\text{ V}$                      |       | ±0.25 |                    |
|   |  | $V_{REF} = V_{DD5} = 1.8\text{ V}$                      |       | ±0.45 |                    |
|   |  | $V_{REF} = \text{DCOUPPL}$ , pre-charge ON              |       | ±1.55 |                    |
|   |  | $V_{REF} = \text{DCOUPPL}$ , pre-charge OFF             |       | ±1.30 |                    |
|   |  | $V_{REF} = \text{ADCREFL}$                              |       | ±1.10 |                    |
| Max code output voltage variation   |  | $V_{REF} = V_{DD5} = 3.8\text{ V}$                      |       | ±0.60 | LSB <sup>(3)</sup> |
|   |  | $V_{REF} = V_{DD5} = 3.0\text{ V}$                      |       | ±0.55 |                    |
|   |  | $V_{REF} = V_{DD5} = 1.8\text{ V}$                      |       | ±0.60 |                    |
|   |  | $V_{REF} = \text{DCOUPPL}$ , pre-charge ON              |       | ±3.45 |                    |
|   |  | $V_{REF} = \text{DCOUPPL}$ , pre-charge OFF             |       | ±2.10 |                    |
|   |  | $V_{REF} = \text{ADCREFL}$                              |       | ±1.90 |                    |

**Table 5-11. Digital-to-Analog Converter (DAC) Characteristics (continued)**

$T_c = 25\text{ }^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$ , unless otherwise noted.

| PARAMETER  | TEST CONDITIONS                                       | MIN | TYP  | MAX | UNIT |
|--|---|-----|------|-----|------|
| Output voltage range<br>Load = Low Power Clocked<br>Comparator | $V_{REF} = V_{DD5} = 3.8\text{ V}$ , code 1           |     | 0.03 |     | V    |
|  | $V_{REF} = V_{DD5} = 3.8\text{ V}$ , code 255         |     | 3.61 |     |      |
|  | $V_{REF} = V_{DD5} = 3.0\text{ V}$ , code 1           |     | 0.02 |     |      |
|  | $V_{REF} = V_{DD5} = 3.0\text{ V}$ , code 255         |     | 2.85 |     |      |
|  | $V_{REF} = V_{DD5} = 1.8\text{ V}$ , code 1           |     | 0.02 |     |      |
|  | $V_{REF} = V_{DD5} = 1.8\text{ V}$ , code 255         |     | 1.71 |     |      |
|  | $V_{REF} = \text{DCOUPPL}$ , pre-charge OFF, code 1   |     | 0.02 |     |      |
|  | $V_{REF} = \text{DCOUPPL}$ , pre-charge OFF, code 255 |     | 1.20 |     |      |
|  | $V_{REF} = \text{DCOUPPL}$ , pre-charge ON, code 1    |     | 1.27 |     |      |
|  | $V_{REF} = \text{DCOUPPL}$ , pre-charge ON, code 255  |     | 2.46 |     |      |
|  | $V_{REF} = \text{ADCREFL}$ , code 1                   |     | 0.02 |     |      |
|  | $V_{REF} = \text{ADCREFL}$ , code 255                 |     | 1.42 |     |      |

### 5.22.3 Temperature and Battery Monitor

**Table 5-12. Temperature Sensor**

 Measured on a Texas Instruments reference design with  $T_c = 25\text{ }^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{ V}$ , unless otherwise noted.

| PARAMETER                                 | TEST CONDITIONS                            | MIN | TYP       | MAX | UNIT                      |
|---|--|-----|-----------|-----|---------------------------|
| Resolution                                |  |     | 2         |     | $^\circ\text{C}$          |
| Accuracy                                  | -40 $^\circ\text{C}$ to 0 $^\circ\text{C}$ |     | $\pm 4.0$ |     | $^\circ\text{C}$          |
| Accuracy                                  | 0 $^\circ\text{C}$ to 105 $^\circ\text{C}$ |     | $\pm 2.5$ |     | $^\circ\text{C}$          |
| Supply voltage coefficient <sup>(1)</sup> |  |     | 3.6       |     | $^\circ\text{C}/\text{V}$ |

(1) The temperature sensor is automatically compensated for VDDS variation when using the TI-provided driver.

**Table 5-13. Battery Monitor**

 Measured on a Texas Instruments reference design with  $T_c = 25\text{ }^\circ\text{C}$ , unless otherwise noted.

| PARAMETER                   | TEST CONDITIONS | MIN | TYP  | MAX | UNIT |
|-----------------------------|-----------------|-----|------|-----|------|
| Resolution                  |                 |     | 25   |     | mV   |
| Range                       |                 | 1.8 |      | 3.8 | V    |
| Integral nonlinearity (max) |                 |     | 23   |     | mV   |
| Accuracy                    | VDDS = 3.0 V    |     | 22.5 |     | mV   |
| Offset error                |                 |     | -32  |     | mV   |
| Gain error                  |                 |     | -1   |     | %    |

## 5.22.4 Comparators

**Table 5-14. Low-Power Clocked Comparator**

$T_c = 25\text{ }^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$ , unless otherwise noted.

| PARAMETER                                 | TEST CONDITIONS  | MIN | TYP           | MAX       | UNIT        |
|---|--|-----|---------------|-----------|-------------|
| Input voltage range                       |  | 0   |               | $V_{DD5}$ | V           |
| Clock frequency                           |  |     | SCLK_LF       |           |             |
| Internal reference voltage <sup>(1)</sup> | Using internal DAC with $V_{DD5}$ as reference voltage, DAC code = 0 - 255 |     | 0.024 - 2.865 |           | V           |
| Offset                                    | Measured at $V_{DD5} / 2$ , includes error from internal DAC               |     | $\pm 5$       |           | mV          |
| Decision time                             | Step from $-50\text{ mV}$ to $50\text{ mV}$                                |     | 1             |           | Clock Cycle |

(1) The comparator can use an internal 8 bits DAC as its reference. The DAC output voltage range depends on the reference voltage selected. See [Table 5-11](#)

**Table 5-15. Continuous Time Comparator**

$T_c = 25\text{ }^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$ , unless otherwise noted.

| PARAMETER                          | TEST CONDITIONS                             | MIN | TYP     | MAX       | UNIT          |
|------------------------------------|---|-----|---------|-----------|---------------|
| Input voltage range <sup>(1)</sup> |   | 0   |         | $V_{DD5}$ | V             |
| Offset                             | Measured at $V_{DD5} / 2$                   |     | $\pm 5$ |           | mV            |
| Decision time                      | Step from $-10\text{ mV}$ to $10\text{ mV}$ |     | 0.78    |           | $\mu\text{s}$ |
| Current consumption                | Internal reference                          |     | 8.6     |           | $\mu\text{A}$ |

(1) The input voltages can be generated externally and connected throughout I/Os or an internal reference voltage can be generated using the DAC

## 5.22.5 Current Source

**Table 5-16. Programmable Current Source**

$T_c = 25\text{ }^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$ , unless otherwise noted.

| PARAMETER  | TEST CONDITIONS | MIN | TYP       | MAX | UNIT          |
|--|-----------------|-----|-----------|-----|---------------|
| Current source programmable output range (logarithmic range) |                 |     | 0.25 - 20 |     | $\mu\text{A}$ |
| Resolution   |                 |     | 0.25      |     | $\mu\text{A}$ |



## 5.22.6 GPIO

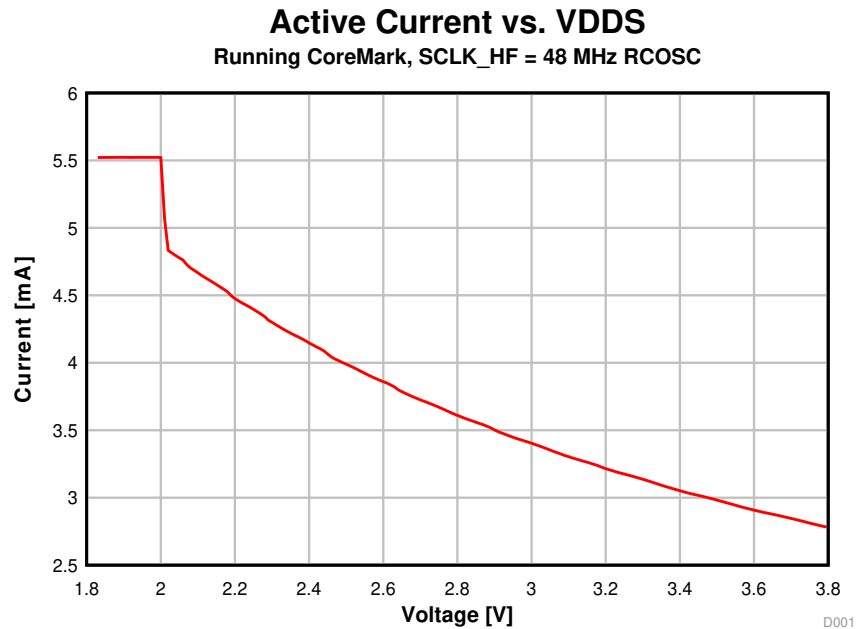
**Table 5-17. GPIO DC Characteristics**

| PARAMETER   | TEST CONDITIONS   | MIN                  | TYP  | MAX | UNIT |
|---|---|----------------------|------|-----|------|
| <b>T<sub>A</sub> = 25 °C, V<sub>DD5</sub> = 1.8 V</b> |   |                      |      |     |      |
| GPIO VOH at 8 mA load                                 | IOCURR = 2, high-drive GPIOs only                               |                      | 1.56 |     | V    |
| GPIO VOL at 8 mA load                                 | IOCURR = 2, high-drive GPIOs only                               |                      | 0.24 |     | V    |
| GPIO VOH at 4 mA load                                 | IOCURR = 1  |                      | 1.59 |     | V    |
| GPIO VOL at 4 mA load                                 | IOCURR = 1  |                      | 0.21 |     | V    |
| GPIO pullup current                                   | Input mode, pullup enabled, Vpad = 0 V                          |                      | 73   |     | μA   |
| GPIO pulldown current                                 | Input mode, pulldown enabled, Vpad = VDD5                       |                      | 19   |     | μA   |
| GPIO low-to-high input transition, with hysteresis    | IH = 1, transition voltage for input read as 0 → 1              |                      | 1.08 |     | V    |
| GPIO high-to-low input transition, with hysteresis    | IH = 1, transition voltage for input read as 1 → 0              |                      | 0.73 |     | V    |
| GPIO input hysteresis                                 | IH = 1, difference between 0 → 1 and 1 → 0 points               |                      | 0.35 |     | V    |
| <b>T<sub>A</sub> = 25 °C, V<sub>DD5</sub> = 3.0 V</b> |   |                      |      |     |      |
| GPIO VOH at 8 mA load                                 | IOCURR = 2, high-drive GPIOs only                               |                      | 2.59 |     | V    |
| GPIO VOL at 8 mA load                                 | IOCURR = 2, high-drive GPIOs only                               |                      | 0.42 |     | V    |
| GPIO VOH at 4 mA load                                 | IOCURR = 1  |                      | 2.63 |     | V    |
| GPIO VOL at 4 mA load                                 | IOCURR = 1  |                      | 0.40 |     | V    |
| <b>T<sub>A</sub> = 25 °C, V<sub>DD5</sub> = 3.8 V</b> |   |                      |      |     |      |
| GPIO pullup current                                   | Input mode, pullup enabled, Vpad = 0 V                          |                      | 282  |     | μA   |
| GPIO pulldown current                                 | Input mode, pulldown enabled, Vpad = VDD5                       |                      | 110  |     | μA   |
| GPIO low-to-high input transition, with hysteresis    | IH = 1, transition voltage for input read as 0 → 1              |                      | 1.97 |     | V    |
| GPIO high-to-low input transition, with hysteresis    | IH = 1, transition voltage for input read as 1 → 0              |                      | 1.55 |     | V    |
| GPIO input hysteresis                                 | IH = 1, difference between 0 → 1 and 1 → 0 points               |                      | 0.42 |     | V    |
| <b>T<sub>A</sub> = 25 °C</b>                          |   |                      |      |     |      |
| VIH   | Lowest GPIO input voltage reliably interpreted as a <i>High</i> | 0.8*V <sub>DD5</sub> |      |     | V    |
| VIL   | Highest GPIO input voltage reliably interpreted as a <i>Low</i> | 0.2*V <sub>DD5</sub> |      |     | V    |

## 5.23 Typical Characteristics

All measurements in this section are done with  $T_c = 25\text{ }^\circ\text{C}$  and  $V_{\text{DDS}} = 3.0\text{ V}$ , unless otherwise noted. See *Recommended Operating Conditions*, [Section 5.3](#), for device limits. Values exceeding these limits are for reference only.

### 5.23.1 MCU Current



**Figure 5-4. Active Mode (MCU) Current vs. Supply Voltage (VDDS)**

**Standby Current vs. Temperature**  
80 kB RAM Retention, no Cache Retention, RTC On  
SCLK\_LF = 32 kHz XOSC

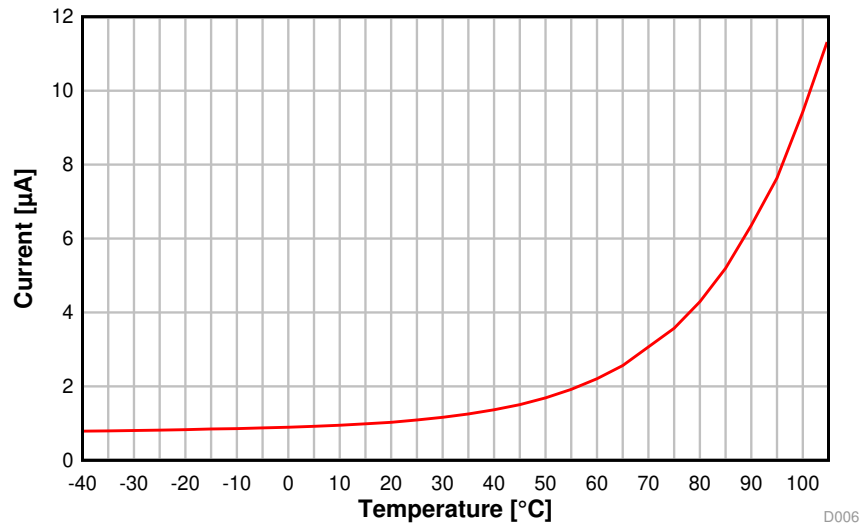


Figure 5-5. Standby Mode (MCU) Current vs. Temperature

**Standby Current vs. Temperature**  
80 kB RAM Retention, no Cache Retention, RTC On  
SCLK\_LF = 32 kHz XOSC VDD5 = 3.6 V

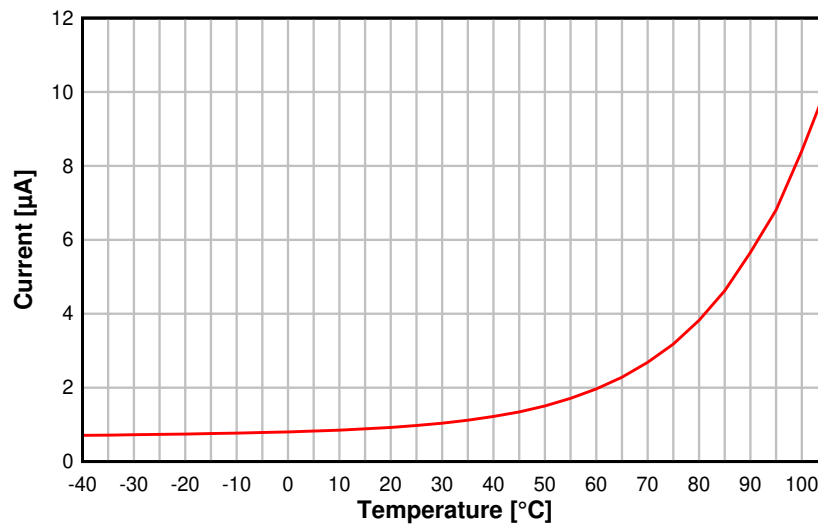
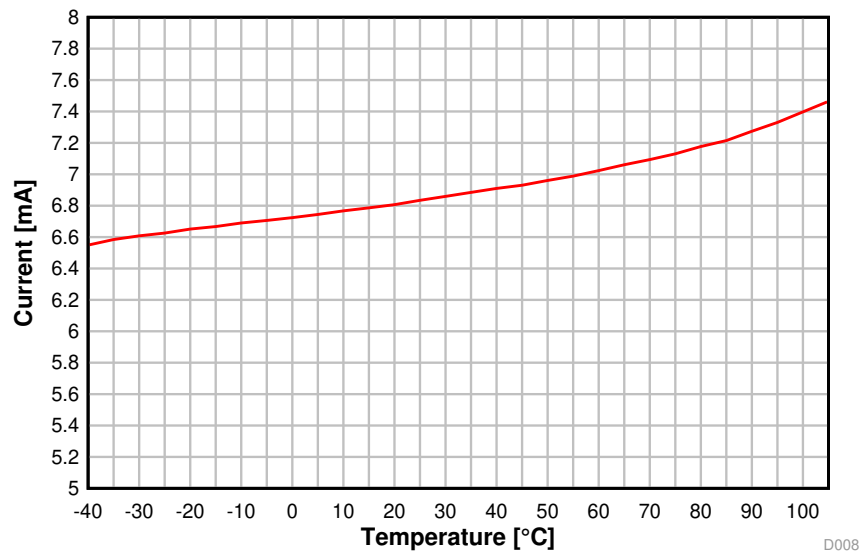


Figure 5-6. Standby Mode (MCU) Current vs. Temperature (VDD5 = 3.6 V)

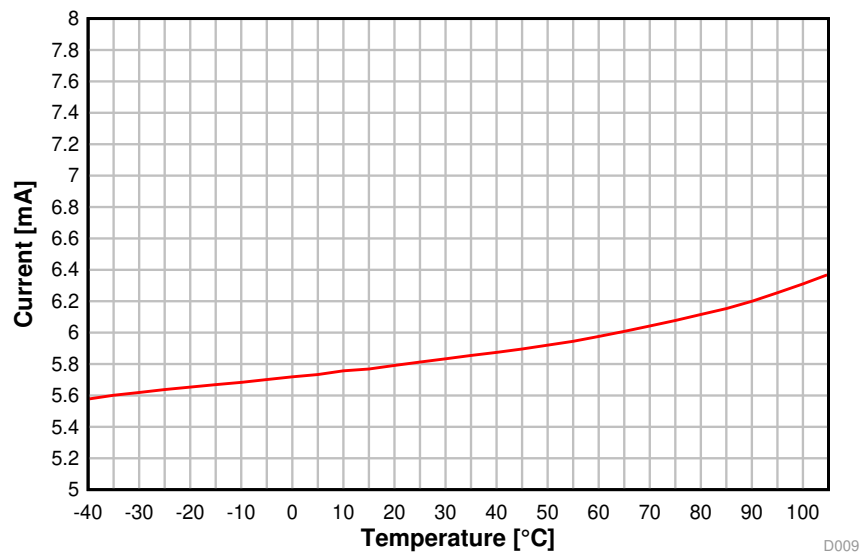
5.23.2 RX Current

**RX Current vs. Temperature**  
50 kbps, 868.3 MHz



**Figure 5-7. RX Current vs. Temperature (50 kbps, 868.3 MHz)**

**RX Current vs. Temperature**  
50 kbps, 868.3 MHz, VDD5 = 3.6 V



**Figure 5-8. RX Current vs. Temperature (50 kbps, 868.3 MHz, VDD5 = 3.6 V)**

### RX Current vs. Temperature BLE 1 Mbps, 2.44 GHz

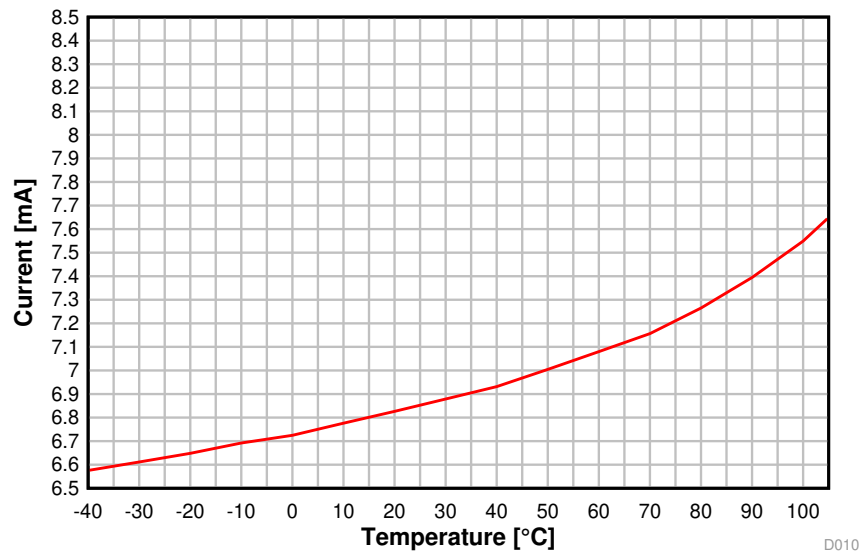


Figure 5-9. RX Current vs. Temperature (BLE 1 Mbps, 2.44 GHz)

### RX Current vs. VDD5 50 kbps, 868.3 MHz

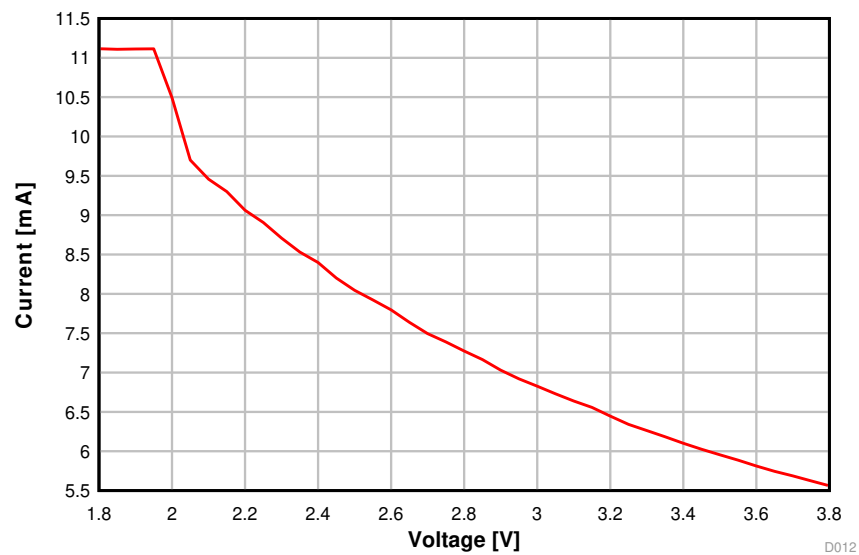


Figure 5-10. RX Current vs. Supply Voltage (VDD5) (50 kbps, 868.3 MHz)

### RX Current vs. VDD5 BLE 1 Mbps, 2.44 GHz

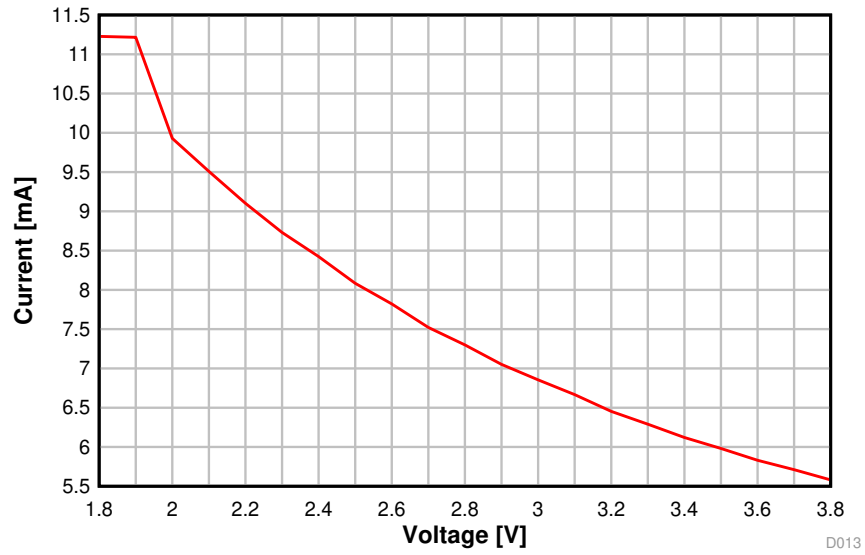
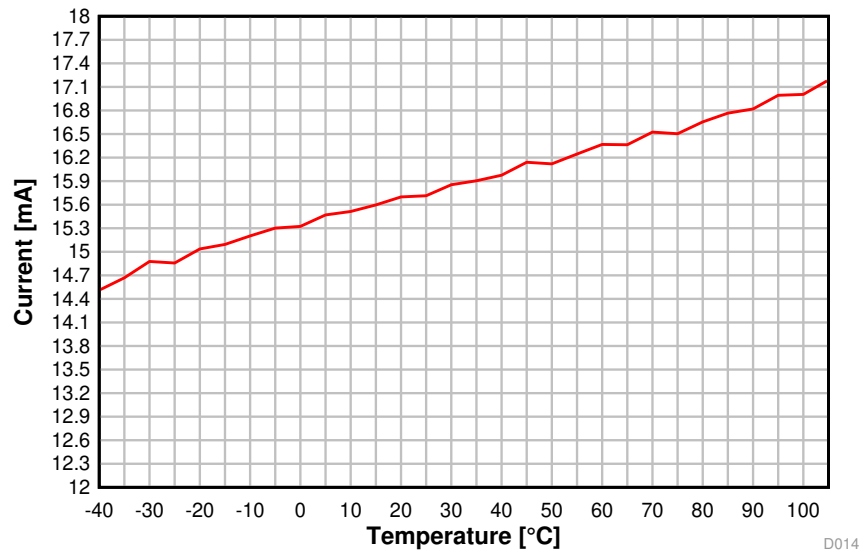


Figure 5-11. RX Current vs. Supply Voltage (VDD5) (BLE 1 Mbps, 2.44 GHz)

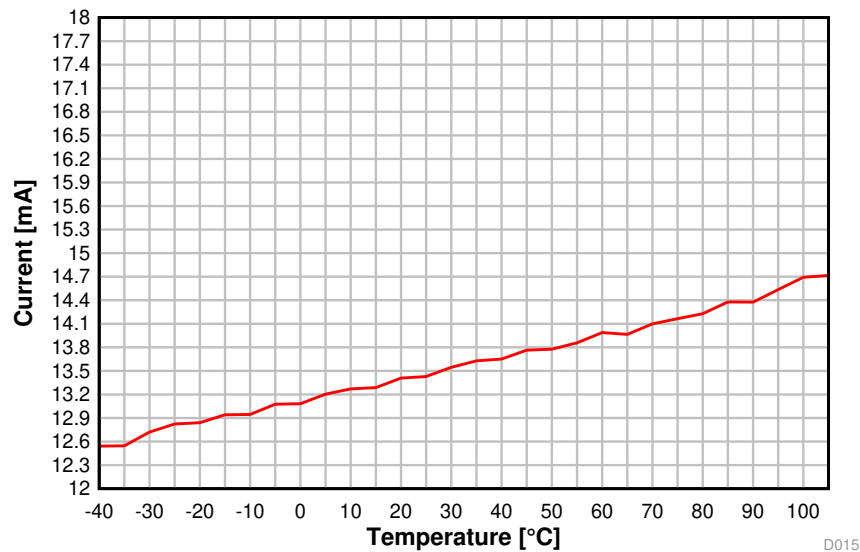
5.23.3 TX Current

**TX Current vs. Temperature**  
50 kbps, 868.3 MHz, +10 dBm



**Figure 5-12. TX Current vs. Temperature (50 kbps, 868.3 MHz)**

**TX Current vs. Temperature**  
50 kbps, 868.3 MHz, +10 dBm, VDD5 = 3.6 V



**Figure 5-13. TX Current vs. Temperature (50 kbps, 868.3 MHz, VDD5 = 3.6 V)**

### TX Current vs. Temperature

50 kbps, 915 MHz, +20 dBm PA, VDDS = 3.3 V

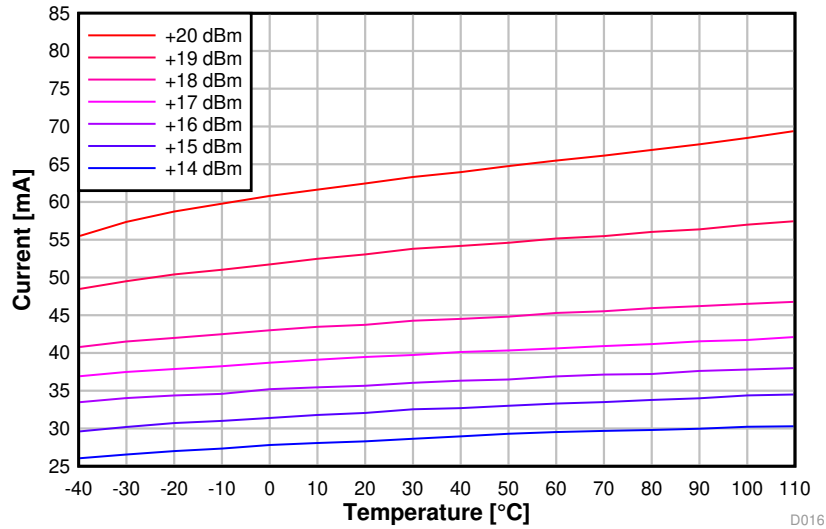


Figure 5-14. TX Current vs. Temperature (50 kbps, 915 MHz, VDDS = 3.3 V)

### TX Current vs. Temperature

BLE 1 Mbps, 2.44 GHz, 0 dBm

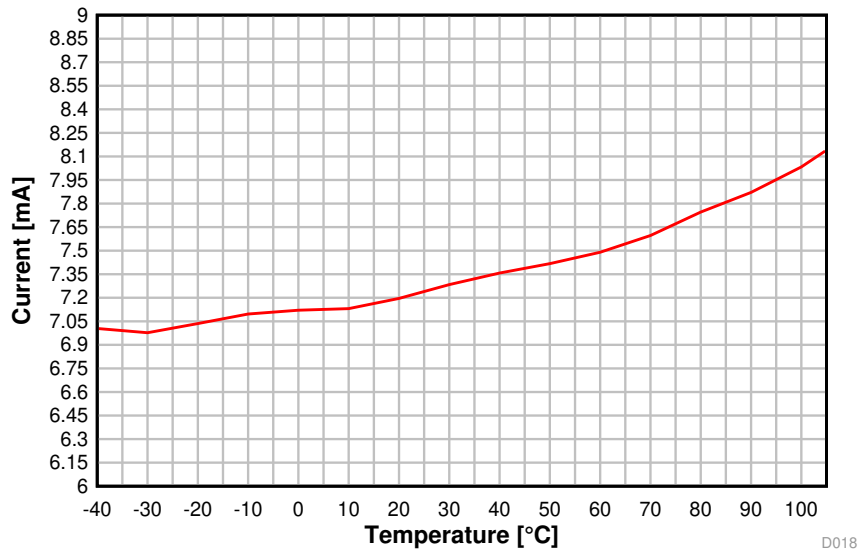


Figure 5-15. TX Current vs. Temperature (BLE 1 Mbps, 2.44 GHz)



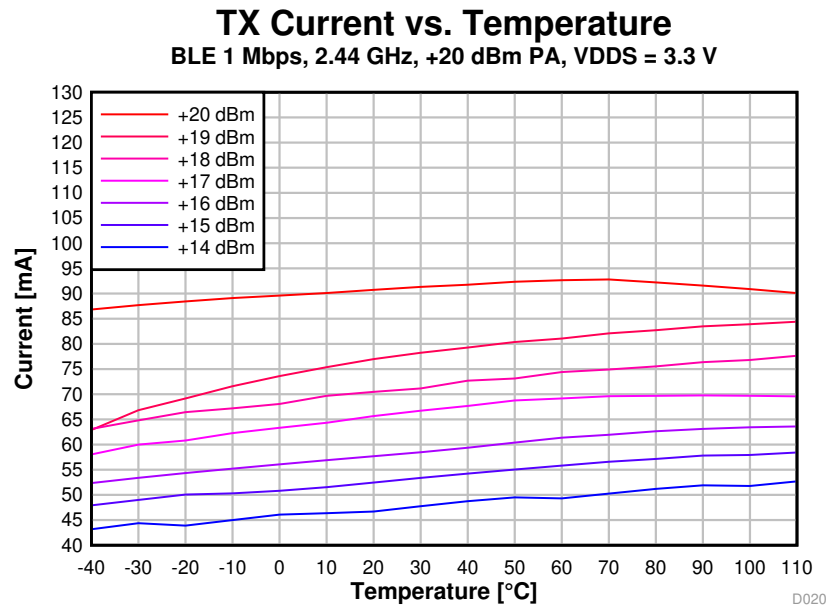


Figure 5-16. TX Current vs. Temperature (BLE 1 Mbps, 2.44 GHz, VDD5 = 3.3 V)

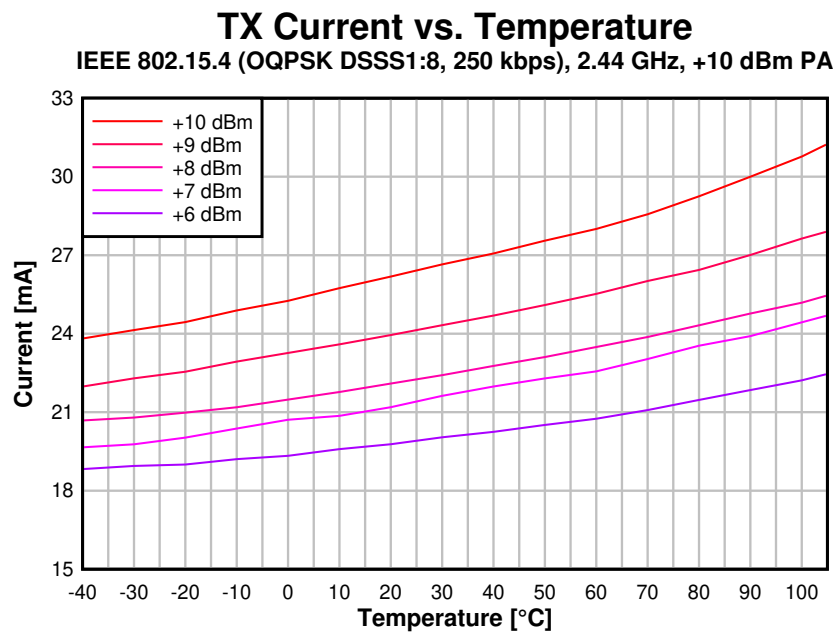


Figure 5-17. TX Current vs. Temperature (250 kbps, 2.44 GHz, +10 dBm PA)

### TX Current vs. VDDS

50 kbps, 868.3 MHz, +10 dBm

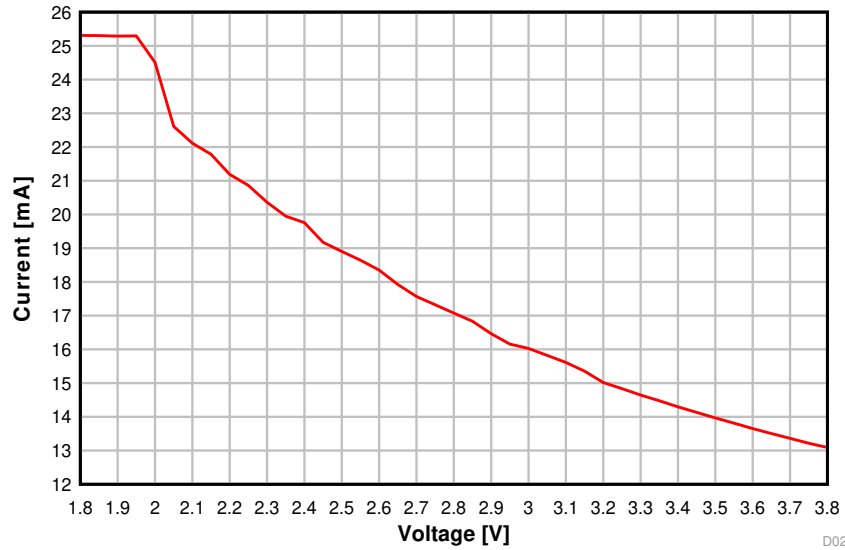


Figure 5-18. TX Current vs. Supply Voltage (VDDS) (50 kbps, 868.3 MHz)

### TX Current vs. VDDS

50 kbps, 915 MHz, +20 dBm PA

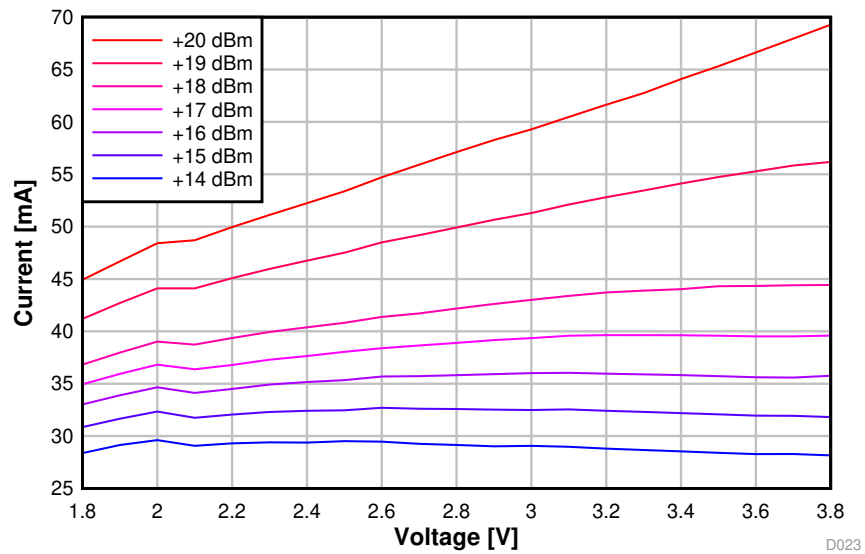


Figure 5-19. TX Current vs. Supply Voltage (VDDS) (50 kbps, 915 MHz)

### TX Current vs. VDDS BLE 1 Mbps, 2.44 GHz, 0 dBm

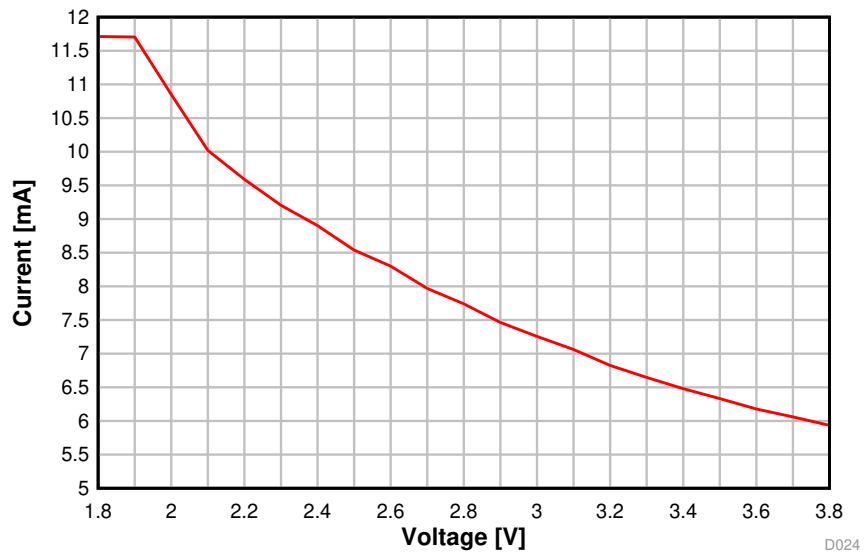


Figure 5-20. TX Current vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz)

### TX Current vs. VDDS BLE 1 Mbps, 2.44 GHz, +20 dBm PA

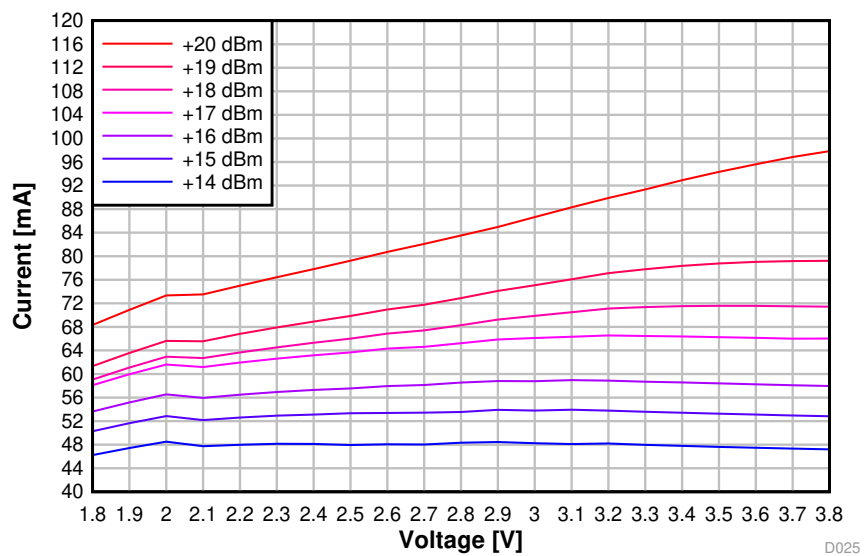
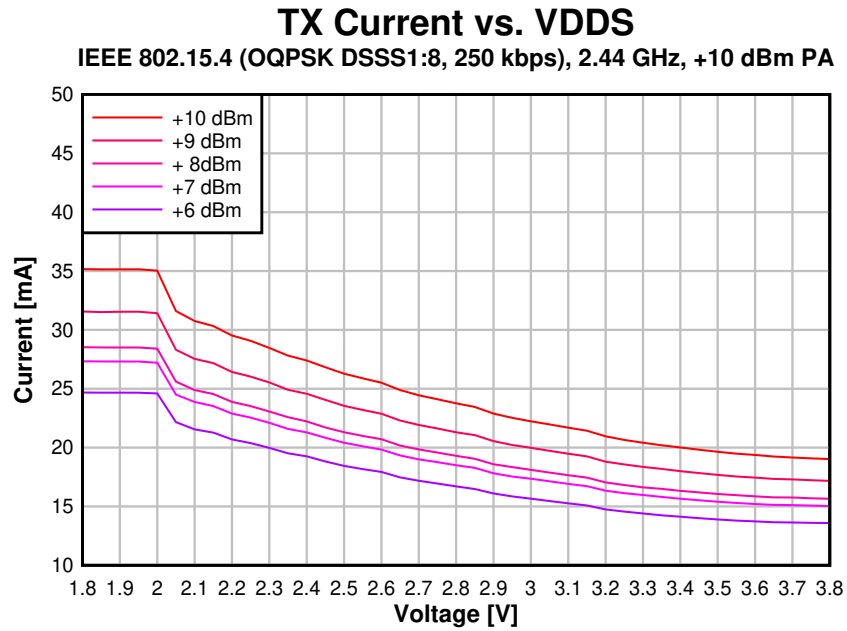


Figure 5-21. TX Current vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, +20 dBm PA)



**Figure 5-22. TX Current vs. Supply Voltage (VDD5) (250 kbps, 2.44 GHz, +10 dBm PA)**

Table 5-18 and Table 5-19 show typical TX current and output power for different output power settings.

**Table 5-18. Typical TX Current and Output Power (915 MHz, VDDS = 3.6 V)**

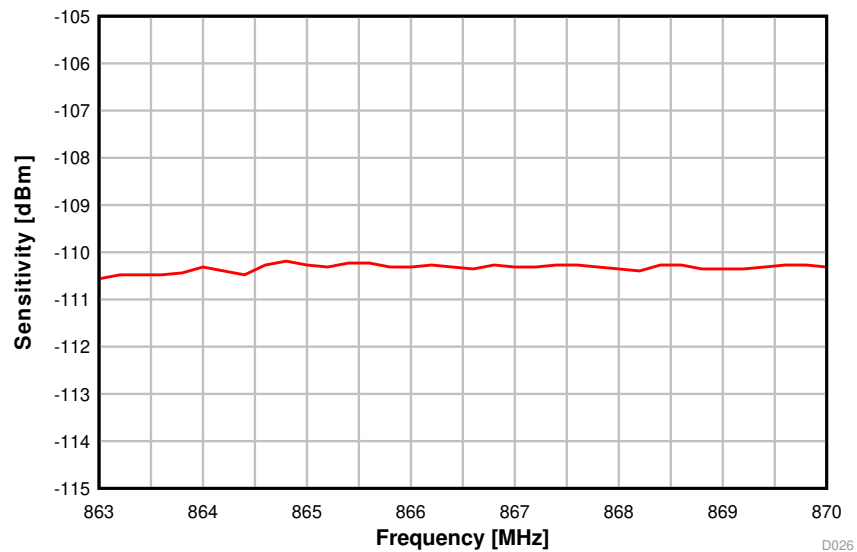
| CC1352P at 915 MHz, VDDS = 3.6 V (Measured on CC1352PEM-XD7793-XD24-PA9093) |                                   |                            |                                  |
|---|-----------------------------------|----------------------------|----------------------------------|
| txPower   | TX Power Setting (SmartRF Studio) | Typical Output Power [dBm] | Typical Current Consumption [mA] |
| 0x013F  | 14                                | 12.8                       | 23                               |
| 0xB224  | 12.5                              | 11.1                       | 16.7                             |
| 0xA410  | 12                                | 10.8                       | 15.8                             |
| 0x669A  | 11                                | 9.8                        | 14.4                             |
| 0x3E92  | 10                                | 8.9                        | 13.2                             |
| 0x3EDC  | 9                                 | 8.1                        | 12.5                             |
| 0x2CD8  | 8                                 | 7.3                        | 11.8                             |
| 0x26D4  | 7                                 | 6                          | 10.8                             |
| 0x20D1  | 6                                 | 4.9                        | 10                               |
| 0x1CCE  | 5                                 | 3.2                        | 9.2                              |
| 0x16CD  | 4                                 | 2.8                        | 8.9                              |
| 0x14CB  | 3                                 | 1.1                        | 8.2                              |
| 0x12CA  | 2                                 | 0.2                        | 7.9                              |
| 0x12C9  | 1                                 | -0.7                       | 7.6                              |
| 0x10C8  | 0                                 | -1.8                       | 7.2                              |
| 0x0AC4  | -5                                | -8.6                       | 5.8                              |
| 0x0AC2  | -10                               | -15                        | 5.1                              |
| 0x06C1  | -15                               | -19.6                      | 4.8                              |
| 0x04C0  | -20                               | -24.6                      | 4.6                              |

**Table 5-19. Typical TX Current and Output Power (2.4 GHz, VDDS = 3.0 V)**

| CC1352P at 2.4 GHz, VDDS = 3.0 V (Measured on CC1352PEM-XD7793-XD24-PA24) |                                   |                            |                                  |
|---|-----------------------------------|----------------------------|----------------------------------|
| txPower   | TX Power Setting (SmartRF Studio) | Typical Output Power [dBm] | Typical Current Consumption [mA] |
| 0x7217  | 5                                 | 3.1                        | 8.7                              |
| 0x4E63  | 4                                 | 1.8                        | 8.2                              |
| 0x385D  | 3                                 | 0.5                        | 7.7                              |
| 0x3259  | 2                                 | -0.7                       | 7.3                              |
| 0x2856  | 1                                 | -1.8                       | 6.9                              |
| 0x2853  | 0                                 | -3.1                       | 6.6                              |
| 0x12D6  | -5                                | -7.7                       | 5.8                              |
| 0x0ACF  | -10                               | -12.6                      | 5.3                              |
| 0x06CA  | -15                               | -17.9                      | 4.9                              |
| 0x04C6  | -20                               | -23.6                      | 4.7                              |

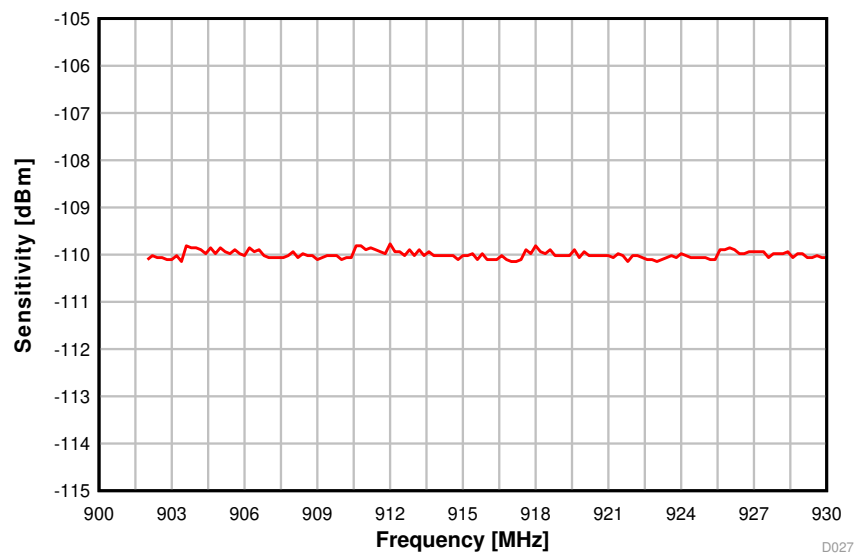
### 5.23.4 RX Performance

**Sensitivity vs. Frequency**  
50 kbps



**Figure 5-23. Sensitivity vs. Frequency (50 kbps, 868 MHz)**

**Sensitivity vs. Frequency**  
50 kbps



**Figure 5-24. Sensitivity vs. Frequency (50 kbps, 915 MHz)**

### Sensitivity vs. Frequency BLE 1 Mbps, 2.44 GHz

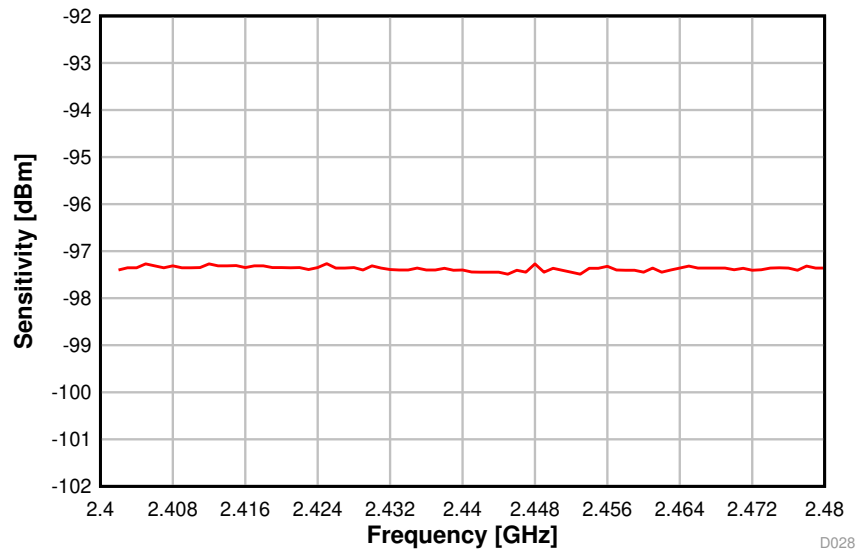


Figure 5-25. Sensitivity vs. Frequency (BLE 1 Mbps, 2.44 GHz)

### Sensitivity vs. Frequency IEEE 802.15.4 (OQPSK DSSS1:8, 250 kbps)

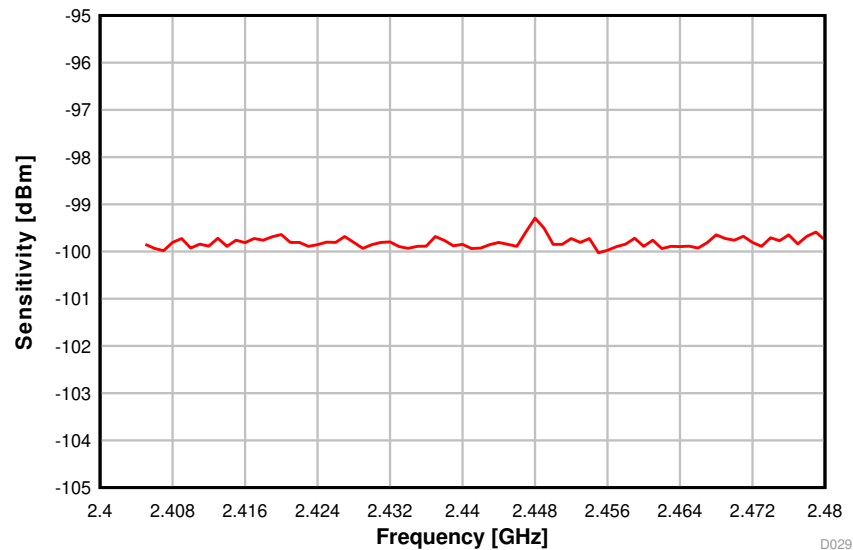


Figure 5-26. Sensitivity vs. Frequency (250 kbps, 2.44 GHz)

### Sensitivity vs. Temperature 50 kbps, 868.3 MHz

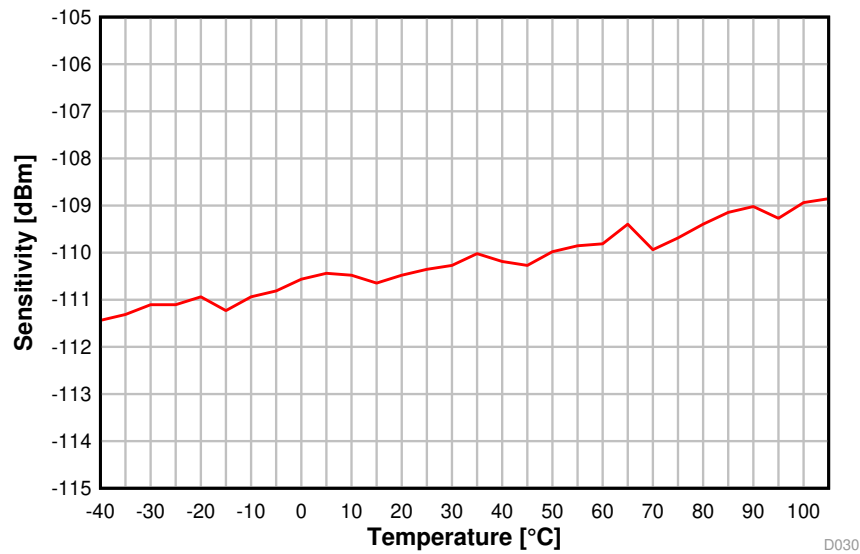


Figure 5-27. Sensitivity vs. Temperature (50 kbps, 868.3 MHz)

### Sensitivity vs. Temperature BLE 1 Mbps, 2.44 GHz

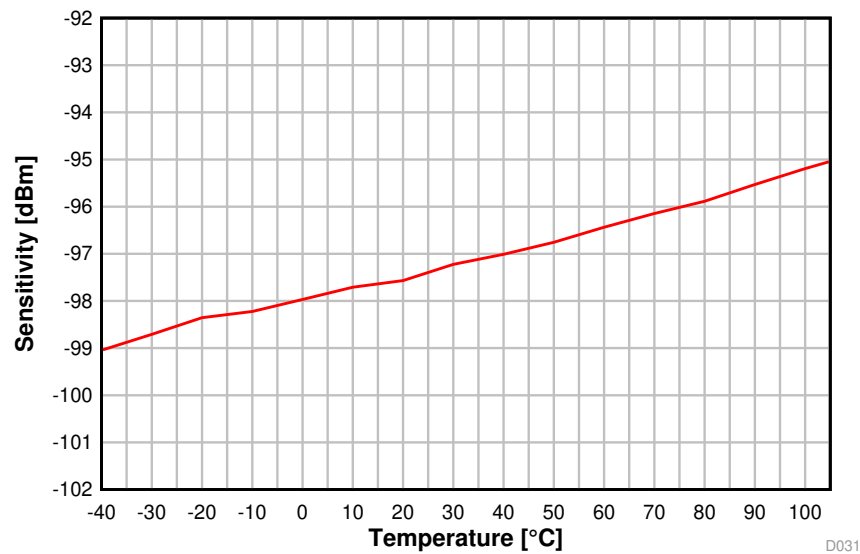
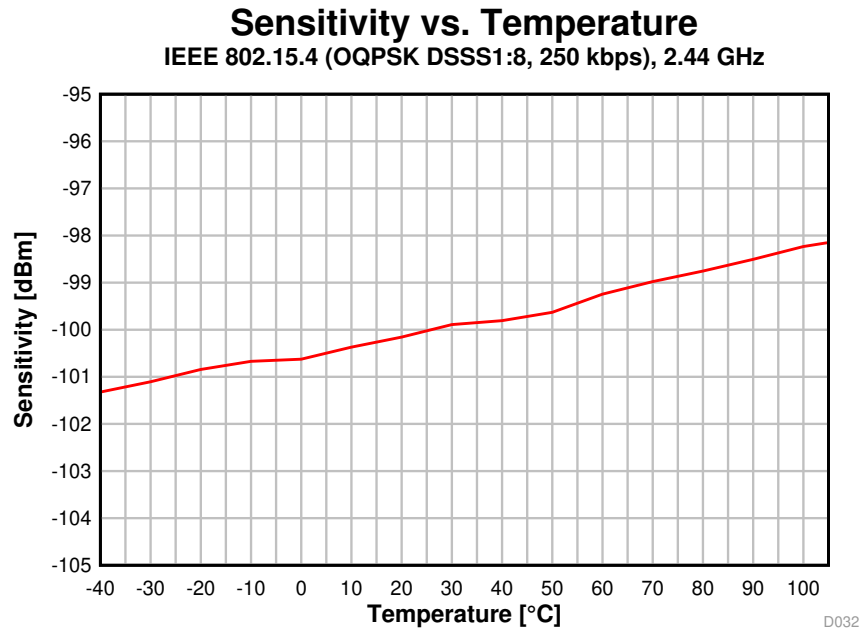
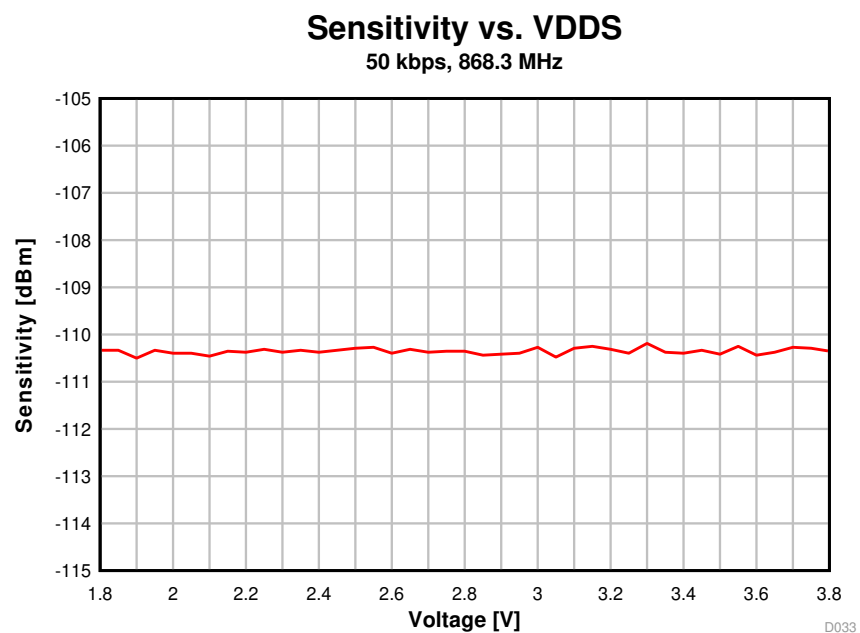


Figure 5-28. Sensitivity vs. Temperature (BLE 1 Mbps, 2.44 GHz)



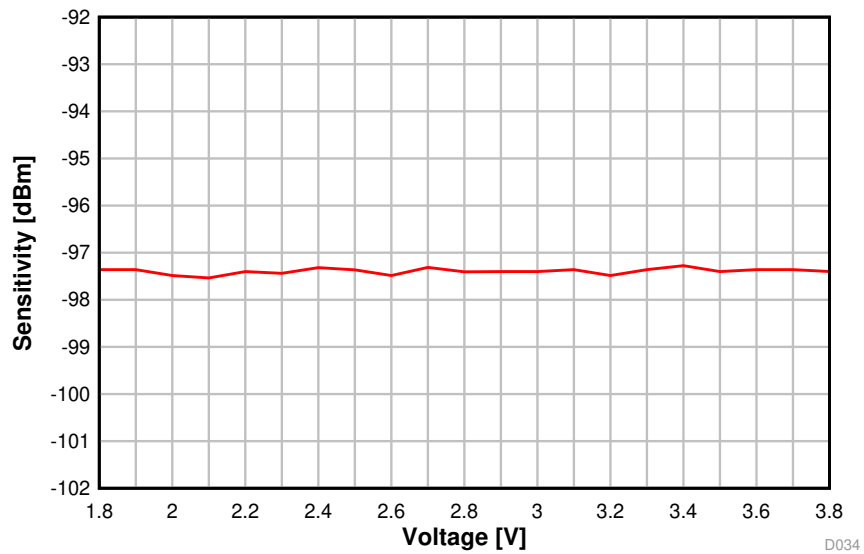


**Figure 5-29. Sensitivity vs. Temperature (250 kbps, 2.44 GHz)**



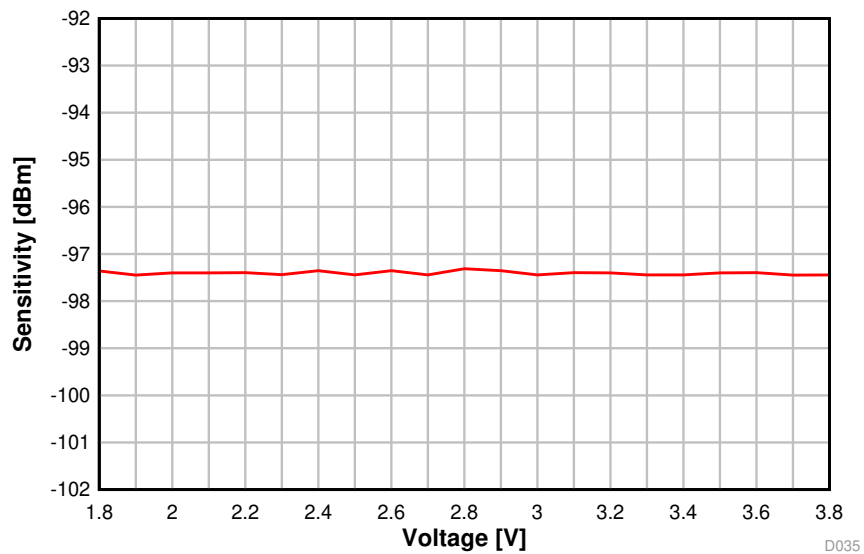
**Figure 5-30. Sensitivity vs. Supply Voltage (VDDS) (50 kbps, 868.3 MHz)**

### Sensitivity vs. VDDS BLE 1 Mbps, 2.44 GHz

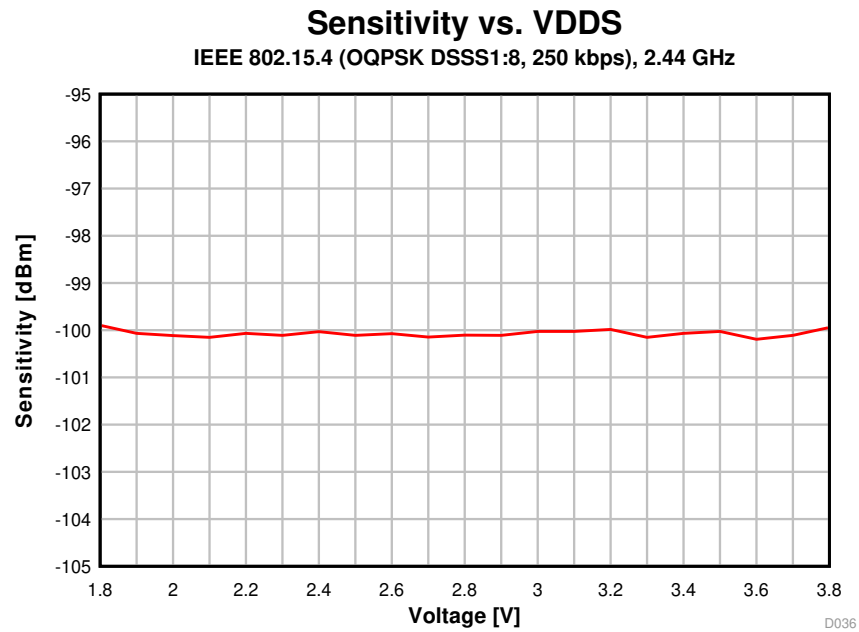


**Figure 5-31. Sensitivity vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz)**

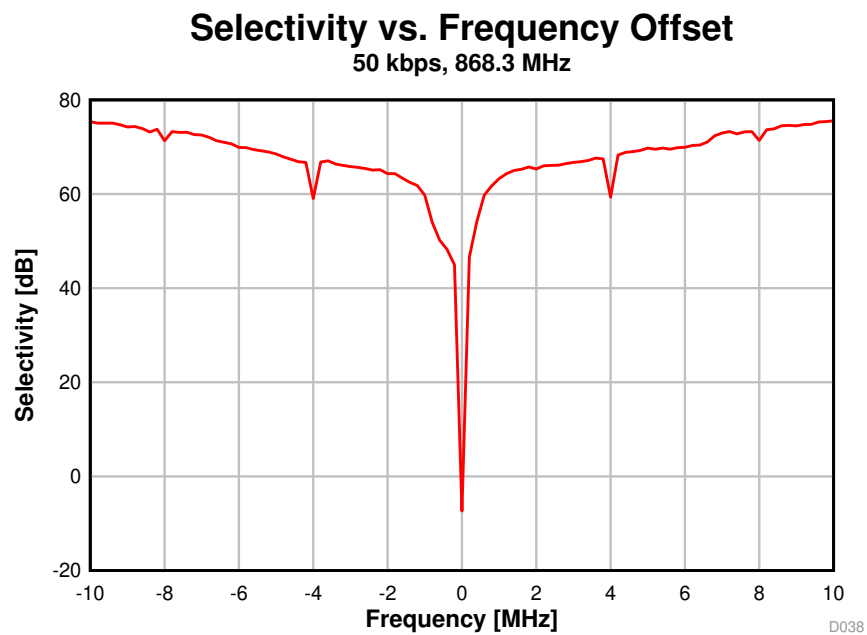
### Sensitivity vs. VDDS BLE 1 Mbps, 2.44 GHz, DCDC Off



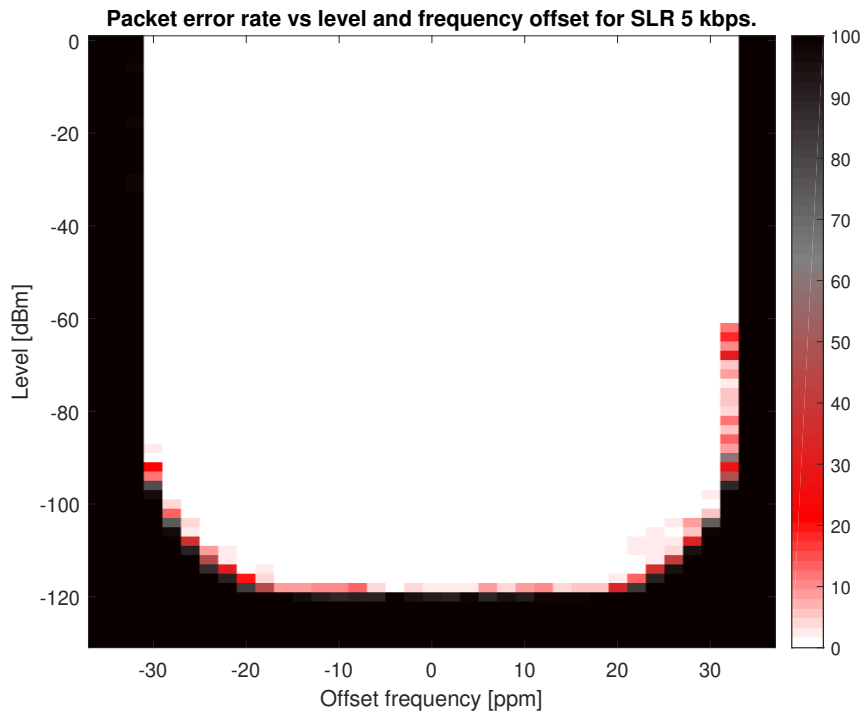
**Figure 5-32. Sensitivity vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, DCDC Off)**



**Figure 5-33. Sensitivity vs. Supply Voltage (VDD5) (250 kbps, 2.44 GHz)**



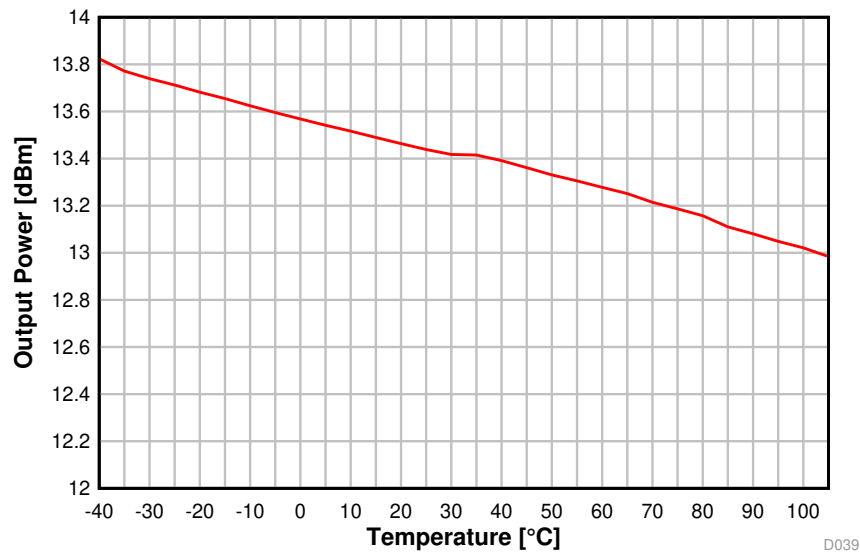
**Figure 5-34. Selectivity vs. Frequency Offset (50 kbps, 868.3 MHz)**



**Figure 5-35. PER vs. Level vs. Frequency (SimpleLink™ Long Range 5 kbps, 868 MHz)**

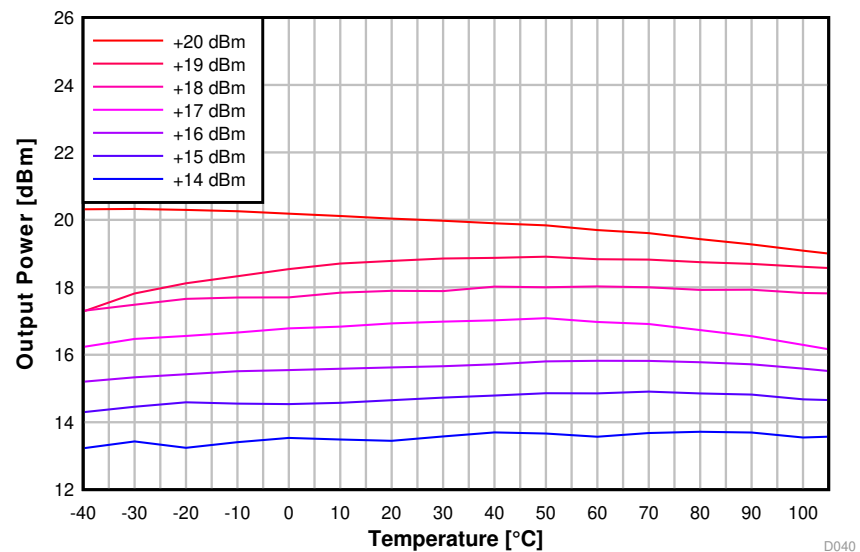
5.23.5 TX Performance

**Output Power vs. Temperature**  
50 kbps, 868.3 MHz, +14 dBm



**Figure 5-36. Output Power vs. Temperature (50 kbps, 868.3 MHz)**

**Output Power vs. Temperature**  
50 kbps, 915 MHz, +20 dBm PA, VDDS = 3.3 V



**Figure 5-37. Output Power vs. Temperature (50 kbps, 915 MHz)**

### Output Power vs. Temperature BLE 1 Mbps, 2.44 GHz, 0 dBm

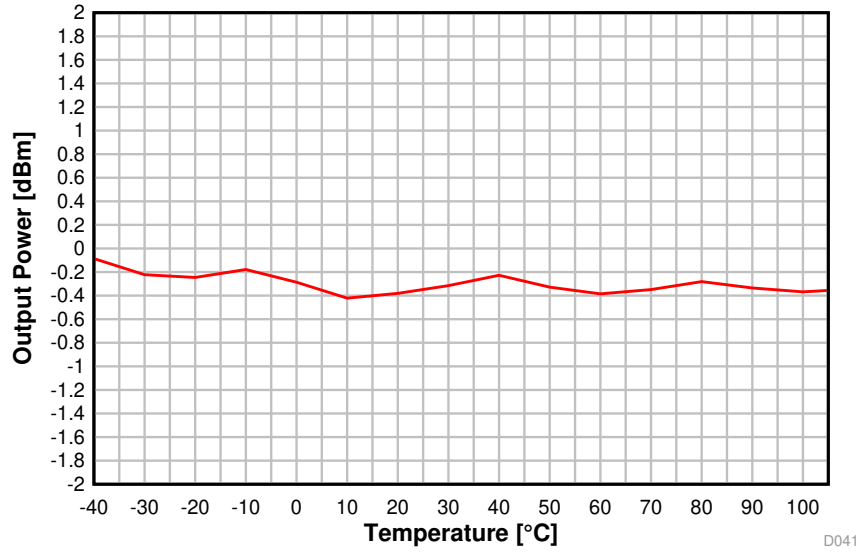


Figure 5-38. Output Power vs. Temperature (BLE 1 Mbps, 2.44 GHz)

### Output Power vs. Temperature BLE 1 Mbps, 2.44 GHz, +5 dBm

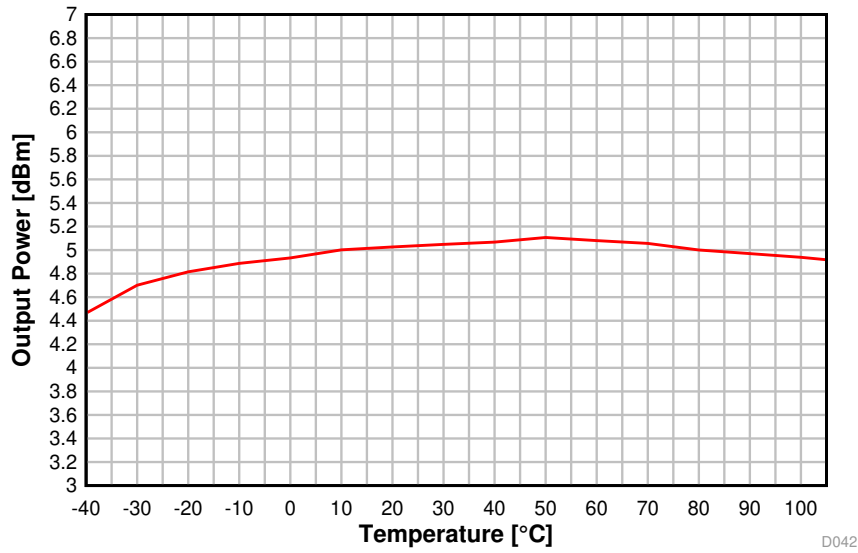


Figure 5-39. Output Power vs. Temperature (BLE 1 Mbps, 2.44 GHz, +5 dBm)

### Output Power vs. Temperature

BLE 1 Mbps, 2.44 GHz, +20 dBm PA, VDD5 = 3.3 V

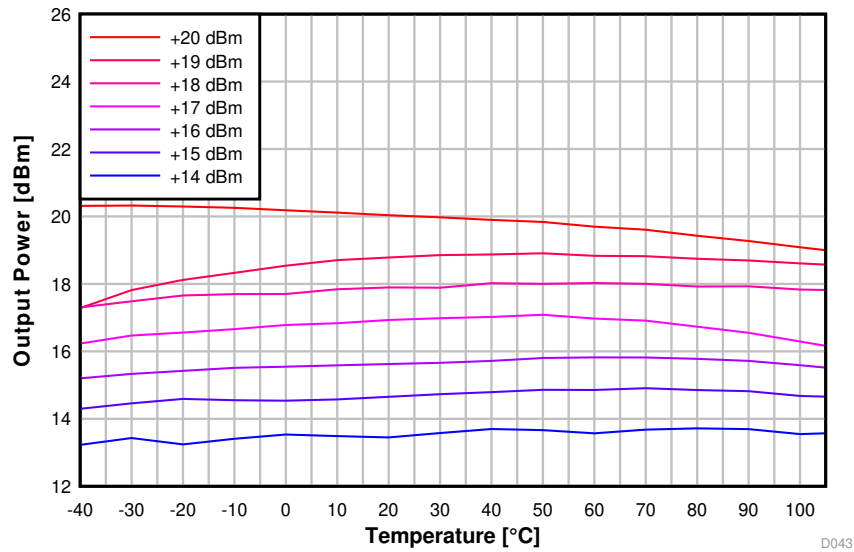


Figure 5-40. Output Power vs. Temperature (BLE 1 Mbps, 2.44 GHz, +20 dBm PA)

### Output Power vs. Temperature

IEEE 802.15.4 (OQPSK DSSS1:8, 250 kbps), 2.44 GHz, +10 dBm PA

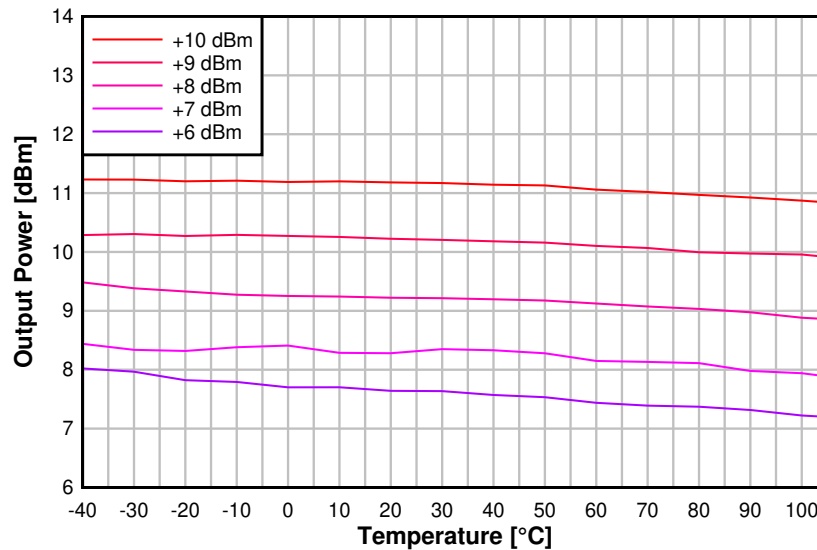
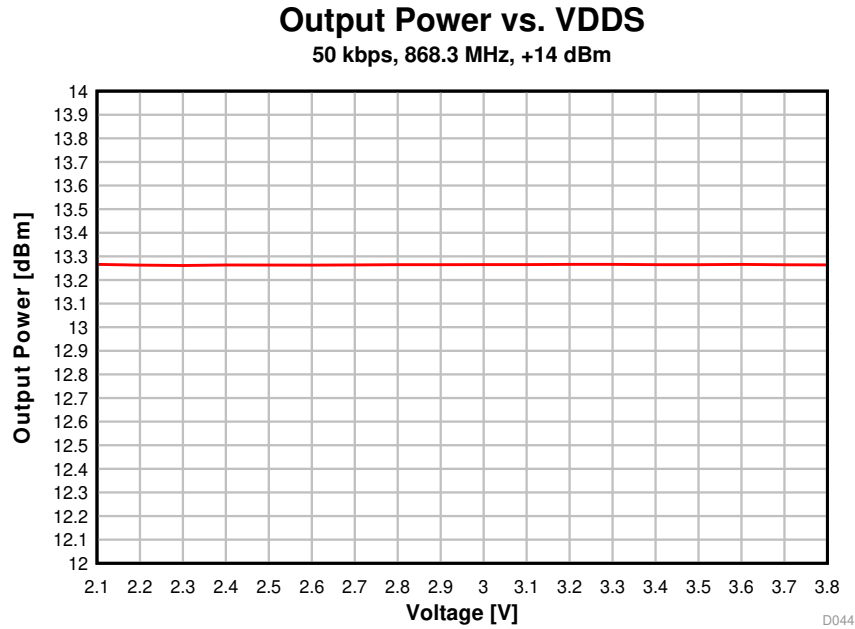
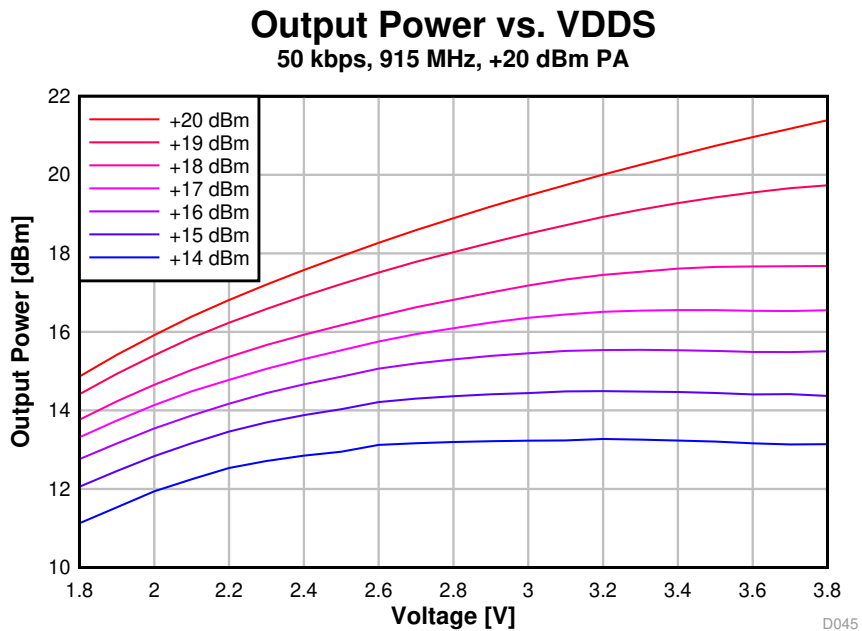


Figure 5-41. Output Power vs. Temperature (2.44 GHz, +10 dBm PA)



**Figure 5-42. Output Power vs. Supply Voltage (VDDS) (50 kbps, 868.3 MHz)**



**Figure 5-43. Output Power vs. Supply Voltage (VDDS) (50 kbps, 915 MHz)**



### Output Power vs. VDD5

BLE 1 Mbps, 2.44 GHz, 0 dBm

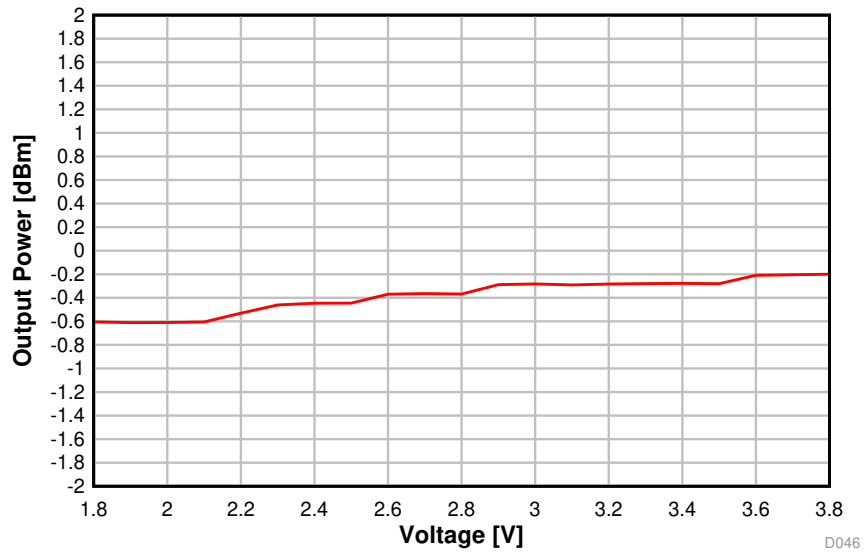


Figure 5-44. Output Power vs. Supply Voltage (VDD5) (BLE 1 Mbps, 2.44 GHz)

### Output power vs. VDD5

BLE 1 Mbps, 2.44 GHz, +5 dBm

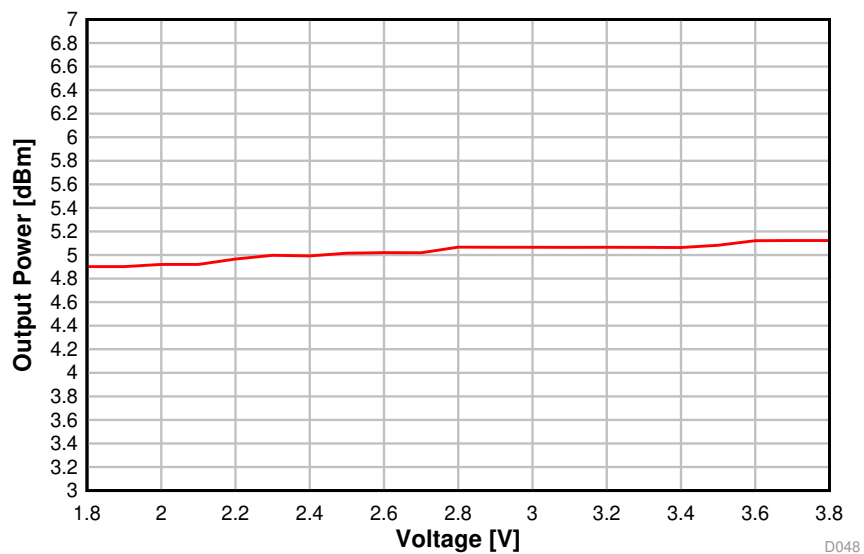


Figure 5-45. Output Power vs. Supply Voltage (VDD5) (BLE 1 Mbps, 2.44 GHz, +5 dBm)

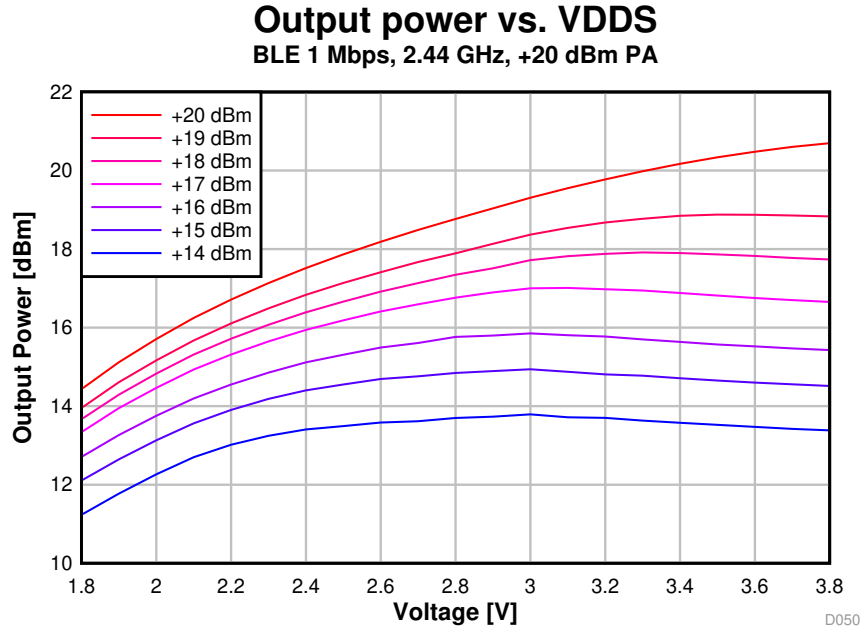


Figure 5-46. Output Power vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, +20 dBm PA)

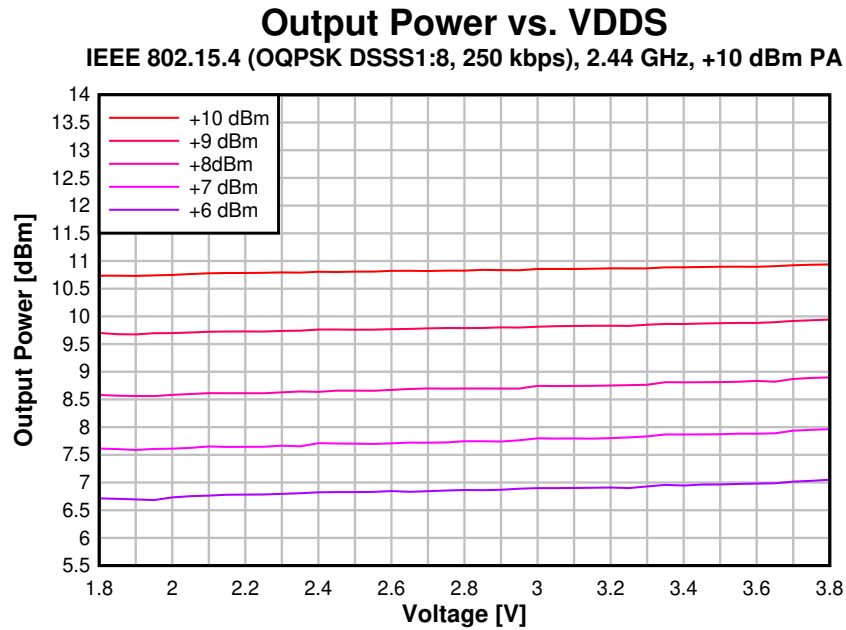


Figure 5-47. Output Power vs. Supply Voltage (VDDS) (2.44 GHz, +10 dBm PA)

### Output Power vs. Frequency 50 kbps, +14 dBm

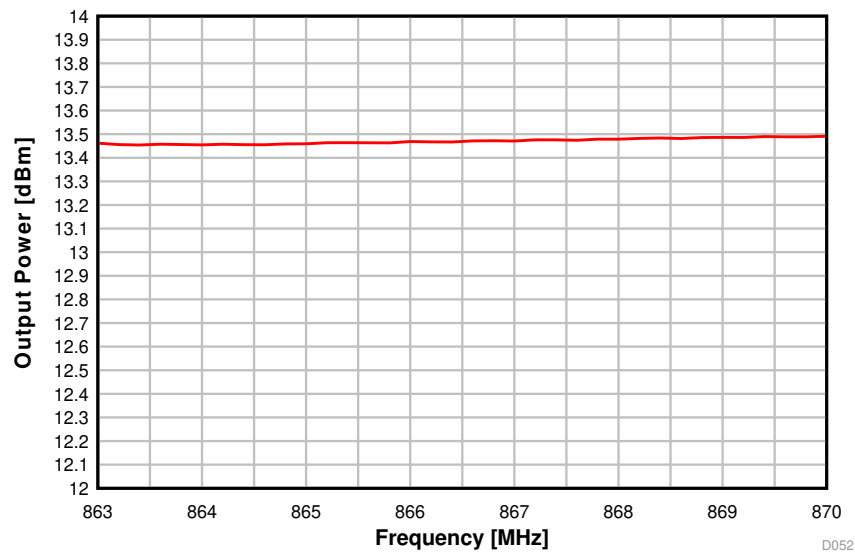


Figure 5-48. Output Power vs. Frequency (50 kbps, 868 MHz)

### Output Power vs. Frequency 50 kbps, +14 dBm

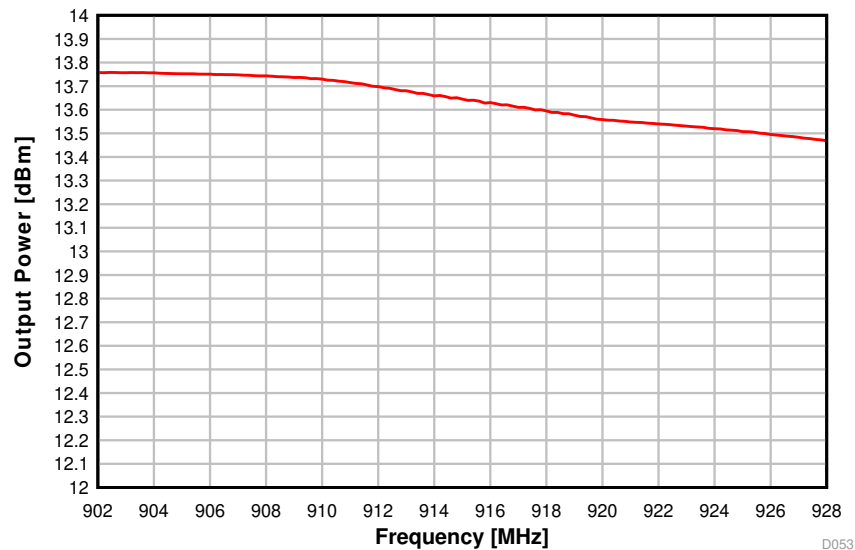


Figure 5-49. Output Power vs. Frequency (50 kbps, 915 MHz)

### Output Power vs. Frequency 50 kbps, +20 dBm PA, VDDS = 3.3 V

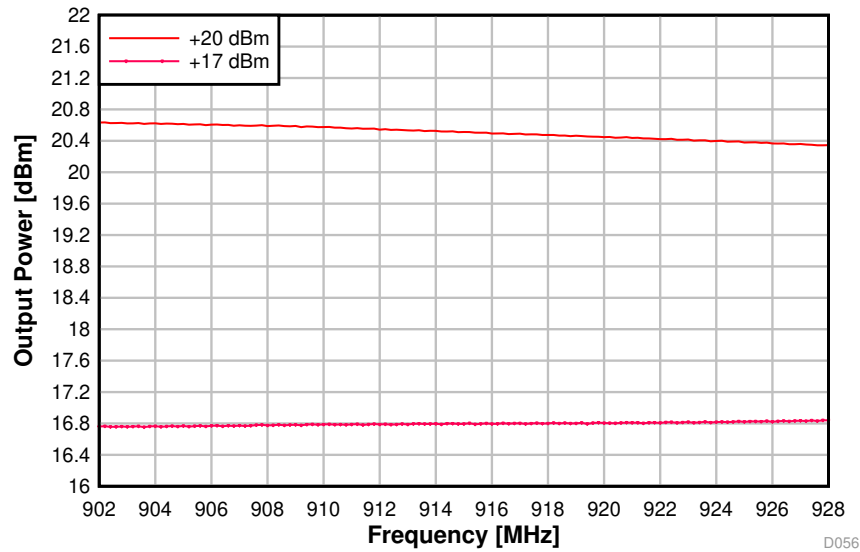


Figure 5-50. Output Power vs. Frequency (50 kbps, 915 MHz, VDDS = 3.3 V)

### Output Power vs. Frequency BLE 1 Mbps, 2.44 GHz, 0 dBm

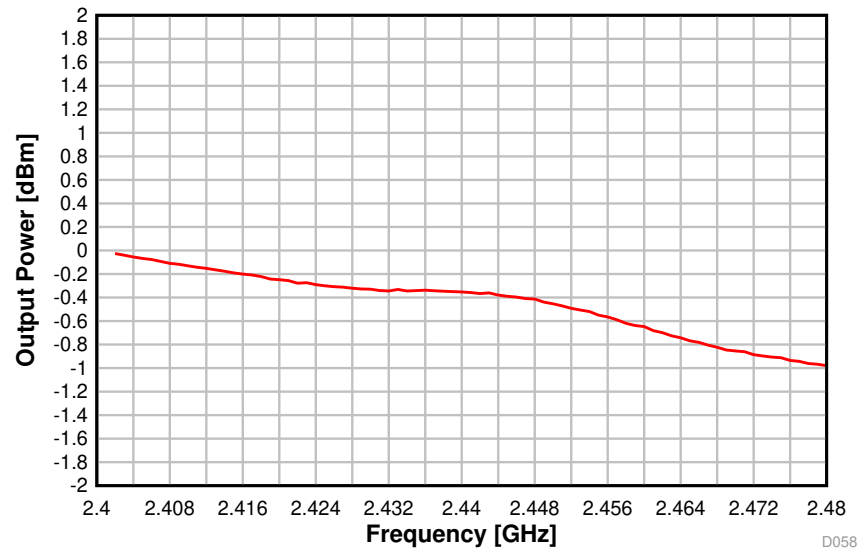


Figure 5-51. Output Power vs. Frequency (BLE 1 Mbps, 2.44 GHz)

### Output Power vs. Frequency BLE 1 Mbps, 2.44 GHz, +5 dBm

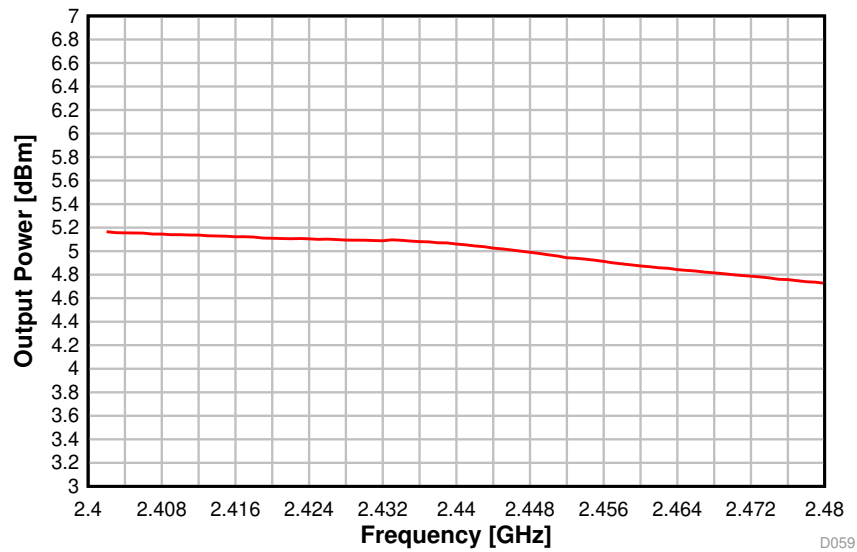


Figure 5-52. Output Power vs. Frequency (BLE 1 Mbps, 2.44 GHz, +5 dBm)

### Output Power vs. Frequency BLE 1 Mbps, +20 dBm PA, VDD5 = 3.3 V

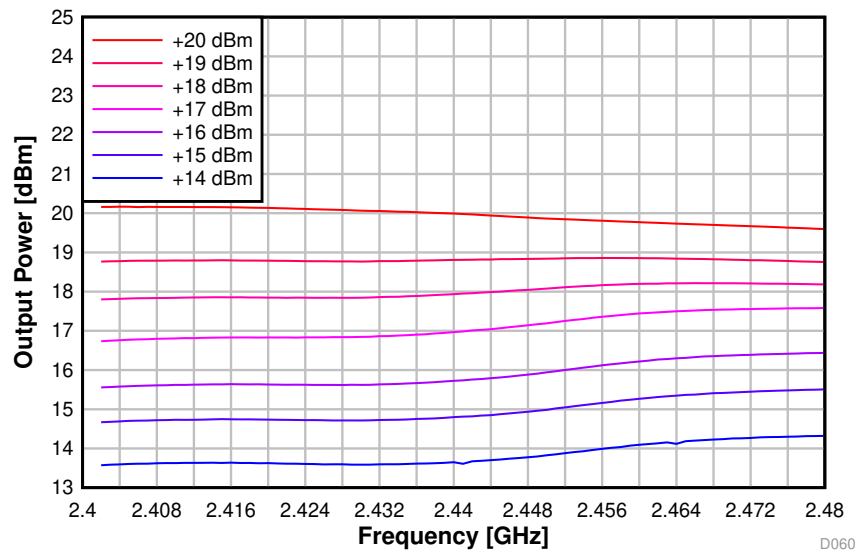
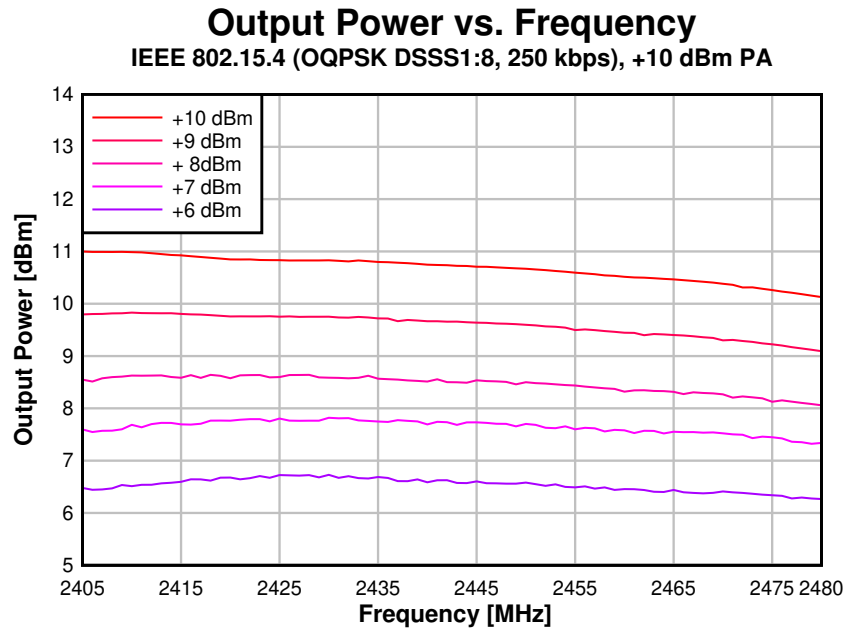


Figure 5-53. Output Power vs. Frequency (BLE 1 Mbps, 2.44 GHz, +20 dBm PA)



**Figure 5-54. Output Power vs. Frequency (250 kbps, +10 dBm PA)**

### 5.23.6 ADC Performance

#### ENOB vs. Input Frequency

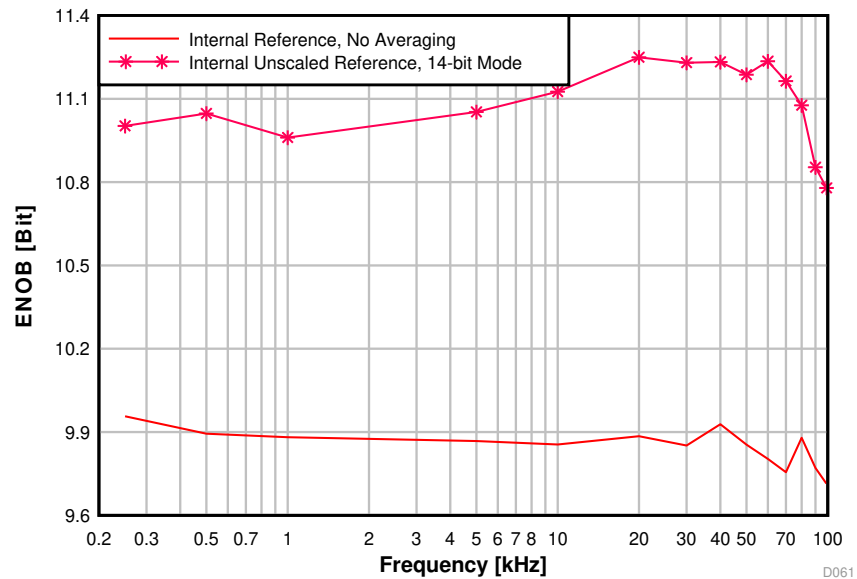


Figure 5-55. ENOB vs. Input Frequency

#### ENOB vs. Sampling Frequency

Vin = 3.0 V Sine wave, Internal reference,  
Fin = Fs / 10

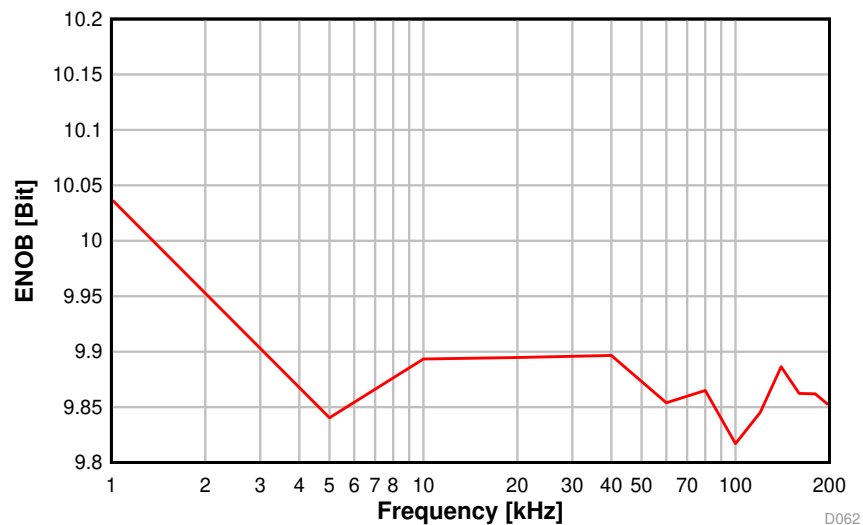


Figure 5-56. ENOB vs. Sampling Frequency

### INL vs. ADC Code

Vin = 3.0 V Sine wave, Internal reference,  
200 kSamples/s

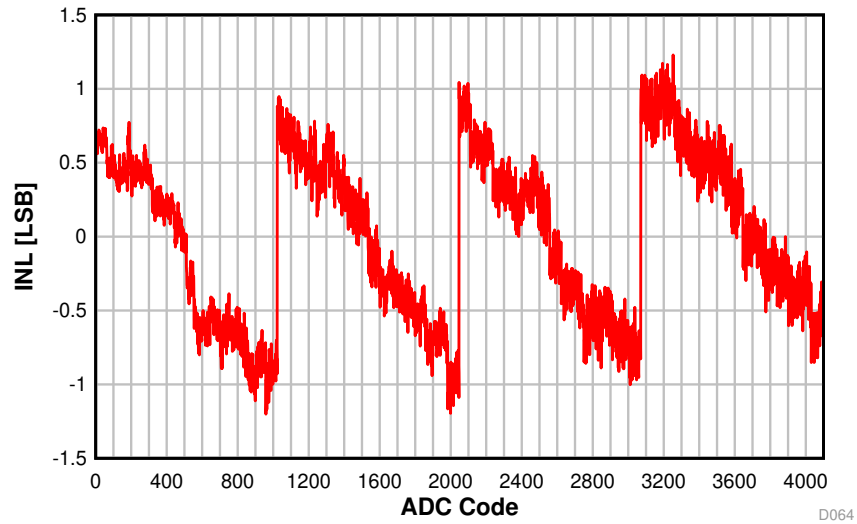


Figure 5-57. INL vs. ADC Code

### DNL vs. ADC Code

Vin = 3.0 V Sine wave, Internal reference,  
200 kSamples/s

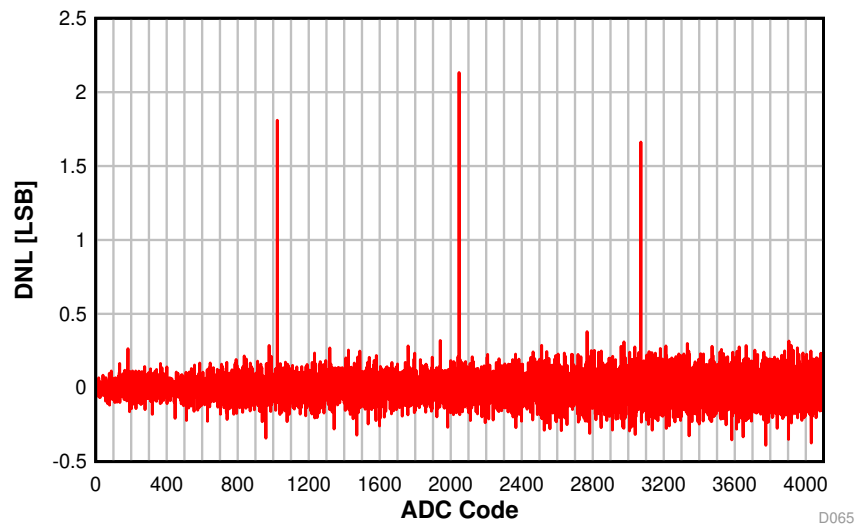


Figure 5-58. DNL vs. ADC Code



### ADC Accuracy vs. Temperature

Vin = 1 V, Internal reference,  
200 kSamples/s

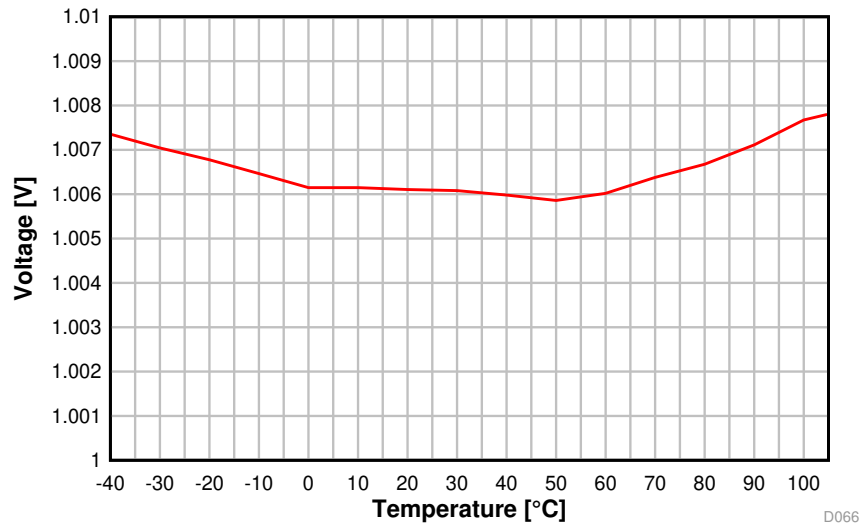


Figure 5-59. ADC Accuracy vs. Temperature

### ADC Accuracy vs. VDDS

Vin = 1 V, Internal reference,  
200 kSamples/s

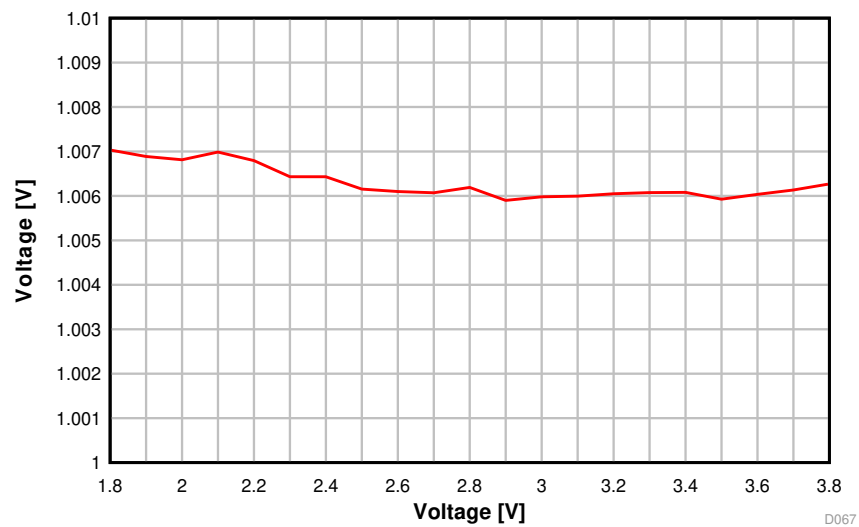


Figure 5-60. ADC Accuracy vs. Supply Voltage (VDDS)

## 6 Detailed Description

### 6.1 Overview

[Section 1.4](#) shows the core modules of the CC1352P device.

### 6.2 System CPU

The CC1352P SimpleLink™ Wireless MCU contains an Arm® Cortex®-M4F system CPU, which runs the application and the higher layers of radio protocol stacks.

The system CPU is the foundation of a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

Its features include the following:

- ARMv7-M architecture optimized for small-footprint embedded applications
- Arm Thumb®-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit Arm core in a compact memory size
- Fast code execution permits increased sleep mode time
- Deterministic, high-performance interrupt handling for time-critical applications
- Single-cycle multiply instruction and hardware divide
- Hardware division and fast digital-signal-processing oriented multiply accumulate
- Saturating arithmetic for signal processing
- IEEE 754-compliant single-precision Floating Point Unit (FPU)
- Memory Protection Unit (MPU) for safety-critical applications
- Full debug with data matching for watchpoint generation
  - Data Watchpoint and Trace Unit (DWT)
  - JTAG Debug Access Port (DAP)
  - Flash Patch and Breakpoint Unit (FPB)
- Trace support reduces the number of pins required for debugging and tracing
  - Instrumentation Trace Macrocell Unit (ITM)
  - Trace Port Interface Unit (TPIU) with asynchronous serial wire output (SWO)
- Optimized for single-cycle flash memory access
- Tightly connected to 8-KB 4-way random replacement cache for minimal active power consumption and wait states
- Ultra-low-power consumption with integrated sleep modes
- 48 MHz operation
- 1.25 DMIPS per MHz

### 6.3 Radio (RF Core)

The RF Core is a highly flexible and future proof radio module which contains an Arm Cortex-M0 processor that interfaces the analog RF and base-band circuitry, handles data to and from the system CPU side, and assembles the information bits in a given packet structure. The RF core offers a high level, command-based API to the main CPU that configurations and data are passed through. The Arm Cortex-M0 processor is not programmable by customers and is interfaced through the TI-provided RF driver that is included with the SimpleLink Software Development Kit (SDK).

The RF core can autonomously handle the time-critical aspects of the radio protocols, thus offloading the main CPU, which reduces power and leaves more resources for the user application. Several signals are also available to control external circuitry such as RF switches or range extenders autonomously.

Dual-band and multiprotocol solutions are enabled through time-sliced access of the radio, handled transparently for the application through the TI-provided RF driver and dual-mode manager.

The various physical layer radio formats are partly built as a software defined radio where the radio behavior is either defined by radio ROM contents or by non-ROM radio formats delivered in form of firmware patches with the SimpleLink SDKs. This allows the radio platform to be updated for support of future versions of standards even with over-the-air (OTA) updates while still using the same silicon.

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#### NOTE

Not all combinations of features, frequencies, data rates, and modulation formats described in this chapter are supported. Over time, TI can enable new physical radio formats (PHYs) for the device and provides performance numbers for selected PHYs in the data sheet. Supported radio formats for a specific device, including optimized settings to use with the TI RF driver, are included in the [SmartRF Studio](#) tool with performance numbers of selected formats found in [Section 5](#).

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### 6.3.1 Proprietary Radio Formats

The CC1352P radio can support a wide range of physical radio formats through a set of hardware peripherals combined with firmware available in the device ROM, covering various customer needs for optimizing towards parameters such as speed or sensitivity. This allows great flexibility in tuning the radio both to work with legacy protocols as well as customizing the behavior for specific application needs.

Table 6-1 gives a simplified overview of features of the various radio formats available in ROM. Other radio formats may be available in the form of radio firmware patches or programs through the Software Development Kit (SDK) and may combine features in a different manner, as well as add other features.

**Table 6-1. Feature Support**

| Feature                                  | Main 2-(G)FSK Mode | High Data Rates      | Low Data Rates       | SimpleLink™ Long Range |
|--|--------------------|----------------------|----------------------|------------------------|
| Programmable preamble, sync word and CRC | Yes                | Yes                  | Yes                  | No                     |
| Programmable receive bandwidth           | Yes                | Yes                  | Yes (down to 4 kHz)  | Yes                    |
| Data / Symbol rate <sup>(1)</sup>        | 20 to 1000 kbps    | ≤ 2 Msps             | ≤ 100 ksps           | ≤ 20 ksps              |
| Modulation format                        | 2-(G)FSK           | 2-(G)FSK<br>4-(G)FSK | 2-(G)FSK<br>4-(G)FSK | 2-(G)FSK               |
| Dual Sync Word                           | Yes                | Yes                  | No                   | No                     |
| Carrier Sense <sup>(2)(3)</sup>          | Yes                | No                   | No                   | No                     |
| Preamble Detection <sup>(3)</sup>        | Yes                | Yes                  | Yes                  | No                     |
| Data Whitening                           | Yes                | Yes                  | Yes                  | Yes                    |
| Digital RSSI                             | Yes                | Yes                  | Yes                  | Yes                    |
| CRC filtering                            | Yes                | Yes                  | Yes                  | Yes                    |
| Direct-sequence spread spectrum (DSSS)   | No                 | No                   | No                   | 1:2<br>1:4<br>1:8      |
| Forward error correction (FEC)           | No                 | No                   | No                   | Yes                    |
| Link Quality Indicator (LQI)             | Yes                | Yes                  | Yes                  | Yes                    |

- (1) Data rates are only indicative. Data rates outside this range may also be supported. For some specific combinations of settings, a smaller range might be supported.
- (2) Carrier Sense can be used to implement HW-controlled listen-before-talk (LBT) and Clear Channel Assessment (CCA) for compliance with such requirements in regulatory standards. This is available through the CMD\_PROP\_CS radio API.
- (3) Carrier Sense and Preamble Detection can be used to implement sniff modes where the radio is duty cycled to save power.

### 6.3.2 **Bluetooth 5.1 Low Energy**

The RF Core offers full support for Bluetooth 5.1 Low Energy, including the high-speed 2-Mbps physical layer and the 500-kbps and 125-kbps long range PHYs (Coded PHY) through the TI provided Bluetooth 5.1 stack or through a high-level Bluetooth API. The Bluetooth 5.1 PHY and part of the controller are in radio and system ROM, providing significant savings in memory usage and more space available for applications.

The new high-speed mode allows data transfers up to 2 Mbps, twice the speed of Bluetooth 4.2 and five times the speed of Bluetooth 4.0, without increasing power consumption. In addition to faster speeds, this mode offers significant improvements for energy efficiency and wireless coexistence with reduced radio communication time.

Bluetooth 5.1 also enables unparalleled flexibility for adjustment of speed and range based on application needs, which capitalizes on the high-speed or long-range modes respectively. Data transfers are now possible at 2 Mbps, enabling development of applications using voice, audio, imaging, and data logging that were not previously an option using Bluetooth low energy. With high-speed mode, existing applications deliver faster responses, richer engagement, and longer battery life. Bluetooth 5.1 enables fast, reliable firmware updates.

### 6.3.3 **802.15.4 (Thread, Zigbee, 6LoWPAN)**

Through a dedicated IEEE radio API, the RF Core supports the 2.4-GHz IEEE 802.15.4-2011 physical layer (2 Mcps per second Offset-QPSK with DSSS 1:8), used in Thread, Zigbee, and 6LoWPAN protocols. The 802.15.4 PHY and MAC are in radio and system ROM. TI also provides royalty-free protocol stacks for Thread and Zigbee as part of the SimpleLink SDK, enabling a robust end-to-end solution.

## 6.4 Memory

The up to 352-KB nonvolatile (Flash) memory provides storage for code and data. The flash memory is in-system programmable and erasable. The last flash memory sector must contain a Customer Configuration section (CCFG) that is used by boot ROM and TI provided drivers to configure the device. This configuration is done through the `cfg.c` source file that is included in all TI provided examples.

The ultra-low leakage system static RAM (SRAM) is split into up to five 16-KB blocks and can be used for both storage of data and execution of code. Retention of SRAM contents in Standby power mode is enabled by default and included in Standby mode power consumption numbers. Parity checking for detection of bit errors in memory is built-in, which reduces chip-level soft errors and thereby increases reliability. System SRAM is always initialized to zeroes upon code execution from boot.

To improve code execution speed and lower power when executing code from nonvolatile memory, a 4-way nonassociative 8-KB cache is enabled by default to cache and prefetch instructions read by the system CPU. The cache can be used as a general-purpose RAM by enabling this feature in the Customer Configuration Area (CCFG).

There is a 4-KB ultra-low leakage SRAM available for use with the Sensor Controller Engine which is typically used for storing Sensor Controller programs, data and configuration parameters. This RAM is also accessible by the system CPU. The Sensor Controller RAM is not cleared to zeroes between system resets.

The ROM includes a TI-RTOS kernel and low-level drivers, as well as significant parts of selected radio stacks, which frees up flash memory for the application. The ROM also contains a serial (SPI and UART) bootloader that can be used for initial programming of the device.

## 6.5 Sensor Controller

The Sensor Controller contains circuitry that can be selectively enabled in both Standby and Active power modes. The peripherals in this domain can be controlled by the Sensor Controller Engine, which is a proprietary power-optimized CPU. This CPU can read and monitor sensors or perform other tasks autonomously; thereby significantly reducing power consumption and offloading the system CPU.

The Sensor Controller Engine is user programmable with a simple programming language that has syntax similar to C. This programmability allows for sensor polling and other tasks to be specified as sequential algorithms rather than static configuration of complex peripheral modules, timers, DMA, register programmable state machines, or event routing.

The main advantages are:

- Flexibility - data can be read and processed in unlimited manners while still [ensuring ultra-low power](#)
- 2 MHz low-power mode enables lowest possible handling of digital sensors
- Dynamic reuse of hardware resources
- 40-bit accumulator supporting multiplication, addition and shift
- Observability and debugging options

[Sensor Controller Studio](#) is used to write, test, and debug code for the Sensor Controller. The tool produces C driver source code, which the System CPU application uses to control and exchange data with the Sensor Controller. Typical use cases may be (but are not limited to) the following:

- Read analog sensors using integrated ADC or comparators
- Interface digital sensors using GPIOs, SPI, UART, or I<sup>2</sup>C (UART and I<sup>2</sup>C are bit-banged)
- Capacitive sensing
- Waveform generation
- Very low-power pulse counting (flow metering)
- Key scan

The peripherals in the Sensor Controller include the following:

- The low-power clocked comparator can be used to wake the system CPU from any state in which the comparator is active. A configurable internal reference DAC can be used in conjunction with the comparator. The output of the comparator can also be used to trigger an interrupt or the ADC.
- Capacitive sensing functionality is implemented through the use of a constant current source, a time-to-digital converter, and a comparator. The continuous time comparator in this block can also be used as a higher-accuracy alternative to the low-power clocked comparator. The Sensor Controller takes care of baseline tracking, hysteresis, filtering, and other related functions when these modules are used for capacitive sensing.
- The ADC is a 12-bit, 200-ksamples/s ADC with eight inputs and a built-in voltage reference. The ADC can be triggered by many different sources including timers, I/O pins, software, and comparators.
- The analog modules can connect to up to eight different GPIOs
- Dedicated SPI master with up to 6 MHz clock speed

The peripherals in the Sensor Controller can also be controlled from the main application processor.

## 6.6 Cryptography

The CC1352P device comes with a wide set of modern cryptography-related hardware accelerators, drastically reducing code footprint and execution time for cryptographic operations. It also has the benefit of being lower power and improves availability and responsiveness of the system because the cryptography operations runs in a background hardware thread.

Together with a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), this allows for secure and future proof IoT applications to be easily built on top of the platform. The hardware accelerator modules are:

- **True Random Number Generator (TRNG)** module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear-combinatorial circuit.
- **Secure Hash Algorithm 2 (SHA-2)** with support for SHA224, SHA256, SHA384, and SHA512
- **Advanced Encryption Standard (AES)** with 128 and 256 bit key lengths
- **Public Key Accelerator** - Hardware accelerator supporting mathematical operations needed for elliptic curves up to 512 bits and RSA key pair generation up to 1024 bits.

Through use of these modules and the TI provided cryptography drivers, the following capabilities are available for an application or stack:

- **Key Agreement Schemes**
  - Elliptic curve Diffie–Hellman with static or ephemeral keys (ECDH and ECDHE)
  - Elliptic curve Password Authenticated Key Exchange by Juggling (ECJ-PAKE)
- **Signature Generation**
  - Elliptic curve Diffie-Hellman Digital Signature Algorithm (ECDSA)
- **Curve Support**
  - Short Weierstrass form (full hardware support), such as:
    - NIST-P224, NIST-P256, NIST-P384, NIST-P521
    - Brainpool-256R1, Brainpool-384R1, Brainpool-512R1
    - secp256r1
  - Montgomery form (hardware support for multiplication), such as:
    - Curve25519
- **SHA2 based MACs**
  - HMAC with SHA224, SHA256, SHA384, or SHA512
- Block cipher mode of operation
  - AESCCM
  - AESGCM
  - AESECB
  - AESCBC
  - AESCBC-MAC
- **True random number generation**

Other capabilities, such as RSA encryption and signatures as well as Edwards type of elliptic curves such as Curve1174 or Ed25519, can also be implemented using the provided hardware accelerators but are not part of the TI SimpleLink SDK for the CC1352P device.



## 6.7 Timers

A large selection of timers are available as part of the CC1352P device. These timers are:

- **Real-Time Clock (RTC)**

A 70-bit 3-channel timer running on the 32 kHz low frequency system clock (SCLK\_LF). This timer is available in all power modes except Shutdown. The timer can be calibrated to compensate for frequency drift when using the LF RCOSC as the low frequency system clock. If an external LF clock with frequency different from 32.768 kHz is used, the RTC tick speed can be adjusted to compensate for this. When using TI-RTOS, the RTC is used as the base timer in the operating system and should thus only be accessed through the kernel APIs such as the Clock module. The real time clock can also be read by the Sensor Controller Engine to timestamp sensor data and also has dedicated capture channels. By default, the RTC halts when a debugger halts the device.

- **General Purpose Timers (GPTIMER)**

The four flexible GPTIMERS can be used as either 4× 32 bit timers or 8× 16 bit timers, all running on up to 48 MHz. Each of the 16- or 32-bit timers support a wide range of features such as one-shot or periodic counting, pulse width modulation (PWM), time counting between edges and edge counting. The inputs and outputs of the timer are connected to the device event fabric, which allows the timers to interact with signals such as GPIO inputs, other timers, DMA and ADC. The GPTIMERS are available in Active and Idle power modes.

- **Sensor Controller Timers**

The Sensor Controller contains 3 timers:

AUX Timer 0 and 1 are 16-bit timers with a  $2^N$  prescaler. Timers can either increment on a clock or on each edge of a selected tick source. Both one-shot and periodical timer modes are available.

AUX Timer 2 is a 16-bit timer that can operate at 24 MHz, 2 MHz or 32 kHz independent of the Sensor Controller functionality. There are 4 capture or compare channels, which can be operated in one-shot or periodical modes. The timer can be used to generate events for the Sensor Controller Engine or the ADC, as well as for PWM output or waveform generation.

- **Radio Timer**

A multichannel 32-bit timer running at 4 MHz is available as part of the device radio. The radio timer is typically used as the timing base in wireless network communication using the 32-bit timing word as the network time. The radio timer is synchronized with the RTC by using a dedicated radio API when the device radio is turned on or off. This ensures that for a network stack, the radio timer seems to always be running when the radio is enabled. The radio timer is in most cases used indirectly through the trigger time fields in the radio APIs and should only be used when running the accurate 48 MHz high frequency crystal is the source of SCLK\_HF.

- **Watchdog timer**

The watchdog timer is used to regain control if the system operates incorrectly due to software errors. It is typically used to generate an interrupt to and reset of the device for the case where periodic monitoring of the system components and tasks fails to verify proper functionality. The watchdog timer runs on a 1.5 MHz clock rate and cannot be stopped once enabled. The watchdog timer pauses to run in Standby power mode and when a debugger halts the device.

## 6.8 Serial Peripherals and I/O

The SSIs are synchronous serial interfaces that are compatible with SPI, MICROWIRE, and TI's synchronous serial interfaces. The SSIs support both SPI master and slave up to 4 MHz. The SSI modules support configurable phase and polarity.

The UARTs implement universal asynchronous receiver and transmitter functions. They support flexible baud-rate generation up to a maximum of 3 Mbps.

The I<sup>2</sup>S interface is used to handle digital audio and can also be used to interface pulse-density modulation microphones (PDM).

The I<sup>2</sup>C interface is also used to communicate with devices compatible with the I<sup>2</sup>C standard. The I<sup>2</sup>C interface can handle 100 kHz and 400 kHz operation, and can serve as both master and slave.

The I/O controller (IOC) controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high-drive capabilities, which are marked in **bold** in [Section 4](#). All digital peripherals can be connected to any digital pin on the device.

For more information, see the [CC13x2, CC26x2 SimpleLink™ Wireless MCU Technical Reference Manual](#).

## 6.9 Battery and Temperature Monitor

A combined temperature and battery voltage monitor is available in the CC1352P device. The battery and temperature monitor allows an application to continuously monitor on-chip temperature and supply voltage and respond to changes in environmental conditions as needed. The module contains window comparators to interrupt the system CPU when temperature or supply voltage go outside defined windows. These events can also be used to wake up the device from Standby mode through the Always-On (AON) event fabric.

## 6.10 $\mu$ DMA

The device includes a direct memory access ( $\mu$ DMA) controller. The  $\mu$ DMA controller provides a way to offload data-transfer tasks from the system CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The  $\mu$ DMA controller can perform a transfer between memory and peripherals. The  $\mu$ DMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

Some features of the  $\mu$ DMA controller include the following (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels
- Transfer modes: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits
- Ping-pong mode for continuous streaming of data

## 6.11 Debug

The on-chip debug support is done through a dedicated cJTAG (IEEE 1149.7) or JTAG (IEEE 1149.1) interface. The device boots by default into cJTAG mode and must be reconfigured to use 4-pin JTAG.

## 6.12 Power Management

To minimize power consumption, the CC1352P supports a number of power modes and power management features (see [Table 6-2](#)).

**Table 6-2. Power Modes**

| MODE                               | SOFTWARE CONFIGURABLE POWER MODES |                     |                     |           | RESET PIN HELD |
|------------------------------------|-----------------------------------|---------------------|---------------------|-----------|----------------|
|                                    | ACTIVE                            | IDLE                | STANDBY             | SHUTDOWN  |                |
| CPU                                | Active                            | Off                 | Off                 | Off       | Off            |
| Flash                              | On                                | Available           | Off                 | Off       | Off            |
| SRAM                               | On                                | On                  | Retention           | Off       | Off            |
| Supply System                      | On                                | On                  | Duty Cycled         | Off       | Off            |
| Register and CPU retention         | Full                              | Full                | Partial             | No        | No             |
| SRAM retention                     | Full                              | Full                | Full                | No        | No             |
| 48 MHz high-speed clock (SCLK_HF)  | XOSC_HF or RCOSC_HF               | XOSC_HF or RCOSC_HF | Off                 | Off       | Off            |
| 2 MHz medium-speed clock (SCLK_MF) | RCOSC_MF                          | RCOSC_MF            | Available           | Off       | Off            |
| 32 kHz low-speed clock (SCLK_LF)   | XOSC_LF or RCOSC_LF               | XOSC_LF or RCOSC_LF | XOSC_LF or RCOSC_LF | Off       | Off            |
| Peripherals                        | Available                         | Available           | Off                 | Off       | Off            |
| Sensor Controller                  | Available                         | Available           | Available           | Off       | Off            |
| Wake-up on RTC                     | Available                         | Available           | Available           | Off       | Off            |
| Wake-up on pin edge                | Available                         | Available           | Available           | Available | Off            |
| Wake-up on reset pin               | On                                | On                  | On                  | On        | On             |
| Brownout detector (BOD)            | On                                | On                  | Duty Cycled         | Off       | Off            |
| Power-on reset (POR)               | On                                | On                  | On                  | Off       | Off            |
| Watchdog timer (WDT)               | Available                         | Available           | Paused              | Off       | Off            |

In **Active** mode, the application system CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see [Table 6-2](#)).

In **Idle** mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event brings the processor back into active mode.

In **Standby** mode, only the always-on (AON) domain is active. An external wake-up event, RTC event, or Sensor Controller event is required to bring the device back to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In **Shutdown** mode, the device is entirely turned off (including the AON domain and Sensor Controller), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake from shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between reset in this way and reset-by-reset pin or power-on reset by reading the reset status register. The only state retained in this mode is the latched I/O state and the flash memory contents.

The Sensor Controller is an autonomous processor that can control the peripherals in the Sensor Controller independently of the system CPU. This means that the system CPU does not have to wake up, for example to perform an ADC sampling or poll a digital sensor over SPI, thus saving both current and wake-up time that would otherwise be wasted. The [Sensor Controller Studio](#) tool enables the user to program the Sensor Controller, control its peripherals, and wake up the system CPU as needed. All Sensor Controller peripherals can also be controlled by the system CPU.

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**NOTE**

The power, RF and clock management for the CC1352P device require specific configuration and handling by software for optimized performance. This configuration and handling is implemented in the TI-provided drivers that are part of the CC1352P software development kit (SDK). Therefore, TI highly recommends using this software framework for all application development on the device. The complete [SDK](#) with TI-RTOS (optional), device drivers, and examples are offered free of charge in source code.

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### 6.13 Clock Systems

The CC1352P device has several internal system clocks.

The 48 MHz SCLK\_HF is used as the main system (MCU and peripherals) clock. This can be driven by the internal 48 MHz RC Oscillator (RCOSC\_HF) or an external 48 MHz crystal (XOSC\_HF). Radio operation requires an external 48 MHz crystal.

SCLK\_MF is an internal 2 MHz clock that is used by the Sensor Controller in low-power mode and also for internal power management circuitry. The SCLK\_MF clock is always driven by the internal 2 MHz RC Oscillator (RCOSC\_MF).

SCLK\_LF is the 32.768 kHz internal low-frequency system clock. It can be used by the Sensor Controller for ultra-low-power operation and is also used for the RTC and to synchronize the radio timer before or after Standby power mode. SCLK\_LF can be driven by the internal 32.8 kHz RC Oscillator (RCOSC\_LF), a 32.768 kHz watch-type crystal, or a clock input on any digital IO.

When using a crystal or the internal RC oscillator, the device can output the 32 kHz SCLK\_LF signal to other devices, thereby reducing the overall system cost.

### 6.14 Network Processor

Depending on the product configuration, the CC1352P device can function as a wireless network processor (WNP - a device running the wireless protocol stack with the application running on a separate host MCU), or as a system-on-chip (SoC) with the application and protocol stack running on the system CPU inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

## 7 Application, Implementation, and Layout

### NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

For general design guidelines and hardware configuration guidelines, refer to [CC13xx/CC26xx Hardware Configuration and PCB Design Considerations Application Report](#).

For optimum RF performance, especially when using the high-power PA, it is important to accurately follow the reference design with respect to component values and layout. Failure to do so may lead to reduced RF performance due to balun mismatch. The amplitude- and phase balance through the balun must be <1 dB and <6 degrees, respectively.

PCB stack-up is also critical for proper operation. The CC1352P EVMs and characterization boards are using a finished thickness between the top layer (RF signals) and layer 2 (ground plane) of 175  $\mu\text{m}$ . It is very important to use the same substrate thickness, or slightly thicker, in an end product implementing the CC1352P device.

Integrated balun devices can be used both at sub-1 GHz frequencies and at 2.4 GHz. The following baluns are recommended for CC1352P high-power PA output:

- Johanson Technology 1720BL15B0200E
- Anaren BD0826J50200AH

### 7.1 Reference Designs

The following reference designs should be followed closely when implementing designs using the CC1352P device.

Special attention must be paid to RF component placement, decoupling capacitors and DCDC regulator components, as well as ground connections for all of these.

The high-power PA requires a specific RF matching to be able to run at 10 dBm output power. Refer to the application note [Optimizing the SimpleLink CC1352P for Coin Cell Operation at 10 dBm Output Power](#) for details.

#### [CC1352PEM-XD7793-XD24-PA9093 Design Files](#)

The CC1352PEM-XD7793-XD24-PA9093 reference design provides schematic, layout and production files for the characterization board used for deriving the performance number found in this document. This board includes tuning for 915 MHz on the high-power PA output.

#### [CC1352PEM-XD7793-XD24-PA24 Design Files](#)

The CC1352PEM-XD7793-XD24-PA24 reference design provides schematic, layout and production files for the characterization board used for deriving the performance number found in this document. This board includes tuning for 2.4 GHz on the high-power PA output.

#### [LAUNCHXL-CC1352P1 Design Files](#)

Detailed schematics and layouts for the multi-band CC1352P LaunchPad evaluation board featuring 868/915 MHz RF matching on the 20 dBm PA output and up to 5 dBm TX power at 2.4 GHz.

#### [LAUNCHXL-CC1352P-2 Design Files](#)

Detailed schematics and layouts for the multi-band CC1352P LaunchPad evaluation board featuring 2.4 GHz RF matching on the 20 dBm PA output and up to 14 dBm TX power at 868/915 MHz.

### LAUNCHXL-CC1352P-4 Design Files

Detailed schematics and layouts for the multi-band CC1352P LaunchPad evaluation board featuring 2.4 GHz RF matching optimized for 10 dBm operation on the 20 dBm PA output and up to 13 dBm TX power at 433 MHz.

### Sub-1 GHz and 2.4 GHz Antenna Kit for LaunchPad™ Development Kit and SensorTag

The antenna kit allows real-life testing to identify the optimal antenna for your application. The antenna kit includes 16 antennas for frequencies from 169 MHz to 2.4 GHz, including:

- PCB antennas
- Helical antennas
- Chip antennas
- Dual-band antennas for 868 MHz and 915 MHz combined with 2.4 GHz

The antenna kit includes a JSC cable to connect to the Wireless MCU LaunchPad Development Kits and SensorTags.

## 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed as follows.

### 8.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to all part numbers and/or date-code. Each device has one of three prefixes/identifications: X, P, or null (no prefix) (for example, XCC1352P is in preview; therefore, an X prefix/identification is assigned).

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null** Production version of the silicon die that is fully qualified.

Production devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, RGZ).

For orderable part numbers of CC1352P devices in the RGZ (7-mm x 7-mm) package type, see the *Package Option Addendum* of this document, the Device Information in [Section 1.3](#), the TI website ([www.ti.com](http://www.ti.com)), or contact your TI sales representative.

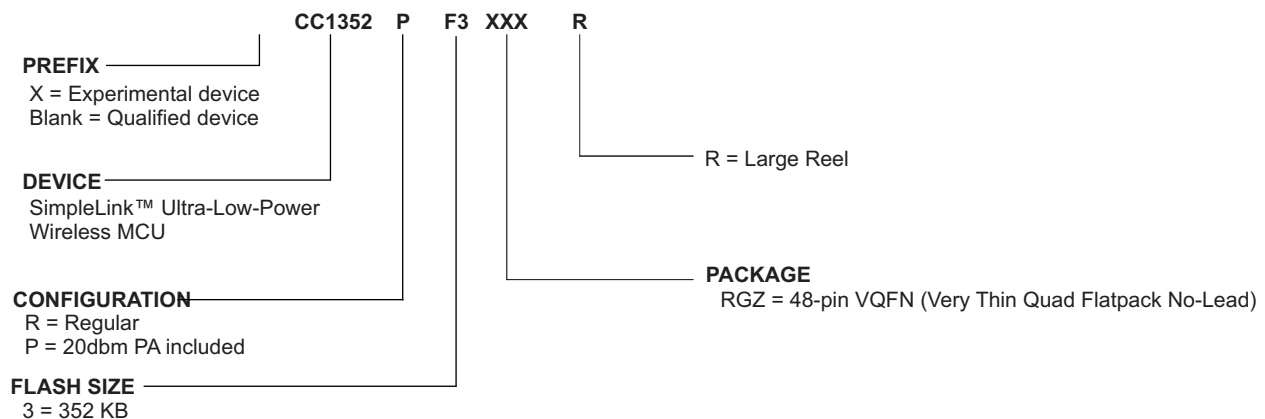


Figure 8-1. Device Nomenclature



## 8.2 Tools and Software

The CC1352P device is supported by a variety of software and hardware development tools.

### Development Kit

#### CC1352P1 LaunchPad™ Development Kit

The CC1352P1 LaunchPad™ Development Kit enables development of high-performance wireless applications in the 863 - 930 MHz and 2.4 GHz frequency bands that benefit from low-power operation. The kit features the CC1352P multi-band and multiprotocol SimpleLink Wireless MCU with an integrated High-Power Amplifier. The kit works with the LaunchPad ecosystem, easily enabling additional functionality like sensors, display, and more. The built-in EnergyTrace™ software is an energy-based code analysis tool that measures and displays the application's energy profile and helps to optimize it for ultra-low power consumption.

The RF configuration of the LaunchPad enables up to +20 dBm output power for 863 to 930 MHz and +5 dBm output power for 2.4 GHz.

#### CC1352P-2 LaunchPad™ Development Kit

The CC1352P-2 LaunchPad™ Development Kit enables development of high-performance wireless applications in the 863 - 930 MHz and 2.4 GHz frequency bands that benefit from low-power operation. The kit features the CC1352P multi-band and multiprotocol SimpleLink Wireless MCU with an integrated High-Power Amplifier. The kit works with the LaunchPad ecosystem, easily enabling additional functionality like sensors, display, and more. The built-in EnergyTrace™ software is an energy-based code analysis tool that measures and displays the application's energy profile and helps to optimize it for ultra-low power consumption.

The RF configuration of the LaunchPad enables up to +14 dBm output power for 863 to 930 MHz and +20 dBm output power for 2.4 GHz.

### Software

#### SimpleLink™ CC13X2-CC26X2 SDK

The SimpleLink CC13X2-CC26X2 Software Development Kit (SDK) provides a complete package for the development of wireless applications on the CC13X2 / CC26X2 family of devices. The SDK includes a comprehensive software package for the CC1352P device, including the following protocol stacks:

- Bluetooth Low Energy 4 and 5.1
- Thread (based on OpenThread)
- Zigbee 3.0
- TI 15.4-Stack - an IEEE 802.15.4-based star networking solution for Sub-1 GHz and 2.4 GHz
- EasyLink - a large set of building blocks for building proprietary RF software stacks
- Multiprotocol support - concurrent operation between stacks using the Dynamic Multiprotocol Manager (DMM)

The SimpleLink CC13X2-CC26X2 SDK is part of TI's SimpleLink MCU platform, offering a single development environment that delivers flexible hardware, software and tool options for customers developing wired and wireless applications. For more information about the SimpleLink MCU Platform, visit <http://www.ti.com/simplelink>.



## Development Tools

### Code Composer Studio™ Integrated Development Environment (IDE)

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse® software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

CCS has support for all SimpleLink Wireless MCUs and includes support for EnergyTrace™ software (application energy usage profiling). A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK.

Code Composer Studio is provided free of charge when used in conjunction with the XDS debuggers included on a LaunchPad Development Kit.

### Code Composer Studio™ Cloud IDE

Code Composer Studio (CCS) Cloud is a web-based IDE that allows you to create, edit and build CCS and Energia™ projects. After you have successfully built your project, you can download and run on your connected LaunchPad. Basic debugging, including features like setting breakpoints and viewing variable values is now supported with CCS Cloud.

### IAR Embedded Workbench® for Arm®

IAR Embedded Workbench® is a set of development tools for building and debugging embedded system applications using assembler, C and C++. It provides a completely integrated development environment that includes a project manager, editor, and build tools. IAR has support for all SimpleLink Wireless MCUs. It offers broad debugger support, including XDS110, IAR I-jet™ and Segger J-Link™. A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK. IAR is also supported out-of-the-box on most software examples provided as part of the SimpleLink SDK.

A 30-day evaluation or a 32 KB size-limited version is available through [iar.com](http://iar.com).

### SmartRF™ Studio

SmartRF™ Studio is a Windows® application that can be used to evaluate and configure SimpleLink Wireless MCUs from Texas Instruments. The application will help designers of RF systems to easily evaluate the radio at an early stage in the design process. It is especially useful for generation of configuration register values and for practical testing and debugging of the RF system. SmartRF Studio can be used either as a standalone application or together with applicable evaluation boards or debug probes for the RF device. Features of the SmartRF Studio include:

- Link tests - send and receive packets between nodes
- Antenna and radiation tests - set the radio in continuous wave TX and RX states
- Export radio configuration code for use with the TI SimpleLink SDK RF driver
- Custom GPIO configuration for signaling and control of external switches

### Sensor Controller Studio

Sensor Controller Studio is used to write, test and debug code for the Sensor Controller peripheral. The tool generates a Sensor Controller Interface driver, which is a set of C source files that are compiled into the System CPU application. These source files also contain the Sensor Controller binary image and allow the System CPU application to control and exchange data with the Sensor Controller. Features of the Sensor Controller Studio include:

- Ready-to-use examples for several common use cases
- Full toolchain with built-in compiler and assembler for programming in a C-like programming language
- Provides rapid development by using the integrated sensor controller task testing and debugging functionality, including visualization of sensor data and verification of algorithms

## CCS UniFlash

CCS UniFlash is a standalone tool used to program on-chip flash memory on TI MCUs. UniFlash has a GUI, command line, and scripting interface. CCS UniFlash is available free of charge.

### 8.2.1 SimpleLink™ Microcontroller Platform

The SimpleLink microcontroller platform sets a new standard for developers with the broadest portfolio of wired and wireless Arm® MCUs (System-on-Chip) in a single software development environment. Delivering flexible hardware, software and tool options for your IoT applications. Invest once in the SimpleLink software development kit and use throughout your entire portfolio. Learn more on [ti.com/simplelink](http://ti.com/simplelink).

### 8.3 Documentation Support

To receive notification of documentation updates on data sheets, errata, application notes and similar, navigate to the device product folder on [ti.com/product/CC1352P](http://ti.com/product/CC1352P). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the MCU, related peripherals, and other technical collateral is listed as follows.

#### TI Resource Explorer

##### TI Resource Explorer

Software examples, libraries, executables, and documentation are available for your device and development board.

#### Errata

##### CC1352P Silicon Errata

The silicon errata describes the known exceptions to the functional specifications for each silicon revision of the device and description on how to recognize a device revision.

#### Application Reports

All application reports for the CC1352P device are found on the device product folder at: [ti.com/product/CC1352P/technicaldocuments](http://ti.com/product/CC1352P/technicaldocuments).

#### Technical Reference Manual (TRM)

##### CC13x2, CC26x2 SimpleLink™ Wireless MCU TRM

The TRM provides a detailed description of all modules and peripherals available in the device family.

## 8.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

## 8.5 Trademarks

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## 8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

# 9 Mechanical, Packaging, and Orderable Information

## 9.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CC1352P1F3RGZR   | ACTIVE        | VQFN         | RGZ             | 48   | 2500        | Green (RoHS & no Sb/Br) | NIPDAU   NIPDAUAG       | Level-3-260C-168 HR  | -40 to 85    | CC1352<br>P1F3          | <a href="#">Samples</a> |
| CC1352P1F3RGZT   | ACTIVE        | VQFN         | RGZ             | 48   | 250         | Green (RoHS & no Sb/Br) | NIPDAU   NIPDAUAG       | Level-3-260C-168 HR  | -40 to 85    | CC1352<br>P1F3          | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CC1352P1F3RGZR | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| CC1352P1F3RGZT | VQFN         | RGZ             | 48   | 250  | 180.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CC1352P1F3RGZR | VQFN         | RGZ             | 48   | 2500 | 336.6       | 336.6      | 31.8        |
| CC1352P1F3RGZT | VQFN         | RGZ             | 48   | 250  | 210.0       | 185.0      | 35.0        |

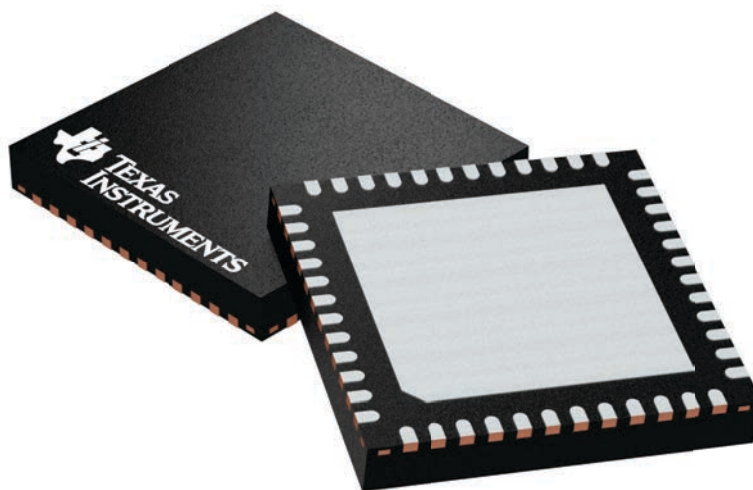
## GENERIC PACKAGE VIEW

**RGZ 48**

**VQFN - 1 mm max height**

7 x 7, 0.5 mm pitch

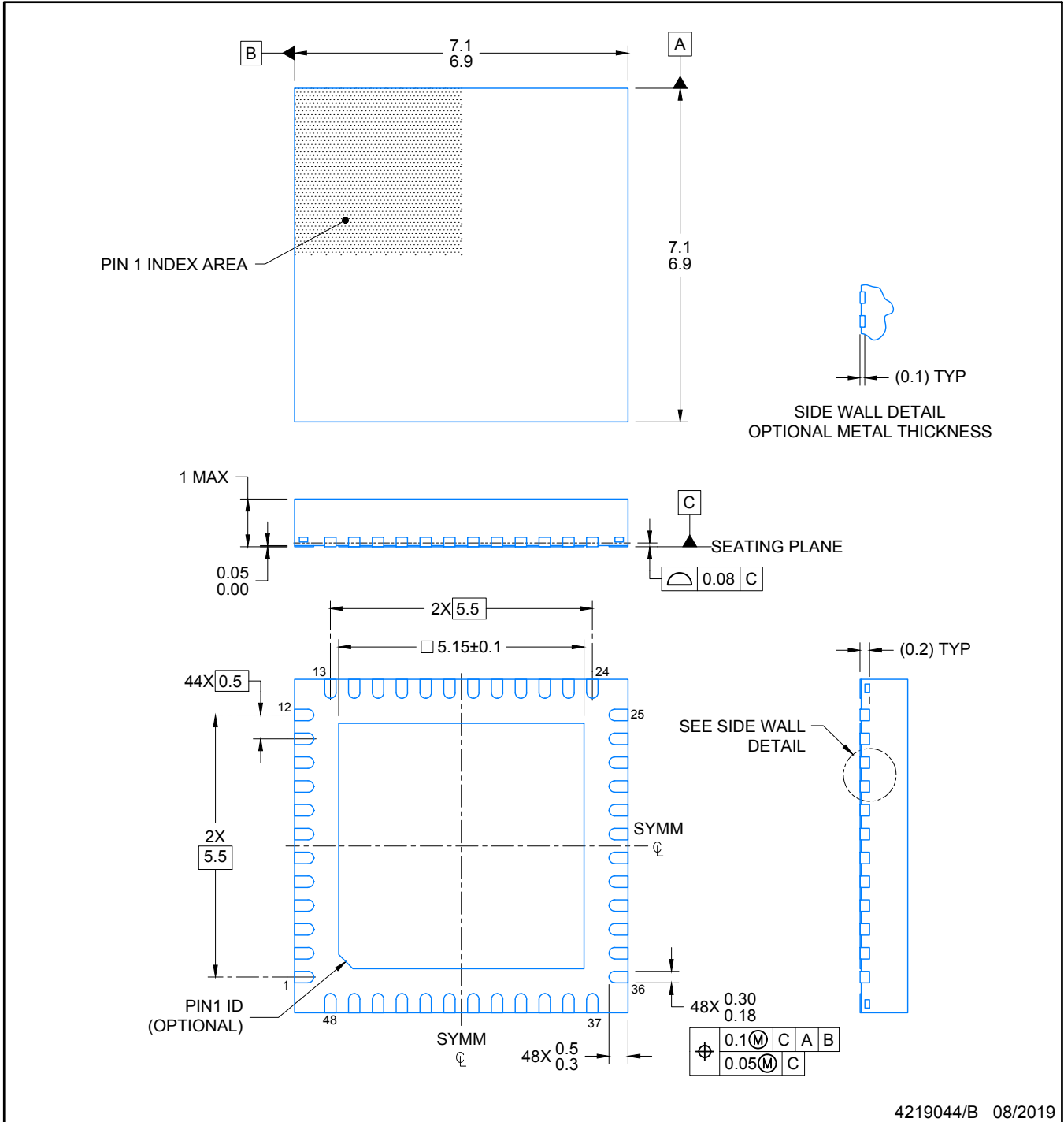
PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224671/A

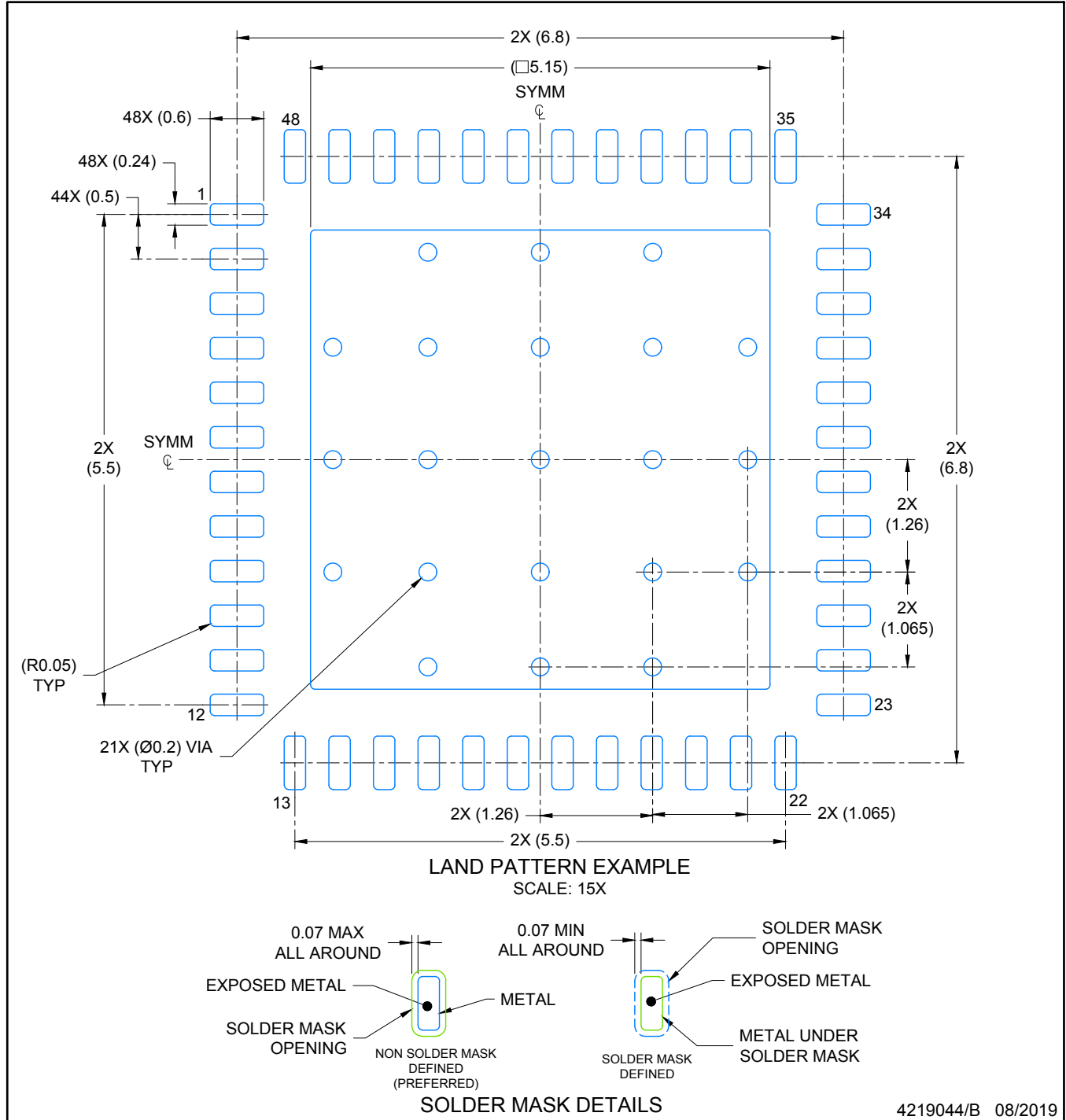




4219044/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



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