MP28301

Ultra-Low 500nA I_Q, Wide Input 2-5.5V, 700mA Step-Down Regulator Plus 300nAI_Q, 2-5.5V Input, 100mA LDO in a 2x2mm QFN

The Future of Analog IC Technology

DESCRIPTION

The MP28301 is a monolithic power-management unit containing a 700mA, high-efficiency, step-down, switching converter and a 100mA LDO regulator. The nA quiescent current provides extremely high efficiency when the load current is in the µA range. With the minimum input voltage as low as 2V, the MP28301 allows the system to operate directly from the battery.

The constant-on-time (COT) control scheme provides fast transient response, high light-load efficiency, and requires minimal capacitance. The regulation is made tight by integrating an error amplifier to correct the output voltage.

A 100mA LDO regulator provides easy system configuration with a clean output voltage.

The CTRL pins control the on/off and output voltage selection functions.

Fault protection features include under-voltage lockout (UVLO), over-current protection (OCP), and thermal shutdown.

The MP28301 requires a minimal number of readily available, standard, external components and is available in a small QFN-12 (2mmx2mm) package.

FEATURES

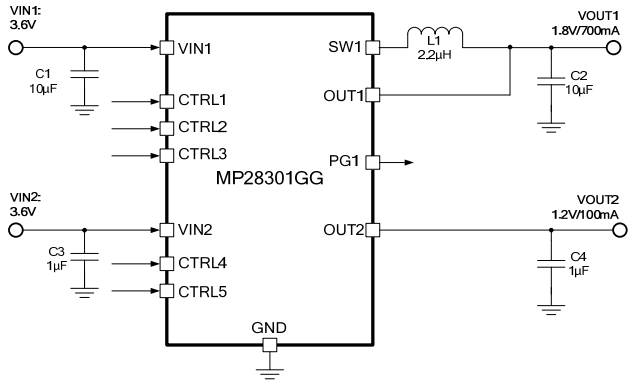
- 700mA Buck Switcher
  - Ultra-Low I_Q: 500nA
  - Wide 2.0V to 5.5V Operating Input Range
  - Seven Selectable Output Voltages
  - Up to 700mA Output Current
  - 1.5MHz Switching Frequency in Continuous Conduction Mode (CCM)
  - 100% Duty Cycle in Dropout
  - 0.25Ω and 0.25Ω Internal Power MOSFET Switches
  - Cycle-by-Cycle Over-Current Protection (OCP)
  - Short-Circuit Protection (SCP) with Hiccup Mode
- 100mA LDO
  - Ultra-Low I_Q: 300nA
  - 2.0V to 5.5V Operating Input Range
  - Three Selectable Output Voltages
  - Over-Temperature Protection (OTP)
- Available in a QFN-12 (2mmx2mm)Package

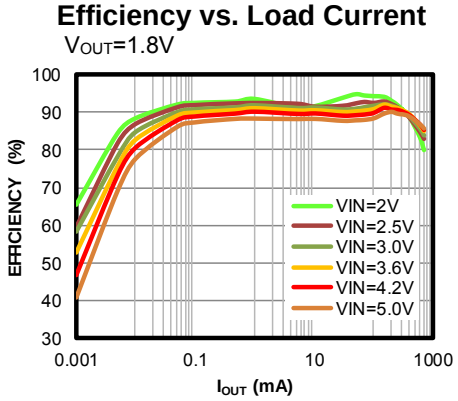
APPLICATIONS

- Wearables
- IoT Devices
- Portable Instruments
- Battery-Powered Devices

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TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP28301GG	QFN-12 (2mmx2mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP28301GG–Z)

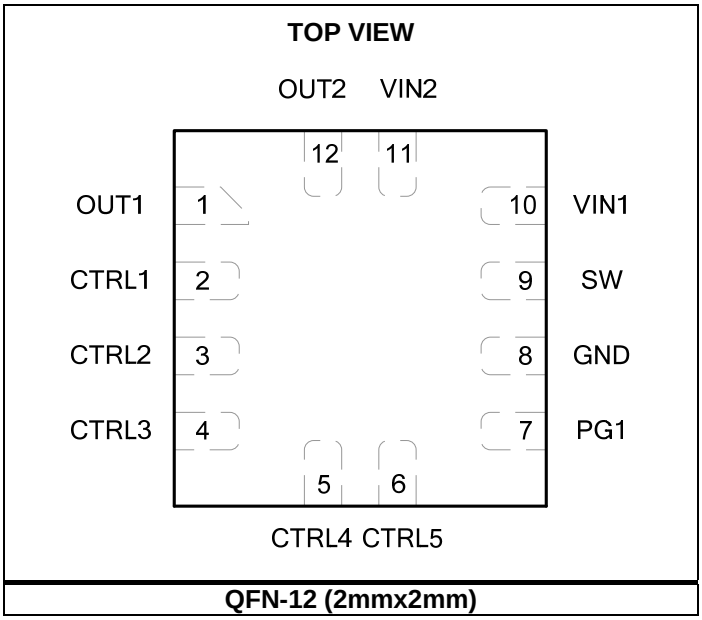
TOP MARKING

EGY

LLL

EG: Product code of MP28301GG
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



QFN-12 (2mmx2mm)

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (VIN1/2)..... 6V
V_{SW1} .....
-0.3V (-5V for <10ns) to
6V (8V for <10ns or 10V for <3ns)
All other pins ..... -0.3V to 6V
Continuous power dissipation (T_A=+25°C)
..... 1.6W(2)
Junction temperature ..... 150°C
Lead temperature..... 260°C
Storage temperature .....-65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (VIN1/2)..... 2.0V to 5.5V
Operating junction temp. (T_J)....-40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-12 (2mmx2mm).....	80	16 ...	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

VIN1 = 3.6V, VIN2 = 3.6V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Buck Section						
Input voltage range(5)	V_{IN1}		2.0		5.5	V
Under-voltage lockout threshold rising for buck	$V_{IN1_UVLO_R}$		1.65	1.8	1.95	V
Under-voltage lockout threshold hysteresis for buck	$V_{IN1_UVLO_H}$			150		mV
Supply current (shutdown)	I_{SD_25}	CTRL1/2/3=0V, or EN=0		70		nA
Supply current (quiescent)	I_{Q_BUCK}	No load, CTRL4/5=0V, CTRL1/2/3=H/L/H, OUT1=1.8V, not switching		500		nA
High-side switch on resistance	R_{DSON1_H}			0.25		Ω
Low-side switch on resistance	R_{DSON1_L}			0.25		Ω
Switch leakage current	I_{LK_SW1}	CTRL1/2/3 = 0V, VIN1=5.5V, V_{SW} = 0V and 5.5V, T_J=25°C	-100	0	100	nA
High-side current limit	I_{LIM1_H}		1000	1200	1400	mA
Low-side switch valley current (sourcing)	I_{LIMV1_L}		750	920		mA
Low-side switch zero crossing current	I_{ZCD}		0	20		mA
On time	T_{ON}	V_{IN1}=3.6V, V_{OUT}=1.8V	280	330	380	ns
Input voltage range for LDO(5)	V_{IN2}	When V_{IN1}>V_{IN1_UVLO}	2.0		5.5	V
Minimum on time	T_{MIN_ON}			60		ns
Minimum off time	T_{MIN_OFF}			100		ns
Maximum duty cycle(5)	D_{MAX}			100		%
Output voltage accuracy	V_{OUT}	CTRL1/2/3=H/L/H, T_J=25°C, I_{OUT}=0.1A	1.782	1.800	1.818	V
		CTRL1/2/3=H/L/H, T_J=-40°C to 85°C, I_{OUT}=0.1A	1.773		1.827	
Line/load regulation of buck(6)		From 2.5V to 5.5V, from 0A to 700mA	-1		1	%
LDO Section						
Supply current (quiescent)	IQ_LDO	No load, CTRL1/2/3 = 0V, CTRL4/5 = L/H, no load current from VIN2		300		nA
Supply current (shutdown)	ISD_25	CTRL4/5 = 0V, or EN = 0		50		nA
Voltage dropout of LDO	VDP	I_{LDO} = 0.1A, V_{OUT} = 3.0V		50		mV
Dropout resistance	RDP			0.5		Ω

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ELECTRICAL CHARACTERISTICS*(continued)*

VIN1 = 3.6V, VIN2 = 3.6V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Current limit of LDO	I_{LIM_LDO}		150	200		mA
DC output voltage accuracy	V_{OUT}	CTRL4/5=H/L, T_J=25°C,	1.188	1.200	1.212	V
		CTRL4/5=H/L,T_J=-40°C to 85°C	1.182		1.218	
		Internal reference, T_A=-40°C to 85°C	0.591	0.600	0.609	
Line regulation of LDO		I_{OUT}=1mA		0		%
Load regulation of LDO		I_{OUT}=1mA to 100mA	-1		1	%
Power supply rejection ratio(6)	PSRR	10Hz, I_{OUT}=100mA		40		dB
		100Hz, I_{OUT}=100mA		20		
		1kHz, I_{OUT}=100mA		15		
Both Buck and LDO						
Internal soft-start time	T_{SS}	Buck		110		µs
		LDO: V_{OUT} = 3.0V, I_{OUT} = 100mA, Co = 1µF		2		ms
Discharge resistance during enable off	R_{DIS_OFF}			50		Ω
CTRL high logic	$CTRL_H$		1.2			V
CTRL low logic	$CTRL_L$				0.4	V
CTRL input current	I_{CTRL}	V_{CTRL} = 3.6V		1		nA
		V_{CTRL} = 0		0		
		V_{EN} = 0V		0		
CTRL 1/2/3 turn-on delay	T_{D123}			200		µs
CTRL4/5turn-on delay	T_{D45}			300		
CTRL pull-down resistor	R_{PD}	Not present when CTRL is high to avoid I_Q impact		2		MΩ
Power good threshold	PG	FB with respect to the regulation		90		%
Power good hysteresis	PG_{Hys}			10		%
Power good delay	PG_{TD}			75		µs
Power good sink current capability	V_{PG_LO}	Sink 1mA			0.4	V
Power good leakage current	I_{PGLK}	V_{PGBUS}=1.8V			10	nA
Thermal shutdown (5)	T_{SD}			150		°C
Thermal hysteresis (5)	T_{SDHY}			30		°C

NOTES:

5) Guaranteed by design.
6) Data derived from bench characterization test.

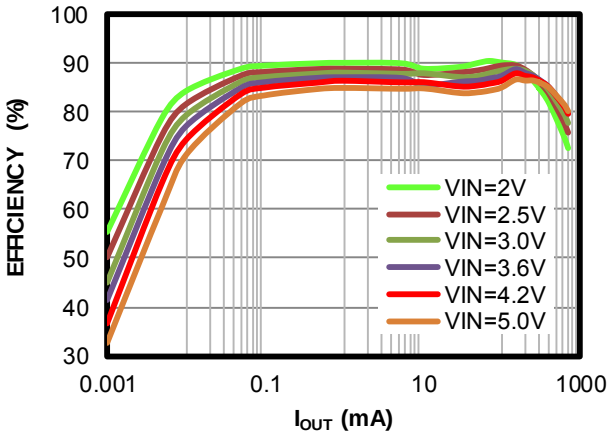
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TYPICAL PERFORMANCE CHARACTERISTICS

VIN1=3.6V, V_{OUT1}=1.8V, L_1=2.2µH, C_{IN1}=10µF, C_{OUT1}=10µF, VIN2=3.6V, V_{OUT2}=1.2V, C_{IN2}=1µF, C_{OUT2}=1µF, T_A = +25°C, unless otherwise noted.

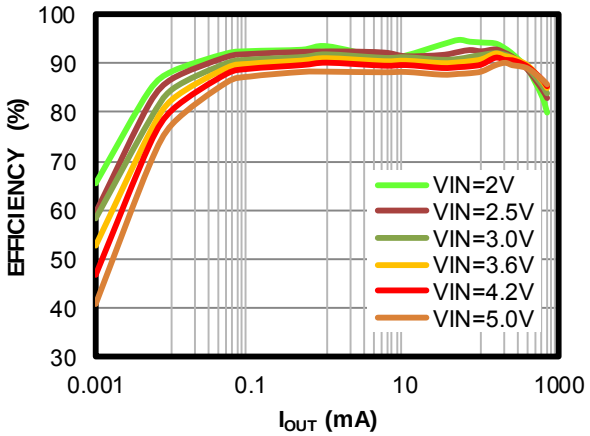
Efficiency vs. Load Current

V_{OUT}=1.2V



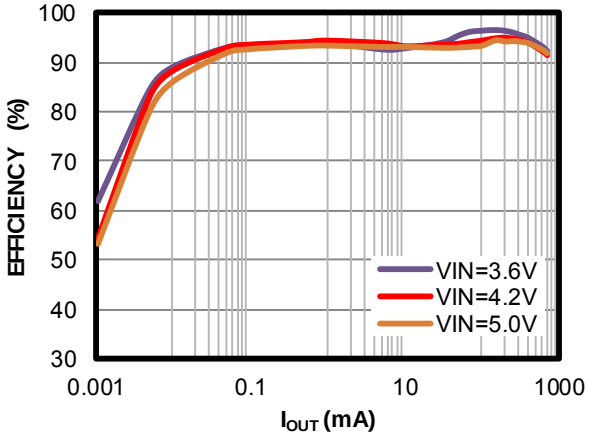
Efficiency vs. Load Current

V_{OUT}=1.8V

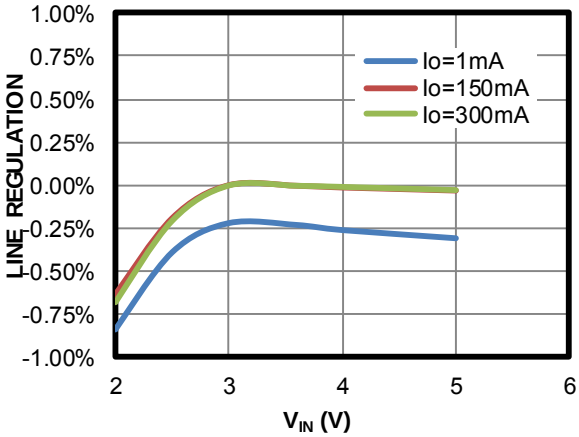


Efficiency vs. Load Current

V_{OUT}=3.3V

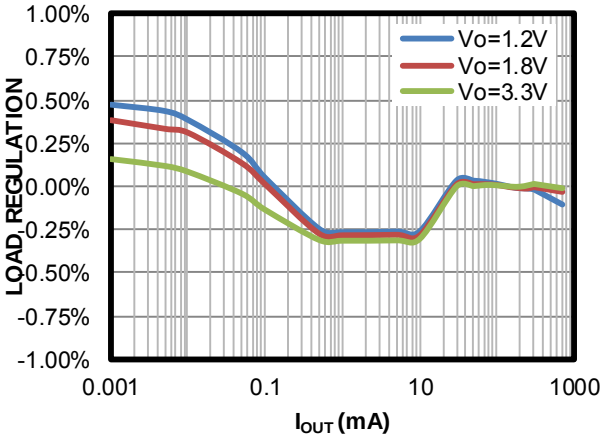


Line Regulation vs. Load Current



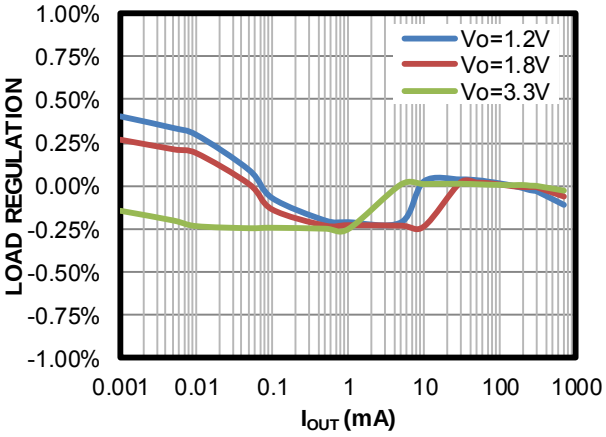
Load Regulation vs. Load Current

V_{IN}=5V



Load Regulation vs. Load Current

V_{IN}=3.6V

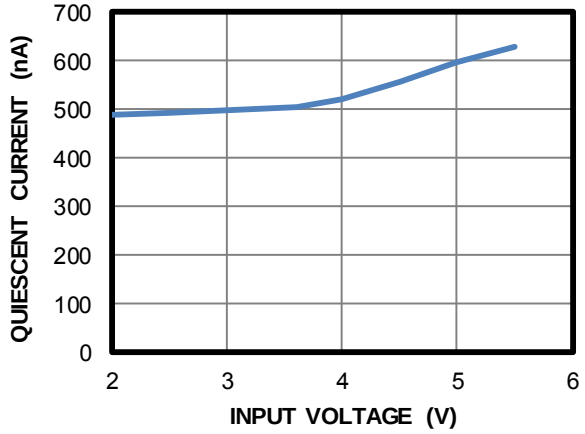


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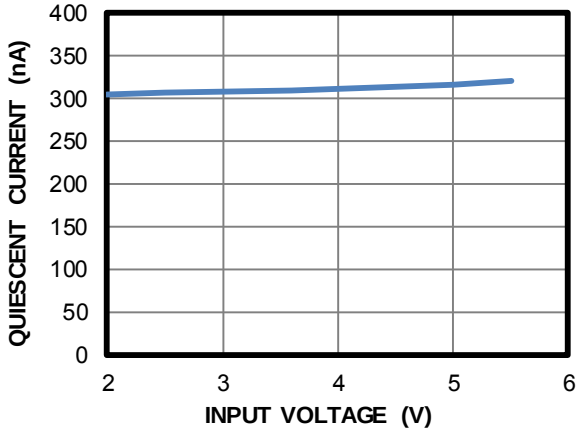
TYPICAL PERFORMANCE CHARACTERISTICS*(continued)*

VIN1=3.6V, V_{OUT1}=1.8V, L_1=2.2µH, C_{IN1}=10µF, C_{OUT1}=10µF, VIN2=3.6V, V_{OUT2}=1.2V, C_{IN2}=1µF, C_{OUT2}=1µF, T_A = +25°C, unless otherwise noted.

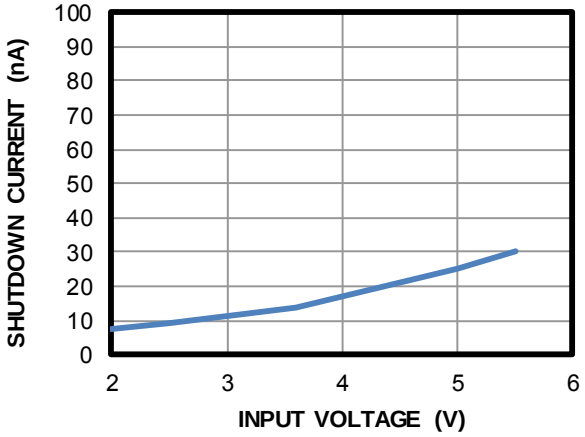
Buck Quiescent Current vs. Input Voltage



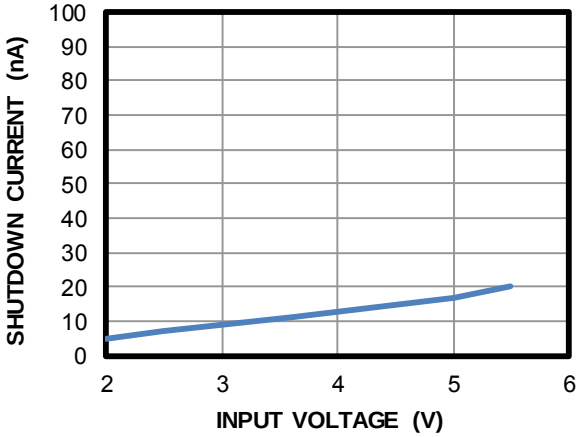
LDO Quiescent Current vs. Input Voltage



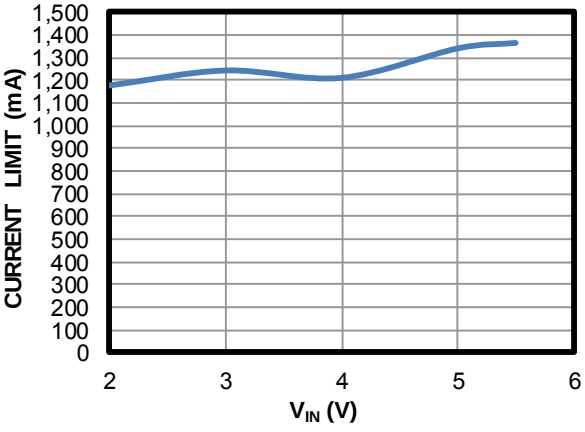
Buck Shutdown Current vs. Input Voltage



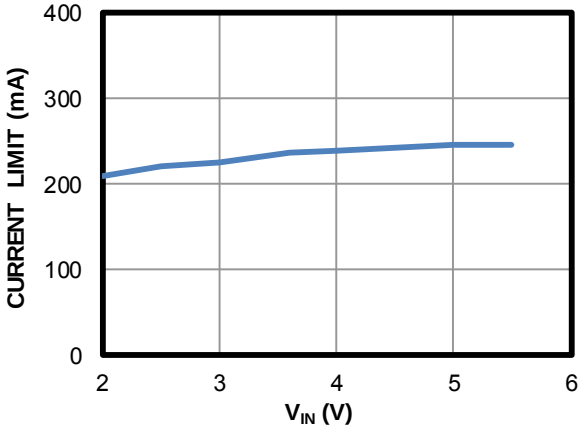
LDO Shutdown Current vs. Input Voltage



Buck Current Limit vs. V_{IN}



LDO Current Limit vs. V_{IN}

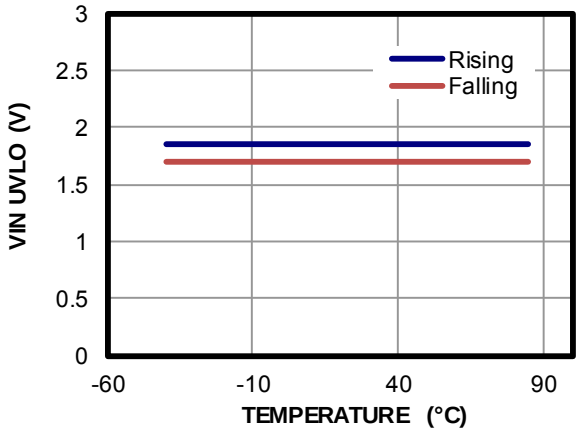


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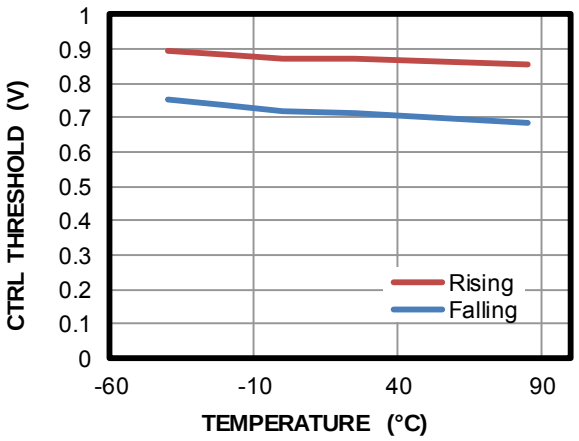
TYPICAL PERFORMANCE CHARACTERISTICS*(continued)*

VIN1=3.6V, V_{OUT1}=1.8V, L_1=2.2µH, C_{IN1}=10µF, C_{OUT1}=10µF, VIN2=3.6V, V_{OUT2}=1.2V, C_{IN2}=1µF, C_{OUT2}=1µF, T_A = +25°C, unless otherwise noted.

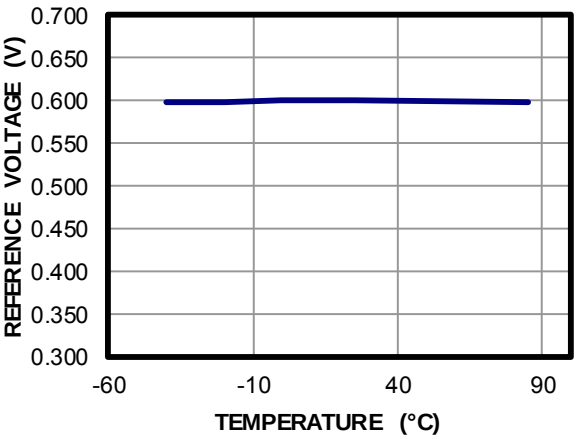
Buck V_{IN} UVLO Rising Threshold vs. Temperature



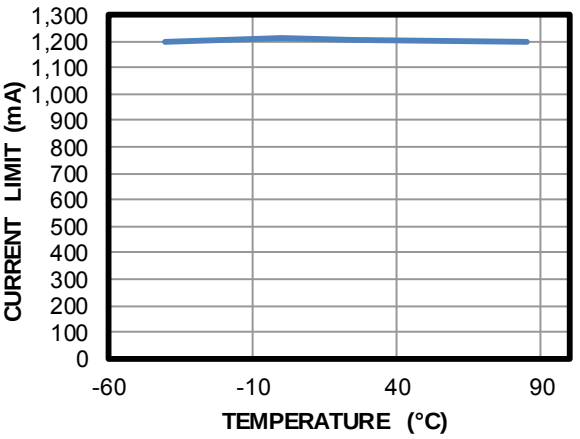
CTRL Rising and Falling Threshold vs. Temperature



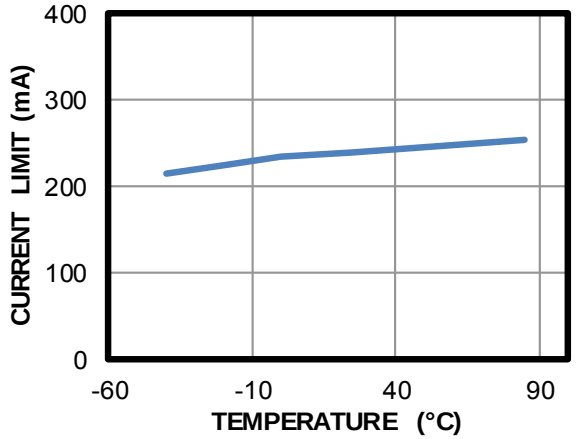
Reference Voltage vs. Temperature



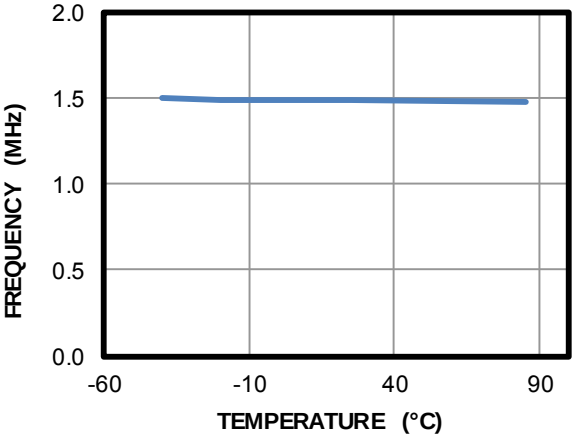
Buck Current Limit vs. Temperature



LDO Current Limit vs. Temperature



Frequency vs. Temperature



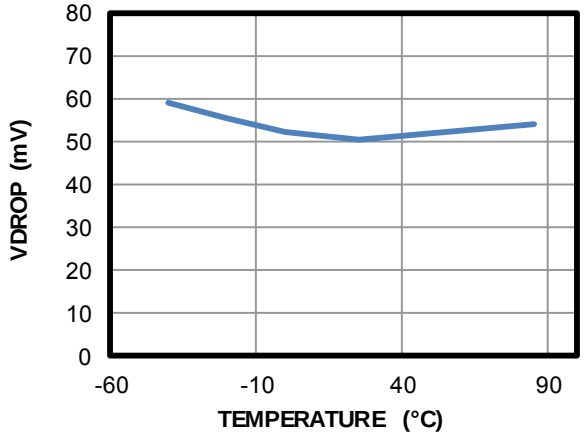
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TYPICAL PERFORMANCE CHARACTERISTICS*(continued)*

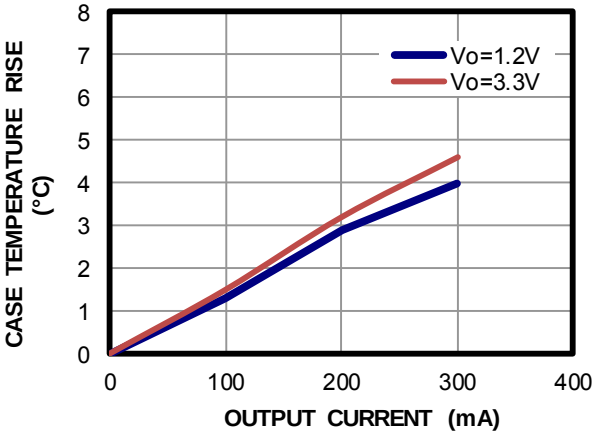
VIN1=3.6V, V_{OUT1}=1.8V, L_1=2.2µH, C_{IN1}=10µF, C_{OUT1}=10µF, VIN2=3.6V, V_{OUT2}=1.2V, C_{IN2}=1µF, C_{OUT2}=1µF, T_A = +25°C, unless otherwise noted.

LDO V_{DROP} vs. Temperature

LDO current=0.1A, V_{OUT}=3V

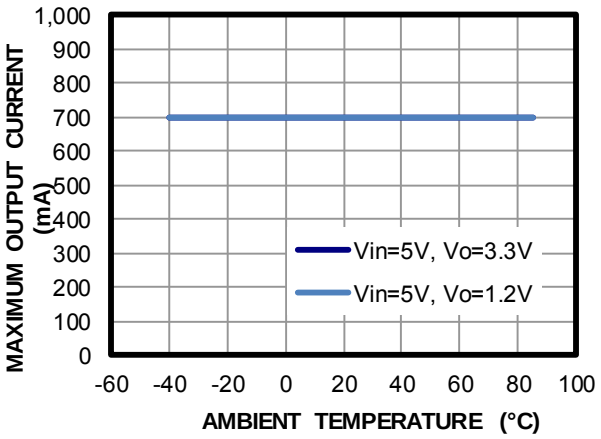


T_{RISING}vs. Output Current



Output Current Derating vs. Ambient Temperature

T_J≤ 125°C

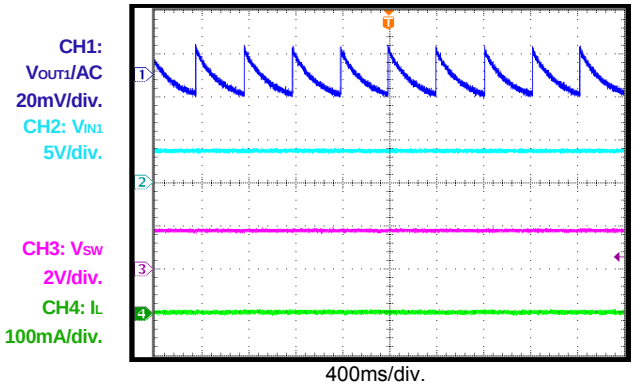


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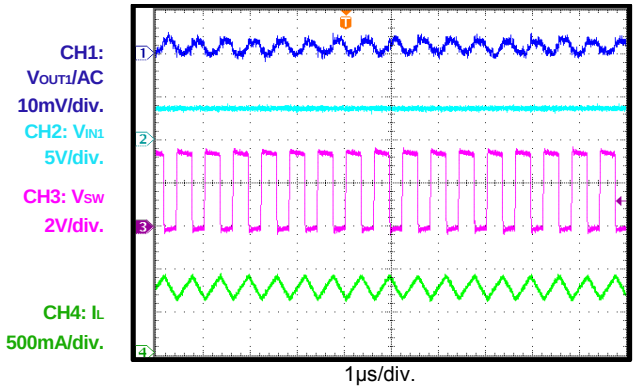
TYPICAL PERFORMANCE CHARACTERISTICS*(continued)*

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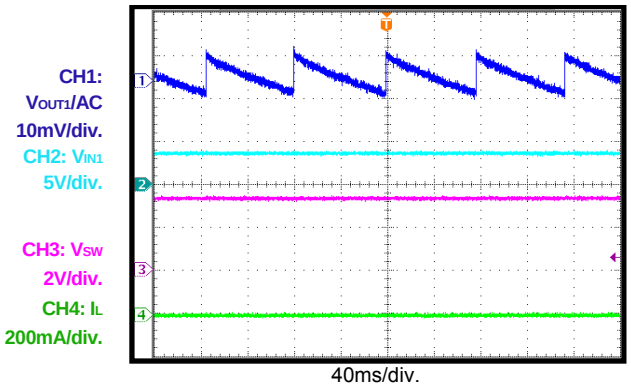
Steady State
I_{OUT1}=0A



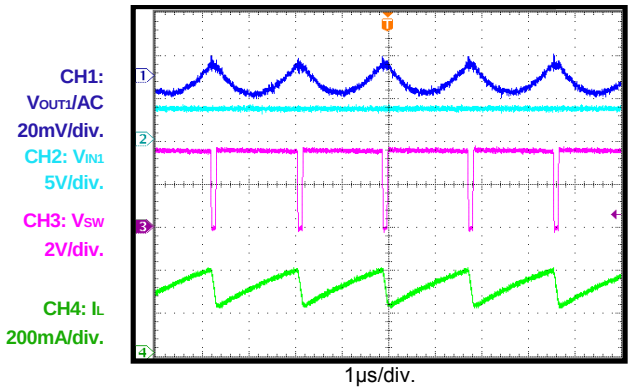
Steady State
I_{OUT1}=0.7A



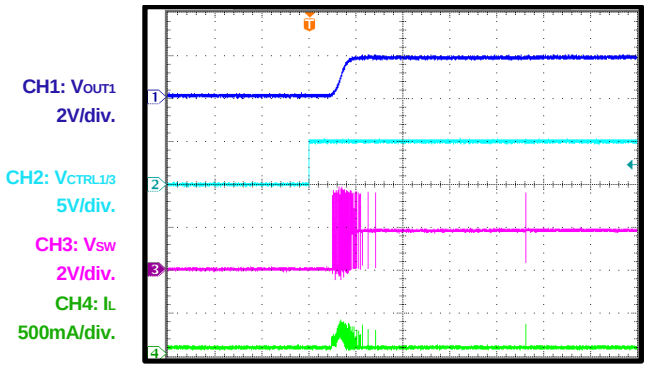
Steady State
V_{OUT1}=3.3V, I_{OUT1}=0A



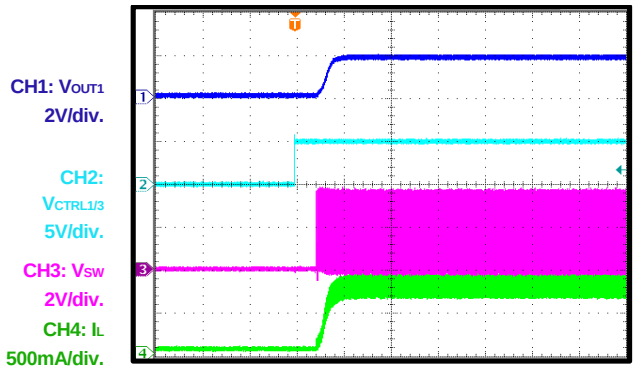
Steady State
V_{OUT1}=3.3V, I_{OUT1}=0.3A



CTRL On
I_{OUT1}=0A



CTRL On
I_{OUT1}=0.7A



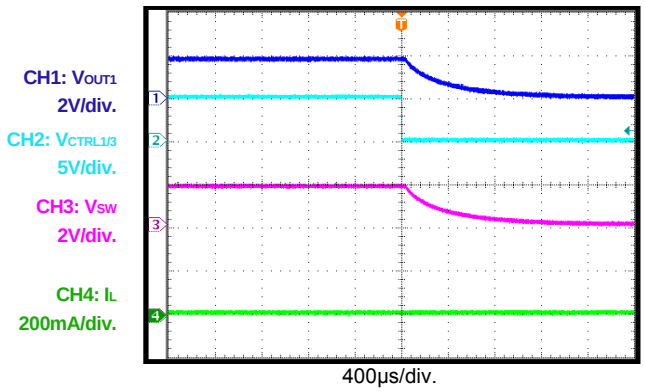
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TYPICAL PERFORMANCE CHARACTERISTICS*(continued)*

VIN1=3.6V, V_{OUT1}=1.8V, L_1=2.2µH, C_{IN1}=10µF, C_{OUT1}=10µF, VIN2=3.6V, V_{OUT2}=1.2V, C_{IN2}=1µF, C_{OUT2}=1µF, T_A = +25°C, unless otherwise noted.

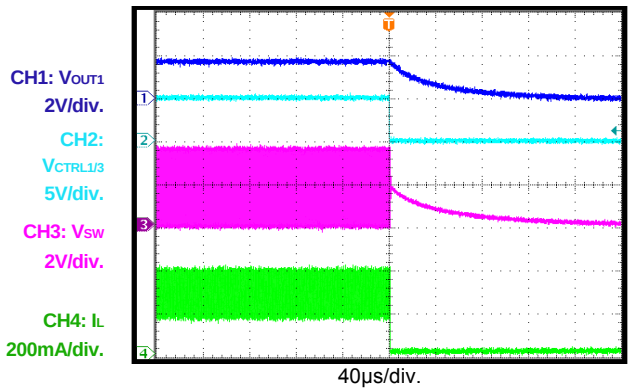
CTRL Off

I_{OUT1}=0A



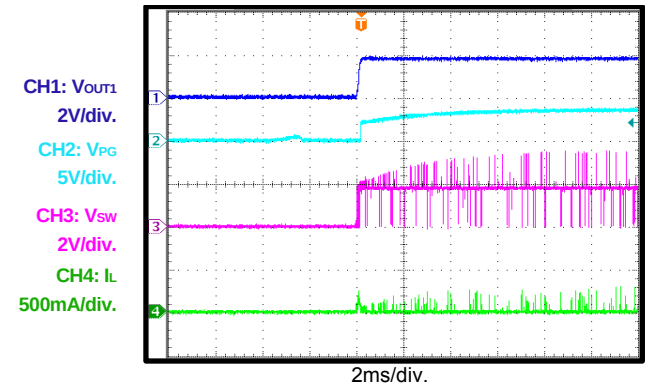
CTRL Off

I_{OUT1}=0.3A



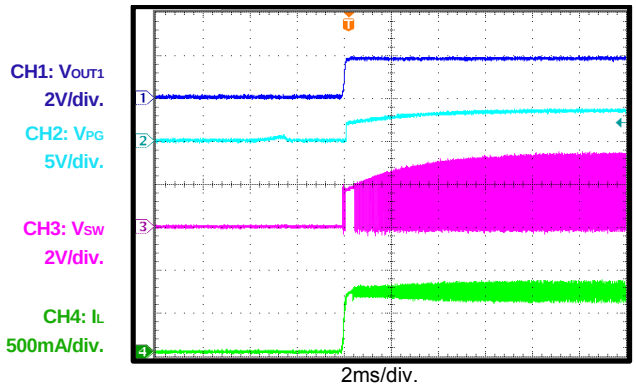
PG On

I_{OUT1}=0A



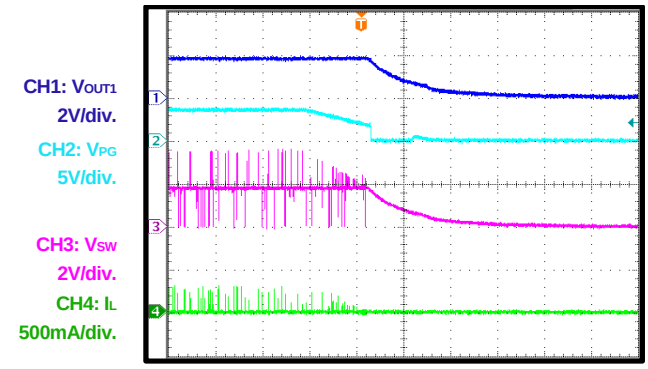
PG On

I_{OUT1}=0.7A



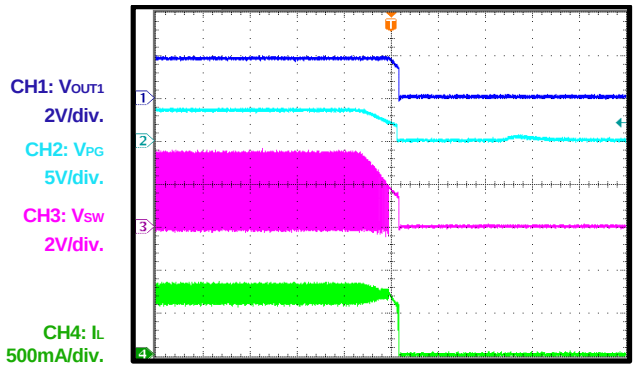
PG Off

I_{OUT1}=0A



PG Off

I_{OUT1}=0.7A



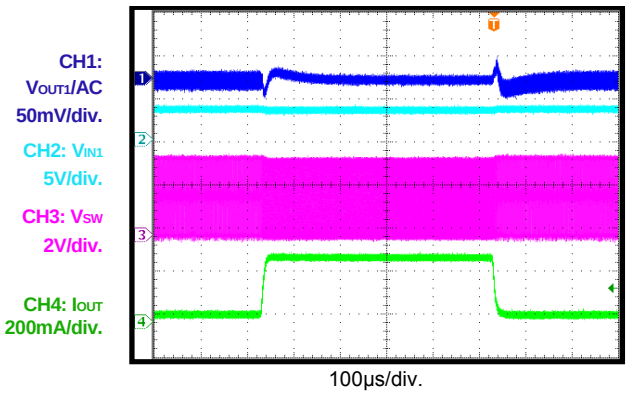
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TYPICAL PERFORMANCE CHARACTERISTICS*(continued)*

VIN1 = 3.6V, V_{OUT1}= 1.8V, L_1 = 2.2µH, C_{IN1} = 10µF, C_{OUT1}= 10µF, VIN2 = 3.6V, V_{OUT2} = 1.2V, C_{IN2}= 1µF, C_{OUT2}= 1µF, T_A = +25°C, unless otherwise noted.

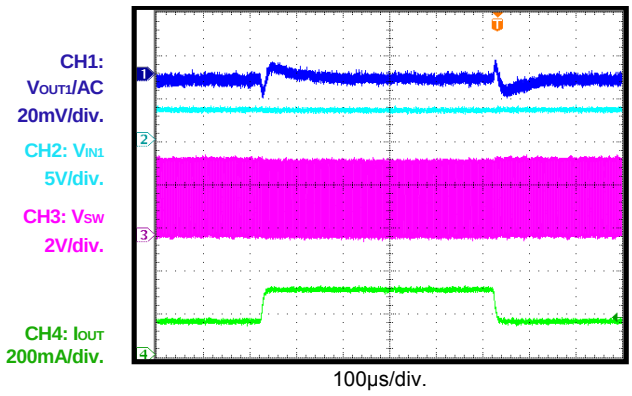
Load Transient

I_{OUT1}=30-300mA, 0.25A/µs

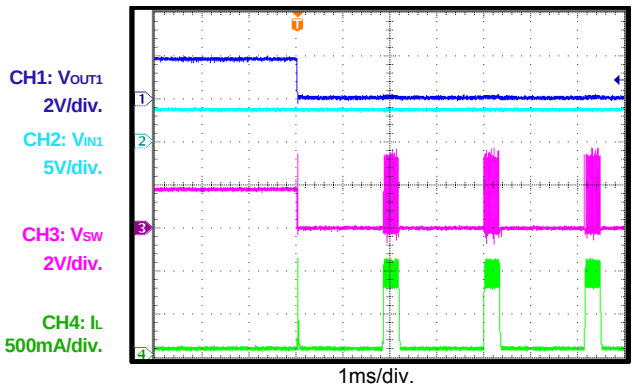


Load Transient

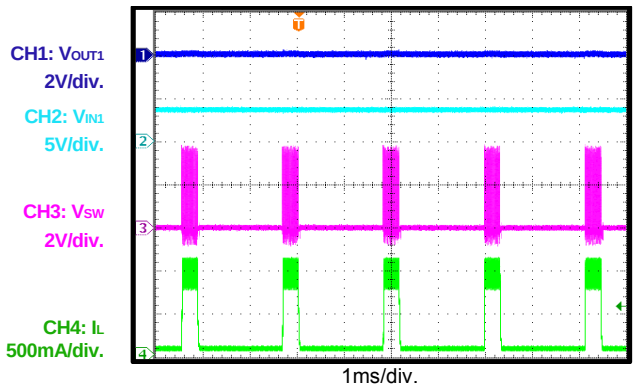
I_{OUT1}=150-300mA, 0.25A/µs



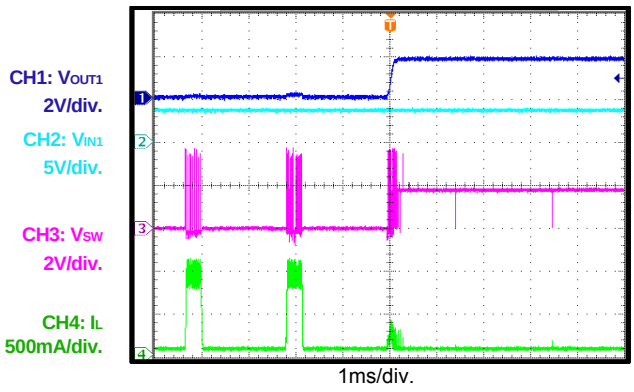
Short-Circuit Enter



Short-Circuit Steady

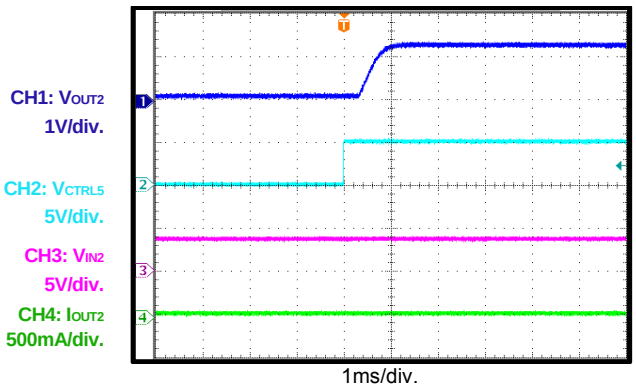


Short-Circuit Recovery



CTRL On

I_{OUT2}=0A

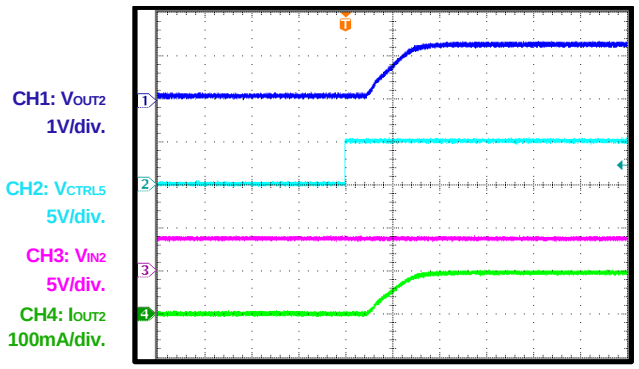


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TYPICAL PERFORMANCE CHARACTERISTICS*(continued)*

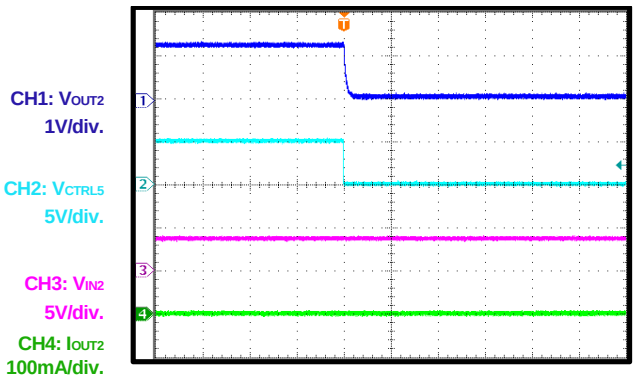
VIN1 = 3.6V, V_{OUT1}= 1.8V, L_1 = 2.2µH, C_{IN1} = 10µF, C_{OUT1}= 10µF, VIN2 = 3.6V, V_{OUT2} = 1.2V, C_{IN2}= 1µF, C_{OUT2}= 1µF, T_A = +25°C, unless otherwise noted.

CTRL On
I_{OUT2}=0.1A



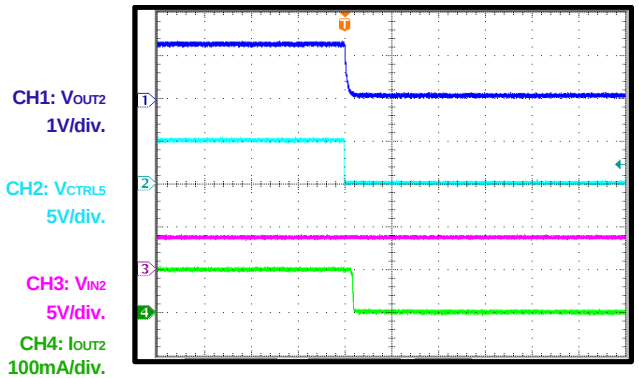
1ms/div.

CTRL Off
I_{OUT2}=0A



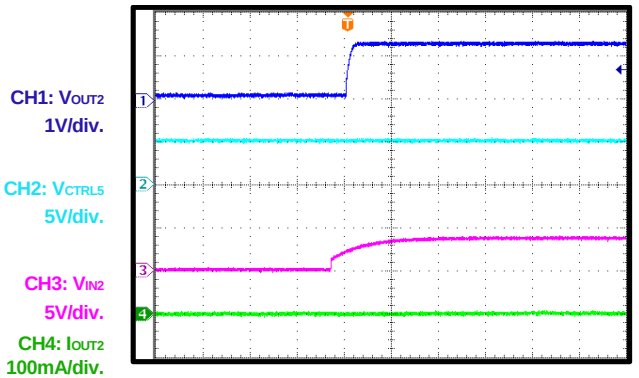
1ms/div.

CTRL Off
I_{OUT2}=0.1A



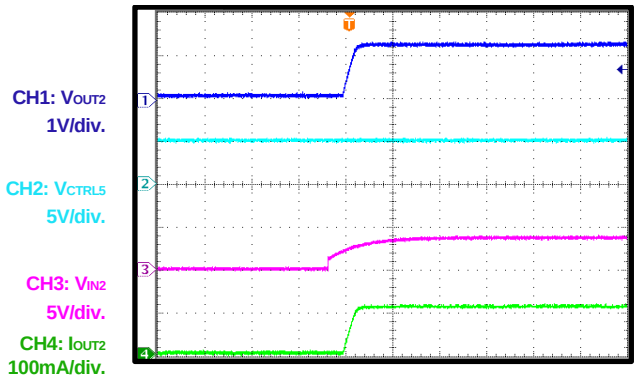
1ms/div.

V_{IN} On
I_{OUT2}=0A



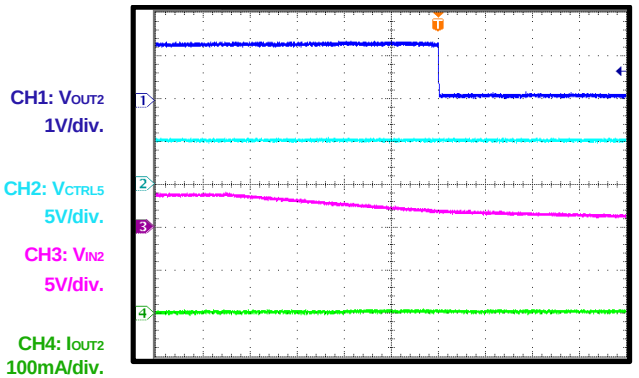
4ms/div.

V_{IN} On
I_{OUT2}=0.1A



4ms/div.

V_{IN} Off
I_{OUT2}=0A



20ms/div.

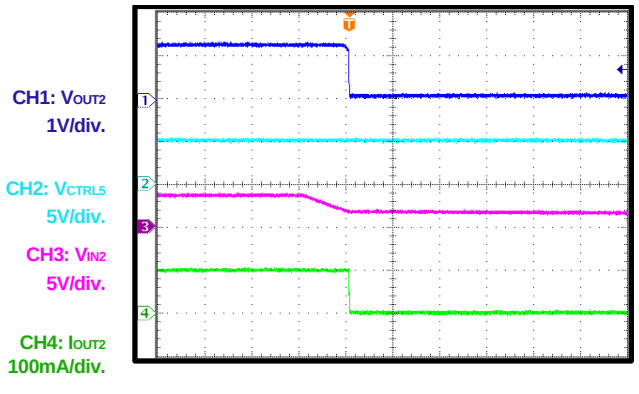
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TYPICAL PERFORMANCE CHARACTERISTICS*(continued)*

VIN1 = 3.6V, V_{OUT1}= 1.8V, L_1 = 2.2µH, C_{IN1} = 10µF, C_{OUT1}= 10µF, VIN2 = 3.6V, V_{OUT2} = 1.2V, C_{IN2}= 1µF, C_{OUT2}= 1µF, T_A = +25°C, unless otherwise noted.

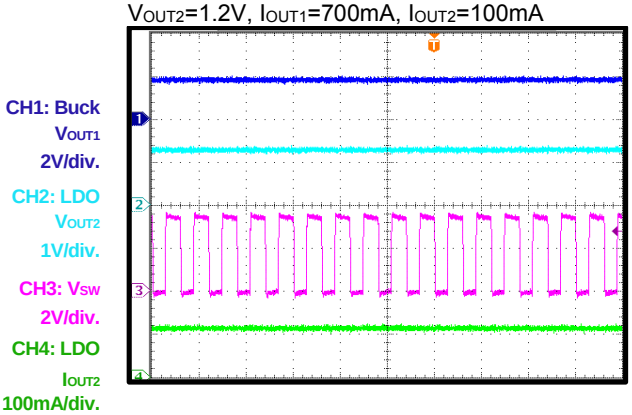
V_{IN} Off

I_{OUT2}=0.1A



Buck+LDO

V_{IN}=3.6V, V_{OUT1}=1.8V, V_{IN}2=VIN1, V_{OUT2}=1.2V, I_{OUT1}=700mA, I_{OUT2}=100mA



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PIN FUNCTIONS

Pin#	Name	Description
1	OUT1	**Output voltage sensing of the step-down switcher.** Connect the load to OUT1. An output capacitor is needed to decrease the output voltage ripple.
2	CTRL1	**Step-down switcher control signal.** Adjust the step-down switcher output voltage value dynamically. Do not float the CTRL pins during application. When used, ensure that the CTRL voltage is not lower than VIN1.If unused, tie CTRL to GND. Refer to Table1 on page 17 to set the buck output value.
3	CTRL2	
4	CTRL3	
5	CTRL4	**LDO control signal**. Adjust the LDO output voltage value dynamically. Do not float CTRL during application. When used, ensure that the CTRL voltage is not lower than VIN2. If unused, tie CTRL to GND. Refer to Table 1 on page 17 to set the LDO output value.
6	CTRL5	
7	PG1	**Power good for the step-down switcher.**PG1 is an open-drain output.
8	GND	**Ground.**
9	SW	**Switch output for the step-down switcher.** SW is the drain of the internal, high-side, P-channel MOSFET. Connect the inductor to SW to complete the converter.
10	VIN1	**Input supply voltage to the step-down switcher.** Place a small decoupling capacitor as close to VIN1 and GND as possible.
11	VIN2	**Input supply voltage to the LDO.** Place a small decoupling capacitor as close to VIN2 and GND as possible.
12	OUT2	**Output voltage sensing of LDO.**OUT2 is the output of the linear regulator. Bypass OUT2 to GND with a 1μF capacitor.

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BLOCK DIAGRAM

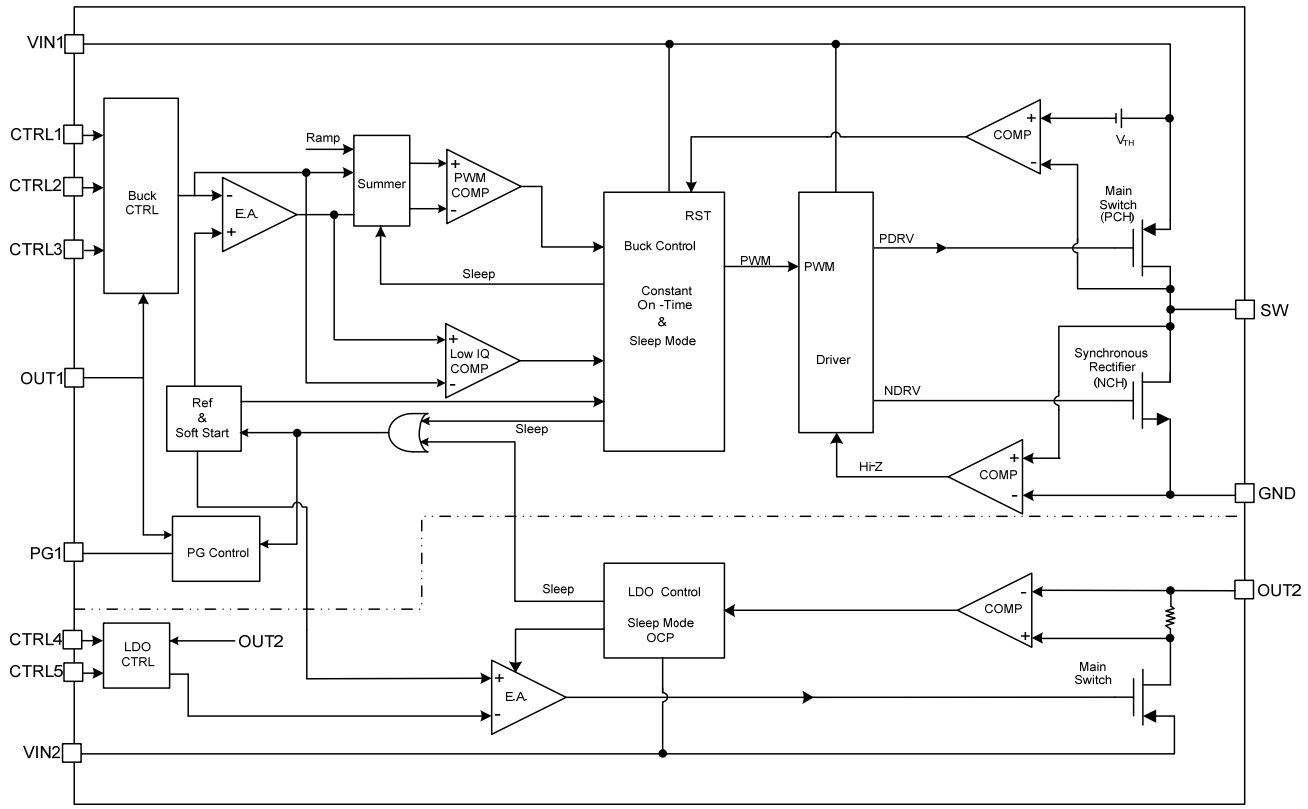


Figure 1: Functional Block Diagram

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OPERATION

The MP28301 has an ultra-low, quiescent current, step-down converter, and low-dropout regulator. The step-down converter has 500nA of quiescent current, allowing the MP28301 to achieve extremely high efficiency at an ultra-low load current. The 300nA low-I_Q LDO provides easy system configuration.

Constant-On-Time (COT) Control of the Buck

The MP28301 use a constant-on-time (COT) control scheme to regulate the output voltage. The one-shot on-timer is controlled by the input and output voltages. At different input and output voltage conditions, the switching frequency is fairly stable, which helps with the system design. The switching frequency is around 1.5MHz, typically. With COT control, the output ripple is small, and the load transient response is fast. COT control minimizes the number of input and output capacitors. The MP28301 enters pulse-skip mode automatically when the low-side switch current reaches the 0A threshold. Pulse-skip mode helps improve light-load efficiency. The COT control scheme provides a seamless transition from pulse-width modulation (PWM) mode to pulse-frequency modulation (PFM) mode and vice versa.

Light-Load Operation

When the load current decreases and the low-side switch current reaches the 0A threshold, both the high-side and low-side switches are turned off. Output energy is provided by the output capacitors during this period until the output voltage drops, reaches the regulation voltage, and triggers another on pulse.

The switching frequency in PFM mode depends on the load current. The switching frequency is lower when the load current is lighter. With PFM control at light-load mode plus the ultra-low quiescent operation current, the MP28301 can achieve the highest efficiency at extremely low load. This helps extend the charge cycle of any battery-powered system.

When the buck works in light-load operation, it needs at least 5μs to exit light load. When a large, quick, and sharp load increase occurs in light-load mode, the output voltage drops during the exit transition. The LDO exits light-load mode after a load of >20mA.

Sleep Mode

When the load gets lighter, the MP28301 enters DCM(Discontinuous Current Mode) and the switching frequency becomes lower. If the switch pulse interval is longer than 6us typically, MP28301 enters Sleep mode and most of the internal blocks are turned off to achieve 500nA quiescent current and high light load efficiency.

In the extreme application case, like when the input voltage is closed to output voltage(what we called large duty cycle application), MP28301 is not able to enter sleep mode. The inductor ripple is very small due to very small input and output voltage difference, thus MP28301 needs to generate more frequent pulse to keep output voltage regulated. The pulse interval could be smaller than 6us and MP28301 is not entering sleep mode in this application. The quiescent current for this application is expected to be higher than 500nA.

Control (CTRL1/2/3)

The control pins (CTRL1/2/3) are used to control start-up and set the output voltages of the step-down regulator. When CTRL1/2/3 are low, the step-down switcher of the MP28301 is disabled. Once either one of CTRL1/2/3 are pulled high, the switcher is enabled. The output voltage is set depending on which CTRL pin is pulled high. This applies for CTRL4/5 for the LDO regulator as well. The output voltage is programmable according toTable1.

Table 1: CTRL vs. Output Voltages

Step-Down Switcher			
CTRL3	**CTRL2**	**CTRL1**	**OUT1**
0	0	0	Disabled
0	0	1	0.8V
0	1	0	1.0V
0	1	1	1.2V
1	0	0	1.5V
1	0	1	1.8V
1	1	0	2.5V
1	1	1	3.3V
LDO			
CTRL5		**CTRL4**	**OUT2**
0		0	Disabled
0		1	1.2V
1		0	2.5V
1		1	3.0V

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The output voltage can be programmable during operation and supports dynamic output voltage scaling. CTRL cannot be floating. Any used CTRL voltage cannot be less than V_{IN}. Any unused CTRL pin must be tied to GND.

Soft Start (SS)

When the converter is enabled, the internal reference is powered up. After a certain amount of delay time, the device enters soft start (SS). The step-down switcher output voltage ramps up to the regulation voltage to around 110μs. The LDO's SS time is about 2ms when $V_{OUT2}$is 3V and C_{OUT2} is 1μF.

Power Good (PG) Indicators of the Buck

The MP28301 has an open-drain output power good (PG) indicator with a maximum $R_{DS(ON)}$ of less than 400Ω. PG requires an external pull-up resistor (100~500kΩ) for power good indication. This resistor can be pulled up to V_{IN} or tied to CTRL if the CTRL voltages do not need to be adjusted dynamically.

The PG comparator is active when the device is enabled. The comparator is driven to a high impedance once the output voltage trips the PG threshold(typically 90% of the regulation voltage)and is pulled low once the output voltage falls below the PG hysteresis threshold (typically 80% of the regulation voltage). The output is also pulled low if the input voltage is lost or the part is disabled.

Output Discharge Function

Both the step-down regulator and the LDO implement the output discharge function once they are disabled. This feature prevents residual charge voltages on the capacitors, which may interfere with a proper power-up of the system. When the input voltage is high and the related converters are disabled, the output discharge is active.

100% Duty Cycle Mode

When the input voltage reduces and is lower than the regulation output voltage, the output voltage drops, and the on time increases. Further reducing the input voltage drives the MP28301 into 100% duty cycle mode. The high-side switch is always on, and the output voltage is determined by the load current times the $R_{DS(ON)}$ composed by the high-side switch and inductor.

LDO Operation

The low-dropout regulator is enabled when either one or both of CTRL4 or CTRL5 is high and the input voltage (VIN2) is higher than the UVLO threshold. CTRL4 and CTRL5 can be programmed to one of three preset output voltages.

Current Limit

The MP28301 has an internal current limit for the step-down converter and LDO converter.

The high-side switch current is monitored cycle-by-cycle and is compared with the current-limit threshold. Once the current-limit comparator is triggered, the high-side switch is turned off, and the low-side switch is turned on, reducing the inductor current. Until the low-side switch current is lower than the low-side current limit, the high-side switch is not allowed to turn on again.

If the current of the LDO reaches the current limit, the LDO current clamps the current at the current limit level, and the output regulation is lost.

Short Circuit and Recovery

If the output voltage of the buck converter is shorted to GND, the under-voltage is detected and the MP28301 enters hiccup mode for the buck converter. The short-circuit condition can also be triggered when the output voltage is lower than 50% of the regulation output voltage and when the current limit is reached simultaneously. The buck disables the output power stage, discharges the output voltage, and then attempts to recover after a hiccup. If the short-circuit condition still remains, the MP28301 repeats this operation until the short circuit is removed and the output rises back to the regulation levels.

When a short circuit occurs in the LDO, the mechanism that follows is similar to the current-limit condition. The current is clamped at the current-limit level.

Thermal Shutdown Circuit and Recovery

When the thermal shutdown signal is triggered, the MP28301 turns off and restarts when the temperature falls below the thermal hysteresis.

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APPLICATION INFORMATION

Selecting the Inductor

Most applications work best with a 1-2.2µH inductor. Select an inductor with a DC resistance less than 200mΩ to optimize efficiency.

High-frequency, switch-mode power supplies with a magnetic device have strong electronic magnetic inference for the system. Any unshielded power inductor should be avoided since it has poor magnetic shielding. Metal alloy or multiplayer chip power shield inductors are recommended for the application since they can decrease influence effectively. Table 2 lists some recommended inductors.

Table 2: Recommended Inductors

Inductance	Manufacturer P/N	Package	Manufacturer
2.2µH	DFE201612P-2R2M	2016	Tokyo
2.2µH	74479775222A	2012	Wurth

For most designs, the inductance value can be calculated with Equation (1):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (1)$$

Where ΔI_L is the inductor ripple current. Choose the inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (2):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (2)$$

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input and the switching noise from the device. Select an input capacitor with a switching frequency impedance less than the input source impedance to prevent high-frequency switching current from passing to the input source. Use low ESR ceramic capacitors with X5R or X7R dielectrics with small temperature coefficients. For most applications, a 10µF capacitor is sufficient.

The input capacitor requires an adequate ripple current rating since it absorbs the input switching current.

Estimate the RMS current in the input capacitor with Equation (3):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

The worst-case scenario occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (4):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, 0.1µF, ceramic capacitor as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Selecting the Output Capacitor

The output capacitor limits the output voltage ripple and ensures a stable regulation loop. Select an output capacitor with low impedance at the switching frequency. For most applications, a 10µF capacitor is sufficient. Estimate the output voltage ripple with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (6)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

The characteristics of the output capacitor also affect the stability of the regulation system.

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PCB Layout Guidelines

Efficient PCB layout of the switching power supply and especially the high-switching frequency converter is critical for stable operation. If the layout is not done carefully, the regulator could show poor line or load regulation and stability issues. For best results, refer to Figure 2 and follow the guidelines below.

1. Place the input capacitor as close to the IC pins as possible for the high speed step-down regulator to provide clean control voltage for the chip.
2. Place the CIN1 close to VIN1 and GND to absorb noise.

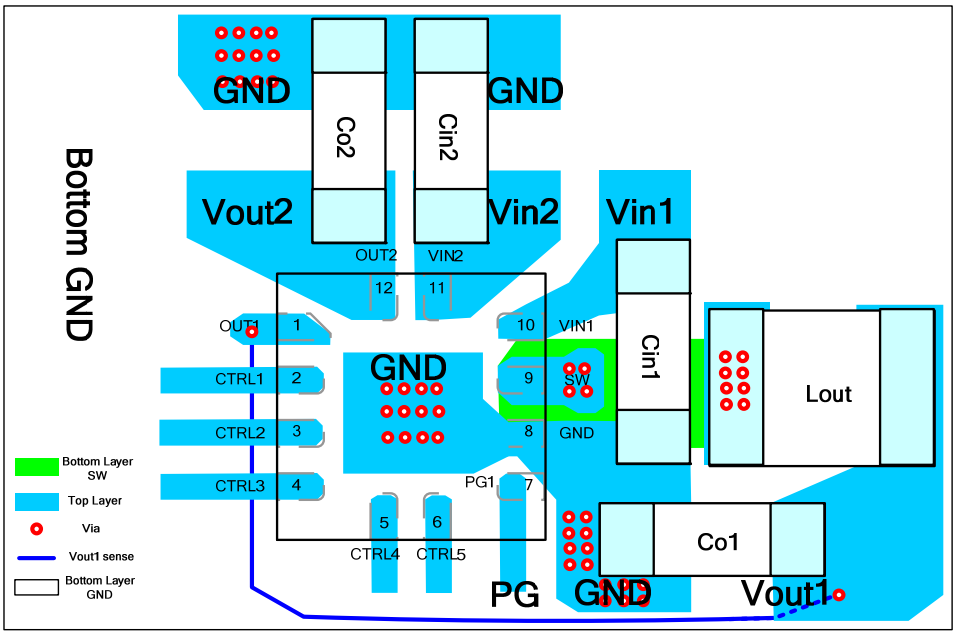


Figure 2: Recommended Layout

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TYPICAL APPLICATION CIRCUITS

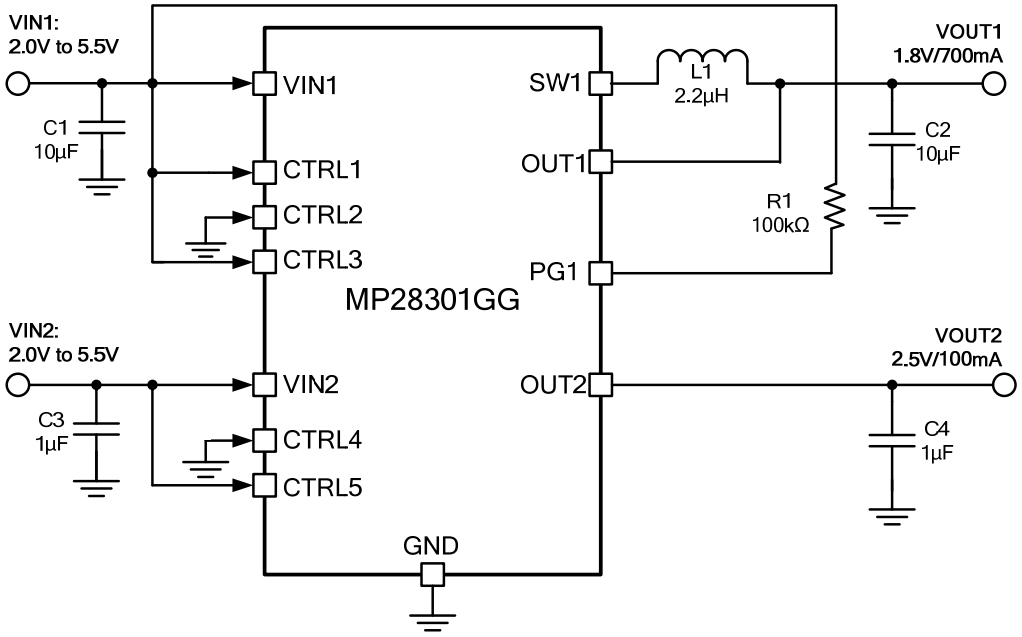


Figure 3: Typical Application Circuit forMP28301GG

NOTE: VIN1 and VIN2 supply power dependently. VIN1 must be more than the V_{IN} UVLO.

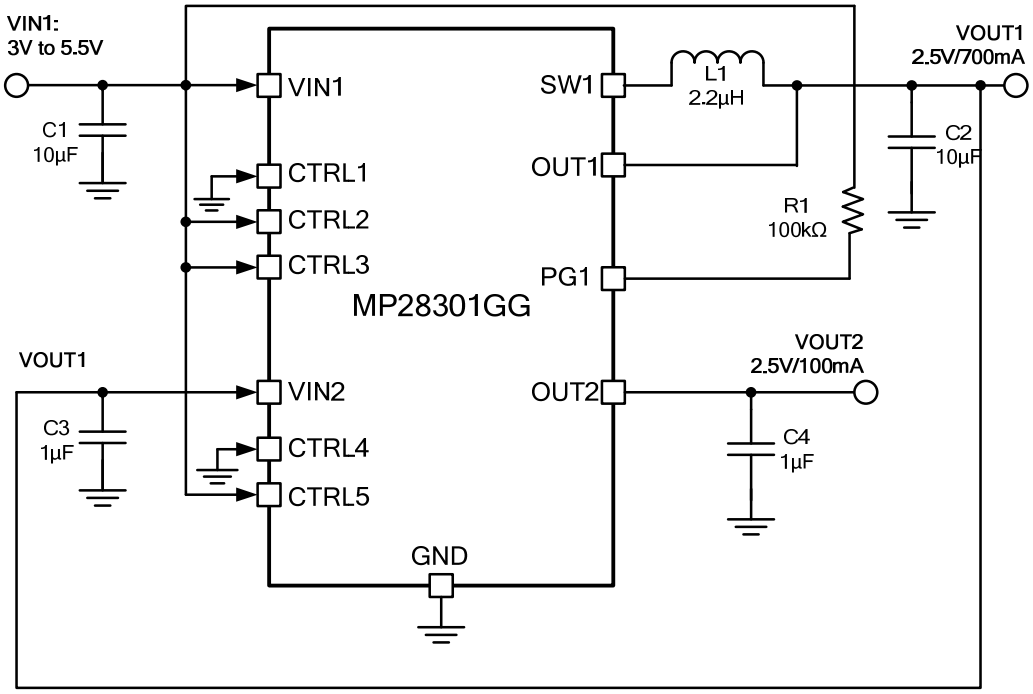
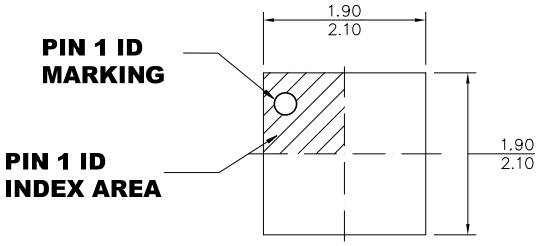


Figure 4: Buck and LDO in Sequence

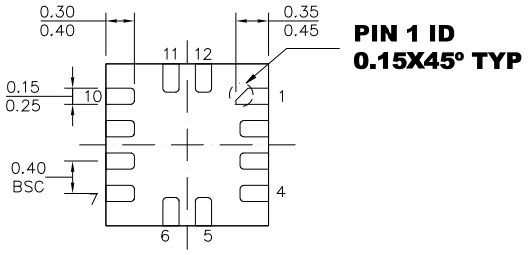
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PACKAGE INFORMATION

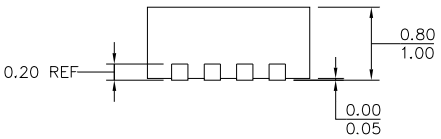
QFN-12 (2mmx2mm)



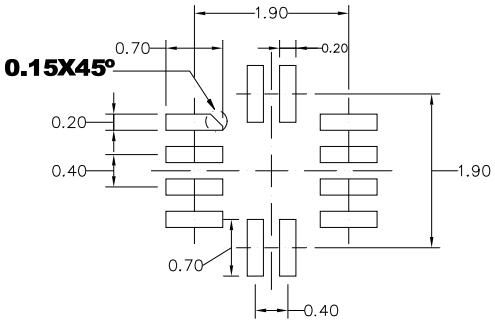
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

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