STL15DN4F5

Automotive-grade dual N-channel 40 V, 8 mΩ typ., 15 A STripFET™ F5 Power MOSFET in a PowerFLAT™ 5x6 DI

Datasheet - production data

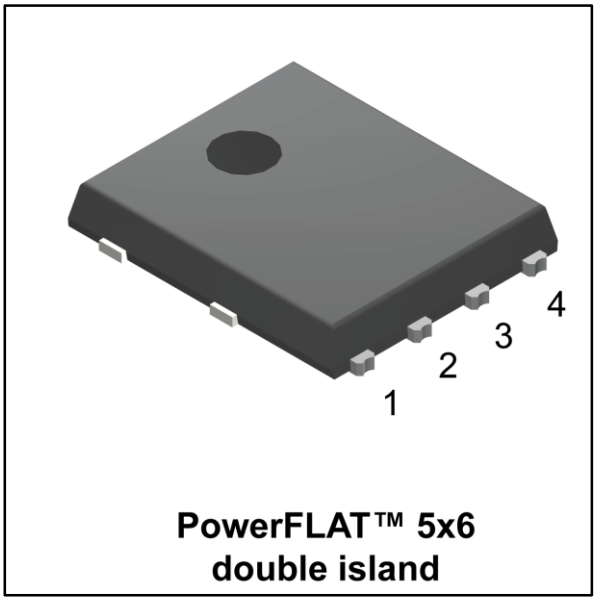
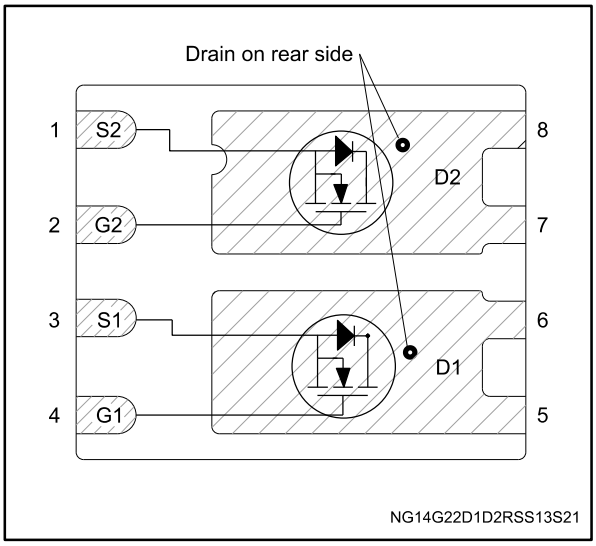


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL15DN4F5	40 V	9 mΩ	15 A

- Designed for automotive applications and AEC-Q101 qualified
- Extremely low $R_{DS(on)}$
- Very low gate charge
- Low gate drive power loss
- Wettable flank package

Applications

- Switching applications

Description

This device is a dual N-channel Power MOSFET developed using STMicroelectronics' STripFET™ F5 technology. The device has been optimized to achieve very low on-state resistance, contributing to a FoM that is among the best in its class.

Table 1: Device summary

Order code	Marking	Package	Packing
STL15DN4F5	15DN4F5	PowerFLAT™ 5x6 double island	Tape and reel

This is information on a product in full production.

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	±20	V
I_D(1)	Drain current (continuous) at T_C = 25 °C	60	A
I_D(2)	Drain current (continuous) at T_{pcb} = 25 °C	15	A
I_D(2)	Drain current (continuous) at T_{pcb} = 100°C	10	A
I_{DM}(2)(3)	Drain current (pulsed)	60	A
P_{TOT}(1)	Total dissipation at T_C = 25 °C	60	W
P_{TOT}(2)	Total dissipation at T_{pcb} = 25°C	4.3	W
T_j	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		

Notes:

(1)The value is rated according $R_{thj\text{-}c}$.

(2)The value is rated according $R_{thj\text{-}pcb}$.

(3)Pulse width limited by safe operating area.

Table 3: Thermal resitance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.5	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	35	°C/W

Notes:

(1)When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 s.

Table 4: Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not-repetitive avalanche current, (pulse width limited by Tj max.)	7.5	A
E_{AS}(1)	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AV}, V_{DD} = 24 V)	150	mJ

Notes:

(1)Tested at wafer level only.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On/Off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0 V	40			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 40 V			1	µA
		V_{GS} = 0 V, V_{DS} = 40 V, T_C= 125 °C (1)			10	µA
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS} , I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 7.5 A		8	9	mΩ

Notes:

(1)Defined by design, not subject to production test

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	1550	-	pF
C_{oss}	Output capacitance		-	230	-	
C_{rss}	Reverse transfer capacitance		-	25	-	
Q_g	Total gate charge	V_{DD} = 20 V, I_D = 15 A, V_{GS} = 10 V (see *Figure 14: "Test circuit for gate charge behavior"*)	-	25	-	nC
Q_{gs}	Gate-source charge		-	6	-	
Q_{gd}	Gate-drain charge		-	5.5	-	

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 20 V, I_D = 7.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Test circuit for resistive load switching times"*)	-	18	-	ns
t_r	Rise time		-	45	-	
$t_{d(off)}$	Turn-off delay time		-	32	-	
t_f	Fall time		-	5	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Forward on voltage		-		15	A
I_{SDM}(1)	Source-drain current (pulsed)		-		60	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0, I_{SD} = 15 A	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 15 A, di/dt = 100 A/µs	-	30		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 32 V, T_j = 150 °C (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	35		nC
I_{RRM}	Reverse recovery current		-	2.2		A

Notes:

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5 %

2.2 Electrical characteristics (curves)

Figure 2: Safe operating area

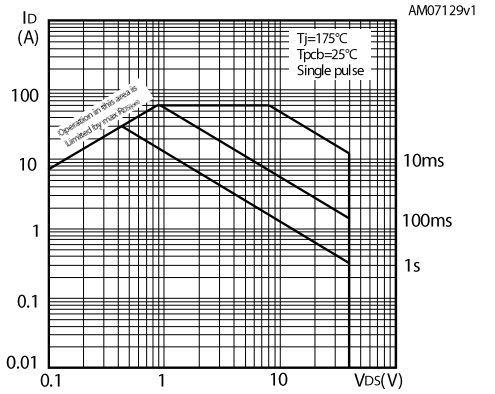


Figure 3: Thermal impedance

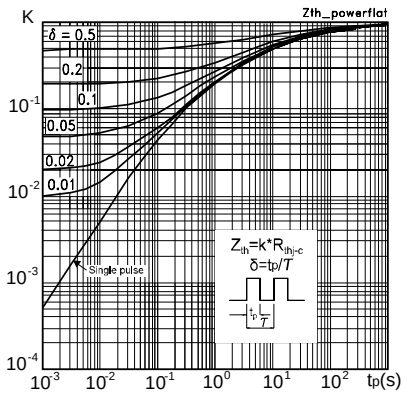


Figure 4: Output characteristics

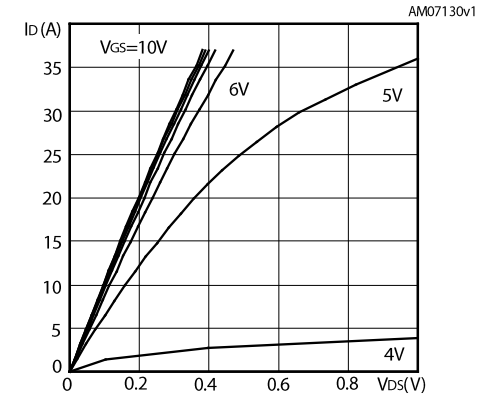


Figure 5: Transfer characteristics

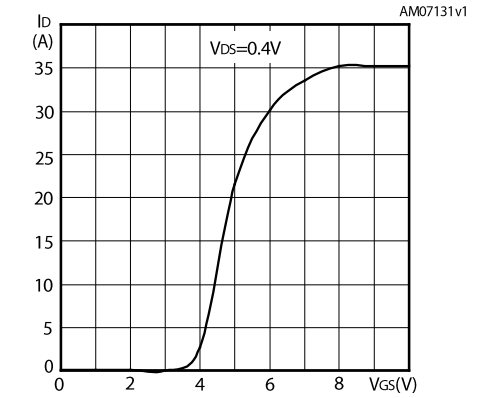


Figure 6: Gate charge vs gate-source voltage

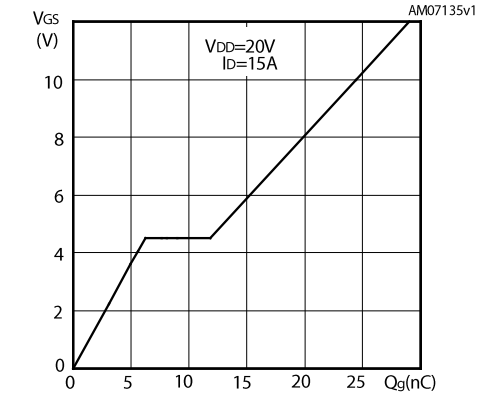


Figure 7: Static drain-source on-resistance

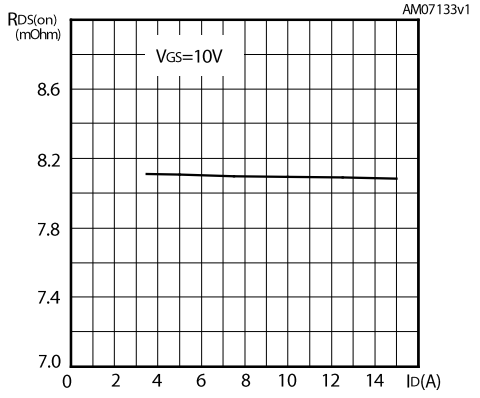


Figure 8: Capacitance variations

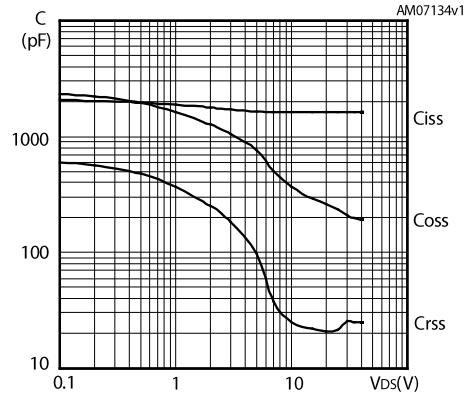


Figure 9: Normalized gate threshold voltage vs temperature

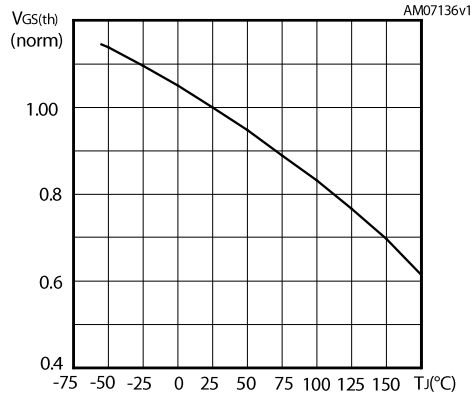


Figure 10: Normalized on-resistance vs temperature

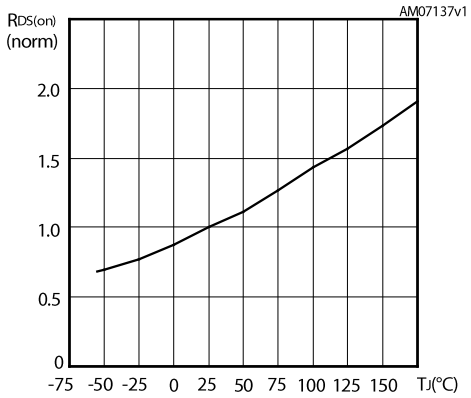


Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

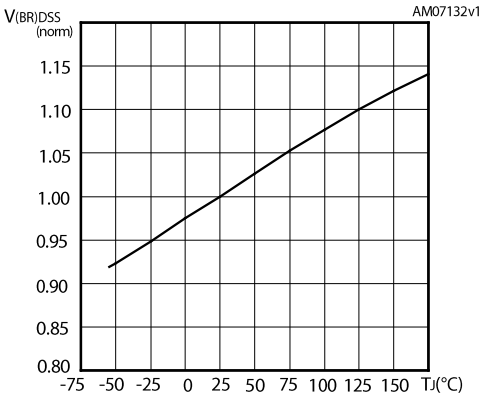
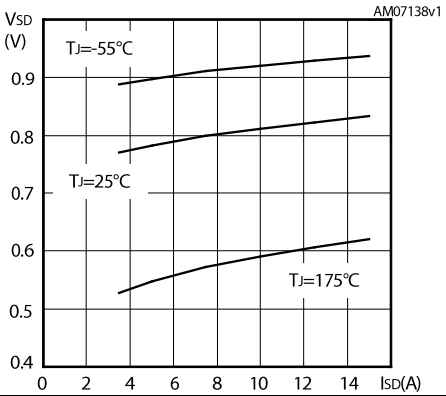


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times

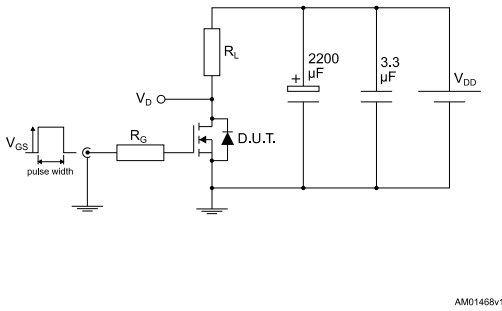


Figure 14: Test circuit for gate charge behavior

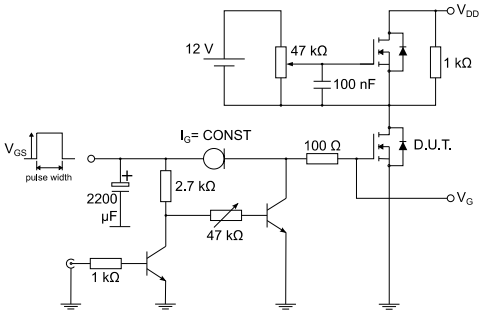


Figure 15: Test circuit for inductive load switching and diode recovery times

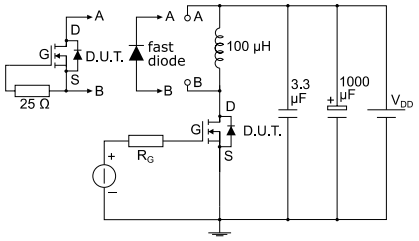


Figure 16: Unclamped inductive load test circuit

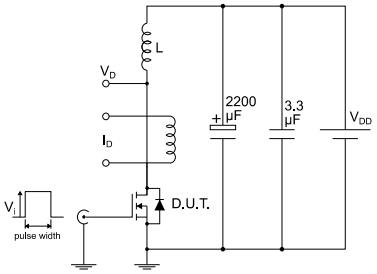


Figure 17: Unclamped inductive waveform

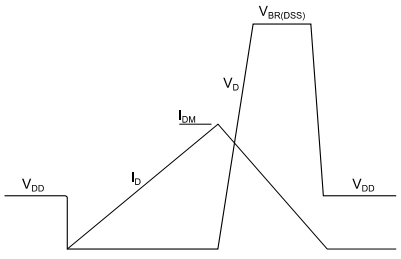
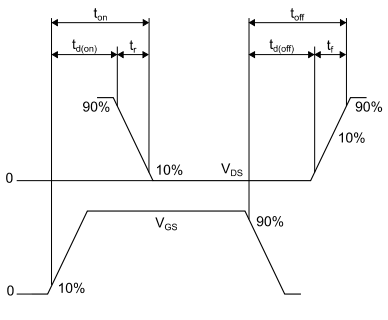


Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT 5x6 double island WF type C package information

Figure 19: PowerFLAT™ 5x6 double island WF type C package outline

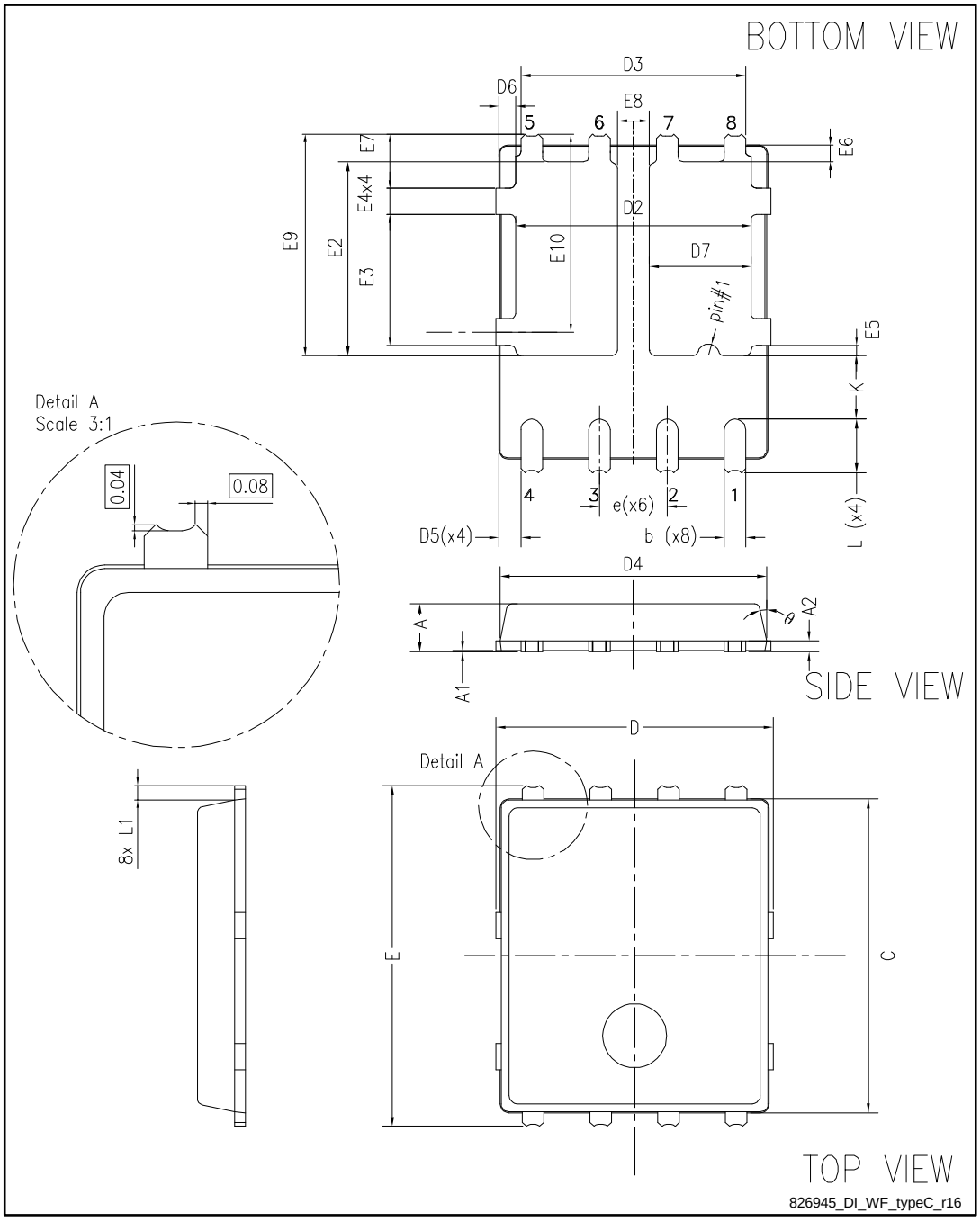
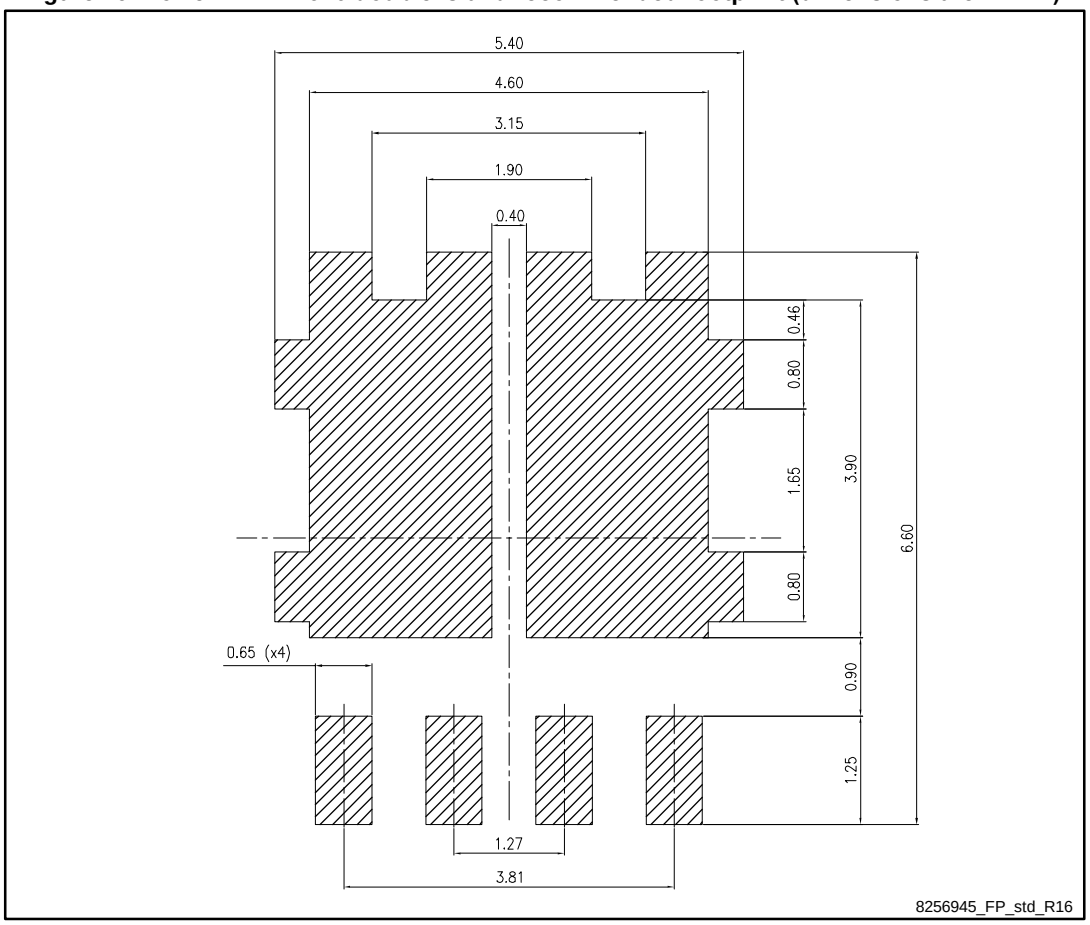


Table 9: PowerFLAT™ 5x6 double island WF type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
D7	1.68		1.98
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E8	0.55		0.75
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
L	0.90	1.00	1.10
L1	0.175	0.275	0.375
K	1.05		1.35
Θ	0°		12°

Figure 20: PowerFLAT™ 5x6 double island recommended footprint (dimensions are in mm)



4.2 Packing information

Figure 21: PowerFLAT™ 5x6 WF tape (dimensions are in mm)

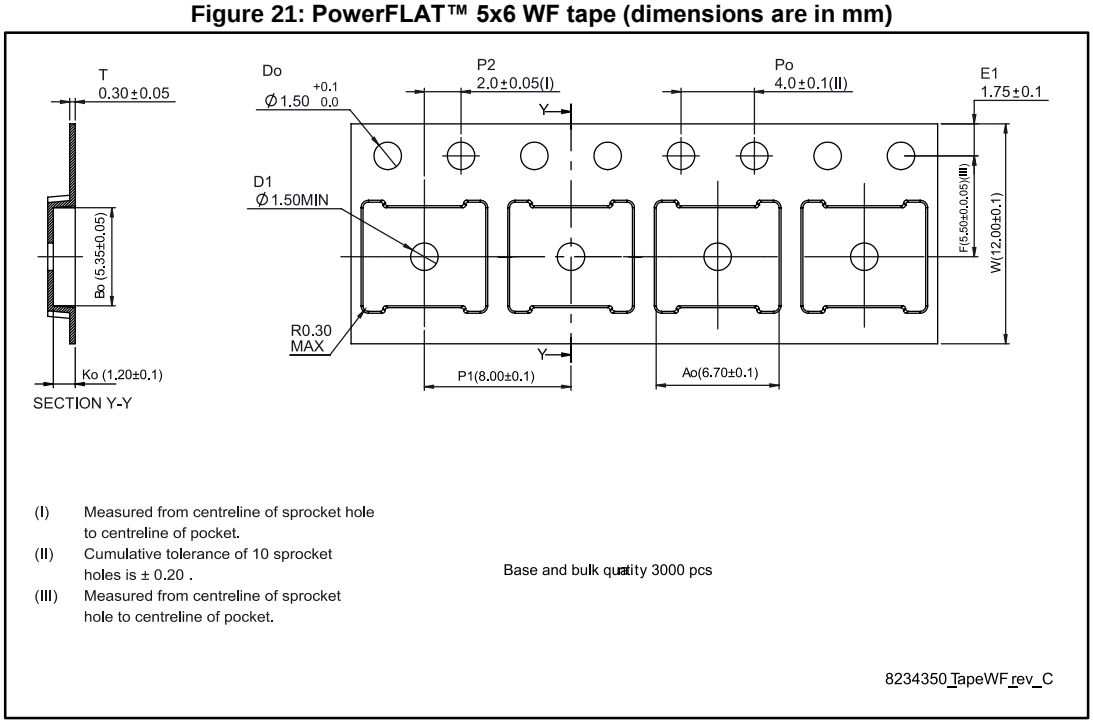


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

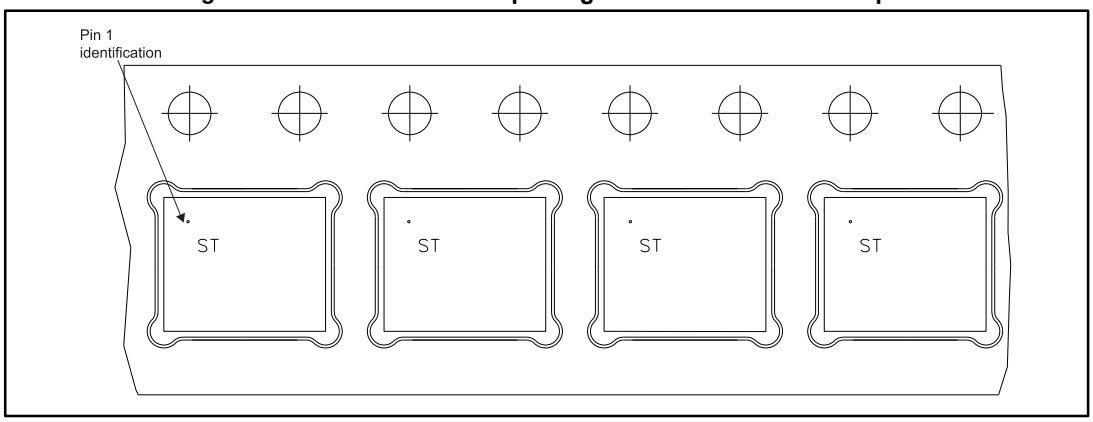
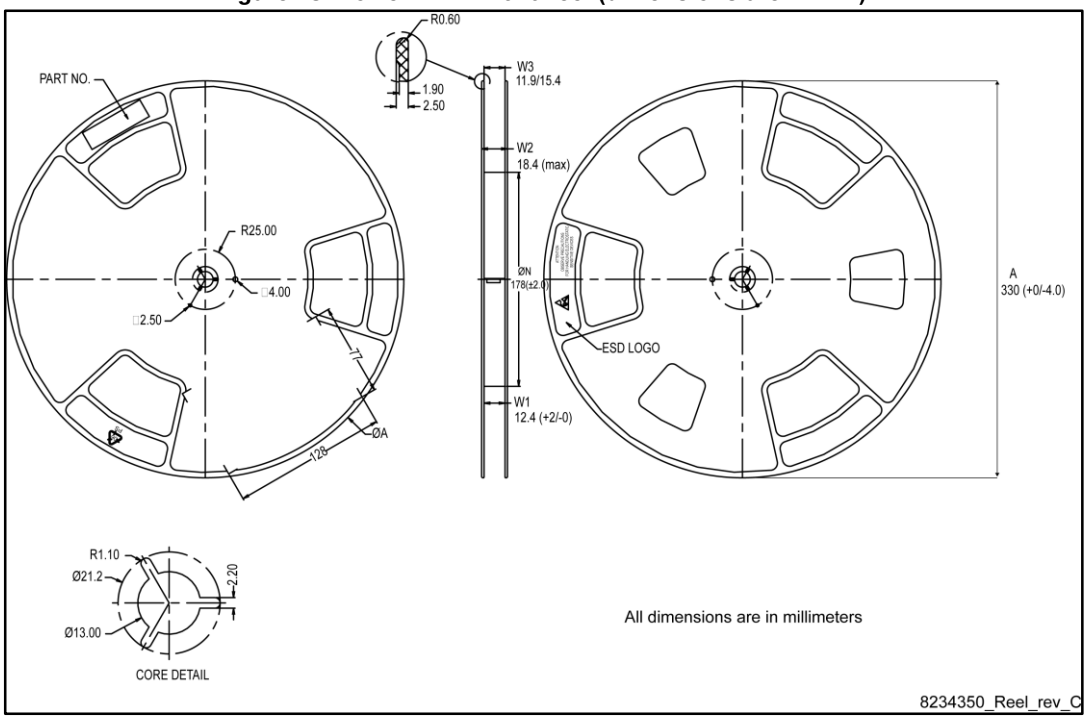


Figure 23: PowerFLAT™ 5x6 reel (dimensions are in mm)



5 Revision history

Table 10: Document revision history

Date	Revision	Changes
02-Sep-2010	1	First release.
01-Jul-2014	2	Updated: *Section 4: Package information*. Minor text changes
13-Feb-2015	3	Updated *Section 4: Package information.* Added *Section 5: Packaging information*
06-Jul-2016	4	Updated: *Section 6.1: "PowerFLAT 5x6 double island WF type C package information"*. Minor text changes.

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