

TXB-EVM Evaluation Module User Guide

This user's guide describes the characteristics, operation, and use of the TXB-EVM Evaluation Module (EVM). A complete printed-circuit board layout, schematic diagrams, and bill of materials are included in this document.

Contents

1	Introduction	2
2	Board Layout	5
3	Schematic and Bill of Materials	6

List of Figures

1	TXB-EVM	3
2	TXB-EVM Layout	5
3	1-Channel TXB0101	6
4	2-Channel TXB0102	6
5	4-Channel TXB0104	7
6	8-Channel TXB0108	7

List of Tables

1	Auto-Bidirectional Families	2
2	TXB-EVM Packages and Devices supported	3
3	TXB Device Voltage Supply Ranges	4
4	TXB-EVM Bill of Materials	8

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

The TXS and TXB auto bidirectional voltage translators are designed for interfacing between 1.2-V to 5.5-V drivers. TXS translation devices specialize in open-drain applications such as I²C, One-Wire, and MMC-card interfacing, while TXB translation devices are suited for high-impedance push-pull driver interfacing. Watch [choosing the right auto-bidirectional translator](#) for a brief comparison of TXB, TXS and LSF families.

This evaluation module (EVM) supports the customizable evaluation of the one, two, four, and eight bit devices of the TXB family. Refer to [TXS-EVM](#) for evaluating the TXS device family.

1.1 Features

1.1.1 TXB Family

The TXB family uses two separate configurable power supply rails V_{CCA} and V_{CCB} with A ports tracking the V_{CCA} supply and B ports tracking the V_{CCB} supply. These devices are fully specified for partial-power-down applications using I_{OFF} . The I_{OFF} circuitry ([SCEA026](#)) disables the outputs, preventing damaging current backflow through the device when it is powered down. The V_{CC} isolation feature ensures that if either V_{CC} supply is powered down (0V), then the I/O ports are in a high-impedance state. Refer to the application note [A guide to voltage translation with the TXB family](#) for more on TXB family characteristics.

Weak driving capability is characteristic of auto-bidirectional translators, allowing the device output to be overridden by the external driver during a direction change, without the need for a separate DIR control pin. TXB devices are designed with buffered I/O architecture suitable for light load push-pull applications. During an edge transition, the One-shot (O.S) circuitry becomes active and lowers the effective output impedance. Once the transition is complete, the weak 4-k Ω buffer drives the output. During a DC state, only the series resistor drives the output, thus allowing the port to be overridden externally. Consequently, external pull-up or pull-down resistor values must be larger than 50-k Ω to avoid affecting V_{OH} or V_{OL} . Refer to the application note [Effects of pull-up and pull-down resistors on TXB devices](#) for further information.

[Table 1](#) shows the comparison between the TXB, TXS and LSF Auto-Bidirectional families of TI.

Table 1. Auto-Bidirectional Families

Metrics	TXB	TXS	LSF
Translation mechanism	Weak buffered translation	Passive translation with NMOS and internal pull-up resistors	Passive translation with NMOS and external pull-up resistors
Drive strength	Very low drive of 20ua due to 4K limiting buffer	No DC drive	No DC drive
Applications/ Interface	Push-pull applications	Open-drain applications	Push-pull and open-drain applications
Speed	Up to 140Mbps	Up to 24Mbps	High speed up to 200Mbps
Translation flexibility	Buffered and fixed translation on A and B ports	Integrated pull-up resistors-reduces BOM cost of the system; Fixed translation on A and B ports	Flexible translation due to external pull-up resistors Frequency vs load balance trade-off
I/O ports	A ports referenced to V_{cca} and B ports referenced to V_{ccb}	A ports referenced to V_{cca} and B ports referenced to V_{ccb}	A ports not referenced to V_{cca} , B ports not referenced to V_{ccb} ; allows multi-voltage translation
Edge- acceleration	Integrated one-shot edge acceleration circuitry	Integrated one-shot edge acceleration circuitry	No integrated one-shot acceleration circuitry
Vih/Vil requirements	Datasheet spec has Vih/Vil specifications	Has Vih /Vil spec but no R_{ON} for the FET	No Vih / Vil conditions, has R_{ON} specifications
Additional care-about	$V_{CCA} \leq V_{CCB}$	$V_{CCA} \leq V_{CCB}$	$V_{CCB} > V_{CCA} + 0.8 V$

TXB-EVM is shown in Figure 1. Table 2 shows the packages supported by the TXB-EVM.

Table 2. TXB-EVM Packages and Devices supported

Device	Package	Pins	Device Populated
TXB0101	DCK (SC-70)	6	Yes
TXB0102	DCU (VSSOP)	8	Yes
TXB0104 (TXB0104-Q1*) ⁽¹⁾	PW (TSSOP)	14	No
	RUT (UQFN)	12	Yes
TXB0108	PW (TSSOP)	20	No
	RGY (VQFN)	20	Yes

⁽¹⁾ -Q1 devices are not populated but can be supported.

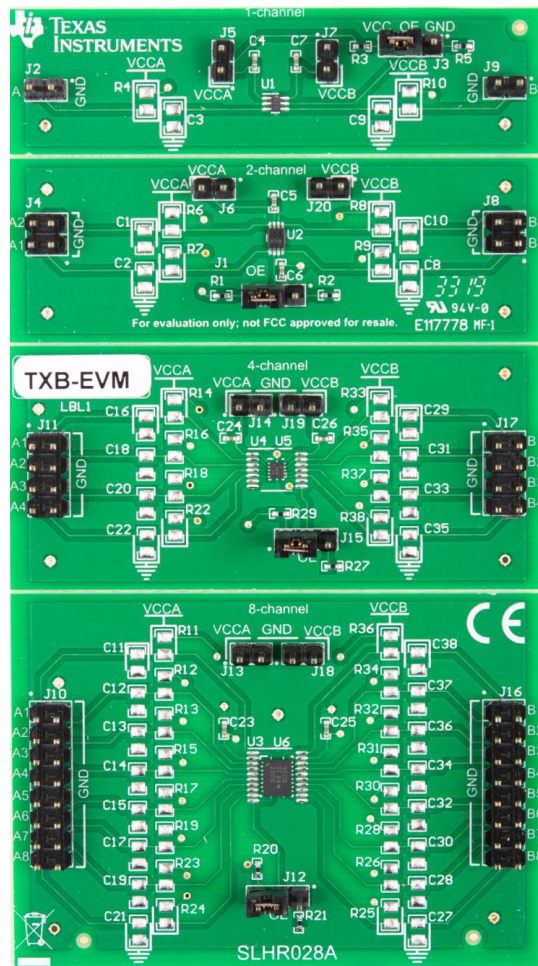


Figure 1. TXB-EVM

1.2 Hardware Description

1.2.1 Headers

All headers on this EVM are 100-mil. Each EVM board has header arrays for connection to the A and B side data pins, with ground oriented towards the device and the data headers closer to the board edges. Data pins are marked A1..A8 and B1..B8 from top to bottom. All ground pins on the board are at the same ground potential.

1.2.2 Voltage Supply

Supply headers are located at the top of each EVM for V_{CCA} and V_{CCB} . [Table 3](#) denotes the operational voltage ranges for TXB devices.

Table 3. TXB Device Voltage Supply Ranges

	V_{CCA} range	V_{CCB} range
TXB0101, TXB0102, TXB0104, TXB0104-Q1, TXB0108	1.2 – 3.6 V	1.65 – 5.5 V

1.2.3 Bypass Capacitors

0.1 μ F Surface Mount (SM) 0402 capacitors are populated near V_{CCA} and V_{CCB} device pins on each board (C4, C5, C6, C7, C23, C24, C25, C26). These are in place to smooth transient voltage supply spikes during start up and normal device operation.

1.2.4 OE Select

A 3x1 100 mil header provides access to the Output Enable (OE) pin on the device. The 100 mil jumper is available for selecting a known state for the OE pin. The outer header pins access V_{CCA} or GND through a 10 k Ω resistor. OE on TXB devices may be referenced to either V_{CCA} or GND, although using a pull up resistor on OE during device power-on is recommended to have the I/O ports at high-impedance before the V_{CCA} becomes stable. Output enable pin is the input for the device and should never be left floating. The CMOS inputs must be held at a known state, either V_{CC} or ground, to ensure proper device operation. Refer to *Implications of Slow or Floating CMOS Inputs* ([SCBA004](#)).

1.2.5 RC Loading

Each data I/O trace connects to an 0805 surface mount (SM) pad with access to V_{CC} for customizable pull-up resistors and a 0805 SM pad with access to GND for a customizable load. Large pads were chosen for ease of access and the option to compose a load out of multiple, smaller, SM components if desired (for load tests, propagation delay, rise/fall time adjustments, etc.). [Figure 1](#) shows the SM pad locations. Pull down pads are marked with a ground symbol, pull up pads are marked with a power port symbol on the board.

2 Board Layout

Figure 2 illustrates the TXB-EVM layout.

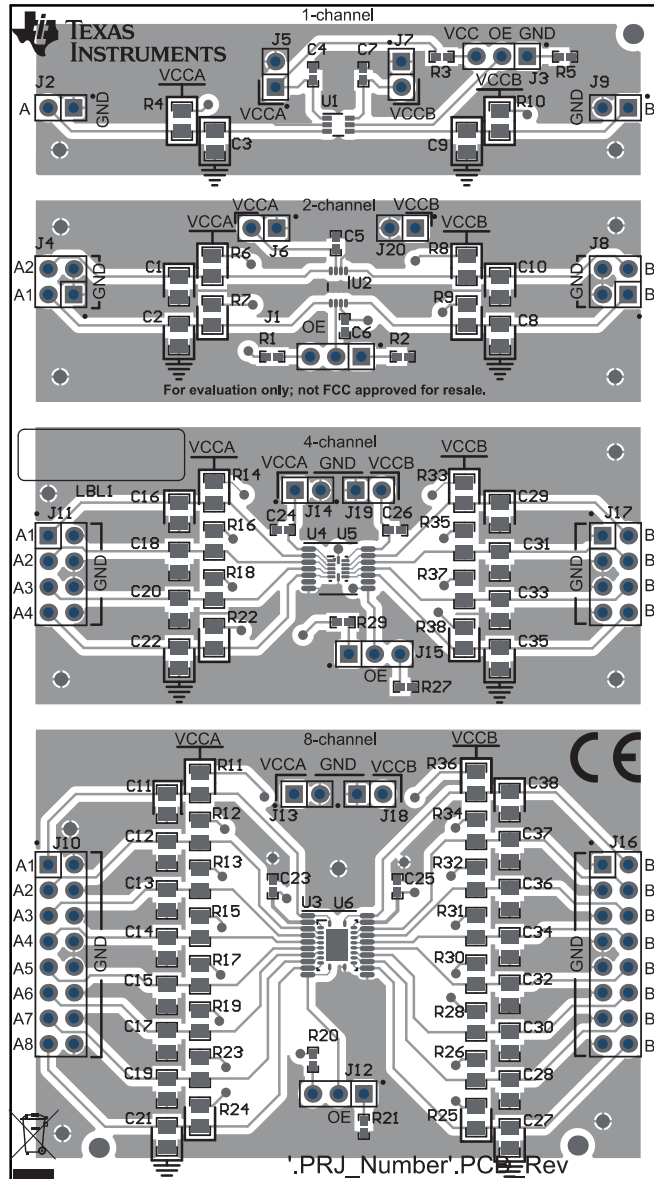


Figure 2. TXB-EVM Layout

3 Schematic and Bill of Materials

3.1 Schematic

Figure 3, Figure 4, Figure 5 and Figure 6 illustrates the TXB-EVM schematic.

1-channel

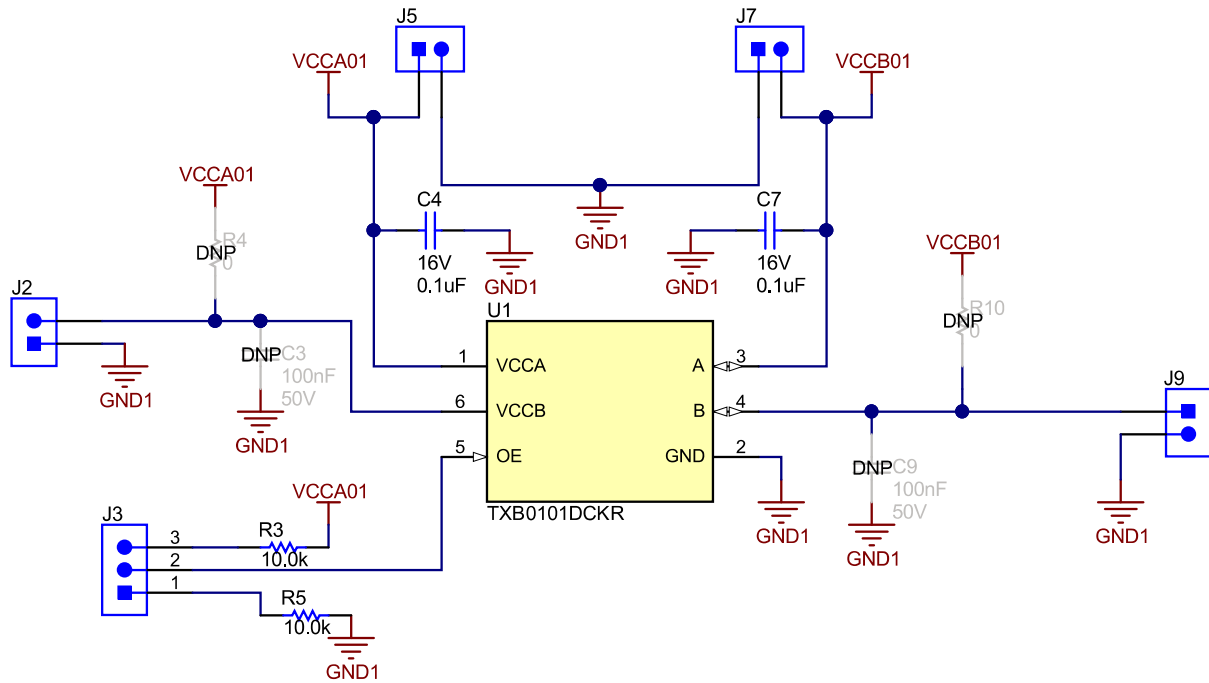


Figure 3. 1-Channel TXB0101

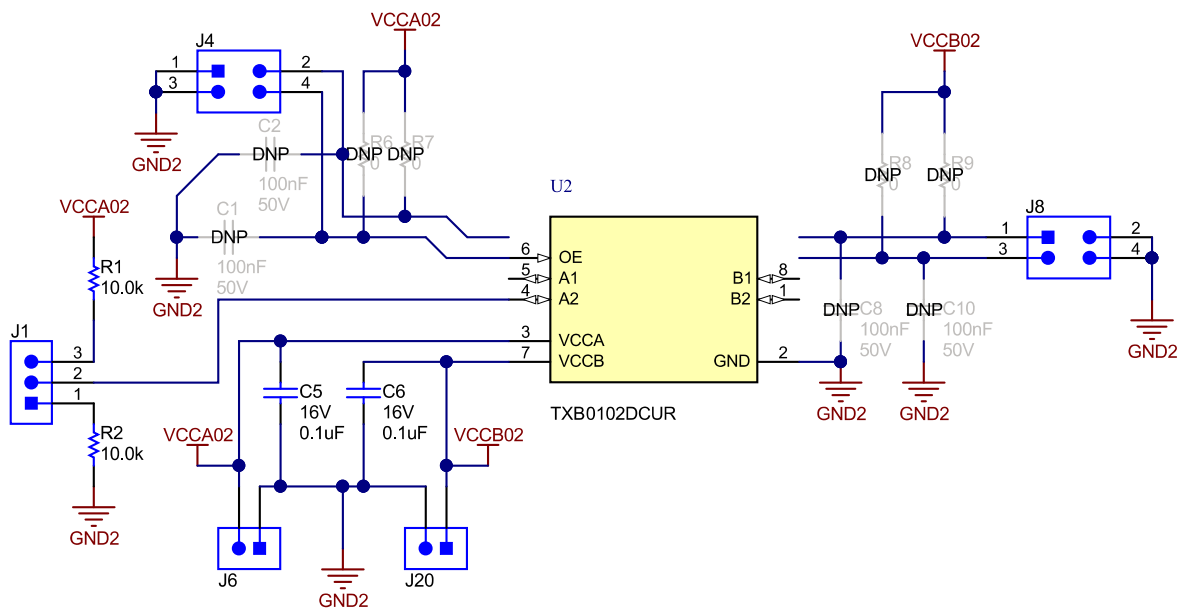


Figure 4. 2-Channel TXB0102

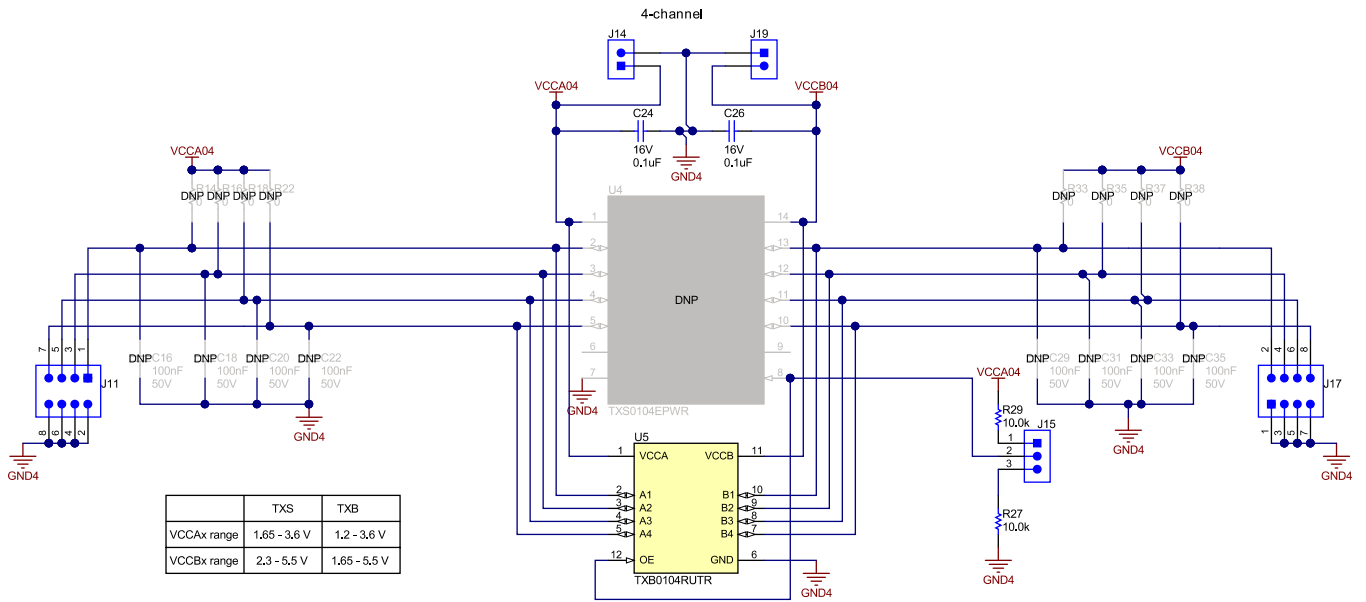


Figure 5. 4-Channel TXB0104

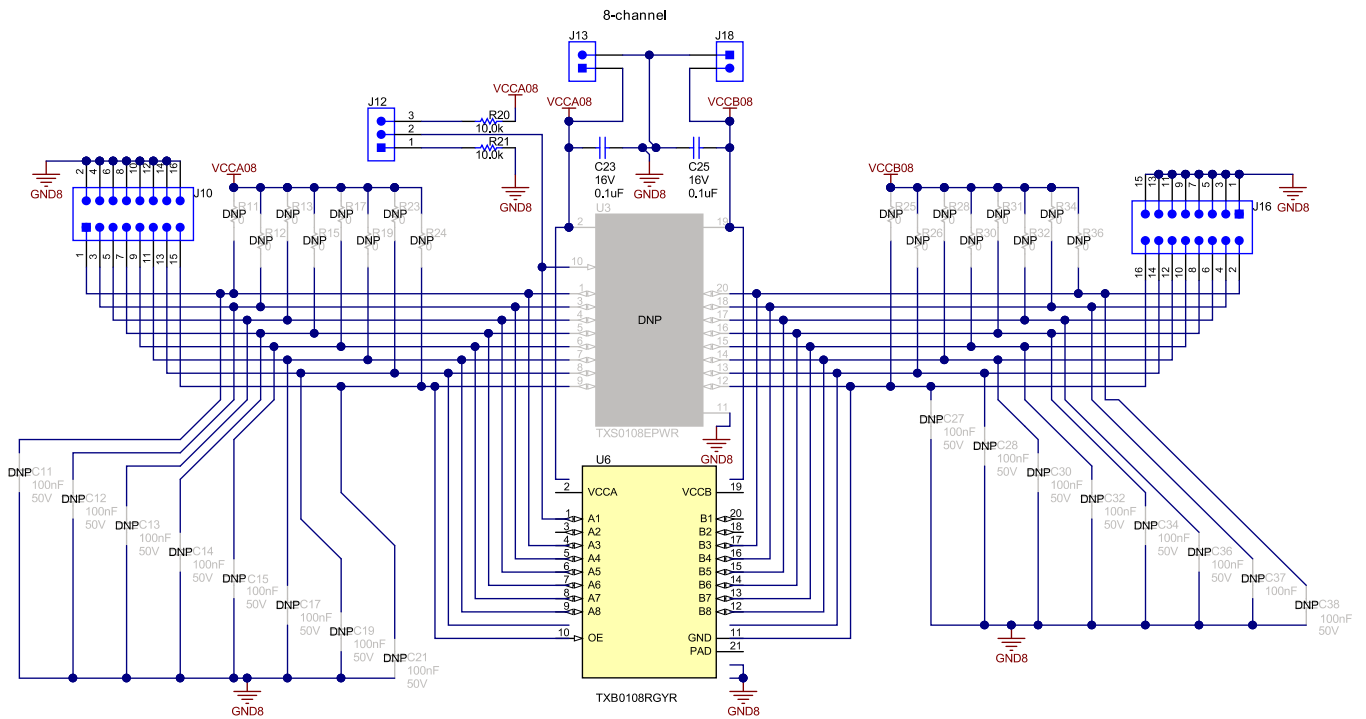


Figure 6. 8-Channel TXB0108

3.2 Bill of Materials

Table 4 lists the TXB-EVM bill of materials.

Table 4. TXB-EVM Bill of Materials

Designator	Quantity	Description	Part Number	Manufacturer
C4, C5, C6, C7, C23, C24, C25, C26	8	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0402	0402YC104KAT2A	AVX
J1, J3, J12, J15	4	Header, 100mil, 3x1, Gold, TH	HTSW-103-07-G-S	Samtec
J2, J5, J6, J7, J9, J13, J14, J18, J19, J20	10	Header, 100mil, 2x1, Gold, TH	HTSW-102-07-G-S	Samtec
J4, J8	2	Header, 100mil, 2x2, Gold, TH	TSW-102-07-G-D	Samtec
J10, J16	2	Header, 100mil, 8x2, Gold, TH	TSW-108-07-G-D	Samtec
J11, J17	2	Header, 100mil, 4x2, Gold, TH	TSW-104-07-G-D	Samtec
R1, R2, R3, R5, R20, R21, R27, R29	8	RES, 10.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	RMCF0402FT10K0	Stackpole Electronics
SH-J1, SH-J3, SH-J12, SH-J15	4	Shunt, 100mil, Flash Gold, Black	SPC02SYAN	Sullins Connector
U1	1	1-Bit Bidirectional Voltage-Level Shifter With Auto Direction Sensing and +/-15-kV ESD Protect, DCK0006A (SOT-SC70-6)	TXB0101DCKR	Texas Instruments
U2	1	2-Bit Bidirectional Voltage-Level Shifter with Auto Direction Sensing and +/-15-kV ESD Protect, DCU0008A (VSSOP-8)	TXB0102DCUR	Texas Instruments
U5	1	4-Bit Bidirectional Voltage-Level Shifter with Auto Direction Sensing and +/-15 kV ESD Protect, RUT0012A (UQFN-12)	TXB0104RUTR	Texas Instruments
U6	1	8-Bit Bidirectional Voltage-Level Shifter with Auto Direction Sensing and +/-15-kV ESD Protect, RGY0020A (VQFN-20)	TXB0108RGYR	Texas Instruments
C1, C2, C3, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38	0	CAP, CERM, 0.1 uF, 50 V, +/- 5%, X7R, 0805	08055C104JAT2A	AVX
R4, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R22, R23, R24, R25, R26, R28, R30, R31, R32, R33, R34, R35, R36, R37, R38	0	RES, 10.0 k, 0.5%, 0.125 W, 0805	RT0805DRE0710KL	Yageo America
U3	0	8-Bit Bidirectional Voltage-Level Shifter For Open-Drain And Push-Pull Application, PW0020A (TSSOP-20)	TXS0108EPWR	Texas Instruments
U4	0	4-Bit Bidirectional Voltage-Level Shifter for Open-Drain and Push-Pull Applications, PW0014A (TSSOP-14)	TXS0104EPWR	Texas Instruments

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated