Low Power Codec with Speaker and Headphone Amplifier

ADAU1373

FEATURES

1 stereo ADC and 2 stereo DACs with sampling rates from 8 kHz to 48 kHz
Low power: 7 mW record, 6 mW playback, 48 kHz at 1.8 V
8 single-ended or 4 differential inputs with PGA
2 microphone bias reference voltages with current sense
2 stereo digital microphone inputs
Flexible analog input/output mixers
1 stereo differential or 2 stereo single-ended line outputs
True ground-centered stereo Class-G headphone amplifier, capable of 2 × 50 mW into 16 Ω at 1.8 V, 10% THD
Filterless stereo Class-D speaker amplifier, capable of 2 × 880 mW into 8 Ω at 3.6 V, 10% THD
Differential earpiece amplifier capable of driving 32 Ω
2 PLLs, supporting input clocks from 8 kHz to 27 MHz
I²C control interface
Digital audio processing
3 digital audio input and output ports with ASRC
I²S, PCM, right-justified, left-justified modes
4.05 mm × 3.82 mm, 81-ball, 0.4 mm pitch WLCSP package
−40°C to +85°C operating temperature range

APPLICATIONS

Mobile phones, tablet PCs, e-books, portable media players

GENERAL DESCRIPTION

The ADAU1373 is a low power, stereo audio codec with integrated digital audio processing that supports stereo 48 kHz record and playback. The stereo audio ADCs and DACs support sampling rates from 8 kHz to 48 kHz, as well as a digital volume control.

Eight single-ended or four differential analog inputs with PGAs are provided for adjusting the gain from −12 dB to +18 dB. They can be configured for microphones or line level signals.

Two stereo digital microphone inputs are supported; four digital microphones can be connected in total. In addition, three serial digital audio input/output ports are provided with asynchronous sample rate converters (ASRCs) to support various sampling rates, allowing for flexible system design in mobile phone applications. The inputs can be mixed and selected before the ADC or configured to bypass the ADC. Two stereo DACs are included, with a flexible mixing option for routing the signals internally.

The analog output side consists of line outputs, headphone output, speaker output, and receiver output. Two stereo single-ended line level outputs, which can be configured as two differential outputs, are included. The headphone output is stereo true ground centered (eliminating the need for coupling capacitors), with efficient Class-G (rail switching) architecture. The efficient stereo filterless Class-D switching amplifier provides ~1 W of stereo power for speakers. The differential receiver amplifier can be used to connect the separate receiver speaker. Two PLL blocks, which can lock to the inputs from 8 kHz to 27 MHz, are included.

The DSP allows system designers to compensate for the real-world limitations of microphones, speakers, amplifiers, and listening environments, resulting in a dramatic improvement in perceived audio quality through equalization, multiband compression, and limiting algorithms. The SigmaStudio™ graphical development tool, which includes audio processing blocks such as filters, mixers, dynamics processors, and amplifiers for fast development of custom signal flows, is used to program the ADAU1373.

FUNCTIONAL BLOCK DIAGRAM

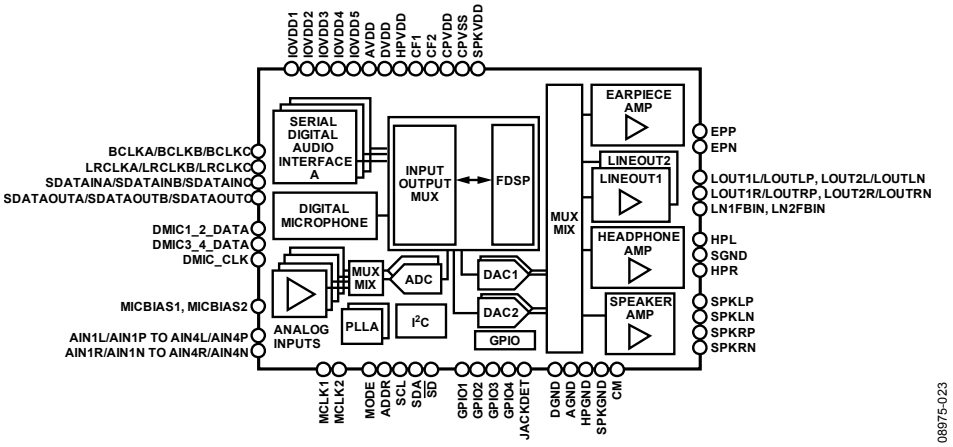


Figure 1.

Rev. 0

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REVISION HISTORY

5/11—Revision 0: Initial Version

SPECIFICATIONS

POWER SUPPLIES

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE RANGES					
Analog	AVDD	1.62	1.8	1.98	V
Digital	DVDD[1]	1.08	1.2	1.98	V
Input/Output	IOVDD	1.62	1.8	3.6	V
Charge Pump	HPVDD	1.62	1.8	1.98	V
Speaker Amplifier	SPKVDD	2.5		5.5	V

[1] For applications using DVDD = 1.8 V, IOVDDx ≥ DVDD.

AUDIO PERFORMANCE

f_S = 48 kHz/24 bits, I²S format, AVDD = HPVDD = IOVDDx = 1.8 V, DVDD = 1.2 V, SPKVDD = 3.6 V, 1 kHz sine wave signal, 20 Hz to 20 kHz measurement bandwidth, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT PROGRAMMABLE GAIN AMPLIFIERS					
Input Resistance					
Single-Ended PGA Mode	+18 dB gain		6.8		kΩ
	0 dB gain		30		kΩ
	−12 dB gain		48		kΩ
Single-Ended Boost Mode	+29 dB gain		20		kΩ
	+9 dB gain		20		kΩ
	0 dB gain		20		kΩ
Differential PGA Mode	+18 dB gain		6.8		kΩ
	0 dB gain		30		kΩ
	−12 dB gain		48		kΩ
Differential Boost Mode	+20 dB gain		20		kΩ
	+9 dB gain		20		kΩ
	0 dB gain		20		kΩ
Gain Range					
PGA Mode	Minimum position		−12		dB
	Maximum position		+18		dB
Boost Mode	0 dB position		0		dB
	+9 dB position		+9		dB
	+20 dB position		+20		dB
Gain Step Size	PGA mode		+1		dB
Maximum Input Level					
Single-Ended PGA Mode	0 dB gain		0.545		V rms
Single-Ended Boost Mode	0 dB gain		0.545		V rms
Differential PGA Mode	0 dB gain		1.09		V rms
Differential Boost Mode	0 dB gain		1.09		V rms
Equivalent Input Noise					
Single-Ended PGA Mode	0 dB gain, unweighted 20 Hz to 20 kHz		7		μV rms
	+18 dB gain, unweighted 20 Hz to 20 kHz		28		μV rms
Single-Ended Boost Mode	0 dB gain, unweighted 20 Hz to 20 kHz		7		μV rms
	+20 dB gain, unweighted 20 Hz to 20 kHz		35		μV rms
Common-Mode Rejection Ratio					
Differential PGA Mode	0 dB gain at 217 Hz		50		dB
Mute Attenuation	Measured at line output reference to full scale (0 dB gain at 1 kHz)		80		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
MICROPHONE BIAS					
Output Voltage	Register 0x21, Bits[5:4] (MICB2GAIN); Bits[3:2] (MICB1GAIN)				
	Setting 00 = 2.9 V	1.71	1.8		V
	Setting 01 = 2.2 V	2.09	2.2		V
	Setting 10 = 2.6 V	2.47	2.6		V
	Setting 11 = 1.8 V	2.75	2.9		V
Output Current		6			mA
Output Noise	Unweighted 20 Hz to 20 kHz		7		μV rms
PSRR	AVDD at 217 Hz = 100 mV p-p		100		dB
	DVDD at 217 Hz = 100 mV p-p		100		dB
	HPVDD at 217 Hz = 100 mV p-p		100		dB
	SPKVDD at 217 Hz = 400 mV p-p		85		dB
Bias Current Detect Threshold	Register 0x22 and Register 0x23, Bits[1:0] (MICBxCURD)				
	Setting 00 = 150 μA		150		μA
	Setting 01 = 330 μA		330		μA
	Setting 10 = 510 μA		510		μA
	Setting 11 = 700 μA		700		μA
Bias Short-Circuit Detect Threshold	Register 0x22 and Register 0x23, Bits[3:2] (MICBxSHT)				
	Setting 00 = 330 μA		330		μA
	Setting 01 = 700 μA		700		μA
	Setting 10 = 1000 μA		1000		μA
	Setting 11 = 1400 μA		1400		μA
MIXER BLOCK					
Mixer ADC					
Mute Attenuation			90		dB
Mixer Line Output					
Mute Attenuation			90		dB
Mixer Headphone Output					
Mute Attenuation			90		dB
Mixer Speaker Output					
Mute Attenuation			90		dB
Mixer Earpiece Output					
Mute Attenuation			90		dB
LINE OUTPUT AMPLIFIER					
Gain			0		dB
Volume Control Step Size	Variable from mute to 0 dB in 32 steps	Mute		0	dB
Mute Attenuation			90		dB
Maximum Output Level					
Single-Ended Mode	Load = 10 kΩ		0.545		V rms
Differential Mode	Load = 10 kΩ		1.09		V rms
Output Resistance	At each output pin: LOUT1L, LOUT1R, LOUT2L, and LOUT2R		0.3		Ω
Common-Mode Voltage	V_{CM} at LOUT1L, LOUT1R, LOUT2L, and LOUT2R		AVDD/2		V
DC Offset	Differential mode between LOUTLP and LOUTLN, LOUTRP and LOUTRN		1		mV
Ground-Loop Rejection Ratio	Measured by injecting 1000 Hz sine wave,100 mV rms at LNxFBIN; referenced to full-scale output voltage		56		dB
Input Resistance into LNxFBIN Pin			120		kΩ

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
HEADPHONE AMPLIFIER					
Gain		−69	0	+6	dB
Volume Control Step Size	Variable from −69 dB to +6 dB in 32 steps	−69		+6	dB
Mute Attenuation			85		dB
Output Level at 1% THD + N	Load = 16 Ω		27		mW
	Load = 32 Ω		24		mW
	Load = 10 kΩ		1.2		V rms
Output Level at 10% THD + N	Load = 16 Ω		50		mW
	Load = 32 Ω		43		mW
	Load = 10 kΩ		1.2		V rms
Efficiency	P_{OUT} = 3 mW, HPVDD = 1.8 V, R_L = 16 Ω		25		%
	P_{OUT} = 3.5 mW, HPVDD = 1.8 V, R_L = 32 Ω		38		%
DC Offset	HPVDD = 1.8 V, R_L = 16 Ω		±3		mV
Output Limiter Threshold	Peak output at HPL, HPR; setting V_{OUT} = 1.1 V peak		1.1		V pk
	Peak output at HPL, HPR; setting V_{OUT} = 0.968 V peak		0.97		V pk
	Peak output at HPL, HPR; setting V_{OUT} = 0.815 V peak		0.82		V pk
	Peak output at HPL, HPR; setting V_{OUT} = 0.56 V peak		0.56		V pk
	Peak output at HPL, HPR; setting V_{OUT} = 0.408 V peak		0.41		V pk
	Peak output at HPL, HPR; setting V_{OUT} = 0.28 V peak		0.28		V pk
	Peak output at HPL, HPR; setting V_{OUT} = 0.23 V peak		0.23		V pk
Load Resistance		12	16		Ω
Load Capacitance				150	pF
Turn On Time			17.1		ms
Turn Off Time			1.9		ms
SPEAKER AMPLIFIER					
Gain	Setting = 12 dB		12		dB
	Setting = 18 dB		18		dB
Volume Control Step Size	Variable from mute to 0 dB in 32 steps	Mute		0	dB
Mute Attenuation			90		dB
Output Power at 1% THD + N	SPKVDD = 2.5 V, 4 Ω + 15 µH (stereo)		0.554		W
	SPKVDD = 3.6 V, 4 Ω + 15 µH (stereo)		1.212		W
	SPKVDD = 4.2 V, 4 Ω + 15 µH (stereo)		1.679		W
	SPKVDD = 5 V, 4 Ω + 15 µH (stereo)		2.4		W
	SPKVDD = 2.5 V, 8 Ω + 33 µH (stereo)		0.33		W
	SPKVDD = 3.6 V, 8 Ω + 33 µH (stereo)		0.71		W
	SPKVDD = 4.2 V, 8 Ω + 33 µH (stereo)		0.98		W
	SPKVDD = 5 V, 8 Ω + 33 µH (stereo)		1.40		W
Output Power at 10% THD + N	SPKVDD = 2.5 V, 4 Ω + 15 µH (stereo)		0.691		W
	SPKVDD = 3.6 V, 4 Ω + 15 µH (stereo)		1.511		W
	SPKVDD = 4.2 V, 4 Ω + 15 µH (stereo)		2.091		W
	SPKVDD = 5 V, 4 Ω + 15 µH (stereo)		2.99		W
	SPKVDD = 2.5 V, 8 Ω + 33 µH (stereo)		0.41		W
	SPKVDD = 3.6 V, 8 Ω + 33 µH (stereo)		0.88		W
	SPKVDD = 4.2 V, 8 Ω + 33 µH (stereo)		1.22		W
	SPKVDD = 5 V, 8 Ω + 33 µH (stereo)		1.73		W
Output Power at 1% THD + N	SPKVDD = 2.5 V, 4 Ω + 15 µH (mono)		0.588		W
	SPKVDD = 3.6 V, 4 Ω + 15 µH (mono)		1.285		W
	SPKVDD = 4.2 V, 4 Ω + 15 µH (mono)		1.78		W
	SPKVDD = 5 V, 4 Ω + 15 µH (mono)		2.55		W
	SPKVDD = 2.5 V, 8 Ω + 33 µH (mono)		0.34		W
	SPKVDD = 3.6 V, 8 Ω + 33 µH (mono)		0.73		W
	SPKVDD = 4.2 V, 8 Ω + 33 µH (mono)		1.00		W
	SPKVDD = 5 V, 8 Ω + 33 µH (mono)		1.43		W

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Output Power at 10% THD + N	SPKVDD = 2.5 V, 4 Ω + 15 µH (mono)		0.733		W
	SPKVDD = 3.6 V, 4 Ω + 15 µH (mono)		1.611		W
	SPKVDD = 4.2 V, 4 Ω + 15 µH (mono)		2.22		W
	SPKVDD = 5 V, 4 Ω + 15 µH (mono)		3.18		W
	SPKVDD = 2.5 V, 8 Ω + 33 µH (mono)		0.43		W
	SPKVDD = 3.6 V, 8 Ω + 33 µH (mono)		0.905		W
	SPKVDD = 4.2 V, 8 Ω + 33 µH (mono)		1.25		W
	SPKVDD = 5 V, 8 Ω + 33 µH (mono)		1.78		W
Efficiency	P_{OUT} = 2.4 W, SPKVDD = 5 V, R_L = 4 Ω + 15 µH (stereo)		89		%
	P_{OUT} = 1.2 W, SPKVDD = 3.6 V, R_L = 4 Ω + 15 µH (stereo)		87		%
	P_{OUT} = 1.4 W, SPKVDD = 5 V, R_L = 8 Ω + 33 µH (stereo)		93		%
	P_{OUT} = 0.71 W, SPKVDD = 3.6 V, R_L = 8 Ω + 33 µH (stereo)		92		%
Average Switching Frequency			350		kHz
R_{DS} On	NMOS at 100 mA		180		mΩ
	PMOS at 100 mA		210		mΩ
DC Offset	Gain = 12 dB, SPKVDD = 3.6 V		±3		mV
Load Resistance	Mono mode	3			Ω
	Stereo mode	4			Ω
Recovery Time from Protect Mode		256		512	ms
Turn On Time	From high-Z (mute) to outputs switching state		3.5		ms
Turn Off Time	From output switching to high-Z (mute) state		1.8		ms
EARPIECE AMPLIFIER					
Gain		0	6	12	dB
Gain Step Size			6		dB
Mute Attenuation			85		dB
Output Level at 1% THD + N	SPKVDD = 2.5 V, load = 8 Ω		53		mW
	SPKVDD = 2.5 V, load = 16 Ω		66		mW
	SPKVDD = 2.5 V, load = 32 Ω		58		mW
	SPKVDD = 3.6 V, load = 8 Ω		123		mW
	SPKVDD = 3.6 V, load = 16 Ω		103		mW
	SPKVDD = 3.6 V, load = 32 Ω		69		mW
	SPKVDD = 5 V, load = 8 Ω		140		mW
	SPKVDD = 5 V, load = 16 Ω		110		mW
	SPKVDD = 5 V, load = 32 Ω		72		mW
Output Power at 10% THD + N	SPKVDD = 2.5 V, load = 8 Ω		74		mW
	SPKVDD = 2.5 V, load = 16 Ω		91		mW
	SPKVDD = 2.5 V, load = 32 Ω		73		mW
	SPKVDD = 3.6 V, load = 8 Ω		162		mW
	SPKVDD = 3.6 V, load = 16 Ω		134		mW
	SPKVDD = 3.6 V, load = 32 Ω		89		mW
	SPKVDD = 5 V, load = 8 Ω		178		mW
	SPKVDD = 5 V, load = 16 Ω		142		mW
	SPKVDD = 5 V, load = 32 Ω		92		mW
DC Offset	SPKVDD = 3.6 V, load = 32 Ω, gain = 0 dB		±1		mV
	SPKVDD = 3.6 V, load = 32 Ω, gain = 6 dB		±2		mV
	SPKVDD = 3.6 V, load = 32 Ω, gain = 12 dB		±3		mV
Load Resistance		8			Ω
Turn On Time			9.6		ms
Turn Off Time			4.1		ms

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG INPUT → ADC → DIGITAL OUTPUT					
ADC Resolution	All ADCs		24		Bits
Dynamic Range	−60 dBFS input at 1 kHz				
Unweighted (RMS)			93		dB
A-weighted (RMS)			96		dB
Signal-to-Noise Ratio	A-weighted (rms), referred to full-scale output		96		dB
THD + N	−1 dBFS input at 1 kHz		0.01		%
Offset Error			±1		mV
Gain Drift			100		ppm/°C
Interchannel Isolation			85		dB
PSRR	AVDD ripple = 100 mV p-p at 217 Hz, input referred for PGA gain = 0 dB		85		dB
	All other supplies (HPVDD, SPKVDD, DVDD, IOVDDx) = 100 mV p-p at 217 Hz, input referred for PGA gain = 0 dB		85		dB
DIGITAL MICROPHONE INPUT → ADC→ DIGITAL OUTPUT					
Dynamic Range	−60 dBFS input at 1 kHz				dB
Unweighted (rms)			93		dB
A-weighted (rms)			96		
Signal-to-Noise Ratio	A-weighted (rms)		96		dB
THD + N	−1 dBFS at 1 kHz		0.01		%
Offset Error			±1		mV
Gain Drift			100		ppm/°C
Interchannel Isolation			85		dB
PSRR	AVDD ripple = 100 mV p-p at 217 Hz, input referred for PGA gain = 0 dB		85		dB
	All other supplies (HPVDD, SPKVDD, DVDD, IOVDDx) = 100 mV p-p at 217 Hz, input referred for PGA gain = 0 dB		85		dB
ANALOG INPUT → LINE OUTPUT					
Dynamic Range	−60 dBFS input at 1 kHz				
Unweighted (RMS)			91		dB
A-weighted (RMS)			94		dB
Signal-to-Noise Ratio	Differential line output, A-weighted (rms), referred to full-scale output		94		dB
THD + N	V_{OUT} = 1 V, 1 kHz, R_L=10 kΩ		0.013		%
	V_{OUT} = 0.5 V, 1 kHz, R_L=10 kΩ		0.017		%
Interchannel Isolation			85		dB
PSRR	AVDD ripple = 100 mV p-p at 217 Hz, input referred for PGA gain = 0 dB		85		dB
	All other supplies (HPVDD, SPKVDD, DVDD, IOVDDx) = 100 mV p-p at 217 Hz, input referred for PGA gain = 0 dB		85		dB
ANALOG INPUT → HEADPHONE OUTPUT					
Dynamic Range	−60 dBFS input at 1 kHz				
	Unweighted (rms)		96		dB
	A-weighted (rms)		99		dB
Signal-to-Noise Ratio	A-weighted (rms), referred to full-scale output		99		dB
THD + N	P_{OUT} = 27 mW, 1 kHz, R_L = 16 Ω		0.01		%
Interchannel Isolation			85		dB
PSRR	HPVDD ripple = 100 mV p-p at 217 Hz, input referred for PGA gain = 0 dB		85		dB
	All other supplies (AVDD, SPKVDD, DVDD, IOVDDx) = 100 mV p-p at 217 Hz, input referred for PGA gain = 0 dB		85		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG INPUT → SPEAKER OUTPUT					
Dynamic Range	−60 dBFS input at 1 kHz				
	Unweighted (rms)		98		dB
	A-weighted (rms)		101		dB
Signal-to-Noise Ratio	A-weighted (rms), referred to 0.7 W at 3.6 V, R_L = 8 Ω		101		dB
THD + N	SPKVDD = 5 V, P_{OUT} = 1 W, 1 kHz, R_L = 8 Ω		0.013		%
	SPKVDD = 3.6 V, P_{OUT} = 0.5 W, 1kHz, R_L = 8 Ω		0.017		%
Interchannel Isolation			85		dB
PSRR	SPKVDD ripple = 100 mV p-p at 217 Hz, input referred for PGA gain = 12 dB		85		dB
	All other supplies (AVDD, HPVDD, DVDD, IOVDDx) = 100 mV p-p at 217 Hz, input referred for PGA gain = 12 dB		85		dB
ANALOG INPUT → EARPIECE OUTPUT					
Dynamic Range	−60 dBFS input at 1 kHz				
	Unweighted (rms)		95		dB
	A-weighted (rms)		98		dB
Signal-to-Noise Ratio	A-weighted (rms), referred to 40 mW at 3.6 V, R_L = 32 Ω		98		dB
THD + N	P_{OUT} = 60 mW, 1 kHz, R_L = 8 Ω		0.1		%
	P_{OUT} = 30 mW, 1 kHz, R_L = 8 Ω		0.2		%
PSRR	AVDD ripple = 100 mV p-p at 217 Hz, input referred for PGA gain = 12 dB		85		dB
	All other supplies (HPVDD, DVDD, SPKVDD, IOVDDx) = 100 mV p-p at 217 Hz, input referred for PGA gain = 12 dB		85		dB
DIGITAL INPUT → DAC → MIXER → LINE OUTPUT					
Dynamic Range	20 Hz to 20 kHz, −60 dBFS input, unweighted (rms)		93		dB
	20 Hz to 20 kHz, −60 dBFS input, A-weighted (rms)		96		dB
Signal-to-Noise Ratio	20 Hz to 20 kHz, A-weighted, relative to full scale		96		dB
THD + N	At −1 dBFS, 1 kHz		0.01		%
Full-Scale Output Voltage	Scales linearly with AVDD		1.0		V rms
Interchannel Isolation			100		dB
Interchannel Phase Deviation			0.1		Degrees
Digital Volume Control					
Step			0.375		dB
Range			95		dB
PSRR	AVDD ripple = 100 mV p-p at 217 Hz, input referred for PGA gain = 12 dB		85		dB
	All other supplies (HPVDD, DVDD, SPKVDD, IOVDDx) = 100 mV p-p at 217 Hz, input referred for PGA gain = 12 dB		85		dB
DIGITAL INPUT → DAC → MIXER → HEADPHONE OUTPUT					
Dynamic Range	20 Hz to 20 kHz, −60 dBFS input, unweighted (rms)		96		dB
	20 Hz to 20 kHz, −60 dBFS input, A-weighted (rms)		99		dB
Signal-to-Noise Ratio	20 Hz to 20 kHz, A-weighted, relative to full scale		99		dB
THD + N	At −1 dBFS, 1 kHz		0.01		%
Full-Scale Output Voltage					V rms
Interchannel Isolation			100		dB
Interchannel Phase Deviation			0.1		Degrees
Digital Volume Control					
Step			0.375		dB
Range			95		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL INPUT → DAC → MIXER → SPEAKER OUTPUT					
Dynamic Range	20 Hz to 20 kHz, −60 dBFS input, unweighted (rms)		93		dB
	20 Hz to 20 kHz, −60 dBFS input, A-weighted (rms)		96		dB
Signal-to-Noise Ratio	20 Hz to 20 kHz, A-weighted, relative to full scale		97		dB
THD + N	At −1 dBFS, 1 kHz		0.01		%
Interchannel Isolation			100		dB
Interchannel Phase Deviation			0.1		Degrees
Digital Volume Control					
Step			0.375		dB
Range			95		dB
DIGITAL INPUT→ DAC → MIXER → EARPIECE OUTPUT					
Dynamic Range	20 Hz to 20 kHz, −60 dBFS input, unweighted (rms)		93		dB
	20 Hz to 20 kHz, −60 dBFS input, A-weighted (rms)		96		dB
Signal-to-Noise Ratio	20 Hz to 20 kHz, A-weighted, relative to full scale		97		dB
THD + N	At −1 dBFS, 1 kHz		0.1		%
Full-Scale Output Voltage	Scales linearly with SPKVDD; SPKVDD = 3.6 V		1.53		V rms
Digital Volume Control					
Step			0.375		dB
Range			95		dB
REFERENCE					
Common-Mode Reference Output	CM pin		AVDD/2		V
CHARGE PUMP					
Supply Voltage		1.62	1.8	1.98	V
Outputs					
CPVDD					
Below Supply Switching Threshold			0.9		V
Above Supply Switching Threshold			1.8		V
CPVSS					
Below Supply Switching Threshold			−0.9		V
Above Supply Switching Threshold			−1.8		V
Switching Frequency			500		kHz
Flying Capacitor Value		0.47	1	10	µF
Supply Switching Threshold			0.4		V
Start-Up Time			0.5		ms
PLLx					
Input Frequency		0.008		27	MHz
Lock Time (Analog PLL)			3		ms
Jitter (Cycle-to-Cycle) rms	Measured at GPIOx with master clock output set at 256 × f_S (12.288 MHz, where f_S = 48 kHz)				
Analog PLL Only (DPLL Bypassed)					
8 MHz Input (Fractional Mode)			470		ps
27 MHz Input (Fractional Mode)			280		ps
12.288 MHz Input (Integer Mode)			200		ps
Digital PLL + Analog PLL					
8 kHz LRCLKx Input			310		ps
96 kHz LRCLKx Input			260		ps
512 kHz (8 kHz × 64) BCLKx Input			310		ps
2.048 MHz (8 kHz × 256) MCLKx Input			210		ps
MCLKx Clock Output Frequency				49.152	MHz
GPIOx					
Drive Capability	IOVDDx = 1.8 V		4		mA
	IOVDDx = 3.3 V		20		mA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
IRQ RESPONSE TIME					
ASRCx_IRQ_STATUS	One clock cycle = 1/256 × f_S = 81.4 ns at f_S = 48 kHz		4		Clock cycles
DRC_IRQ_STATUS, PLL_UNLOCK_STATUS			3		Clock cycles
HP_CFG_STATUS, HP_DECT_STATUS, AFAULT_STATUS			256 ms + 3		Clock cycles
JACK DETECT					
Debounce Time			128		ms
DIGITAL MICROPHONE INPUT					
Clock Output Frequency	Depends on internal sample rate = 64 × f_S		3.072		MHz
Decimator Operating Frequency	Depends on internal sample rate = 128 × f_S		6.144		MHz

POWER CONSUMPTION

Table 3 lists some commonly used paths, as well as the typical current that is consumed by the part under quiescent conditions. The total power consumed includes the power in the loads, as specified. T_A = 25°C, line output load = 10 kΩ, headphone stereo = 16 Ω, speaker load = 8 Ω + 33 μH, and earpiece = 32 Ω, audio port configured as the slave, f_S = 48 kHz, MCLK = 12.288 MHz, unless otherwise specified.

Table 3.

Mode	AVDD (V)	DVDD (V)	HPVDD (V)	SPKVDD (V)	IOVDD (V)	I_{AVDD} (mA)	I_{DVDD} (mA)	I_{HPVDD} (mA)	I_{SPKVDD} (mA)	I_{IOVDD} (mA)	Total Power (mW)
POWER-DOWN											
No Clocks	1.62	1.08	1.62	2.5	1.62	0.008	0.01	0.001	0.0014	0.008	0.04184
	1.8	1.2	1.8	3.6	1.8	0.012	0.011	0.0014	0.0035	0.008	0.06432
	1.8	1.2	1.8	4.2	1.8	0.0124	0.011	0.0015	0.0055	0.008	0.07572
	1.98	1.98	1.98	5.5	3.63	0.0178	0.0149	0.002	0.0147	0.008	0.178596
MCLKx = 12.288 MHz	1.62	1.08	1.62	2.5	1.62	0.032	0.19	0.001	0.0014	0.017	0.2897
	1.8	1.2	1.8	3.6	1.8	0.0378	0.22	0.0014	0.0035	0.017	0.37776
	1.8	1.2	1.8	4.2	1.8	0.0378	0.22	0.0015	0.0055	0.017	0.38844
	1.98	1.98	1.98	5.5	3.63	0.045	0.4	0.002	0.0147	0.017	1.02762
POWER-UP											
No Clocks (Default State)	1.62	1.08	1.62	2.5	1.62	0.31	0.046	0.0012	0.041	0.008	0.669284
	1.8	1.2	1.8	3.6	1.8	0.32	0.0495	0.0018	0.065	0.008	0.88704
	1.8	1.2	1.8	4.2	1.8	0.32	0.0495	0.0018	0.079	0.008	0.98484
	1.98	1.98	1.98	5.5	3.63	0.34	0.083	0.0023	0.118	0.008	1.520134
MCLKx = 12.288 MHz, PLL Bypassed	1.62	1.08	1.62	2.5	1.62	0.34	0.23	0.0013	0.041	0.017	0.931346
	1.8	1.2	1.8	3.6	1.8	0.35	0.256	0.0018	0.065	0.017	1.20504
	1.8	1.2	1.8	4.2	1.8	0.35	0.256	0.0018	0.079	0.017	1.30284
	1.98	1.98	1.98	5.5	3.63	0.37	0.47	0.0023	0.118	0.017	2.378464
With Clocks (PLL Enabled, LRCLKA = 48 kHz, DPLL + APLL Enabled, Master Mode)	1.62	1.08	1.62	2.5	1.62	1.77	1.06	0.0013	0.041	1.72	6.903206
	1.8	1.2	1.8	3.6	1.8	1.83	1.26	0.0018	0.065	1.72	8.13924
	1.8	1.2	1.8	4.2	1.8	1.83	1.26	0.0018	0.079	1.72	8.23704
	1.98	1.98	1.98	5.5	3.63	1.91	2.34	0.0023	0.118	1.72	15.31215
ANALOG BYPASS (NO CLOCKS)											
Analog Input → Line Output	1.62	1.08	1.62	2.5	1.62	1.62	0.045	0.0012	0.041	0.008	2.790404
	1.8	1.2	1.8	3.6	1.8	1.66	0.049	0.0018	0.068	0.008	3.30924
	1.8	1.2	1.8	4.2	1.8	1.66	0.049	0.0018	0.086	0.008	3.42564
	1.98	1.98	1.98	5.5	3.63	1.72	0.083	0.0023	0.128	0.008	4.307534
Analog Input → Headphone Output	1.62	1.08	1.62	2.5	1.62	1.33	0.045	1.35	0.041	0.008	4.50566
	1.8	1.2	1.8	3.6	1.8	1.35	0.05	1.37	0.065	0.008	5.2044
	1.8	1.2	1.8	4.2	1.8	1.35	0.05	1.37	0.079	0.008	5.3022
	1.98	1.98	1.98	5.5	3.63	1.37	0.083	1.39	0.118	0.008	6.30718
Analog Input → Speaker Output (Mono)	1.62	1.08	1.62	2.5	1.62	1.44	0.045	0.0012	3.58	0.008	11.3463
	1.8	1.2	1.8	3.6	1.8	1.46	0.05	0.0018	4.47	0.008	18.79764
	1.8	1.2	1.8	4.2	1.8	1.47	0.05	0.0018	4.92	0.008	23.38764
	1.98	1.98	1.98	5.5	3.63	1.49	0.083	0.0023	5.94	0.008	35.81813
Analog Input → Speaker Output (Stereo)	1.62	1.08	1.62	2.5	1.62	1.98	0.045	0.0012	5.67	0.008	17.4461
	1.8	1.2	1.8	3.6	1.8	2.02	0.05	0.0018	7.17	0.008	29.52564
	1.8	1.2	1.8	4.2	1.8	2.01	0.05	0.0018	7.99	0.008	37.25364
	1.98	1.98	1.98	5.5	3.63	2.04	0.083	0.0023	9.77	0.008	57.97213
Analog Input → Earpiece Output	1.62	1.08	1.62	2.5	1.62	0.89	0.045	0.0012	0.82	0.008	3.555304
	1.8	1.2	1.8	3.6	1.8	0.91	0.049	0.0018	0.9	0.008	4.95444
	1.8	1.2	1.8	4.2	1.8	0.91	0.049	0.0018	0.94	0.008	5.66244
	1.98	1.98	1.98	5.5	3.63	0.92	0.083	0.0023	1.07	0.008	7.904534

Mode	AVDD (V)	DVDD (V)	HPVDD (V)	SPKVDD (V)	IOVDD (V)	I_{AVDD} (mA)	I_{DVDD} (mA)	I_{HPVDD} (mA)	I_{SPKVDD} (mA)	I_{IOVDD} (mA)	Total Power (mW)
RECORD PATH (MCLK = 12.288 MHz)											
Analog Input → ADC → Digital Audio Interface A	1.62	1.08	1.62	2.5	1.62	2.73	0.73	0.0014	0.041	0.017	5.343308
	1.8	1.2	1.8	3.6	1.8	3.42	0.64	0.0018	0.065	0.017	7.19184
	1.8	1.2	1.8	4.2	1.8	3.4	0.64	0.0018	0.079	0.017	7.25364
	1.98	1.98	1.98	5.5	3.63	3.78	1.15	0.0023	0.0118	0.017	9.892564
Digital Microphone Input → Decimator → Digital Audio Interface A	1.62	1.08	1.62	2.5	1.62	0.038	0.59	0.0012	0.041	0.017	0.830744
	1.8	1.2	1.8	3.6	1.8	0.044	0.655	0.0018	0.065	0.017	1.13304
	1.8	1.2	1.8	4.2	1.8	0.044	0.655	0.0018	0.079	0.017	1.23084
	1.98	1.98	1.98	5.5	3.63	0.05	1.18	0.0023	0.0118	0.017	2.566564
PLAYBACK PATH											
Digital Input → DAC → Line Output	1.62	1.08	1.62	2.5	1.62	2.62	0.045	0.0012	0.041	0.017	4.424984
	1.8	1.2	1.8	3.6	1.8	2.82	0.82	0.0018	0.068	0.017	6.33864
	1.8	1.2	1.8	4.2	1.8	2.82	0.82	0.0018	0.086	0.017	6.45504
	1.98	1.98	1.98	5.5	3.63	2.92	1.486	0.0023	0.128	0.017	9.494144
Digital Input → DAC → Headphone Output	1.62	1.08	1.62	2.5	1.62	2.44	0.73	1.35	0.041	0.017	7.05824
	1.8	1.2	1.8	3.6	1.8	2.51	0.82	1.37	0.068	0.017	8.2434
	1.8	1.2	1.8	4.2	1.8	2.51	0.82	1.37	0.086	0.017	8.3598
	1.98	1.98	1.98	5.5	3.63	2.59	1.49	1.39	0.128	0.017	11.59631
Digital Input → DAC → Speaker Output	1.62	1.08	1.62	2.5	1.62	3.09	0.732	0.0013	5.68	0.017	20.02601
	1.8	1.2	1.8	3.6	1.8	3.18	0.82	0.0018	7.17	0.017	32.55384
	1.8	1.2	1.8	4.2	1.8	3.18	0.82	0.0018	7.97	0.017	40.21584
	1.98	1.98	1.98	5.5	3.63	3.27	1.49	0.0023	9.73	0.017	63.00606
Digital Input → DAC → Earpiece Output	1.62	1.08	1.62	2.5	1.62	1.97	0.66	0.0012	0.82	0.017	5.983684
	1.8	1.2	1.8	3.6	1.8	2.06	0.74	0.0018	0.897	0.017	7.85904
	1.8	1.2	1.8	4.2	1.8	2.06	0.74	0.0018	0.94	0.017	8.57784

DIGITAL FILTER/SRC CHARACTERISTICS

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC DECIMATION FILTER					
Pass Band	±0.04 dB	0		0.423 f_S	Hz
	−6 dB		0.5 f_S		Hz
Pass-Band Ripple				±0.04	dB
Stop Band		0.577 f_S			Hz
Stop-Band Attenuation	f > 0.577 f_S	−60			dB
Group Delay [1950/(128 × f_S)]	f_S = 48 kHz		0.317		ms
DAC INTERPOLATION FILTER					
Pass Band	±0.03 dB	0		0.423 f_S	Hz
	−6 dB		0.5 f_S		Hz
Pass-Band Ripple				±0.03	dB
Stop Band		0.577 f_S			Hz
Stop-Band Attenuation	f > 0.577 f_S	−60			dB
Group Delay [1791/(128 × f_S)]	f_S = 48 kHz		0.292		ms
SAMPLE RATE CONVERTER					
Pass Band	0.04 dB	0		0.418 f_S	Hz
	−6 dB		0.5 f_S		Hz
Pass-Band Ripple				0.02	dB
Stop Band		0.582 f_S			Hz
Stop-Band Attenuation	f > 0.582 f_S	−100			dB
Output/Input Sample Rate Ratio		1:8		8:1	
Signal-to-Noise Ratio, A-weighted				100	dB
Dynamic Range, A-weighted		100		120	dB
THD + N		90			dB
Maximum Group Delay	48 kHz in, 8 kHz out		3.7		ms
Maximum Start-Up Time	48 kHz in, 8 kHz out		15		ms

DIGITAL INPUT/OUTPUT SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT SPECIFICATIONS					
Input Voltage High (V_{IH})		0.6 × IOVDD			V
Input Voltage Low (V_{IL})				0.25 × IOVDD	V
Input Leakage	I_{IH} at V_{IH} = 2.4 V			10	µA
	I_{IL} at V_{IL} = 0.8 V			10	µA
OUTPUT SPECIFICATIONS					
High Output Voltage High (V_{OH})	I_{OH} = 1 mA	IOVDD − 0.6			V
Output Voltage Low (V_{OL})	I_{OL} = 1 mA			0.4	V
INPUT CAPACITANCE				5	pF

DIGITAL TIMING SPECIFICATIONS

−40°C < T_A < +85°C, IOVDDx = 1.8 V ± 10%.

Table 6.

Parameter	Limit		Unit	Description
	t_{MIN}	t_{MAX}		
MASTER CLOCK				
Duty Cycle	45	55	%	
SERIAL PORT				
t_{BIL}	5		ns	BCLKx pulse width low
t_{BIH}	5		ns	BCLKx pulse width high
t_{LIS}	5		ns	LRCLKx setup; time to BCLK rising
t_{LIH}	5		ns	LRCLKx hold; time from BCLK rising
t_{SIS}	5		ns	DAC_SDATA setup; time to BCLK rising
t_{SIH}	5		ns	DAC_SDATA hold; time from BCLK rising
t_{SODM}		50	ns	ADC_SDATA delay; time from BCLK falling in master mode
I²C PORT				
f_{SCL}		400	kHz	SCL frequency
t_{SCLH}	0.6		µs	SCL high
t_{SCLL}	1.3		µs	SCL low
t_{SCS}	0.6		µs	Setup time; relevant for repeated start condition
t_{SCH}	0.6		µs	Hold time; after this period of time, the first clock is generated
t_{DS}	100		ns	Data setup time
t_{DH}	5		ns	Data hold time
t_{SCR}		300	ns	SCL rise time
t_{SCF}		300	ns	SCL fall time
t_{SDR}		300	ns	SDA rise time
t_{SDF}		300	ns	SDA fall time
t_{BFT}	0.6		µs	Bus-free time; time between stop and start
DIGITAL MICROPHONE				R_L = 1 MΩ, C_L = 14 pF
t_{DCF}		10	ns	Digital microphone clock fall time
t_{DCR}		10	ns	Digital microphone clock rise time
t_{DDV}	22	30	ns	Digital microphone delay time for valid data
t_{DDH}	0	12	ns	Digital microphone delay time for data, three-stated

Digital Timing Diagrams

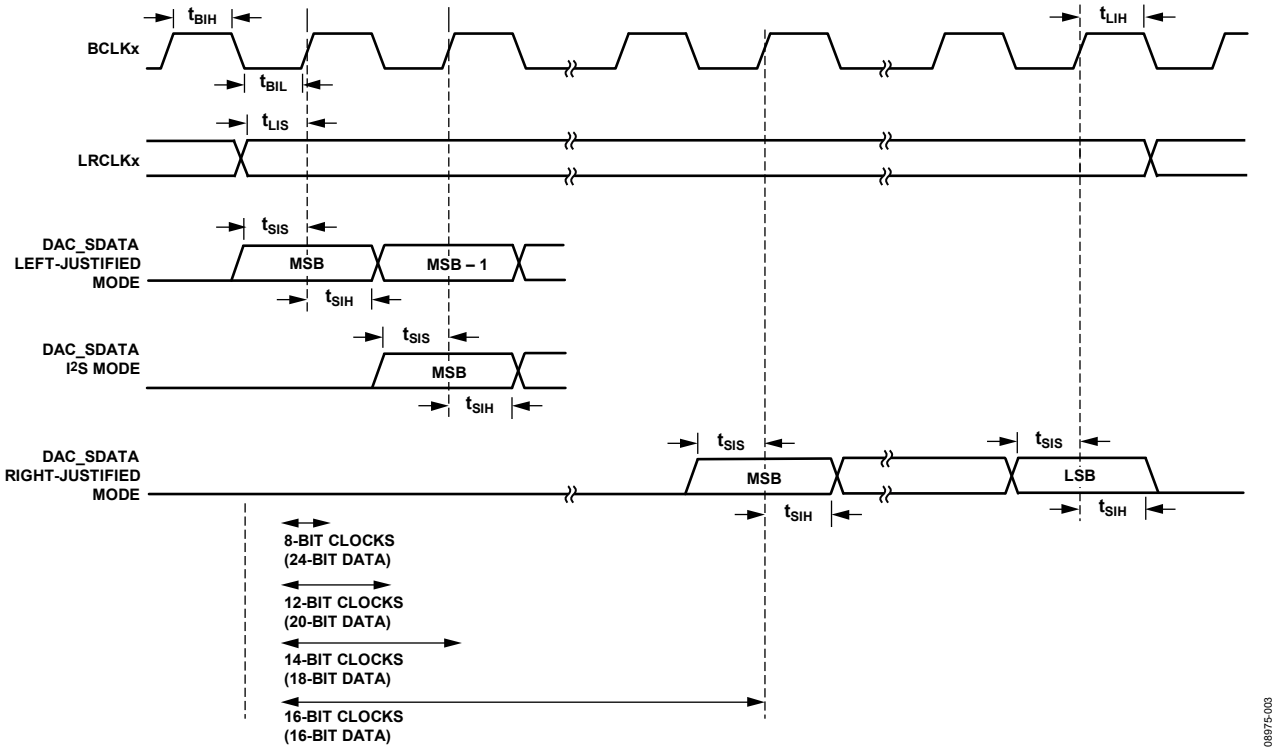


Figure 2. Serial Input Port Timing

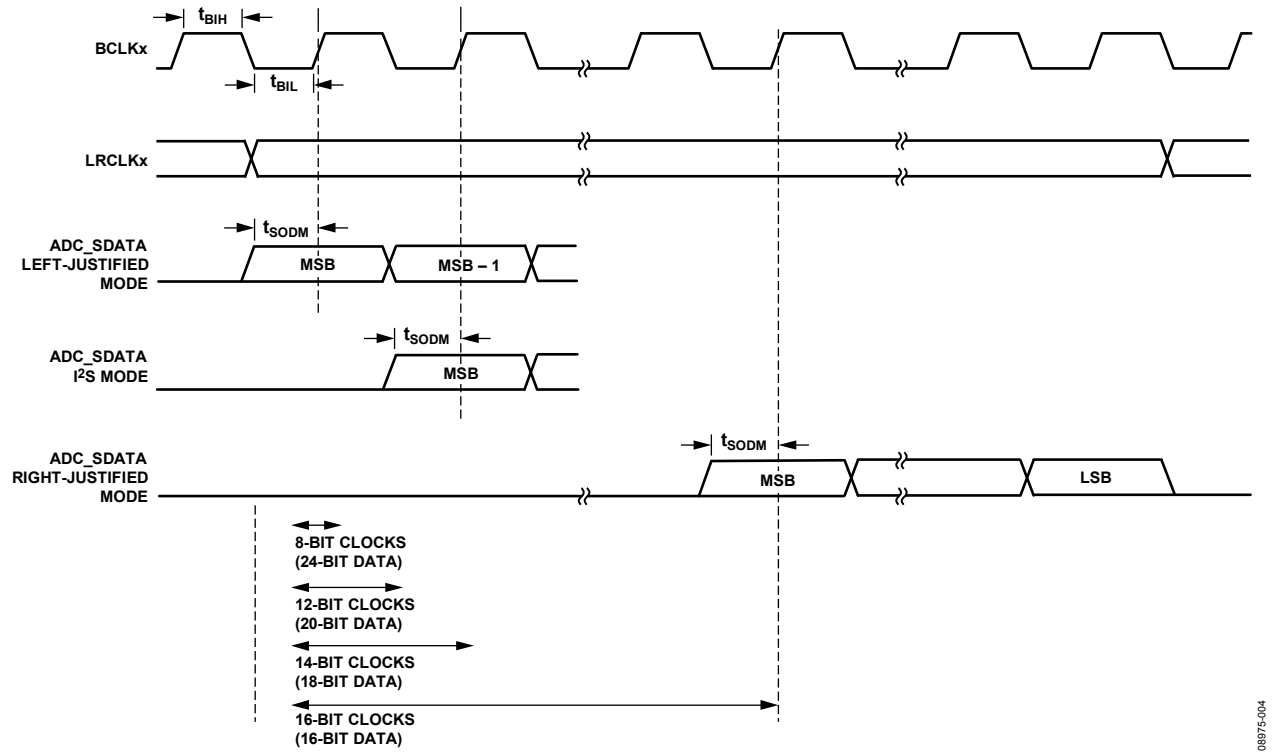


Figure 3. Serial Output Port Timing

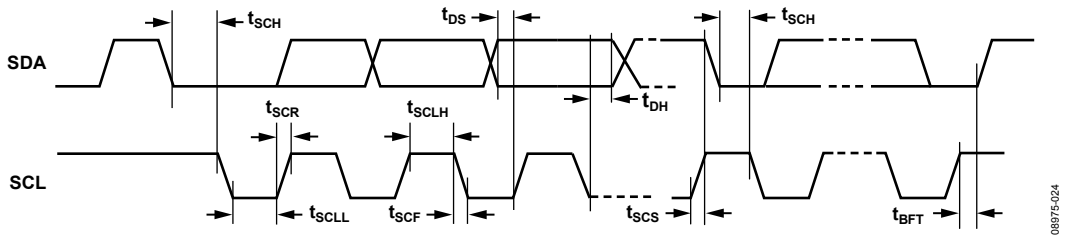


Figure 4. I²C Port Timing

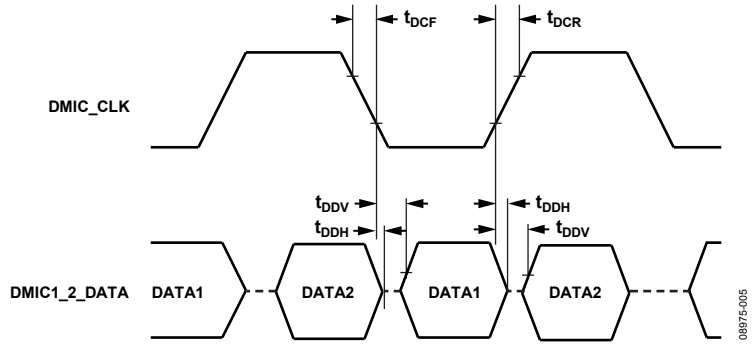


Figure 5. Digital Microphone Timing

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Power Supply	
SPKVDD, IOVDDx	−0.3 V to +5.5 V
DVDD, AVDD	−0.3 V to +1.98 V
HPVDD	−0.3 V to +1.98 V
Analog Input Voltage (Signal Pins)	
AIN4R/AIN4N, AIN3R/AIN3N, AIN2R/AIN2N, AIN1R/AIN1N, AIN4L/AIN4P, AIN3L/AIN3P, AIN2L/AIN4P, AIN1L/AIN1P	−0.3 V to AVDD + 0.3 V
Digital Input Voltage (Signal Pins)	
MCLK1, BCLKA, LRCLKA, SDATAINA, GPIO1	−0.3 V to IOVDD1 + 0.3 V
MCLK2, BCLKB, LRCLKB, SDATAINB, GPIO2	−0.3 V to IOVDD2 + 0.3 V
BCLKC, LRCLKC, SDATAINC, GPIO3	−0.3 V to IOVDD3 + 0.3 V
DMIC1_2_DATA, DMIC3_4_DATA, DMIC_CLK	−0.3 V to IOVDD4 + 0.3 V
SDA, SCL, GPIO4, MODE, ADDR, $\overline{SD}$	−0.3 V to IOVDD5 + 0.3 V
Temperature	
Operating Range	−40°C to +85°C
Storage Range	−65°C to +150°C
Junction Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 8. Thermal Resistance

Package Type	θ_{JA}	Unit
81-Lead, 4.0 mm × 3.8 mm WLCSP[1]	30	°C/W

[1] Applicable for a 4-layer board. For more information on the WLCSP, see the AN-617 Application Note, *MicroCSP Wafer Level Chip Scale Package*.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

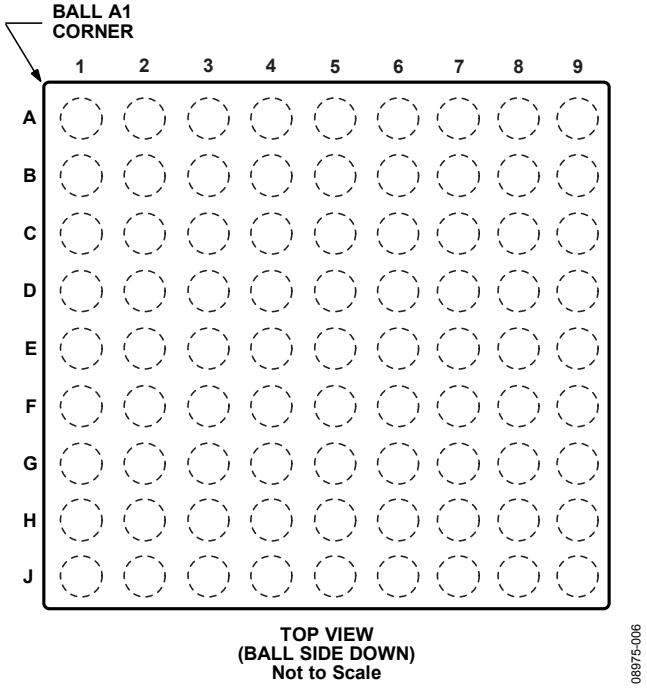


Figure 6. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
A1	DGND	PWR	Digital Ground. The AGND and DGND pins must be tied directly together in a common ground plane.
A2	MODE	D_IN	Mode Select I²C Operation. Must be pulled low for I²C mode.
A3	IOVDD4	PWR	Supply for Digital Microphone Input Port. Set IOVDD4 between 1.8 V and 3.3 V and decouple to DGND using a 100 nF capacitor.
A4	DMIC_CLK	D_OUT	Clock Output for Digital Microphone.
A5	AIN4R/AIN4N	A_IN	Right Channel Input 4 (AIN4R)/Inverting Input 4 (AIN4N).
A6	AIN3R/AIN3N	A_IN	Right Channel Input 3 (AIN3R)/Inverting Input 3 (AIN3N).
A7	AIN2R/AIN2N	A_IN	Right Channel Input 2 (AIN2R)/Inverting Input 2 (AIN2N).
A8	AIN1R/AIN1N	A_IN	Right Channel Input 1 (AIN1R)/Inverting Input 1 (AIN1N).
A9	AVDD	PWR	1.5 V to 1.8 V Analog Supply for DAC and Microphone Bias. Decouple this pin to AGND using a 100 nF capacitor.
B1	DVDD	PWR	Digital Core Supply. Decouple this pin to DGND with a 100 nF capacitor.
B2	ADDR	D_IN	Address Setting Pin for I²C Port. Pull high/low to IOVDD4, using a resistor for the desired chip address.
B3	IOVDD5	PWR	Supply for I²C Port. Set IOVDD5 between 1.8 V and 3.3 V and decouple to DGND using a 100 nF capacitor.
B4	DMIC1_2_DATA	D_IN	Serial Data Input Digital Microphone 1 and Serial Data Input Digital Microphone 2.
B5	AIN4L/AIN4P	A_IN	Left Channel Input 4 (AIN4L)/Noninverting Input 4 (AIN4P).
B6	AIN3L/AIN3P	A_IN	Left Channel Input 3 (AIN3L)/Noninverting Input 3 (AIN3P).
B7	AIN2L/AIN2P	A_IN	Left Channel Input 2 (AIN2L)/Noninverting Input 2 (AIN2P).
B8	AIN1L/AIN1P	A_IN	Left Channel Input 1 (AIN1L)/Noninverting Input 1 (AIN1P).
B9	CM	A_OUT	AVDD/2 V Common-Mode Reference. Connect a 1 µF ceramic decoupling capacitor between this pin and ground to reduce crosstalk between the ADCs and DACs. This pin can be used to bias external analog circuits, as long as they are not drawing current from CM (for example, the noninverting input of an op amp).

Pin No.	Mnemonic	Type	Description
C1	IOVDD1	PWR	Supply for Digital Audio Input/Output Interface A. Set IOVDD1 between 1.8 V and 3.3 V. Decouple this pin to DGND with a 100 nF capacitor.
C2	MCLK1	D_IN	External Master Clock Input 1 (8 kHz to 27 MHz).
C3	SDA	D_I/O	Serial Data for I²C. This pin is a bidirectional open drain and must be pulled up to IOVDD5 with a resistor.
C4	GPIO4	D_I/O	General-Purpose Input/Output 4.
C5	SCL	D_IN	Serial Clock for I²C Port. This pin is input only and must be pulled up to IOVDD5 with a resistor.
C6	DMIC3_4_DATA	D_IN	Serial Data Input Digital Microphone 3 and Serial Data Input Digital Microphone 4.
C7	LOUT1L/LOUTLP	A_OUT	Left Channel Line Output 1, Single-Ended Mode (LOUT1L)/Noninverting Left Channel Line Output, Differential Mode (LOUTLP).
C8	MICBIAS1	A_OUT	Bias Voltage for Electret Microphone 1.
C9	MICBIAS2	A_OUT	Bias Voltage for Electret Microphone 2.
D1	MCLK2	D_IN	External Master Clock Input 2 (8 kHz to 27 MHz).
D2	BCLKA	D_I/O	Serial Bit Clock, Digital Audio Interface A.
D3	LRCLKA	D_I/O	Frame Clock, Digital Audio Interface A.
D4	SDATAOUTA	D_OUT	Serial Data Output, Digital Audio Interface A.
D5	SDATAINA	D_IN	Serial Data Input, Digital Audio Interface A.
D6	GPIO1	D_I/O	General-Purpose Input/Output 1.
D7	LOUT1R/LOUTRP	A_OUT	Right Channel Line Output 1, Single-Ended Mode (LOUT1R)/Noninverting Right Channel Line Output, Differential Mode (LOUTRP).
D8	LOUT2L/LOUTLN	A_OUT	Left Channel Line Output 2, Single-Ended Mode (LOUT2L)/Inverting Left Channel Line Output, Differential Mode (LOUTLN).
D9	LOUT2R/LOUTRN	A_OUT	Right Channel Line Output 2, Single-Ended Mode (LOUT2R)/Inverting Right Channel Line Output, Differential Mode (LOUTRN).
E1	IOVDD3	PWR	Supply for Digital Audio Input/Output Interface C. Set IOVDD3 between 1.8 V and 3.3 V and decouple to DGND with a 100 nF capacitor.
E2	LRCLKB	D_I/O	Frame Clock, Digital Audio Interface B.
E3	SDATAOUTB	D_OUT	Serial Data Output, Digital Audio Interface B.
E4	BCLKB	D_I/O	Serial Bit Clock, Digital Audio Interface B.
E5	DGND	PWR	Digital Ground. The AGND and DGND pins must be tied directly together in a common ground plane.
E6	GPIO2	D_I/O	General-Purpose Input/Output 2.
E7	LN1FBIN	A_IN	Line Output Amplifier 1 Feedback. This pin can be used to sense the ground noise at the line output jack; use a 2.2 µF capacitor to connect this pin to AGND at the line output jack.
E8	LN2FBIN	A_IN	Line Output Amplifier 2 Feedback. This pin can be used to sense the ground noise at the line output jack; use a 2.2 µF capacitor to connect this pin to AGND at the line output jack.
E9	AVDD	PWR	1.5 V to 1.8 V Analog Supply for DAC and Microphone Bias. Decouple this pin to AGND with a 100 nF capacitor in parallel with a 10 µF capacitor.
F1	LRCLKC	D_I/O	Frame Clock, Digital Audio Interface C.
F2	BCLKC	D_I/O	Serial Bit Clock, Digital Audio Interface C.
F3	SDATAINC	D_IN	Serial Data Input, Digital Audio Interface C.
F4	IOVDD2	PWR	Supply for Digital Audio Input/Output Interface B. Set IOVDD2 between 1.8 V and 3.3 V and decouple to DGND with a 100 nF capacitor.
F5	GPIO3	D_I/O	General-Purpose Input/Output 3.
F6	SDATAINB	D_IN	Serial Data Input, Digital Audio Interface B.
F7, F8	AGND	PWR	Analog Ground.
F9	RESERVED	A_IN	Reserved for Internal Use. Do not connect.
G1, G2	SPKVDD	PWR	Supply for Speaker Class-D Amplifier.
G3	SDATAOUTC	D_OUT	Serial Data Output, Digital Audio Interface C.
G4	RESERVED	D_IN	Reserved. Connect to DGND.
G5	JACKDET	D_IN	TLL-Compatible Logic Input. Detects insertion/removal of headphone plug.
G6	$\overline{SD}$	D_IN	Shutdown Control. Set high for normal operation; set low for full chip power-down.
G7	SGND	A_IN	Headphone Signal Return Sense. Connect directly to headphone socket ground for lowest dc offset.
G8	HPL	A_OUT	Left Headphone Output.
G9	HPR	A_OUT	Right Headphone Output.

Pin No.	Mnemonic	Type	Description
H1	SPKRN	A_OUT	Right Channel Speaker Output, Negative.
H2, H3	SPKVDD	PWR	Supply for Speaker Amplifier.
H4, H5	SPKGND	PWR	Ground for Speaker Amplifier.
H6	EPP	A_OUT	Earpiece Amplifier Output, Positive.
H7	CPVSS	PWR	Headphone Amplifier Charge Pump, Negative Supply Output. Decouple this pin to HPGND with a 1 µF MLCC X7R capacitor.
H8	HPVDD	PWR	1.62 V to 2 V Supply for Headphone Amplifier Charge Pump. Decouple this pin to AGND with a 1 µF capacitor.
H9	CPVDD	PWR	Headphone Amplifier Charge Pump, Positive Supply Output. Decouple this pin to HPGND with a 1 µF MLCC X7R capacitor.
J1	SPKGND	PWR	Ground for Speaker Amplifier.
J2	SPKRP	A_OUT	Right Channel Speaker Output, Positive.
J3	SPKLN	A_OUT	Left Channel Speaker Output, Negative.
J4	SPKLP	A_OUT	Left Channel Speaker Output, Positive.
J5	SPKGND	PWR	Ground for Speaker Amplifier.
J6	EPN	A_OUT	Earpiece Amplifier Output, Negative.
J7	CF2	PWR	Charge Pump Flying Capacitor Connection 2.
J8	HPGND	PWR	Charge Pump Ground.
J9	CF1	PWR	Charge Pump Flying Capacitor Connection 1.

TYPICAL PERFORMANCE CHARACTERISTICS

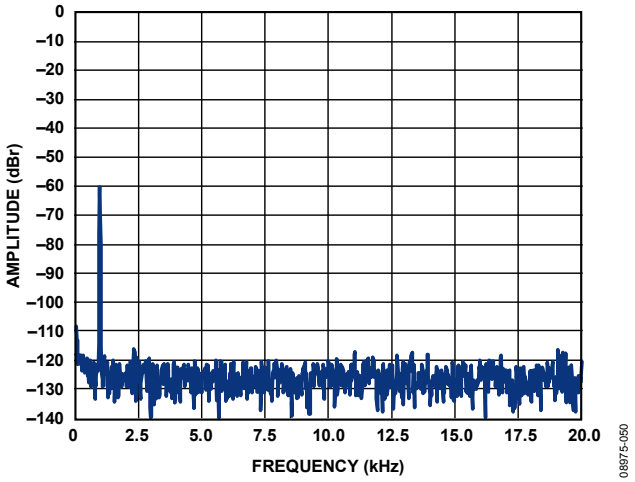


Figure 7. FFT, –60 dBFS, Analog In → Line Out

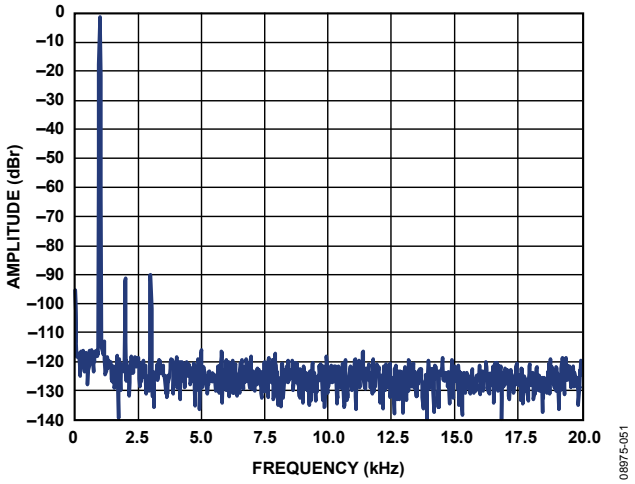


Figure 8. FFT, –1 dBFS, Analog In → Line Out

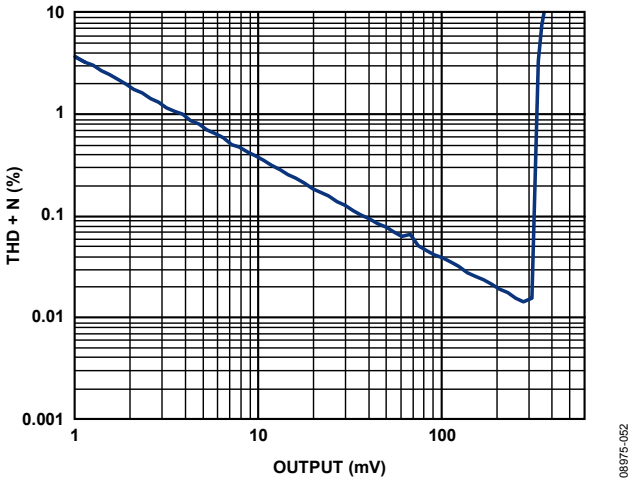


Figure 9. THD + N vs. Output Level, Analog In → Line Out

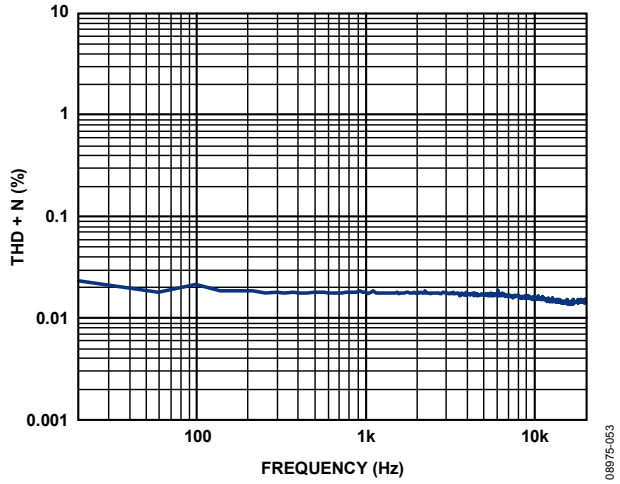


Figure 10. THD + N vs. Frequency, –20 dBFS, Analog In → Line Out

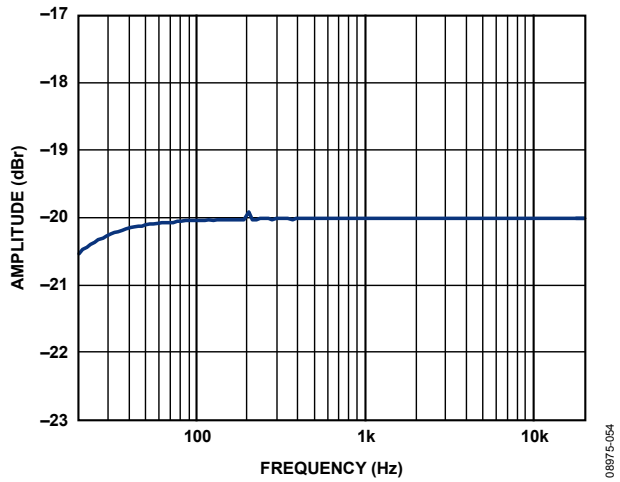


Figure 11. Frequency Response, –20 dBFS, Analog In → Line Out

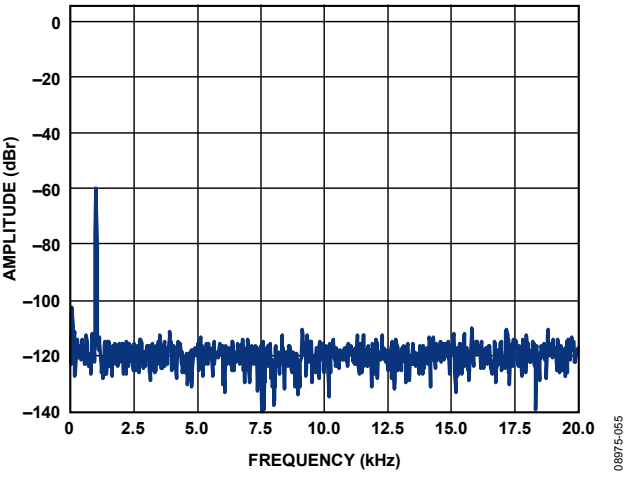


Figure 12. FFT, –60 dBFS, Analog In → Speaker Out

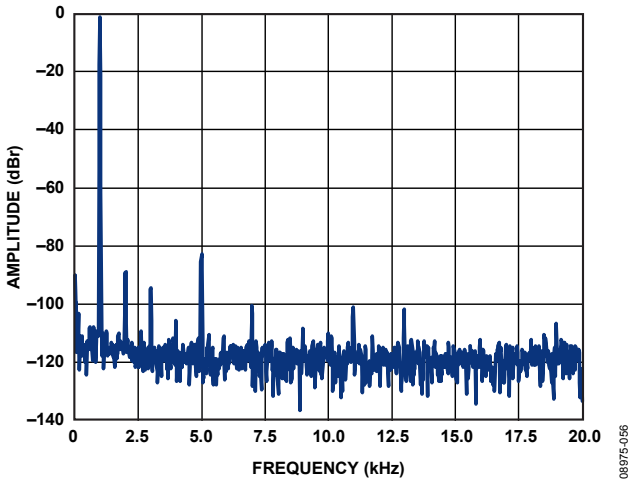


Figure 13. FFT, −1 dBFS, Analog In → Speaker Out

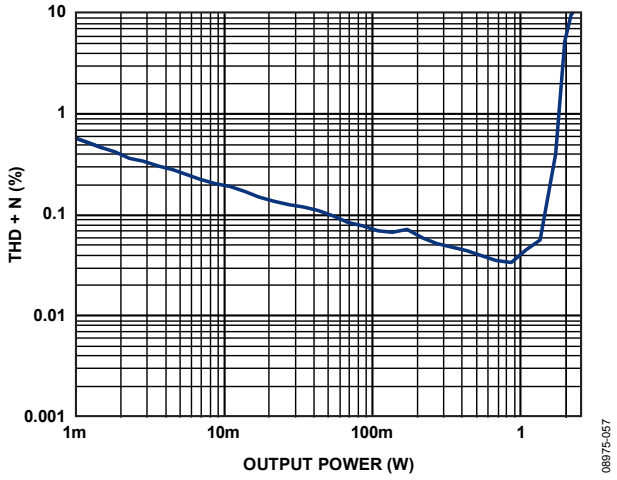


Figure 14. THD + N vs. Output Power, 4 Ω + 15 µH, Analog In → Speaker Out

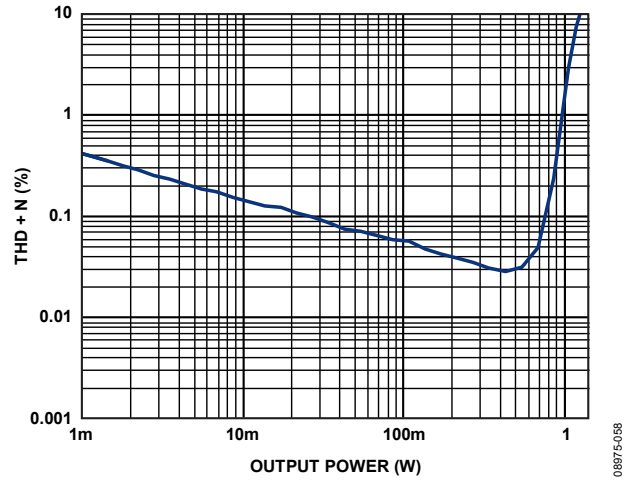


Figure 15. THD + N vs. Output Power, 8 Ω + 33 µH, Analog In → Speaker Out

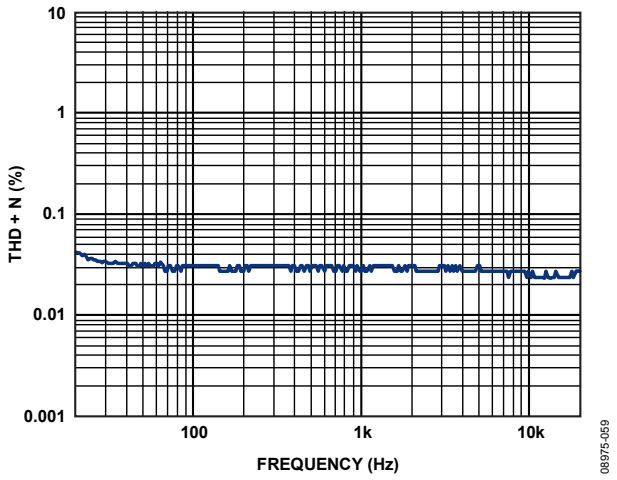


Figure 16. THD + N vs. Frequency, −20 dBFS, Analog In → Speaker Out

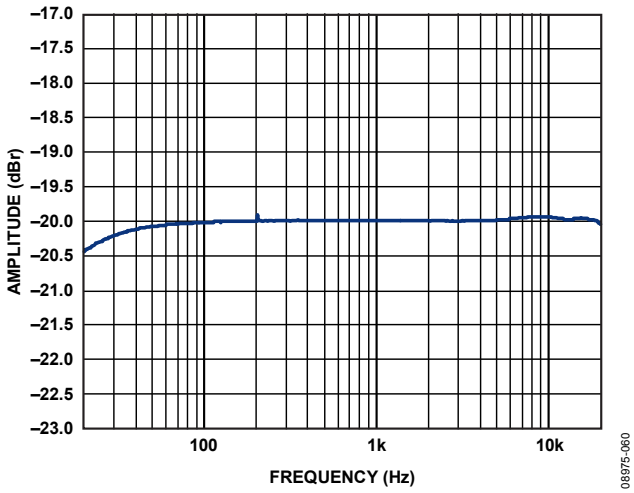


Figure 17. Frequency Response, 8 Ω + 33 µH, Analog In → Speaker Out

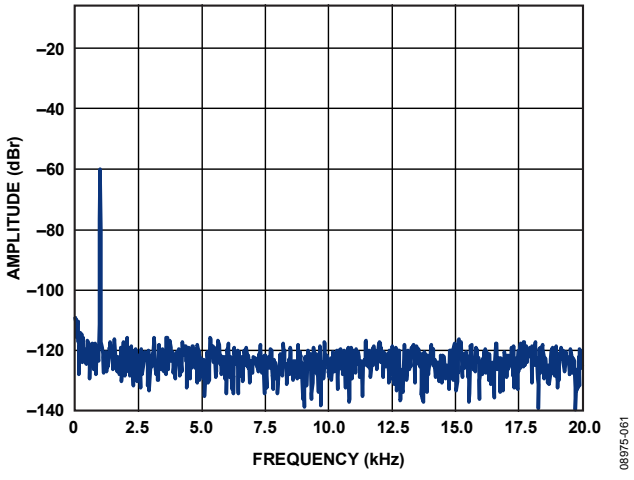


Figure 18. FFT, −60 dBFS, Analog In → Headphone Out

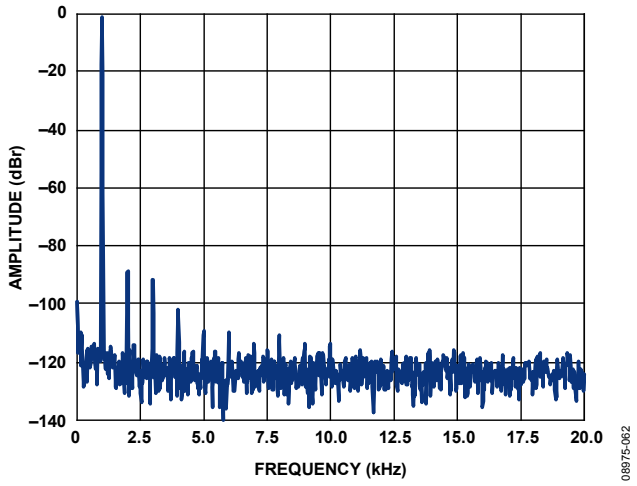


Figure 19. FFT, −1 dBFS, Analog In → Headphone Out

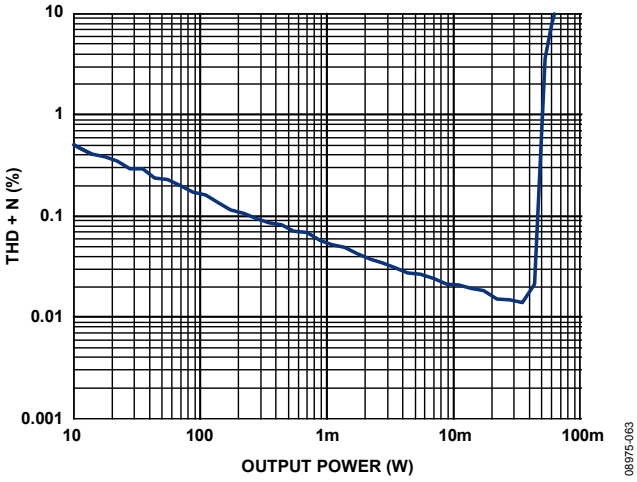


Figure 20. THD+N vs. Output Power, 16 Ω, Analog In → Headphone Out

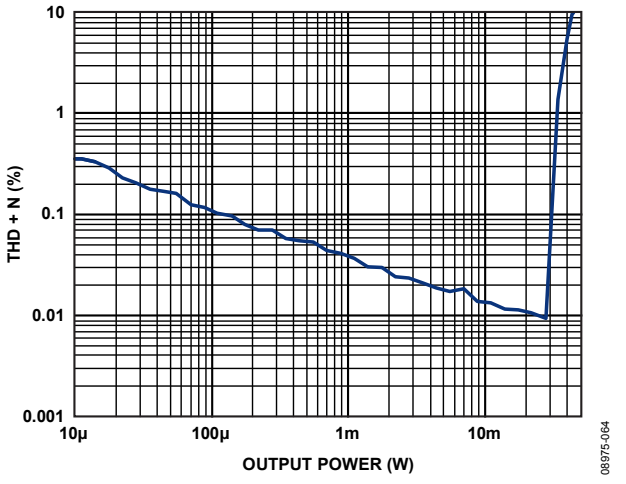


Figure 21. THD + N vs. Output Power, 32 Ω, Analog In → Headphone Out

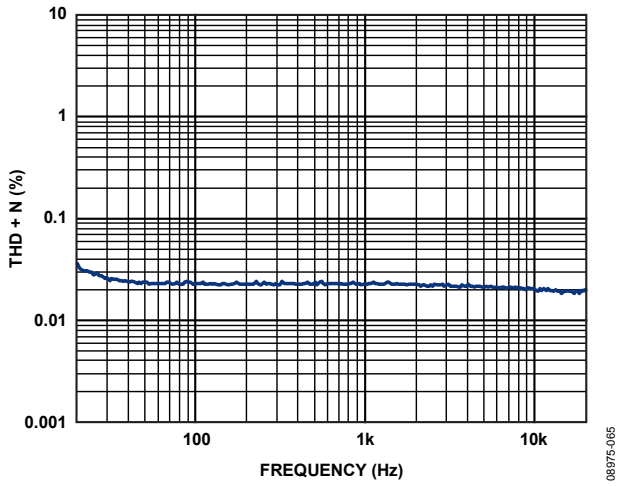


Figure 22. THD + N vs. Frequency, −20 dBFS, 16 Ω, Analog In → Headphone Out

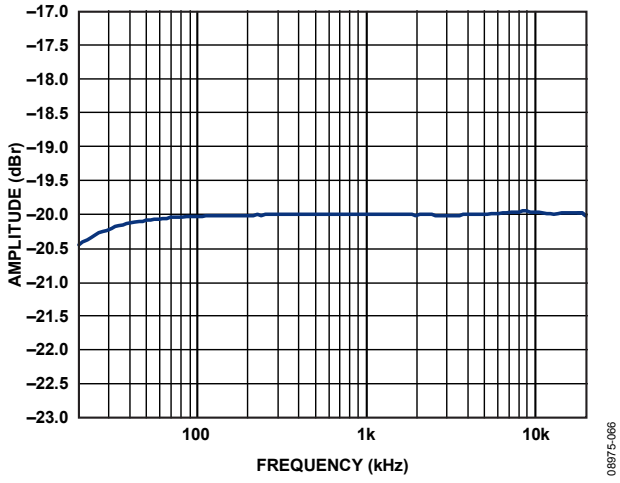


Figure 23. Frequency Response, −20 dBFS, 16 Ω, Analog In → Headphone Out

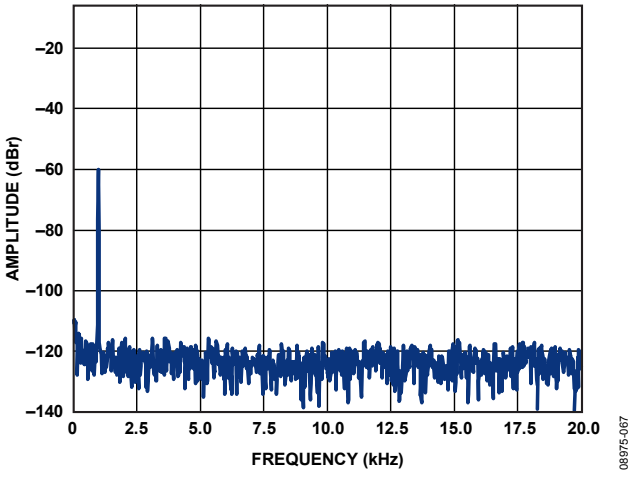


Figure 24. FFT, −60 dBFS, Analog In → Earpiece Out

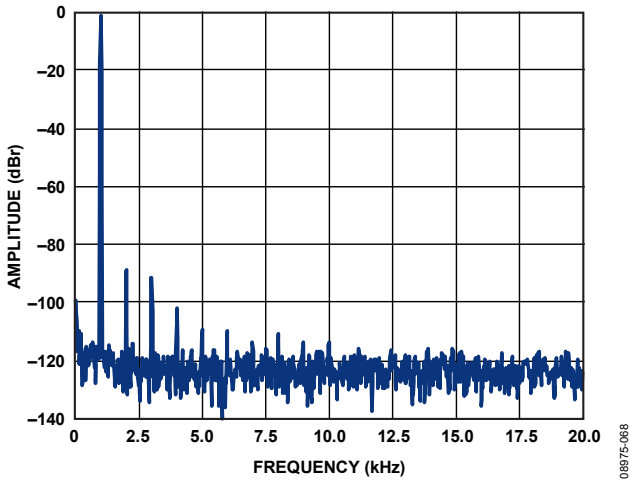


Figure 25. FFT, −1 dBFS, Digital Microphone In → Earpiece Out

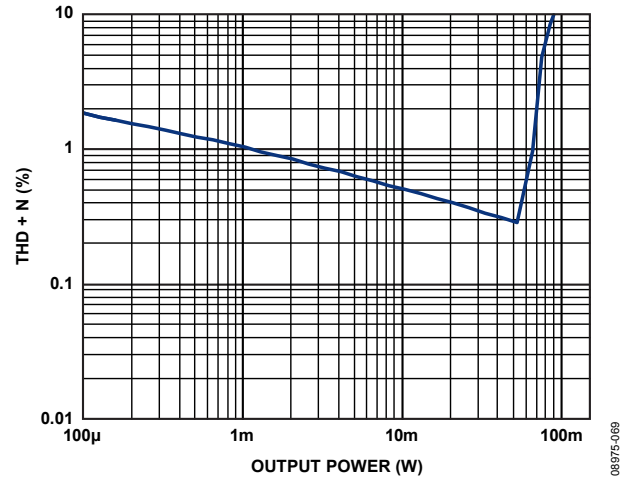


Figure 26. THD + N vs. Output Power, 32 Ω, Analog In → Earpiece Out

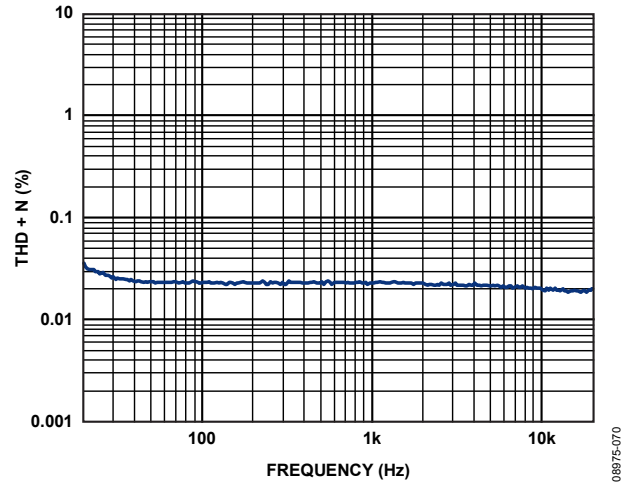


Figure 27. THD + N vs. Frequency, −20 dBFS, 32 Ω, Analog In → Earpiece Out

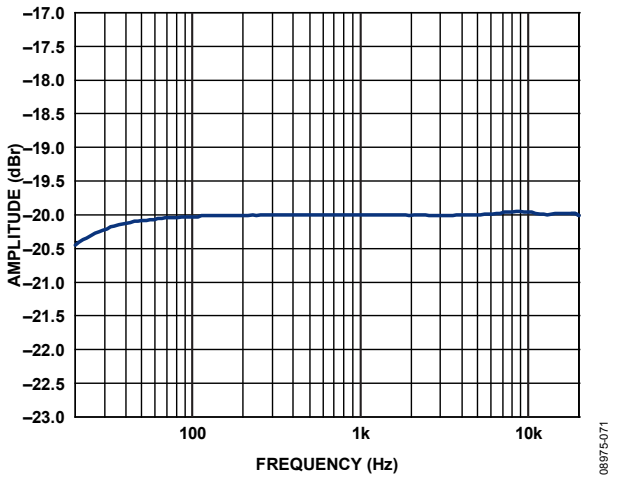


Figure 28. Frequency Response, 32 Ω, Analog In → Earpiece Out

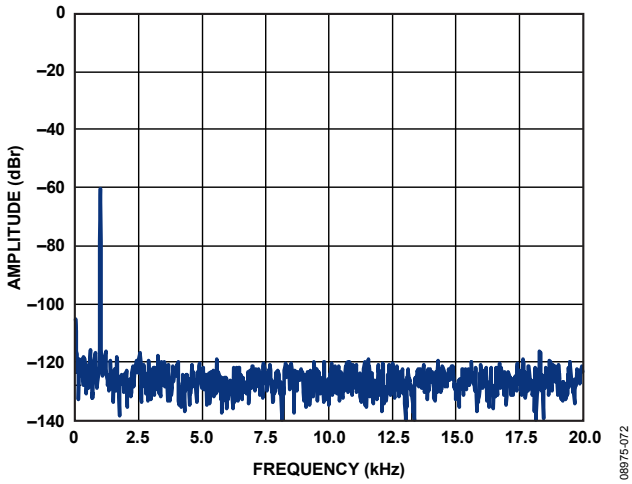


Figure 29. FFT, −60 dBFS, Digital In → Line Out

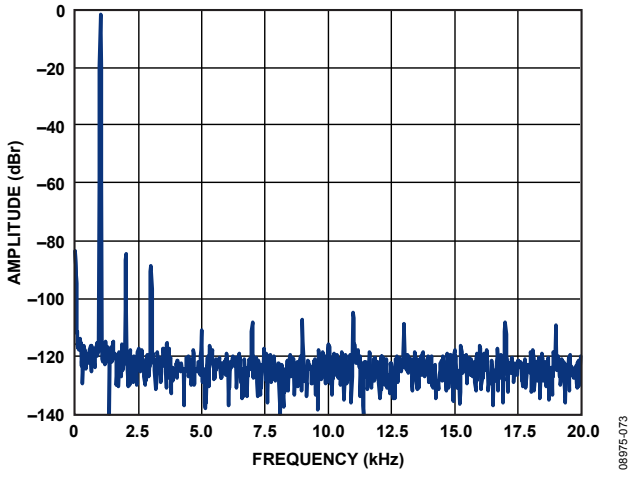


Figure 30. FFT, −1 dBFS, Digital In → Line Out

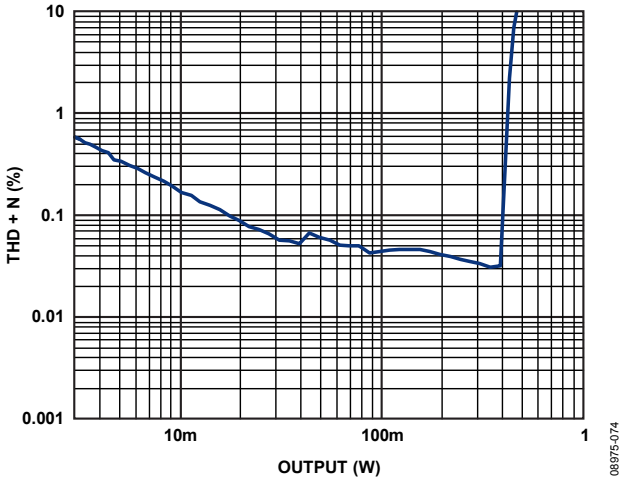


Figure 31. THD + N vs. Output Level, Digital In → Line Out

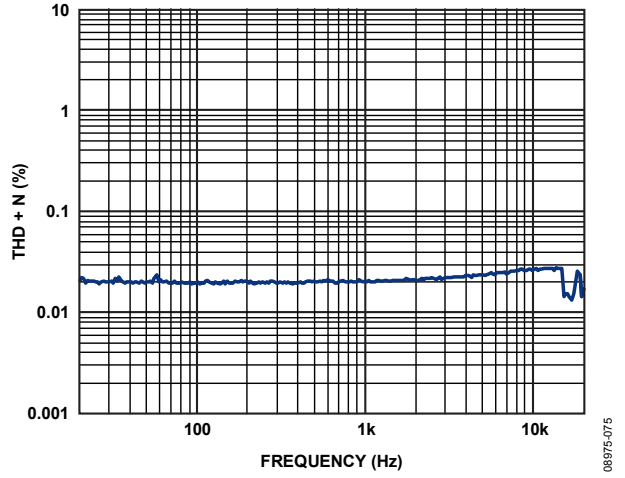


Figure 32. THD+N vs. Frequency, −20 dBFS, Digital In → Line Out

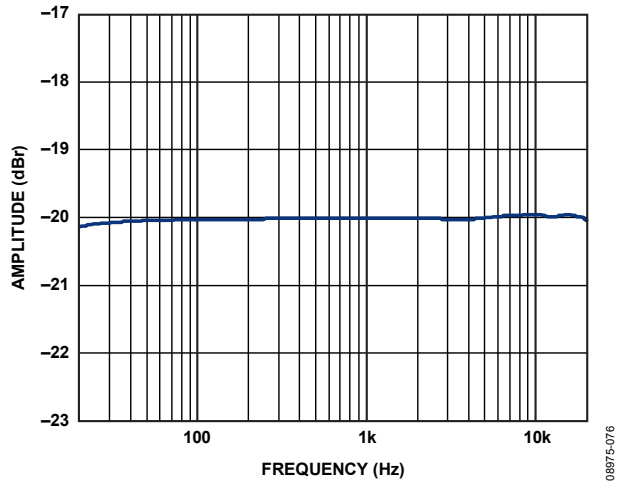


Figure 33. Frequency Response, −20 dBFS, Digital In → Line Out

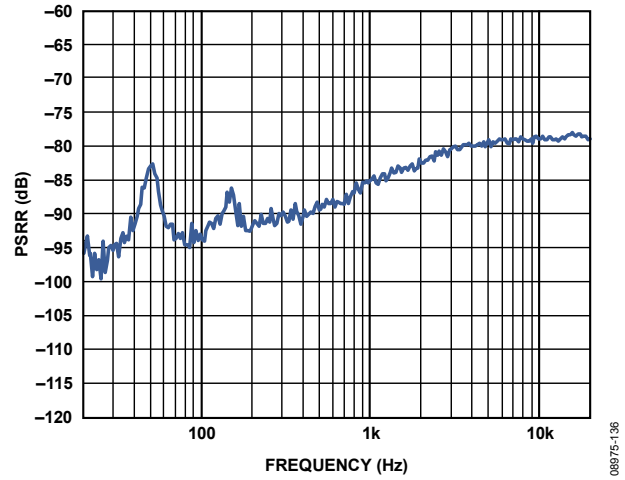


Figure 34. PSRR vs. Frequency Ripple on AVDD, Digital In → Line Out

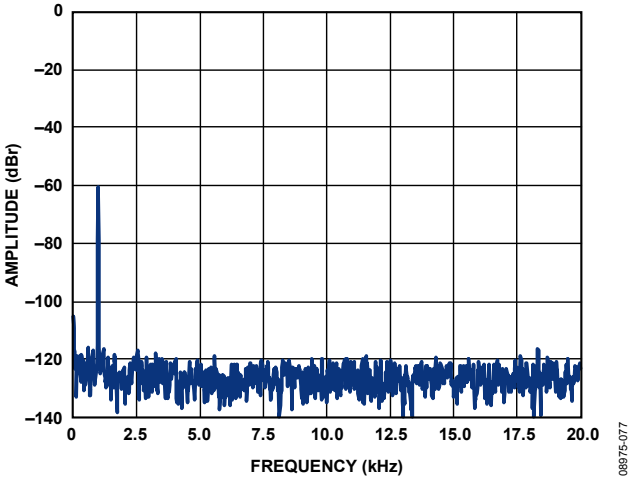


Figure 35. FFT, −60 dBFS, 8 Ω + 33 µH, Digital In → Speaker Out

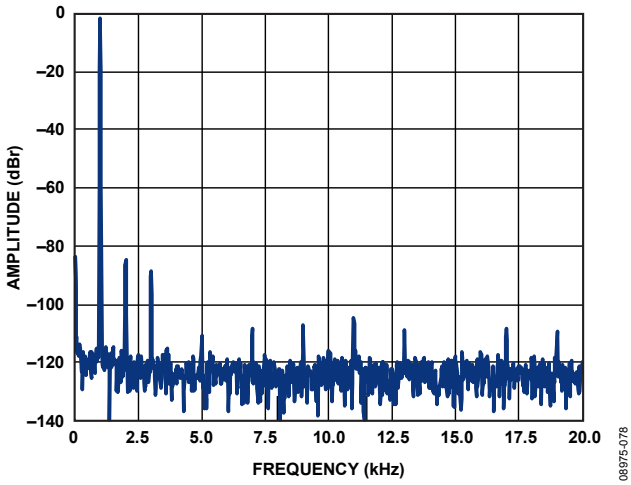


Figure 36. FFT, −1 dBFS, 8 Ω + 33 µH, Digital In → Speaker Out

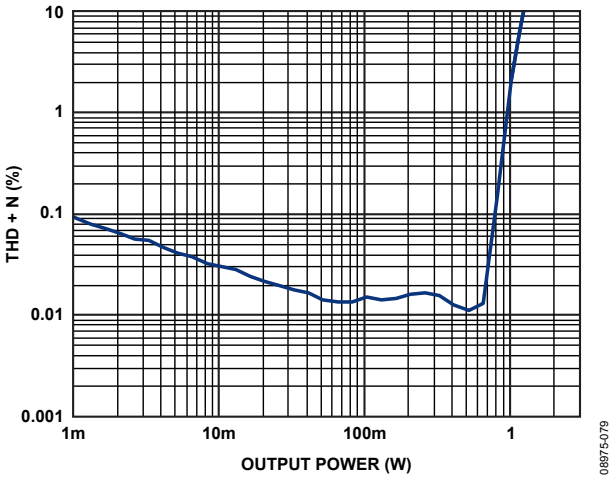


Figure 37. THD + N vs. Output Power, 8 Ω + 33 µH, Digital In → Speaker Out

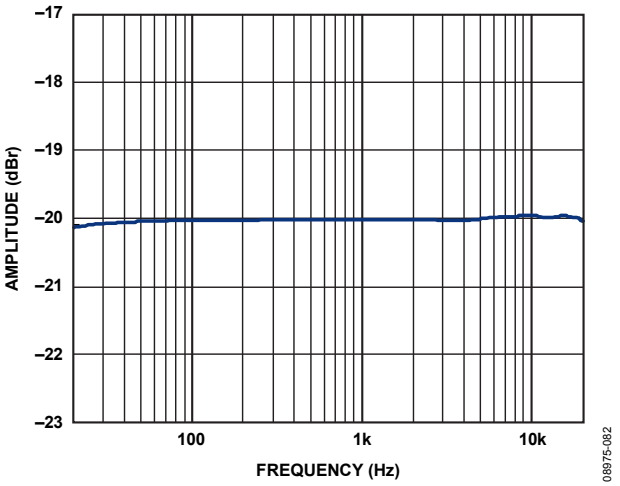


Figure 40. Frequency Response, 8 Ω + 33 µH, Digital In → Speaker Out

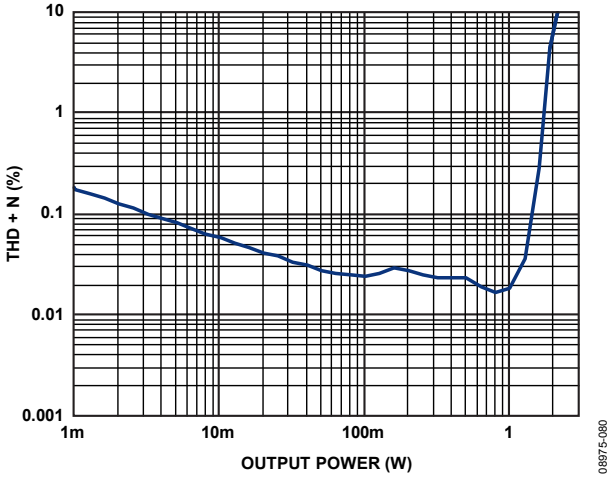


Figure 38. THD + N vs. Output Power, 4 Ω + 15 µH, Digital In → Speaker Out

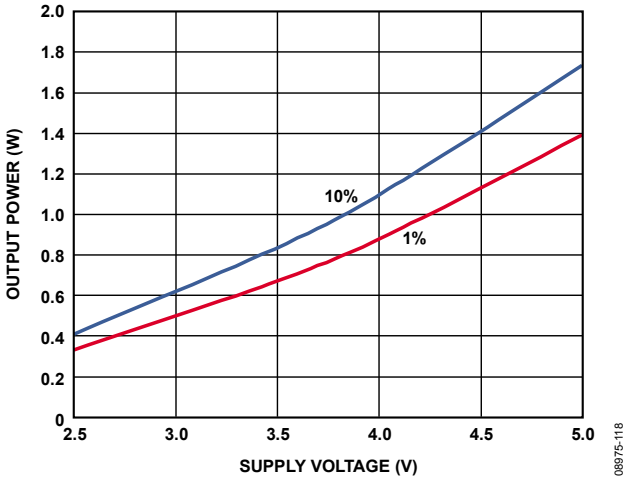


Figure 41. Output Power vs. SPKVDD, 8 Ω + 33 µH (Stereo), Digital In → Speaker Out

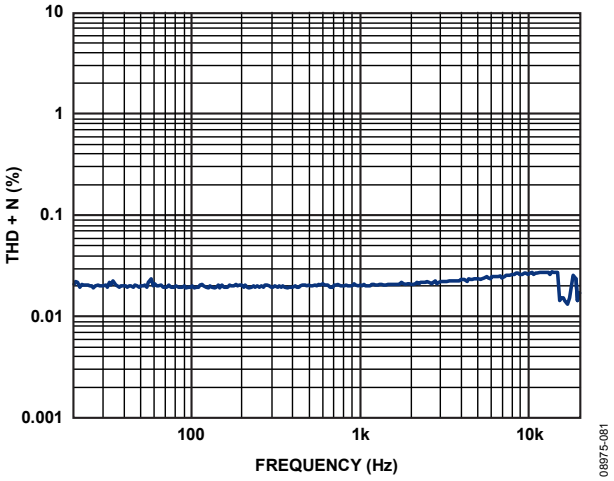


Figure 39. THD + N vs. Frequency, –20 dBFS, 8 Ω + 33 µH, Digital In → Speaker Out

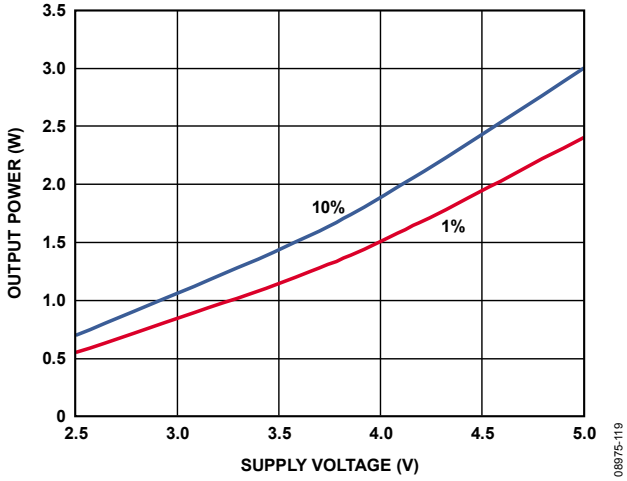


Figure 42. Output Power vs. SPKVDD, 4 Ω + 15 µH (Stereo), Digital In → Speaker Out

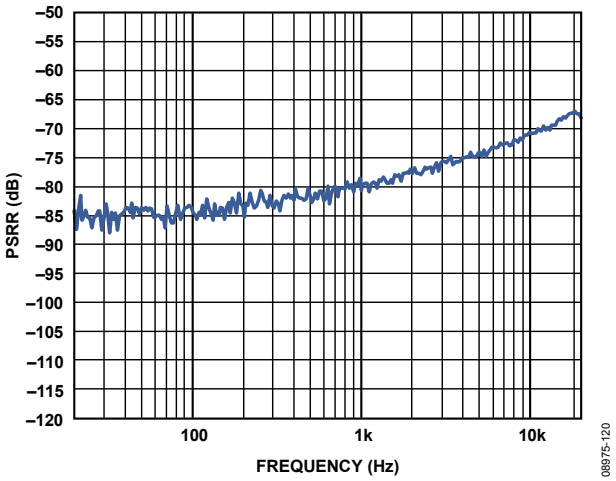


Figure 43. PSRR vs. Frequency Ripple on SPKVDD, 8 Ω + 33 µH, Digital In → Speaker Out

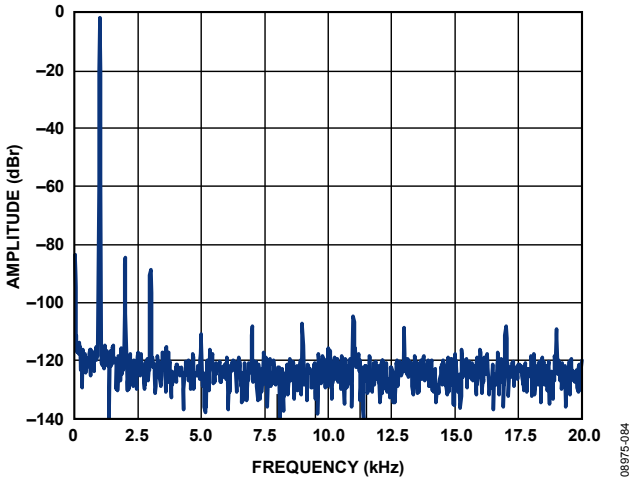


Figure 46. FFT, −1 dBFS, 16 Ω, Digital In → Headphone Out

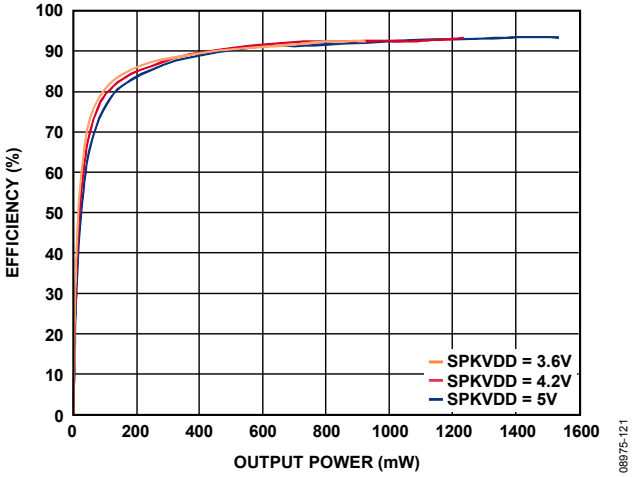


Figure 44. Efficiency vs. Output Power, 8 Ω + 33 µH, Digital In → Speaker Out

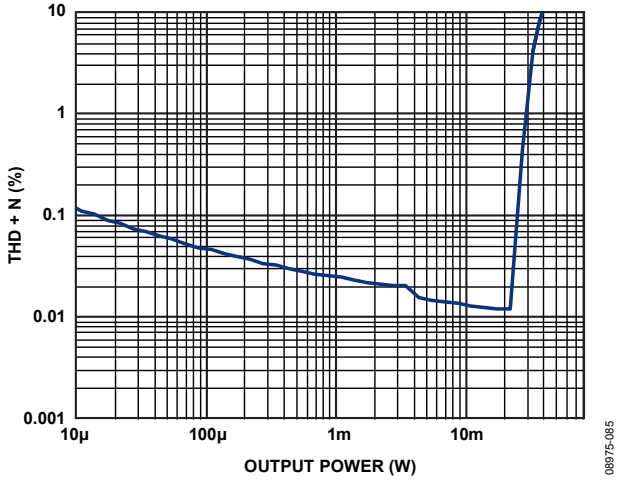


Figure 47. THD + N vs. Output Power, 16 Ω, Digital In → Headphone Out

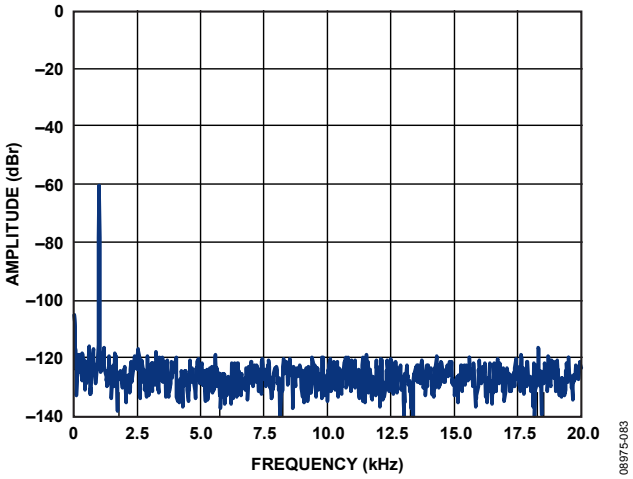


Figure 45. FFT, −60 dBFS, 16 Ω, Digital In → Headphone Out

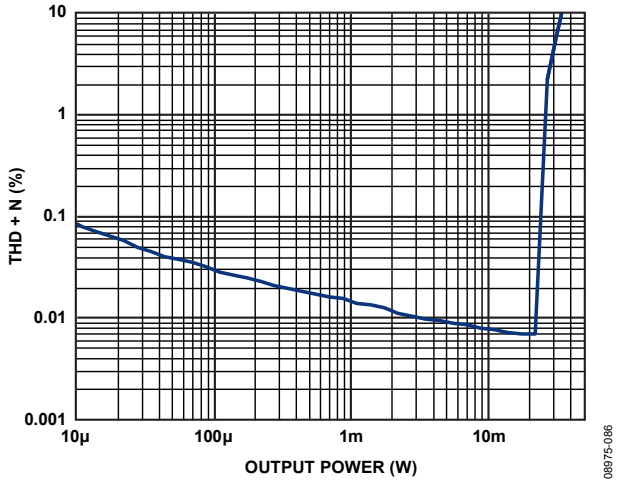


Figure 48. THD + N vs. Output Power, 32 Ω, Digital In → Headphone Out

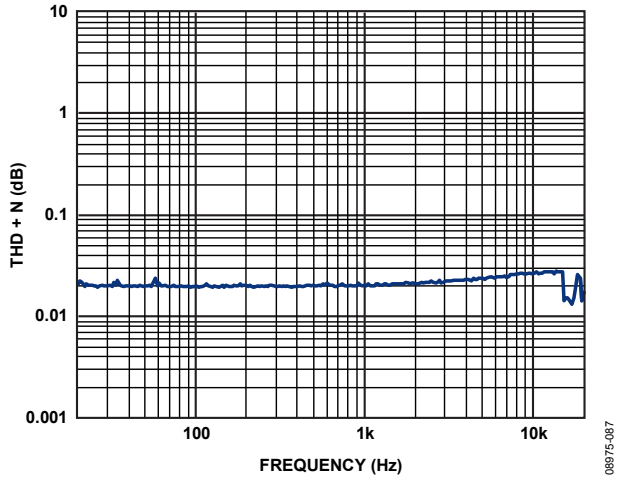


Figure 49. THD + N vs. Frequency, –20 dBFS,16 Ω, Digital In → Headphone Out

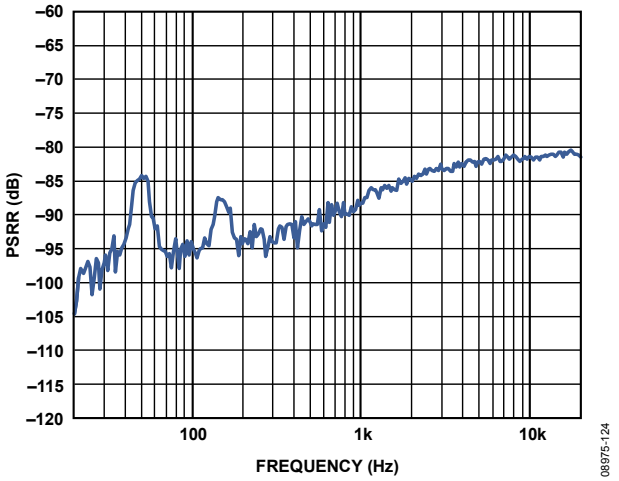


Figure 52. PSRR vs. Frequency, 16 Ω, Digital In → Headphone Out

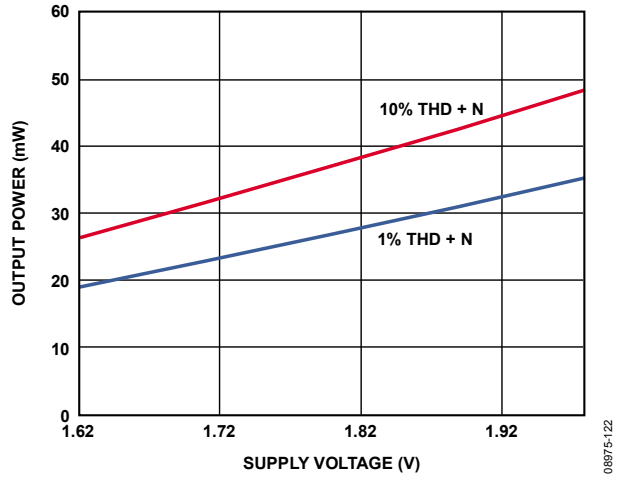


Figure 50. Output Power vs. HPVDD, 16 Ω, Digital In → Headphone Out

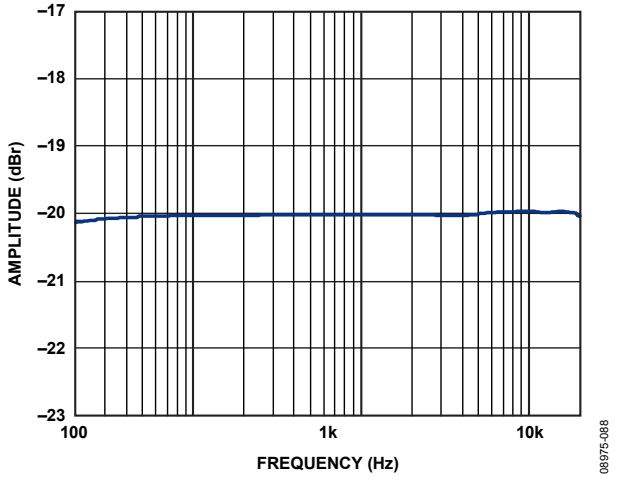


Figure 53. Frequency Response, –20 dBFS, 16 Ω, Digital In → Headphone Out

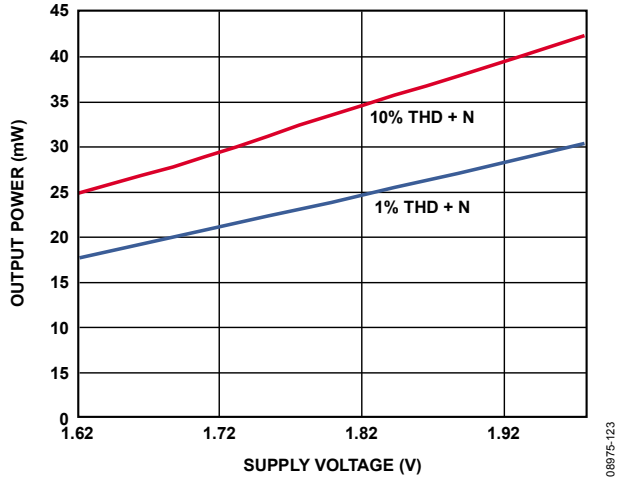


Figure 51. Output Power vs. HPVDD, 32 Ω, Digital In → Headphone Out

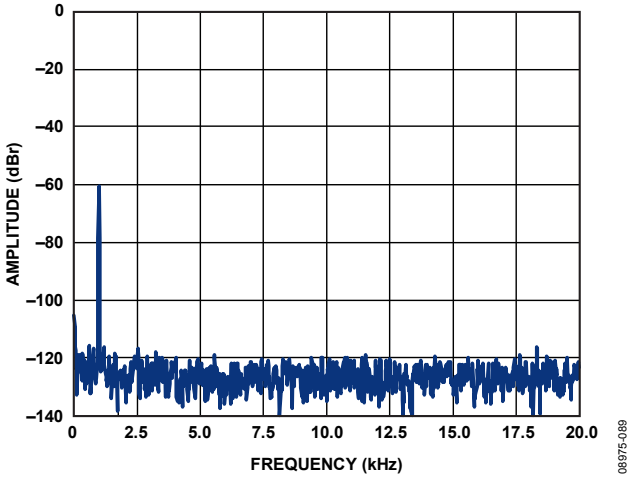


Figure 54. FFT, –60 dBFS, 32 Ω, Digital In → Earpiece Out

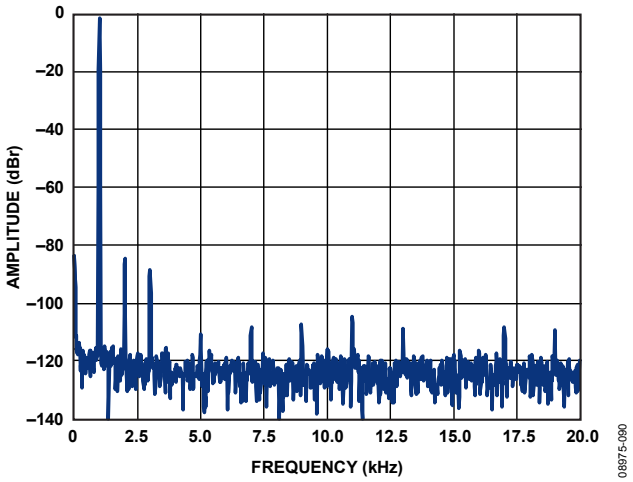


Figure 55. FFT, −1 dBFS, 32 Ω, Digital In → Earpiece Out

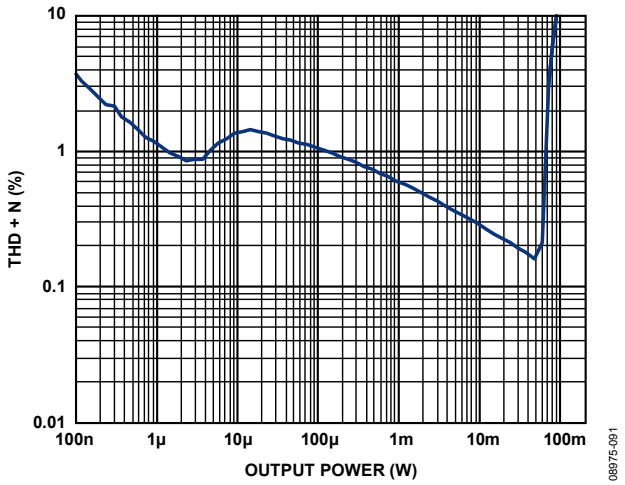


Figure 56. THD + N vs. Output Power, 32 Ω, Digital In → Earpiece Out

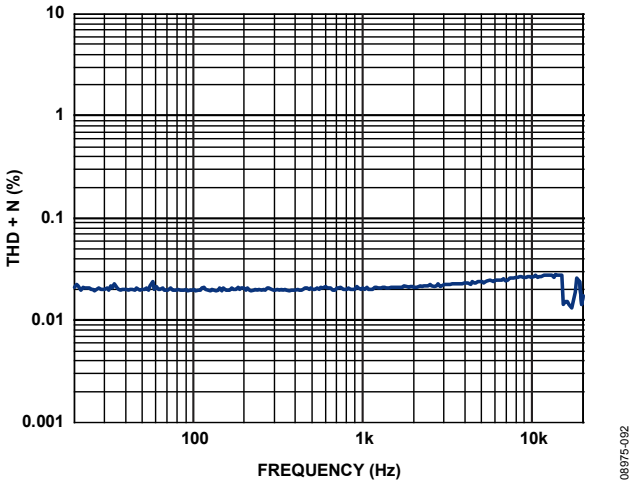


Figure 57. THD + N vs. Frequency, −20 dBFS, 32 Ω, Digital In → Earpiece Out

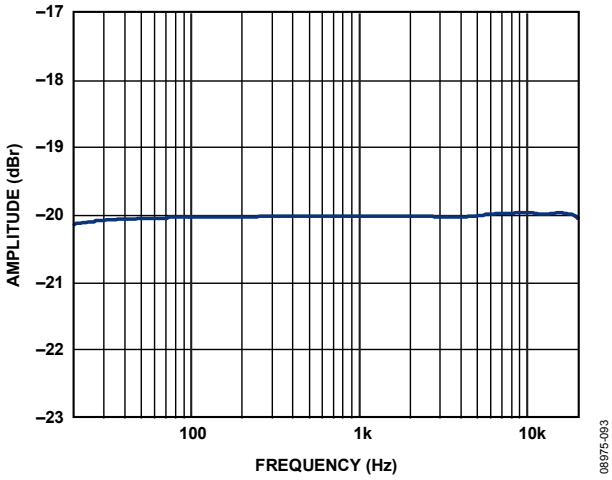


Figure 58. Frequency Response, 32 Ω, Digital In → Earpiece Out

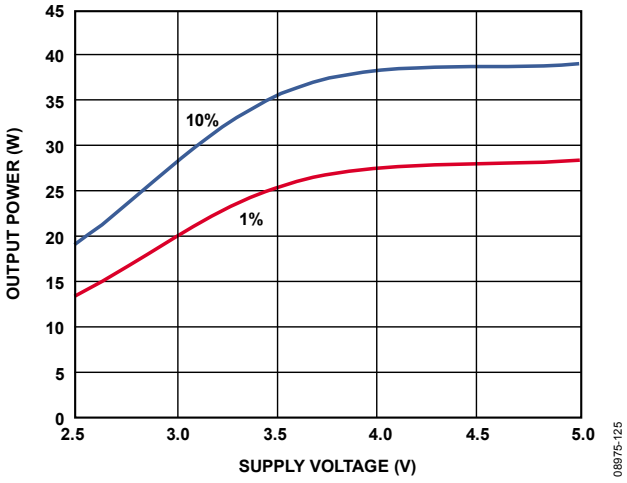


Figure 59. Output Power vs. SPKVDD, 32 Ω, Digital In → Earpiece Out

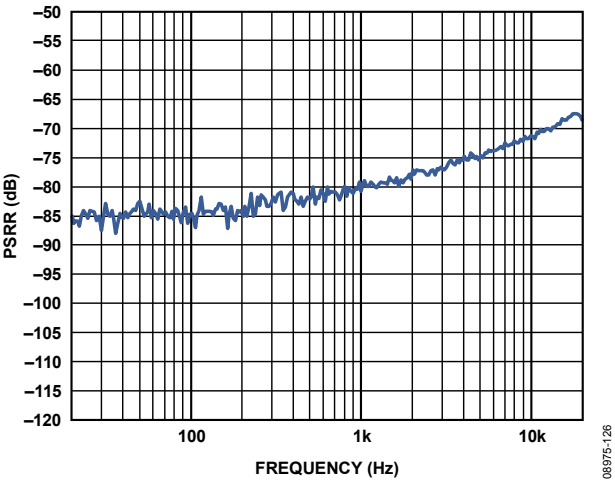


Figure 60. PSRR vs. Frequency, 32 Ω, Digital In → Earpiece Out

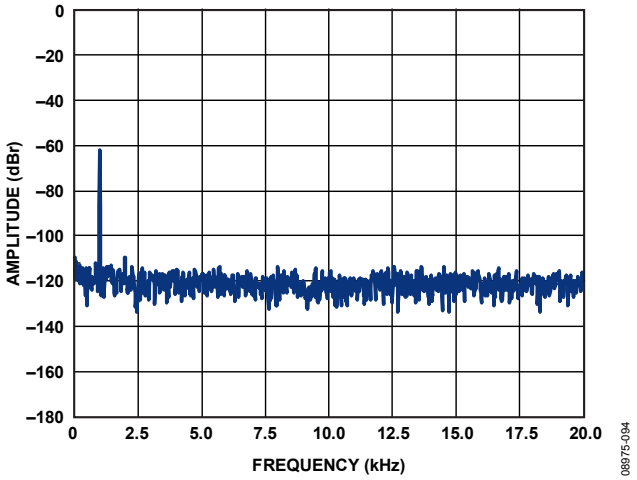


Figure 61. FFT, −60 dBFS, Analog In → Digital Out, PGA Gain = 0 dB

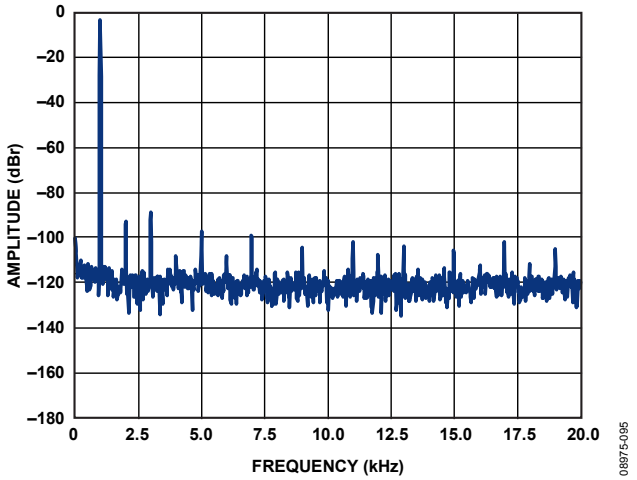


Figure 62. FFT, −1 dBFS, Analog In → Digital Out, PGA Gain = 0 dB

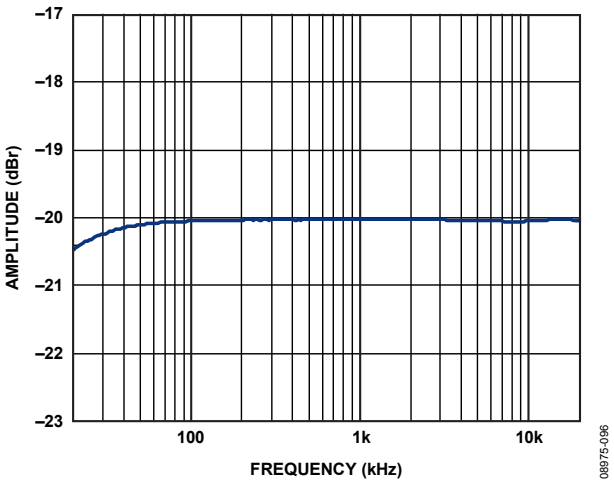


Figure 63. Frequency Response, −20 dBFS, Analog In → Digital Out, PGA Gain = 0 dB

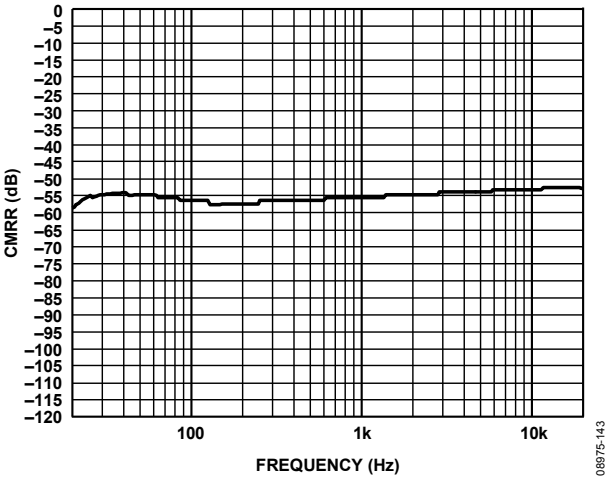


Figure 64. CMRR vs. Frequency, Analog In → Digital Out, PGA Gain = 0 dB

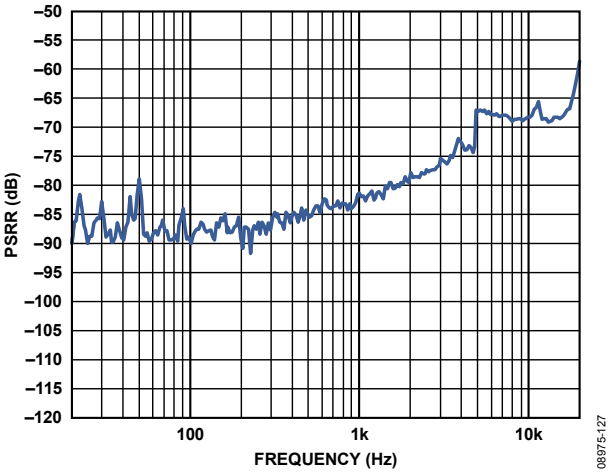


Figure 65. PSRR vs. Frequency Ripple on AVDD, Analog In → Digital Out, PGA Gain = 0 dB

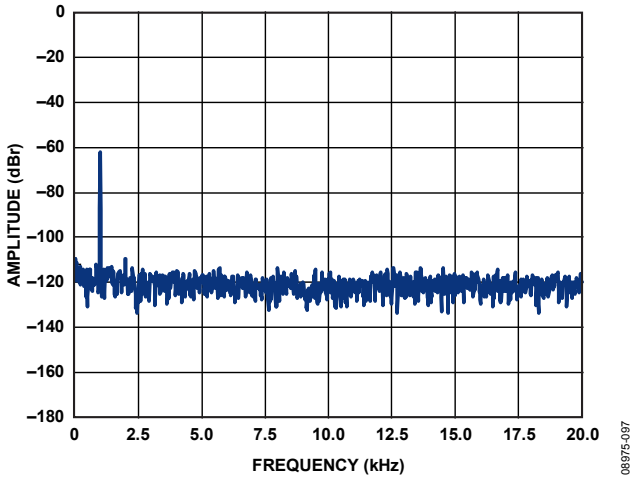


Figure 66. FFT, −60 dBFS, Digital In → Digital Out

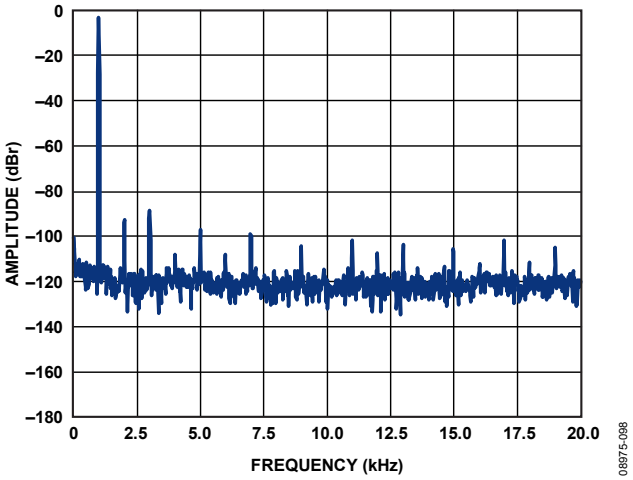


Figure 67. FFT, −1 dBFS, Digital In → Digital Out

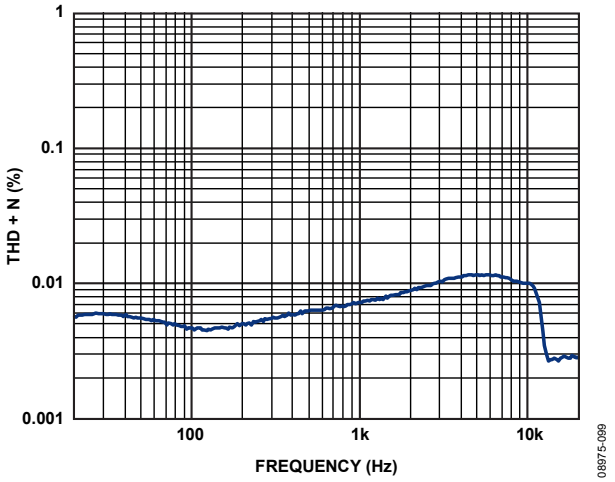


Figure 68. THD + N vs. Frequency, 0 dBFS, Digital In → Digital Out

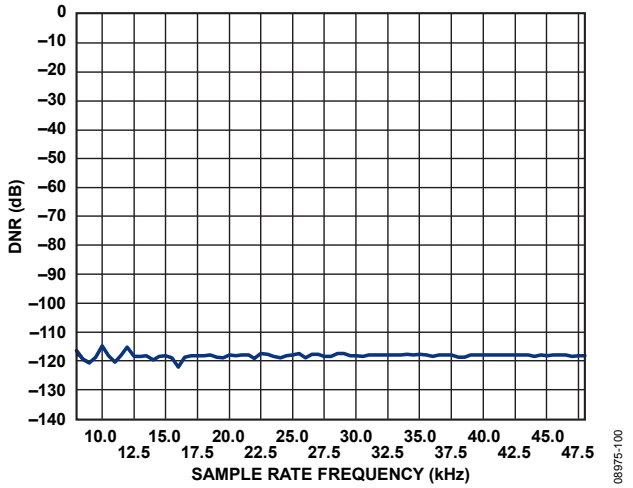


Figure 69. DNR vs. f_S Out Sample Rate, f_S In = 8 kHz, ASRC

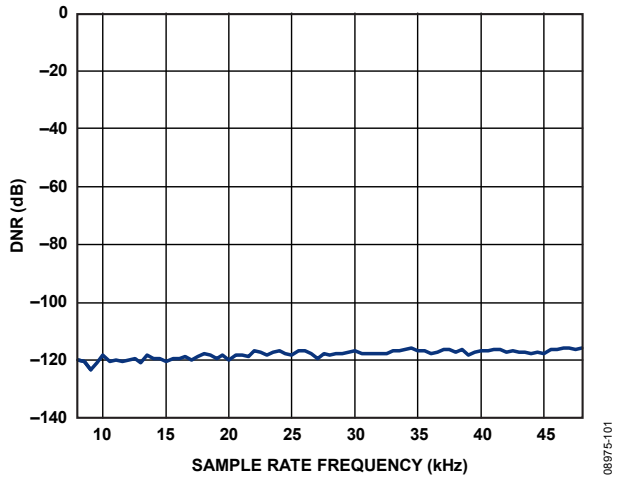


Figure 70. DNR vs. f_S Out Sample Rate, f_S In = 8 kHz, ASRC

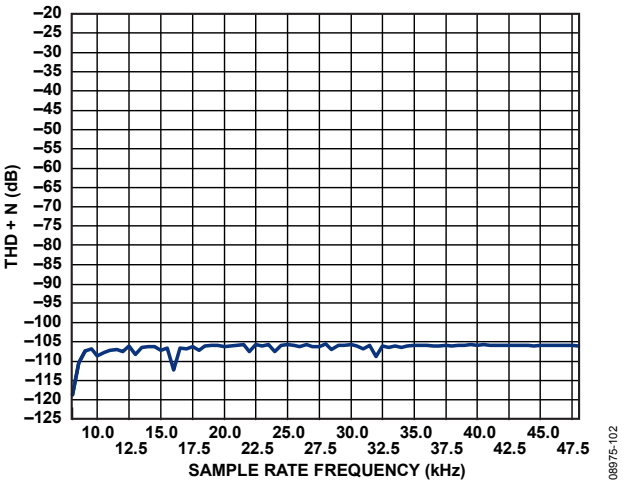


Figure 71. THD + N vs. f_S Out Sample Rate, f_S In = 8 kHz, ASRC

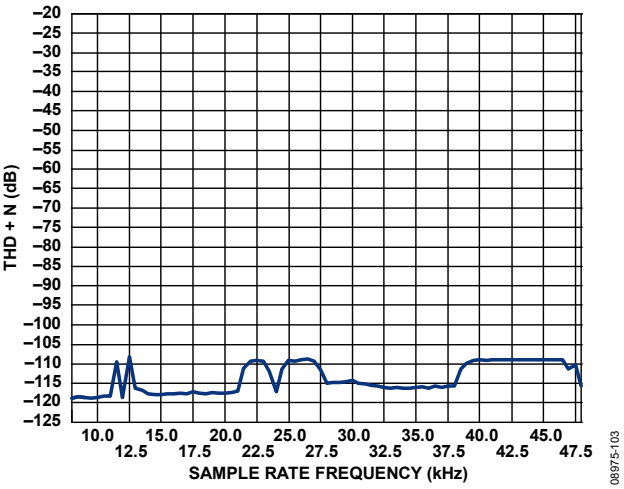


Figure 72. THD + N vs. f_S Out Sample Rate, f_S In = 48 kHz, ASRC

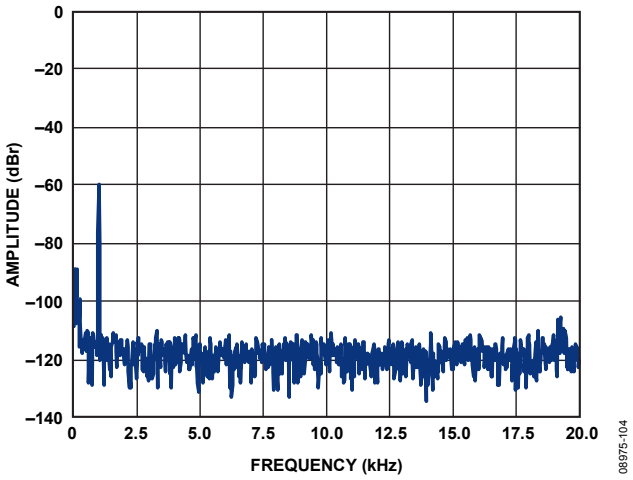


Figure 73. FFT, –60 dBFS, Analog In → ADC → DAC → Line Out

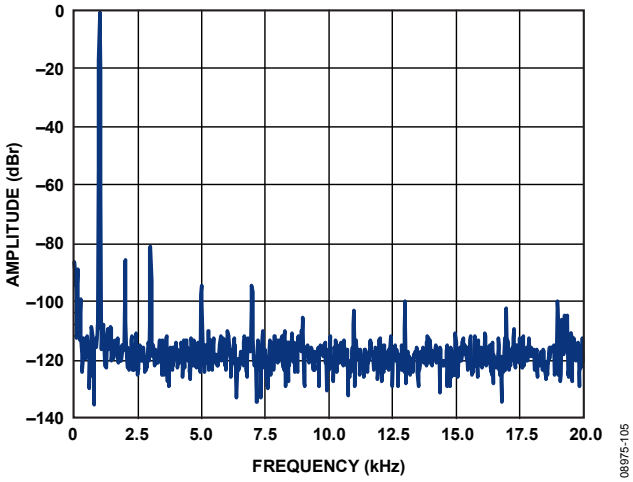


Figure 74. FFT, –1 dBFS, Analog In → ADC → DAC → Line Out

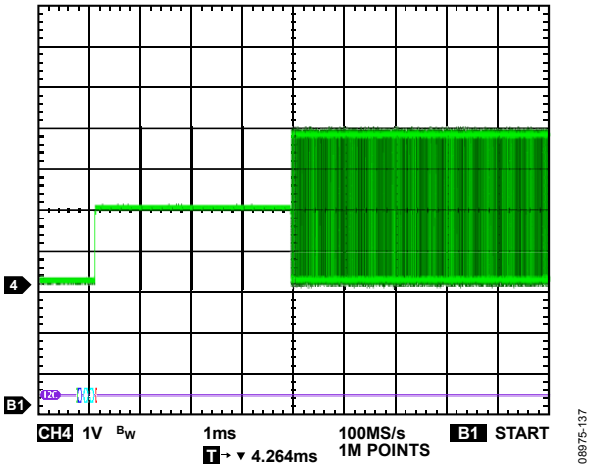


Figure 75. Turn On Speaker Out

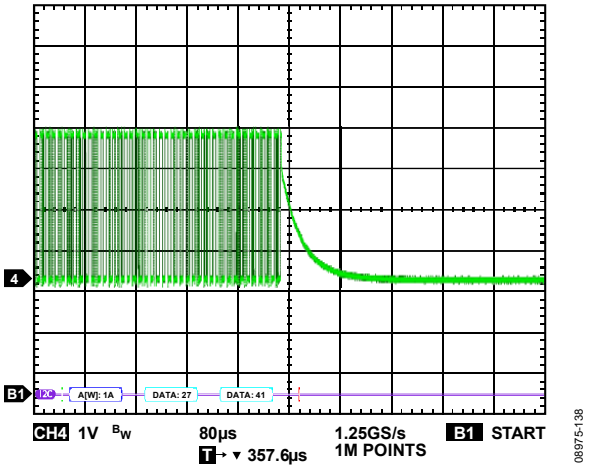


Figure 76. Turn Off Speaker Out

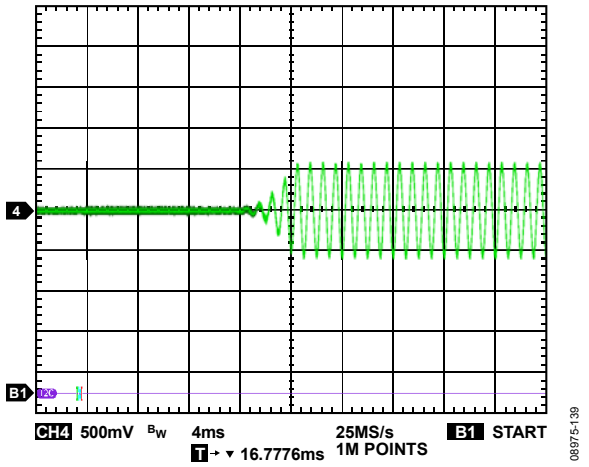


Figure 77. Turn On Headphone Out

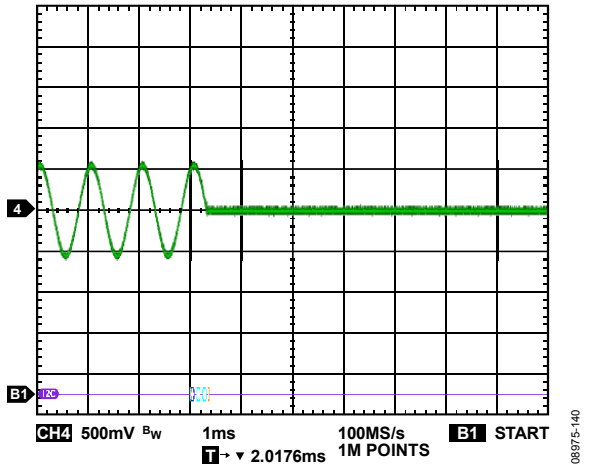


Figure 78. Turn Off Headphone Out

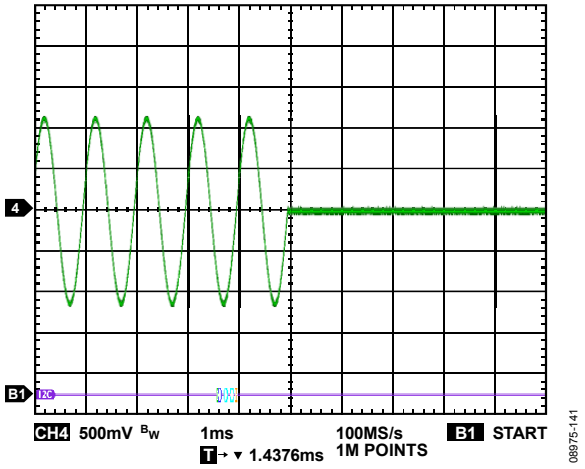


Figure 79. Turn On Earpiece Out

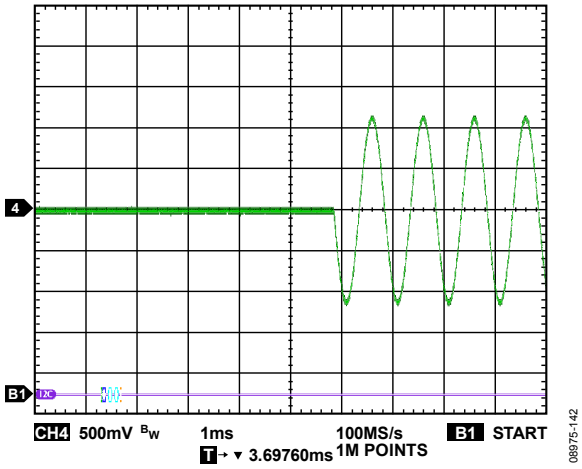


Figure 80. Turn Off Earpiece Out

DETAILED BLOCK DIAGRAM

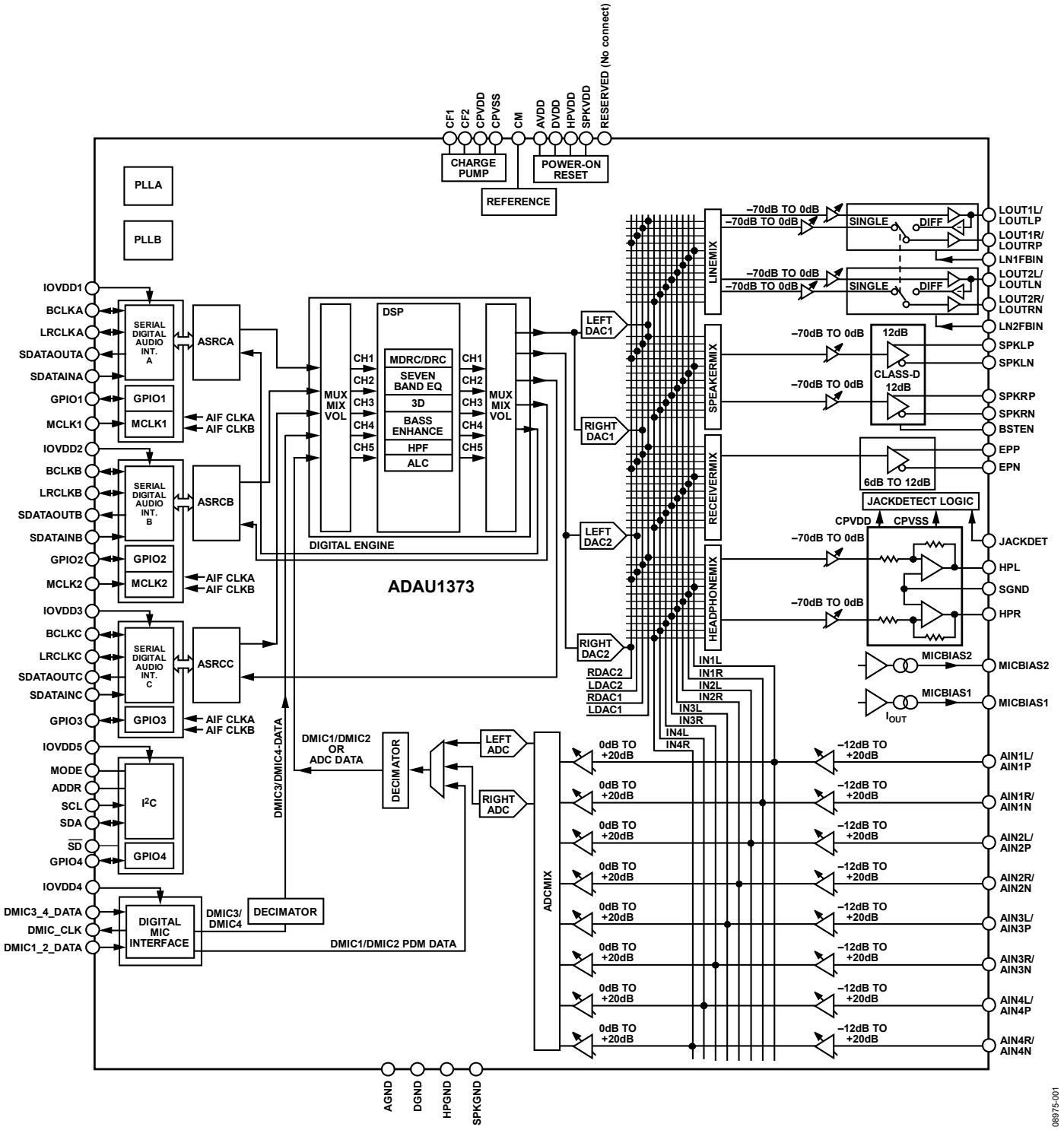


Figure 81.

THEORY OF OPERATION

ANALOG INPUTS

The ADAU1373 provides four stereo (unbalanced)/mono differential inputs. Each input gain and mode of operation can be set independently, using the I²C registers. Figure 82 shows the typical input block for the stereo and mono differential inputs in the programmable gain amplifier (PGA) modes and boost modes.

Each input can receive either a microphone or a line level signal. Each input can be set to either stereo single-ended mode or mono differential mode. In addition, the gain for the input amplifiers can be set to PGA mode or boost mode. In PGA mode, the gain can be varied from −12 dB to +18 dB (in 1 dB steps); whereas in boost mode, it can be varied using one of the following three steps: 0 dB, 9 dB, or 20 dB. In PGA mode, the input resistance varies as per the gain, with a minimum of ~5.6 kΩ. In boost mode, the input resistance is constant at ~20 kΩ.

Stereo Single-Ended Mode

In stereo single-ended mode, the AINxL/AINxP pins are used as the left channel inputs, and the AINxR/AINxN pins are used as the right channel inputs.

Mono Differential Mode

In mono differential mode, the AINxL/AINxP pins are used as positive inputs, and the AINxR/AINxN pins are used as negative inputs for the differential amplifier.

The input amplifers use AVDD as the supply voltage. The AINxP/AINxN input pins are internally biased to AVDD/2, which is the common-mode voltage for the amplifiers. The common-mode pin (CM, Ball B9) must be decoupled using the 10 µF electrolytic capacitor, as well as a 100 nF, X7R ceramic capacitor to keep the reference clean for lower noise. In addition, the input pins must be provided with an ac coupling capacitor to the desired source.

The typical value of the coupling capacitor can be calculated using the desired 3 dB roll-off frequency, as follows:

$$Frequency\ f\ (3\ \text{dB}) = 1/(2 \times \pi \times R_{IN} \times C_{IN}) \quad (1)$$

where R_{IN} = 5.6 kΩ.

Typically, a 2.2 µF capacitor is recommended. This sets the lower frequency cutoff, at 20 Hz, at approximately −1.5 dB.

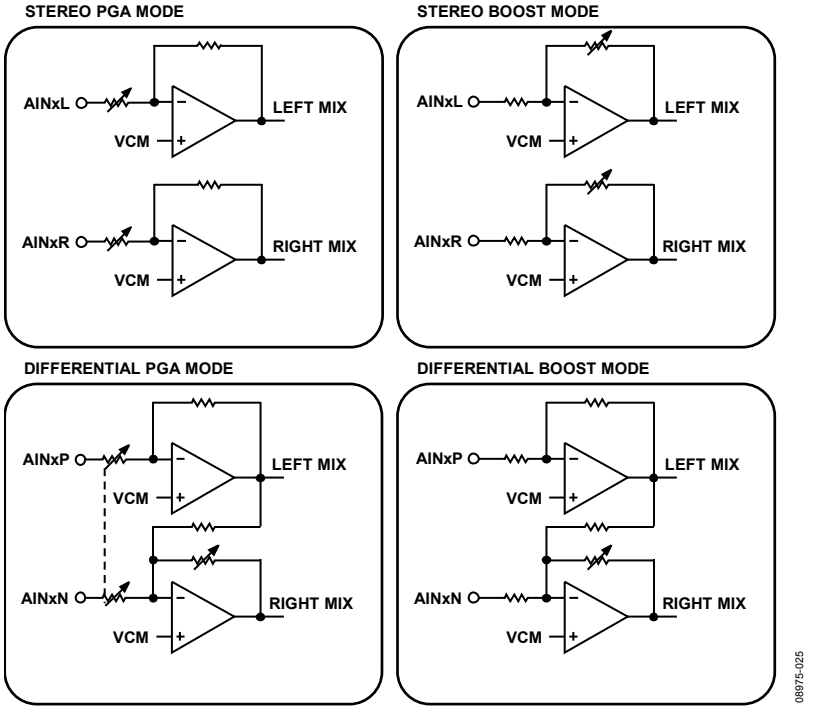


Figure 82. Typical Input Block for Stereo/Mono Differential Inputs in PGA Modes and Boost Modes

Microphone Bias

The MICBIAS1 and MICBIAS2 pins (Ball C8 and Ball C9, respectively) provide a voltage reference for electret analog microphones. These pins are independent MICBIASx voltage outputs that can be set using Register 0x21 to Register 0x23 of the I²C control registers. The MICBIASx voltage can be set via Register 0x21. Four output voltage settings are available: 1.8 V, 2.2 V, 2.6 V, and 2.9 V.

Current sense circuits can detect the current going out of the MICBIAS1 pin or MICBIAS2 pin. This current detect function can be used to sense the presence of the electret microphone. The internally generated current sense logic output can be used as an interrupt on any of the four GPIOs to communicate to the system controller. The current sense can be enabled or disabled using Register 0x22 for MICBIAS1 and Register 0x23 for MICBIAS2. Additional options include overcurrent protection, which can be used to sense the short circuit of MICBIAS1 or MICBIAS2 to ground at the microphone inputs. The overcurrent threshold is programmable, allowing for flexibility in system design.

The MICBIASx pins can also be used to supply voltage to digital microphones or analog microphones with separate power supply pins. However, the maximum current that is available from the MICBIAS1 or MICBIAS2 pin is 1.8 mA.

Microphone Input Connection

To use the microphone input, first identify the type of microphone being used. The ADAU1373 provides microphone bias for condenser microphones. Set the bias voltage as required in the application. It is recommended that the bias be connected to the desired microphone input using a 2 kΩ resistor.

If using a single-ended condenser microphone, see Figure 83 for the correct connection configuration.

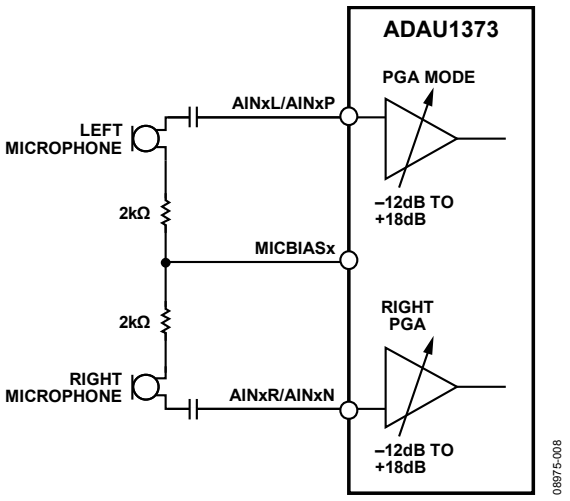


Figure 83. Condenser Microphone Input, Single-Ended

If using a differential or balanced condenser microphone configuration, see Figure 84.

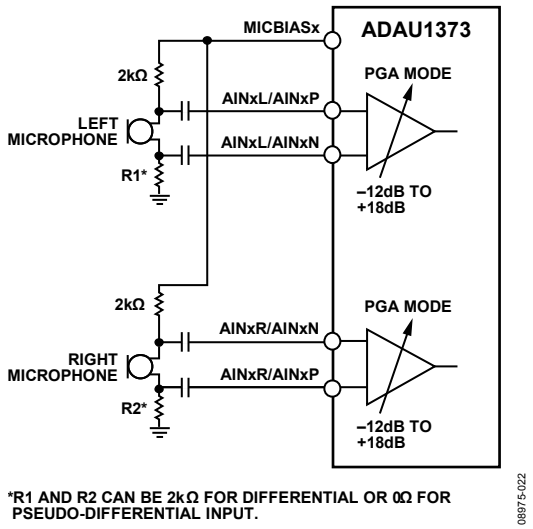


Figure 84. Condenser Microphone Input, Differential

Line Input Connection

To use the analog input as the line input, configure the input to either stereo (single-ended) or mono (differential), as desired (see Figure 85 or Figure 86, respectively).

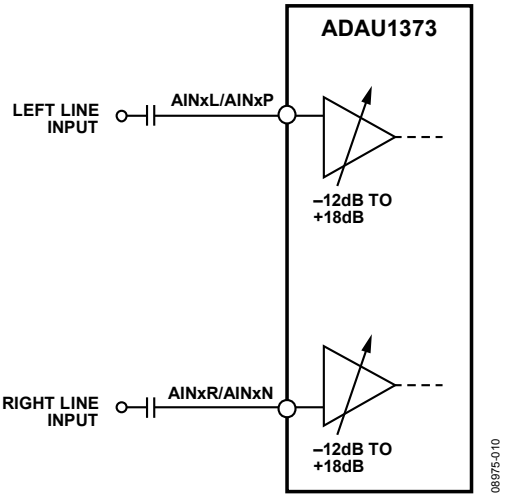


Figure 85. Single-Ended Line Input

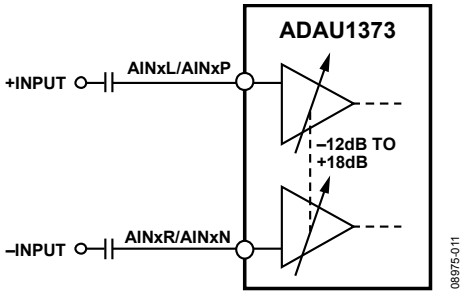


Figure 86. Differential Line Input

Input Impedance

The input resistance for Analog Input 1 through Analog Input 4 (AINx, Ball A5 through Ball A8 and Ball B5 through Ball B8) depends on the gain mode setting. The input resistance is lowest (at approximately 5.6 kΩ) for a +18 dB gain in PGA mode, and it is highest (at approximately 47 kΩ) for a −12 dB setting. In boost mode, the input resistance is constant at 20 kΩ. The input resistance must be considered when calculating the required input coupling capacitor. It is recommended that the lowest value of the impedance be used when determining the microphone input coupling capacitor.

Common-Mode Input Voltage

The common-mode voltage at the input pins (AINx) is typically at AVDD/2. The common-mode voltage at the inputs is turned off when the inputs are muted. The common-mode voltage rises slowly as the inputs are unmuted and charges the input capacitors. To prevent the turn on pop, it is recommended that the inputs be unmuted in the ADAU1373 and be muted at the source. If this recommendation is not adhered to, there is a possibility of a turn on pop as the common-mode voltage at the inputs charges up.

MIXER BLOCK

The ADAU1373 provides the analog mixer block for mixing the analog inputs. The mixer block is available prior to the ADC, line output, headphone output, speaker output, and earpiece output, which provides the system designer with many configuration options.

ADC Mixer Input

The mixer prior to the ADC input allows selection of any or all of the four analog inputs. When multiple inputs are selected, they are mixed prior to the ADC. Register 0x12 and Register 0x13 can be used to select the signals that are input to the ADC mixer.

Line Mixer Output

The mixer prior to the line output amplifier allows selection of any or all of the four analog inputs, as well as the DAC outputs. When multiple inputs are selected, they are mixed prior to the line output amplifier. Register 0x14 through Register 0x17 can be used to select the signals that are input to the line mixer.

Headphone Mixer Output

The mixer prior to the headphone output amplifier allows selection of any or all of the four analog inputs, as well as the DAC outputs. When multiple inputs are selected, they are mixed prior to the headphone output amplifier. Register 0x1A and Register 0x1B can be used to select the signals going to the headphone mixer.

Speaker Mixer Output

The mixer prior to the headphone output amplifier allows selection of any or all of the four analog inputs, as well as the DAC outputs. Register 0x18 and Register 0x19 can be used to select the signals going to the speaker mixer.

Earpiece Mixer Output

The mixer prior to the earpiece amplifier allows selection of any or all of the four analog inputs, as well as the DAC output. When multiple inputs are selected, they are mixed prior to the earpiece output amplifier. Register 0x1C can be used to select the signals going to the earpiece mixer.

ANALOG OUTPUTS

Line Output

The ADAU1373 provides two single-ended stereo line level outputs on LOUT1L (Ball C7) and LOUT1R (Ball D7) or on LOUT2L (Ball D8) and LOUT2R (Ball D9). The line level outputs can be configured as single-ended or differential. The stereo differential outputs are available on LOUTLP (Ball C7) and LOUTLN (Ball D8) or on LOUTRP (Ball D7) and LOUTRN (Ball D9). The line output control register (Register 0x24) can be used to set the line output mode. The outputs have series resistance to protect against output short circuit. The typical recommended load impedance is approximately 47 kΩ. The line output amplifier uses AVDD as its supply; therefore, the common-mode output level on the line output pins is AVDD/2. Coupling capacitors must be used before connecting the outputs to the desired load. The value of the capacitors can be determined by the following:

$$Frequency\ f\ (3\ \text{dB}) = 1/(2 \times \pi \times R_{OUT} \times C_{OUT})$$

where R_{OUT} = 0.3 Ω.

Set the desired 3 dB low frequency at the output. The line outputs can receive input from any or all of the four inputs directly or from the DAC (see Figure 87 and Figure 88 for block diagrams).

The line outputs have a ground noise rejection feature that can be enabled using Register 0x24, Bit 2 (LNFBEN). When enabled, the line output amplifier rejects the noise on LN1FBIN (Ball E7) and LN2FBIN (Ball E8). To use this feature, E7 and E8 must be connected directly to the ground node (typically, the sleeve contact of the line output socket) using a capacitor. The ground noise rejection feature is very useful in applications where the line outputs are used to connect to an external audio system (such as a home theater or docking station) that works on a different power supply and can cause a ground loop when connected to the line output using a single-ended (unbalanced) connection.

Line Output Full-Scale Level

The full-scale output for the line output depends on AVDD. At AVDD = 1.8 V, the full-scale output level is 0.5 V rms single-ended or 1 V rms differential. The full-scale input level scales linearly with the level of AVDD.

Line Output Volume Control

The line output level can be controlled using Register 0x09 (Left Channel Line Output 1 volume control), Register 0x0A (Right Channel Line Output 1 volume control), Register 0x0B (Left Channel Line Output 2 volume control), and Register 0x0C (Right Channel Line Output 2 volume). The volume control range is from mute to 0 dB in 32 steps.

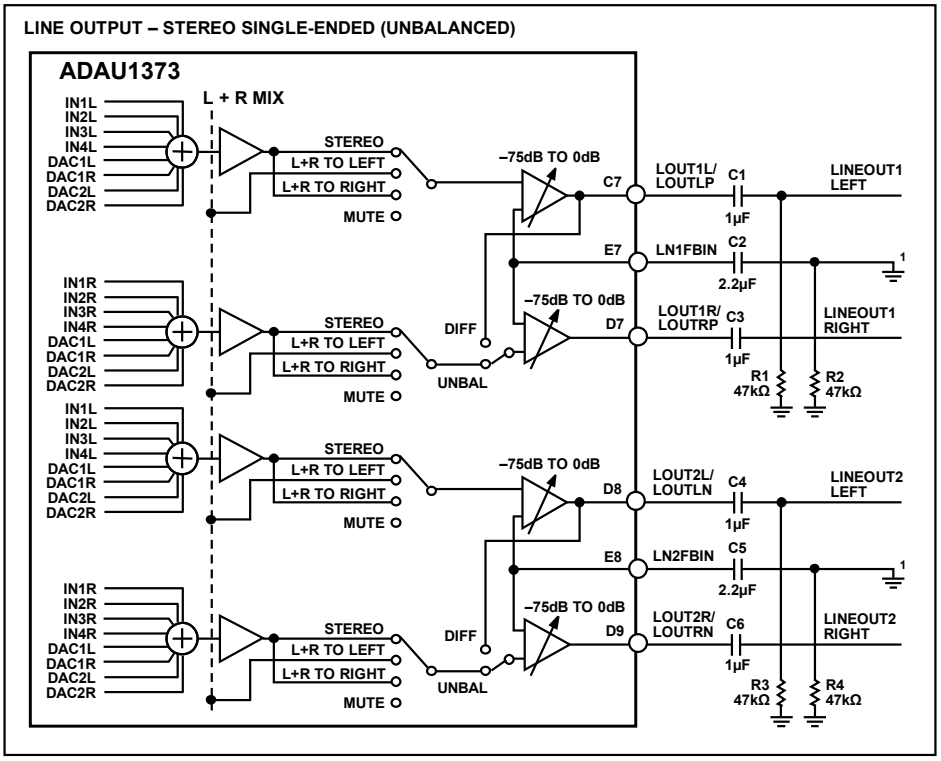


Figure 87. Line Output Block Diagram, Stereo Single-Ended

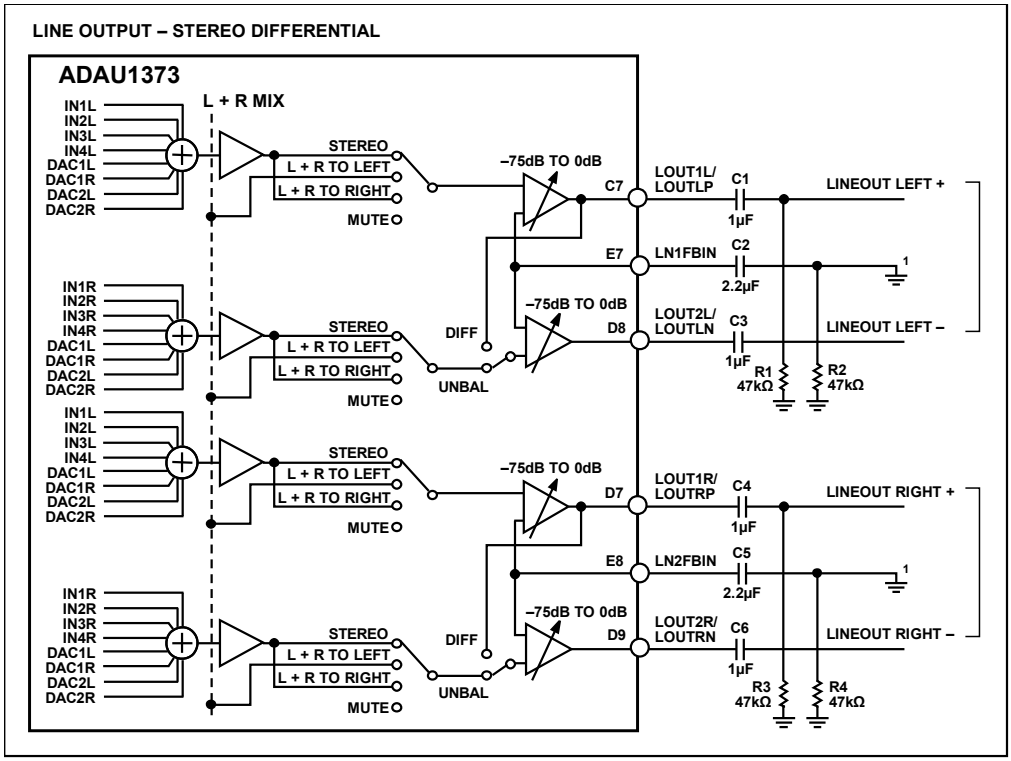


Figure 88. Line Output Block Diagram, Stereo Differential

HEADPHONE OUTPUT

The ADAU1373 provides a high efficiency Class-G stereo headphone output that is true ground centered; therefore, no external coupling capacitors are required for connection to the headphones. The headphones can be connected directly to the headphone output pins, HPL (Ball G8) and HPR (Ball G9). The headphone amplifier uses the supply provided at HPVDD (Ball H8). The recommended operating supply voltage is 1.8 V. This supply voltage must be decoupled with a 1 µF electrolytic capacitor, along with a 100 nF ceramic X7R capacitor. The headphone amplifier uses Class-G architecture and generates the required power supplies, using a flying capacitor with a built-in charge pump connected across CF1 (Ball J9) and CF2 (Ball J7). The charge pump switching frequency is approximately 500 kHz. The generated supply voltages are available at CPVDD (Ball H9, positive rail), and CPVSS (Ball H7, negative rail).

The voltage at this node depends on the input signal to the amplifier. For lower input signal levels, the positive and negative rails are lowered, typically ±0.9 V for 1.8 V HPVDD. As the signal level increases, CPVDD and CPVSS are raised to a higher voltage of ±1.8 V for 1.8 V HPVDD. This rail switching allows the amplifier to achieve higher efficiency. In most typical usage conditions, the amplifier works on the lower ±0.9 V CPVDD and CPVSS voltages, thereby consuming lower power. In addition, as the amplifier generates the positive and negative rails, the output amplifier is true ground centered, thereby eliminating the need for big coupling capacitors to drive the load. For good audio performance, it is recommended that 1 µF, X7R ceramic decoupling capacitors be used for CPVDD and CPVSS. These capacitors serve as a reservoir for the headphone amplifier.

The amplifier has built-in short-circuit protection and, therefore, shuts down in the event of a short circuit on the headphone outputs.

SGND (Ball G7) is provided for sensing the dc potential at the headphone socket. It is recommended that SGND be connected directly to the ground pin of the headphone socket, which ensures the lowest dc offset at the amplifier output and eliminates pop-and-click turn on/turn off for the amplifier. In addition, it helps reduce crosstalk between the left and right channel outputs.

The headphone amplifier is designed to drive headphones with a minimum impedance of 16 Ω. The output level of the amplifier can be controlled using Register 0x0F (left channel headphone output volume control bits) and Register 0x10 (right channel headphone output volume control bits).

In addition, the headphone amplifier can be set to different working modes, depending on the performance and power consumption requirements (Register 0x1D, Bits[3:2]). The available modes include Class-G (default), high efficiency, and low efficiency. In Class-G mode, the amplifier rails are switched between ±0.9 V and ±1.8 V, depending on the signal level. The threshold for rail switching in Class-G operation can be set to 300 mV, 400 mV, or 500 mV using Register 0x1E, Bits[6:5].

In high efficiency mode, the rails are fixed at ±0.9 V, independent of the input signal level. This mode reduces the output power available from the amplifier and also reduces the amount of current consumed by the battery.

In low efficiency mode, the rails are fixed at ±1.8 V, independent of the input signal level. This mode enables the amplifier to produce higher output levels, but current consumption is higher than in high efficiency mode.

It is recommended that the default mode, Class-G mode, be used because the supply rails are switched based on the input level.

The headphone amplifier also has a built-in overcurrent protection circuit that protects the amplifier against a short circuit to ground on the outputs. The overcurrent detect threshold level can be programmed to the desired load impedance level using Register 0x1D, Bits[1:0]. The available settings are 200 mA, 250 mA, 300 mA, and 350 mA.

The turn on time for the headphone amplifier is programmable using Register 0x1D, Bits[5:4]. Four settings are available: 2 ms, 4 ms, 8 ms, and 16 ms.

The headphone jack insertion detect feature can be used to turn off the speaker amplifier when the headphones are connected to the amplifier, thereby saving extra power consumed from the battery. Register 0x36, Bits[1:0] and Register 0x38, Bit 4 are provided to turn on this feature. Note that this feature requires the use of a headphone jack with a switch. See Figure 89 for more information.

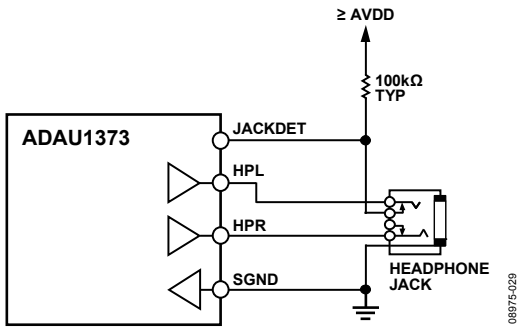


Figure 89. Headphone Jack Detect Option 1

In a typical application, the headphone amplifier is powered down, and its output is typically high impedance when inactive. Using Register 0x1E, Bit 4 (HIZ), the headphone outputs can be pulled down with a 300 Ω resistor. When set to a lower impedance, the JACKDET pin (Ball G5) is pulled to ground via the 300 Ω internal resistance of the headphone amplifier. When the headphone plug is inserted into the headphone socket, the switch at the tip of the socket is disconnected. This, in turn, pulls the JACKDET pin to logic high via Resistor R1. This change in logic level at the JACKDET pin can be used to initiate the interrupt on the GPIOx pin or can be read in the IRQ status register (Register 0xE7), Bit 1 (HP_DECT_STATUS).

Figure 90 shows another option for similar functionality. The circuit in Figure 90 does not use the amplifier to pull down the JACKDET pin (Ball G5); instead, it uses an isolated switch in the headphone jack.

The logic change of the JACKDET pin is reported in Bit 4, Register 0x38. In addition, the debounced version of the logic change is provided in Register 0xE6, Bit 1. Register 0x36 can be used to control the state of the headphone amplifier and speaker amplifier. Table 10 lists the possible settings.

Table 10. Headphone/Speaker Amplifier Control Settings

JACKDET Pin Status	Reg. 0x36, Bit 1	Reg. 0x36, Bit 0	Headphone Amplifier Status	Speaker Amplifier Status
X[1]	0	X[1]	No change	No change
1	1	0	Power-down	No change
0	1	0	No change	Power-down
1	1	1	Power-down	Power-down
0	1	1	No change	No change

[1] X = don't care.

For example, if Register 0x36, Bits[1:0] = 10 and JACKDET is high, the headphone amplifier is shut down, and the speaker amplifier status is unchanged. Note that the headphone or speaker amplifier cannot be turned on automatically, based on a JACKDET pin event. The amplifiers must be enabled via Register 0x27, a power management register.

SPEAKER OUTPUT

The ADAU1371 provides stereo Class-D amplifier outputs to drive the speakers directly. The three-level switching scheme allows the speaker load to be connected directly without any output filters; it also reduces idle power consumption and EMI by reducing switching. The amplifier outputs are differential and use full bridge topology. The amplifier has basic protections, such as the output short to SPKVDD, SPKGND, and the SPKxP and SPKxN outputs. In addition, it monitors the junction temperature internally and shuts down if the temperature exceeds 150°C ± 15°C. In fault situations, the amplifier is switched to high-Z mode for safe and reliable operation.

The amplifier uses three-level PDM switching and an analog modulator with internal feedback. This method ensures good PSRR on the outputs. Three-level switching eliminates the need for an external output filter for connecting the speakers. However, it is important to ensure that the speakers be placed within 10 cm from the ADAU1373 to reduce EMI from the switching outputs. For best EMI performance, proper board layout is required. It is recommended that the supply voltage pins (G1, G2, H2, and H3) be decoupled to SPKGND (H4, H5, J1, and J5) with two 100 nF, X7R ceramic capacitors.

The high efficiency amplifier outputs reduce power dissipation; however, thermal performance depends on layout of the board. The amplifier receives the input from the speaker mixer and includes a circuit to prevent pop-and-click during turn off and turn on.

The amplifier output level can be controlled using Register 0x0D (speaker out left gain control) and Register 0x0E (speaker out right gain control).

The amplifier can be set to work in mono or stereo mode using Register 0x1F. In mono mode, the left and right channel signals are mixed before being output to the speaker. The summed signal can be made available to either the left or right speaker output.

Register 0x1F, Bits[5:4] can be used to set the mono amplifier mode for higher output current capability to drive low impedance loads. In this mode, the left and right channel output FETs are fed from one modulator only. The corresponding left and right channel outputs must be connected externally to take advantage of the low impedance drive capability.

The default amplifier gain is 12 dB; it can be changed to 18 dB using Register 0x1F, Bit 3 (right channel) and Bit 2 (left channel).

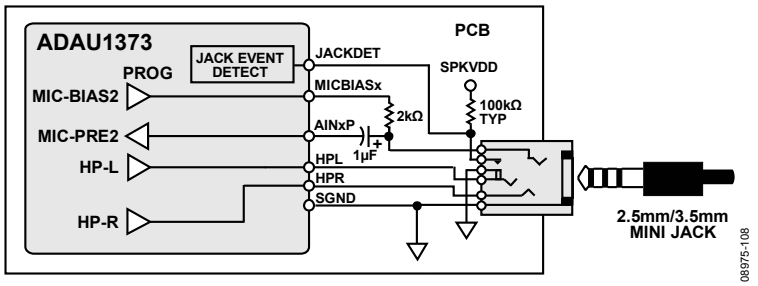


Figure 90. Headphone Jack Detect Option 2

In addition, the amplifier provides edge rate control. The edge rate control can be used to set the switching output slew rate for precise EMI control. The edge rate can be used to reduce EMI in the 30 MHz to 100 MHz band. The slower edge rate reduces EMI but also compromises audio performance. The higher edge rate improves audio performance, but there is more energy in the 30 MHz to 100 MHz band than at the lower edge rate. The EDGE bits (Bits[1:0]) in Register 0x1F can be used for edge rate control.

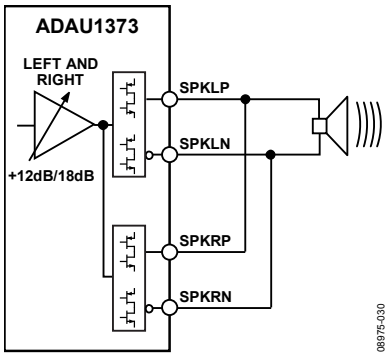


Figure 91. Amplifier Connection Diagram, Mono Mode

If only the DAC output is used during playback through the speaker, a mode is available that allows the DAC output to be sent directly and internally to the speaker simplifier block input instead of passing it through the mixer stage, which improves the signal-to-noise ratio at the speaker output by 6 dB. However, in this mode, the speaker mixer block is disabled, and only the DAC output can be routed to the speaker amplifier. The DIRCD bit (Bit 6) in Register 0x1F is used to enable this feature.

ANALOG-TO-DIGITAL CONVERTER (ADC)

The ADAU1373 consists of a stereo sigma-delta (Σ-Δ) ADC. The ADC uses a 128 × f_S clock and 24-bit resolution. The input signal to the ADC is provided via the ADC mixer. Any or all of the four inputs can be selected to be sent to the ADC using the ADCLMIXx bits (Bits[4:0]) in Register 0x12 for the left channel and the ADCRMIXx bits (Bits[4:0]) in Register 0x13 for the right channel. The ADC output can be made available on the digital audio ports or sent to the on-chip DAC for analog output.

ADC Full-Scale Level

The full-scale input to the ADCs (0 dBFS) depends on AVDD. At AVDD = 3.3 V, the full-scale input level is 0.55 V rms single-ended or 1 V rms differential. The full-scale input level scales linearly with the level of AVDD. For single-ended and pseudo-differential signals, the full-scale value corresponds to the signal level at the pins, which is 0 dBFS. Signal levels above the full-scale value cause the ADCs to clip.

Digital ADC Volume Control

The ADC output level can be controlled before DSP processing in Register 0x72 (ADC left channel recording volume control) and Register 0x73 (ADC right channel recording volume control).

Peak Detect

The ADC has a peak detection feature that can be enabled or disabled using the PDETECT bit (Bit 0) in Register 0x3C.

ADC RESET

The ADC can be reset by writing Bits[2:1] = 11 in Register 0x3C. By default, ADC reset is disabled.

ADC STATUS

The ADC status bits are available for reading via the NOCLKADC bit (Bit 0) in Register 0x37.

DIGITAL-TO-ANALOG CONVERTER (DAC)

The ADAU1373 consists of two stereo Σ-Δ DACs (DAC1 and DAC2). Each DAC uses a 128 × f_S clock and 24-bit resolution. The DACs receive input from either the DSP or the ADC.

DAC output can be routed to the line output, headphone output, earpiece output, or speaker output.

DAC Full-Scale Level

The full-scale output for the DAC, with 0 dBFS input, depends on AVDD. At AVDD = 3.3 V, the full-scale output level is 0.55 V rms single-ended or 1 V rms differential. The full-scale input level scales linearly with the level of AVDD.

Digital DAC Volume Control

The DAC output level can be attenuated using Register 0x6E (DAC1 left channel playback volume control), Register 0x6F (DAC1 right channel playback volume control), Register 0x70 (DAC2 left channel playback volume control), and Register 0x71 (DAC2 right channel playback volume control).

DAC Status

The DAC status bits are available for reading at Bits[6:5] in Register 0x37.

CLOCK GENERATION AND DISTRIBUTION

The ADAU1373 requires an external clock for operation. Flexible clocking control enables the use of many different input clock rates. The on-chip PLL can be used to dejitter the external clock. Two identical PLL blocks, PLLA and PLLB, are provided and can be bypassed if not required. Figure 92 shows the top level block diagram for PLL.

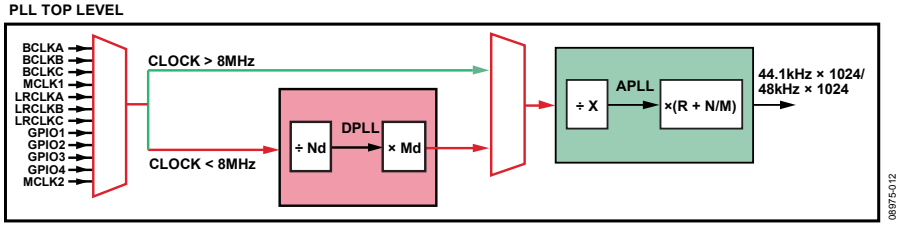


Figure 92. PLL Top Level Block Diagram

The PLL block consists of a digital PLL (DPLL), followed by an analog PLL (APLL) with multiplexer. This architecture allows flexibility in providing the clock to the ADAU1373. The DPLL can accept clock rates from 8 kHz to 8 MHz and outputs clock frequencies from 8 MHz to 27 MHz. The APLL can accept the clock output from the DPLL and provide further fine resolution to generate the clocks for internal blocks. If the input clock is greater than 8 MHz, the DPLL can be powered down to save power. In such a case, the external clock can be sent directly to the APLL. See Figure 93 for a diagram of clock distribution inside the ADAU1373.

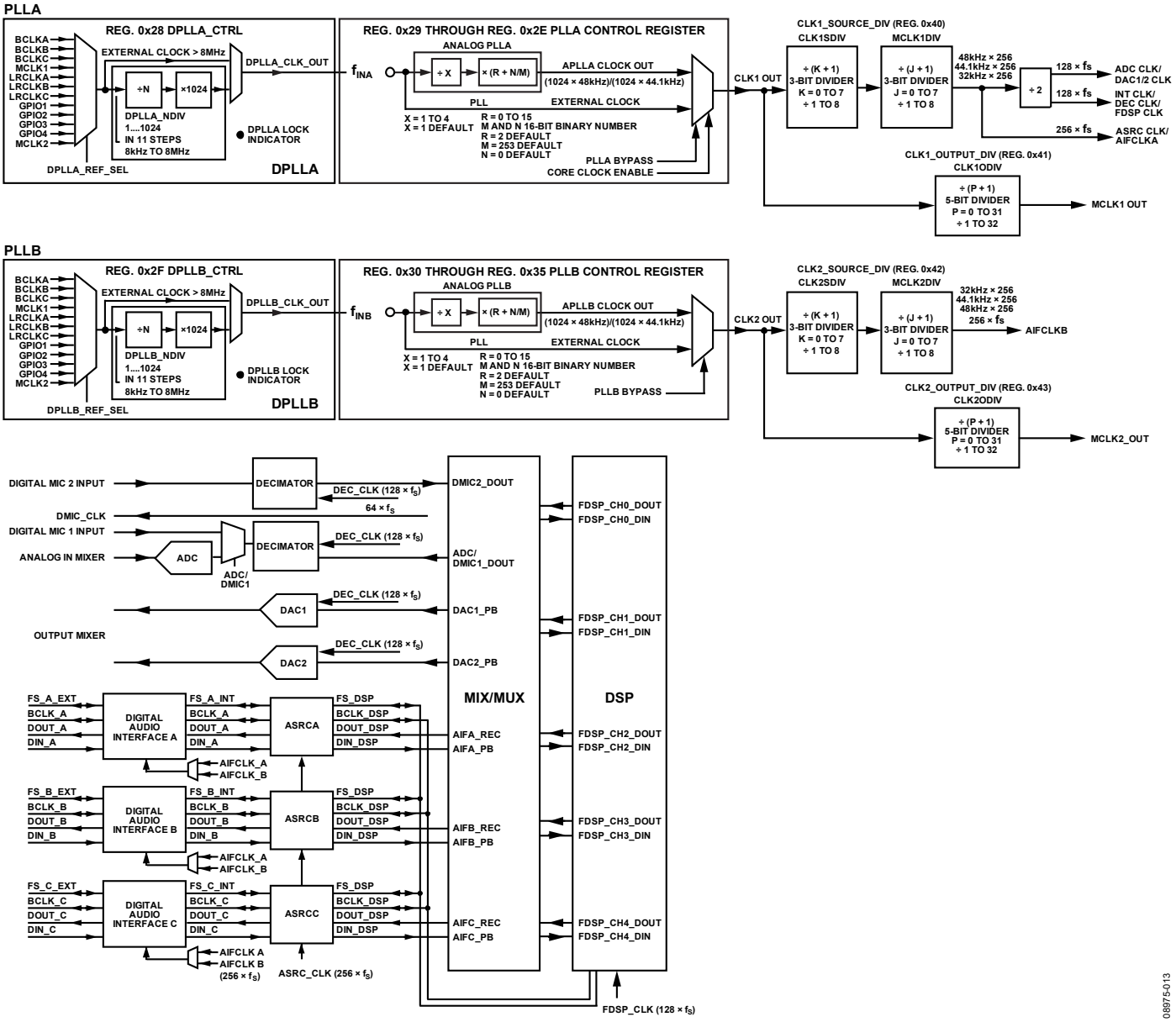


Figure 93. Clock Distribution

DPLL

The DPLL consists of a phase comparator, followed by a high-pass filter and integrators. The following equation shows the relationship of input-to-output frequency:

$$f_{OUT} = (f_{IN}/N_D) \times M_D$$

where:
f_{OUT} is the DPLL output frequency (8 MHz to 27 MHz).
f_{IN} is the DPLL input frequency (8 kHz to 8 MHz).
N_D is the divider. It can be set to 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, or 1024, using Bits[3:0] (DPLLA_NDIV) in Register 0x28 for DPLLA and Bits[3:0] (DPLLB_NDIV) Register 0x2F for DPLLB.
M_D is the multiplier (fixed internally to 1024).

DPLL Divider Example

f_{IN} = 8 kHz
f_{OUT} = 8 MHz
$N_D = 8 \times 1024/8 = 1.024$

Setting N_D to 1 results in $f_{OUT} \geq 8$ MHz. Therefore, N_D should be set to 1.

Core Clock

The core clock is derived directly from the external clock at the MCLK1 or MCLK2 pins or from the PLL. The PLLA_EN bit for PLLA (Bit 0 in Address 0x2E) and the PLLB_EN bit for PLLB (Bit 0 in Address 0x35) can be used to enable or disable the PLL. Clocks for the converters, the serial ports, and the DSP are derived from the core clock. The core clock rate is always an integer multiple of the desired sample rate used inside the part.

Case 1—PLL Bypassed (Using External Clock as Core Clock)

If the PLL is bypassed, the clock available at MCLK1 (Ball C2) or MCLK2 (Ball D1) is used as the core clock. Therefore, $f_{CORE} = f_{IN}$. As the PLL is bypassed, the frequency of the clock at the MCLKx pins must be set properly, using the clock divider bits, CLK1SDIV, Bits[5:3], and MCLK1DIV, Bits[2:0], in Register 0x40 for PLLA and CLK2SDIV, Bits[5:3], and MCLK2DIV, Bits[2:0] in Register 0x42 for PLLB. The required external clock rate can be determined by the following equation, in which J and K are the clock dividers:

$$f_{IN} = 256 \times f_S \times (J + 1) \times (K + 1)$$

See Table 14, Table 15, and Table 16 for some possible options for external clock rates. Note that clock rates greater than 50 MHz require careful attention to the clock driver and board layout to maintain signal integrity.

Be sure that this clock is available to the MCLKx input pins before enabling the COREN bit (Bit 7, core clock enable) in Register 0x40.

Case 2—PLL Enabled

The internal PLL can be used to generate the core clock from the external clock. The internal PLL has two modes of operation: integer mode and fractional mode. Therefore, $f_{CORE} = f_{PLL}$.

APLL

The APLL provides the fine resolution required to generate clocks for the internal blocks. It uses either the clock input at the MCLK1 pin (Ball C2) or a DPLL output as a reference to generate the core clock. The PLL can be set for either integer or fractional mode. The PLL multiplier and divider (X, R, M, and N) are programmed using Register 0x29 to Register 0x2D for PLLA and Register 0x30 to Register 0x34 for PLLB. The PLL can accept input frequencies in the range of 8 MHz to 27 MHz, either directly from an external source, if the external clock input is greater than 8 MHz, or from the DPLL, if the external clock input is within a range of 8 kHz to 8 MHz. The PLL lock range is 45.158 MHz to 49.152 MHz.

This sets the PLL output frequency based on the sample rate governed by the following equation:

$$f_{PLL} = 256 \times f_S \times (J + 1) \times (K + 1)$$

where $J, K = 0, 1, 2, \ldots 7$.

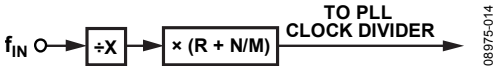


Figure 94. APLL Block Diagram

The APLL can be used in either integer mode or fractional mode.

Integer Mode

Integer mode is used when the MCLK frequency is an integer multiple of the PLL output ($1024 \times f_S$) frequency, governed by the following equation:

$$f_{PLL} = (R/X) \times f_{IN}$$

where $f_{PLL} = 1024 \times f_S$

For example, if f_{IN} = 12.288 MHz and f_S = 48 kHz, then

f_{PLL} (*PLL Required Output*) = 1024 × 48 kHz = 49.152 MHz

R/X = 49.152 MHz/12.288 MHz = 4

Therefore, R and X are set as follows: R = 4, and X = 1 (default).

In integer mode, the values set for N and M are ignored. Table 13 shows common integer PLL parameter settings for f_S = 48 kHz sampling rates.

Fractional Mode

Fractional mode is used when the available MCLK is a fractional multiple of the desired PLL output; it is governed by the following:

$$f_{PLL} = f_{IN} \times (R + (N/M))/X$$

For example, MCLK = 12 MHz and f_S = 48 kHz.
The PLL output is $1024 \times f_S$.

PLL Output = 1024 × 48 kHz = 49.152 MHz

To find the values of R, N, and M, use the following equation:

$$f_{PLL} = f_{IN} \times (R + (N/M))/X$$

where f_{PLL} = 49.152, and f_{IN} = 12 MHz.

$(R + (N/M))/X$ = 49.152 MHz/12 MHz = 4 + (12/125)

See Table 11 and Table 12 for common fractional PLL parameter settings for 44.1 kHz and 48 kHz sampling rates.

Table 11, Table 12, and Table 13 also list the typical PLL settings at 44.1 kHz and 48 kHz sample rates. Note that the PLL control setting in hexadecimal format represents the 48 bits (six bytes) for either PLLA or PLLB. For PLLA, the six bytes should be written starting from Register 0x29 through Register 0x2E. For PLLB, the six bytes should be written starting from Register 0x30 through Register 0x35.

PLL Lock Acquisition

The core clock for the device is disabled until the core clock enable bit (Bit 7, COREN) in Register 0x40 is set to 1. It is recommended that the audio outputs not be turned on until PLL lock is established.

To program the PLL during initialization or reconfiguration of the clock setting, use the following procedure:

1. Bring the required blocks out of power-down (Register 0x25 to Register 0x27).
2. Ensure that the core clock is disabled (Register 0x40, Bit 7 = 0).
3. Enable the PLL (Register 0x2E, Bit 0, for PLLA; Register 0x35, Bit 0, for PLLB).
4. Set the PLL control registers for the desired clock rate (Register 0x28 to Register 0x2D for PLLA and Register 0x2F to Register 0x34 for PLLB).
5. Poll the lock bit (Register 0x2E, Bit 2, and Register 0x35, Bit 2, for APLL and Register 0x2E, Bit 3, and Register 0x35, Bit 3, for DPLL). If the lock bit is set, proceed to Step 6; otherwise, continue to poll. If no lock is established, check the clock rate settings and clock to the device.
6. To ensure that the various blocks in the device are clocked correctly, assert the core clock enable bit only after PLL lock is acquired.

Table 11. Fractional PLL Parameter Settings for 44.1 kHz Base Sample Rate (PLL Output = 45.1584 MHz = 1024 × f_S)

MCLK Input (MHz)	Input Divider (X)	Integer (R)	Denominator (M)	Numerator (N)	PLL Control Setting (Hex)
8	1	5	625	403	0x0271 0193 2901
12	1	3	625	477	0x0271 01DD 1901
13	1	3	8125	3849	0x1FBD 0F09 1901
14.4	2	6	125	34	0x007D 0022 3301
19.2	2	4	125	88	0x007D 0058 2301
19.68	2	4	1025	604	0x0401 025C 2301
19.8	2	4	1375	772	0x055F 0304 2301
24	2	3	625	477	0x0271 01DD 1B01
26	2	3	8125	3849	0x1FBD 0F09 1B01
27	2	3	1875	647	0x0753 0287 1B01

Table 12. Fractional PLL Parameter Settings for 48 kHz Base Sample Rate (PLL Output = 49.152 MHz = 1024 × f_S)

MCLK Input (MHz)	Input Divider (X)	Integer (R)	Denominator (M)	Numerator (N)	PLL Control Setting (Hex)
8	1	6	125	18	0x007D 0012 3101
12	1	4	125	12	0x007D 000C 2101
13	1	3	1625	1269	0x0659 04F5 1901
14.4	2	6	75	62	0x004B 003E 3301
19.2	2	5	25	3	0x0019 0003 2B01
19.68	2	4	205	204	0x00CD 00CC 2301
19.8	2	4	825	796	0x0339 031C 2301
24	2	4	125	12	0x007D 000C 2301
26	2	3	1625	1269	0x0659 04F5 1B01
27	2	3	1125	721	0x0465 02D1 1B01

Table 13. Integer PLL Parameter Settings for f_S = 48 kHz (PLL Output = 49.152 MHz = 1024 × f_S)

MCLK Input (MHz)	Input Divider (X)	Integer (R)	Denominator (M)	Numerator (N)	PLL Control Setting (Hex)[1]
12.288	1	4	Don't care	Don't care	0xXXXX XXXX 2001
24.576	1	2	Don't care	Don't care	0xXXXX XXXX 1001

[1] X = don't care.

SAMPLING RATES

The ADCs, DACs, and DSP share a common sampling rate (f_S) that is determined based on the core clock rate. Three digital audio interface ports are available for the ADAU1373. Each port is provided with an asynchronous sample rate converter (ASRC). If the ASRCs are used, the sample rate at the digital ports can be different from the internal sample rate. However, the sample rate used internally must be equal to or higher than the sample rate at the ports.

SETTING THE PLL AND CLOCK RATES

For proper operation of the ADAU1373, the device must be set for correct clock rates. Following are the recommended steps:

Step 1—Sample Rate (f_S)

Determine the desired operating sample rate (f_S) for the internal blocks. f_S is based on either 48 kHz (48 kHz, 32 kHz, 24 kHz, 16 kHz, 8 kHz) or 44.1 kHz (44.1 kHz, 22.05 kHz, 11.025 kHz, 8.0182 kHz). If the ASRCs are bypassed, this is the operating sample rate at Digital Audio Interface A, Digital Audio Interface B, and Digital Audio Interface C.

Step 2—Determine Divider J and Divider K

The PLL output or external clock input is divided down to get the required 256 × f_S core clock. Two clock dividers (CLK1SDIV, Bits[5:3], and MCLK1DIV, Bits[2:0] in Register 0x40 for PLLA and CLK2SDIV, Bits[5:3], and MCLK2DIV, Bits[2:0] in Register 0x42 for PLLB) are provided; each clock divider can be set from 1 to 8. The CLKxSDIV bits set the K value, and the MCLKxDIV bits set the J value of the divider. See Figure 93 for more details. See Table 14, Table 15, and Table 16 for some possible options.

Next, depending on the whether the direct external clock or PLL is used, select the appropriate equation from the following sections.

External Mode

In the external mode, the external clock frequency determines the internal device operation clock rate.

If using external mode,

$$f_{IN} = 256 \times D \times f_S$$

where $D = (J + 1) \times (K + 1)$.

For external clock use, see Table 14, Table 15, and Table 16 for some possible choices.

Note that clock input frequencies above 50 MHz, although possible, require careful attention—especially on clock driver and board layout to maintain signal integrity and lower EMI.

Table 14. 48 kHz Sample Rate (f_S)

Input MCLK	Register Setting	Divider	Divider Ratio	Register Setting	Divider	Divider Ratio
f_{IN}	CLKxSDIV, Bits[5:3]	K = 0	K + 1	MCLKxDIV, Bits[5:3]	J	J + 1
256 × f_S (12.288 MHz)	000	0	1	000	0	1
512 × f_S (24.576 MHz)	000	0	1	001	1	2
768 × f_S (36.864 MHz)	000	0	1	010	2	3
1024 × f_S (49.152 MHz)	000	0	1	011	3	4

Table 15. 44.1 kHz Sample Rate (f_S)

Input MCLK	Register Setting	Divider	Divider Ratio	Register Setting	Divider	Divider Ratio
f_{IN}	CLKxSDIV, Bits[5:3]	K = 0	K + 1	MCLKxDIV, Bits[5:3]	J	J + 1
256 × f_S (11.289 MHz)	000	0	1	000	0	1
512 × f_S (22.5792 MHz)	000	0	1	001	1	2
768 × f_S (33.8688 MHz)	000	0	1	010	2	3
1024 × f_S (45.1584 MHz)	000	0	1	011	3	4

Table 16. 32 kHz Sample Rate (f_S)

Input MCLK	Register Setting	Divider	Divider Ratio	Register Setting	Divider	Divider Ratio
f_{IN}	CLKxSDIV, Bits[5:3]	K = 0	K + 1	MCLKxDIV, Bits[5:3]	J	J + 1
256 × f_S (8.192 MHz)	000	0	1	000	0	1
512 × f_S (16.384 MHz)	000	0	1	001	1	2
768 × f_S (24.576 MHz)	000	0	1	010	2	3
1024 × f_S (32.768 MHz)	000	0	1	011	3	4
1280 × f_S (40.96 MHz)	000	0	1	100	4	5
1536 × f_S (49.152 MHz)	000	0	1	101	5	6

PLL Mode

If using the PLL, set the dividers so that f_{PLL} is within the range of 45.158 MHz (1024 kHz × 44.1 kHz) to 49.152 MHz (1024 kHz × 48 kHz).

$$f_{PLL} = 256 \times f_S \times (J + 1) \times (K + 1)$$

Example 1—Using a PLL Sample Rate of 48 kHz

For a 48 kHz sample rate (f_S), select the J and K such that f_{PLL} is within the range of 45 MHz to 50 MHz.

$$f_{PLL} = 256 \times D \times 48{,}000$$

where $D = (J + 1) \times (K + 1)$.

For D = 3, f_{PLL} = 36.864 MHz; for D = 4, f_{PLL} = 49.152 MHz; and for D = 5, f_{PLL} = 61.44 MHz. Setting D = 4 ensures that f_{PLL} is within the PLL range of 45 MHz to 50 MHz.

To determine the divider values, there are two options, as follows:

- By setting J = K = 1, then D = 4 because D = (J + 1) × (K + 1).
- By setting J = 0, K = 3 also results in D = (J + 1) × (K + 1) = 4.

Example 2—Using a PLL Sample Rate of 44.1 kHz

For a 44.1 kHz sample rate (f_S), select the J and K such that f_{PLL} is within the range of 45 MHz to 50 MHz.

$$f_{PLL} = 256 \times D \times 44{,}100$$

where $D = (J + 1) \times (K + 1)$.

For D = 3, f_{PLL} = 33.868 MHz; for D = 4, f_{PLL} = 45.158 MHz; and for D = 5, f_{PLL} = 56.448 MHz. Setting D = 4 ensures that f_{PLL} is within the PLL range of 45 MHz to 50 MHz.

To determine the divider values, there are two options, as follows:

- By setting J = K = 1, then D = 4 because X = (J + 1) × (K + 1).
- By setting J = 0, K = 3 also results in D = (J + 1) × (K + 1) = 4.

Example 3—Using a PLL Sample Rate of 32 kHz

For a 32 kHz sample rate (f_S), select the J and K such that f_{PLL} is within the range of 45 MHz to 50 MHz.

$$f_{PLL} = 256 \times D \times 32{,}000$$

where $D = (J + 1) \times (K + 1)$.

For D =5, f_{PLL} = 40.96 MHz; for D = 6, f_{PLL} = 49.152 MHz; and for D = 7, f_{PLL} = 57.344 MHz. Setting D = 6 ensures that f_{PLL} is within the PLL range of 45 MHz to 50 MHz.

To determine the divider values, there are two options, as follows:

- Setting J = 1 and K = 2 can result in D = 6.
- Setting J = 0 and K = 5 also results in D = 6.

Step 3—Calculate APLL multiplier/dividers (X, R, N, M)

If using the analog PLL only, then $f_{IN} \geq 8$ MHz.

Next, using the f_{PLL} calculated in Step 2, calculate the PLL X, R, N, and M values.

For integer mode, use the following:

$$f_{PLL} = (R/X) \times f_{IN}$$

N and M are ignored.

For fractional mode, use the following:

$$f_{PLL} = f_{IN} \times (R + (N/M))/X$$

Select the values of R and X for integer mode or R, X, N, and M for fractional mode.

If the available clock in the system (f_{IN}) is known, and using the PLL output frequency (f_{PLL}) from Step 2, the values required for X, R, N, and M for fractional mode or X and R for integer mode can be calculated using the following equation:

$$(R/X) = f_{IN}/f_{PLL} \text{ (integer mode)}$$

$$(R + N/M)/X = f_{IN}/f_{PLL} \text{ (fractional mode)}$$

Wide selections are possible; refer to Table 11, Table 12, and Table 13 for popular choices.

Step 4—Master Clock Output

The internal core clock, f_{CORE}, can be made available at the GPIO1/GPIO2/GPIO3/GPIO4 pins by setting Register 0xE3 or Register 0xE4. The master clock output frequency can be set using the 5-bit divider (Register 0x41 for PLLA and Register 0x43 for PLLB). Table 17 lists the registers that are used to set the PLL, and Table 18 provides descriptions of the 48 bits that are used for PLL control.

Table 17. PLL Control Register Summary

Reg	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x28	DPLLA_CTRL	DPLLA_REF_SEL				DPLLA_NDIV				0x00	RW
0x29	PLLA_CTRL1	PLLA_M_HI								0x00	RW
0x2A	PLLA_CTRL2	PLLA_M_LO								0x00	RW
0x2B	PLLA_CTRL3	PLLA_N_HI								0x00	RW
0x2C	PLLA_CTRL4	PLLA_N_LO								0x00	RW
0x2D	PLLA_CTRL5	RESERVED	PLLA_R				PLLA_X		PLLA_TYPE	0x00	RW
0x2E	PLLA_CTRL6	RESERVED				DPLLA_LOCKED	PLLA_LOCKED	DPLLA_BYPASS	PLLA_EN	0x10	RW
0x2F	DPLLB_CTRL	DPLLB_REF_SEL				DPLLB_NDIV				0x00	RW
0x30	PLLB_CTRL1	PLLB_M_HI								0x00	RW
0x31	PLLB_CTRL2	PLLB_M_LO								0x00	RW
0x32	PLLB_CTRL3	PLLB_N_HI								0x00	RW
0x33	PLLB_CTRL4	PLLB_N_LO								0x00	RW
0x34	PLLB_CTRL5	RESERVED	PLLB_R				PLLB_X		PLLB_TYPE	0x00	RW
0x35	PLLB_CTRL6	RESERVED				DPLLB_LOCKED	PLLB_LOCKED	DPLLB_BYPASS	PLLB_EN	0x02	RW
0x40	CLK1_ SOURCE_DIV	COREN	CLK1S_SEL	CLK1SDIV			MCLK1DIV			0x00	MMRW
0x41	CLK1_ OUTPUT_DIV	RESERVED		CLK1OEN		CLK1ODIV				0x00	RW
0x42	CLK2_ SOURCE_DIV	CLK2EN	CLK2S_SEL	CLK2SDIV			MCLK2DIV			0x00	MMRW
0x43	CLK2_ OUTPUT_DIV	RESERVED		CLK2OEN		CLK2ODIV				0x00	RW

Table 18. PLLA/PLLB Control Register Settings (PLLA: Register 0x28 to Register 0x2E; PLLB: Register 0x2F to Register 0x35)

Bits	Bit Name	Settings	Description
[47:32]	PLLx_M_HI[7:0], PLLx_M_LO[7:0]		Denominator of the fractional APLL: a 16-bit binary number. The PLLA/PLLB Control M value can be set using Register 0x29 and Register 0x2A for PLLA and Register 0x30 and Register 0x31 for PLLB. The M integer is 16 bits wide. The upper eight bits are stored in Register 0x29 and Register 0x30, and the lower eight bits are stored in Register 0x2A and Register 0x31. The default value is 0x00FD: M = 253.
[31:16]	PLLx_N_HI[7:0], PLLx_N_LO[7:0]		Numerator of the fractional APLL: a 16-bit binary number. The N value can be set using Register 0x2B and Register 0x2C for PLLA and Register 0x32 and Register 0x33 for PLLB. The upper eight bits are stored in Register 0x2B and Register 0x32, and the lower eight bits are stored in Register 0x2C and Register 0x33. The default value is 0: N = 0.
[15]	Reserved		Reserved.
[14:11]	PLLx_R[3:0]		Integer part of APLL: four bits. Only values of 2 to 8 are valid. The four bits are stored in Register 0x2D for PLLA (Bits[6:3]) and Register 0x34 for PLLB (Bits[6:3]).
		0010	R = 2 (default).
		0011	R = 3.
		0100	R = 4.
		0101	R = 5.
		0110	R = 6.
		0111	R = 7.
		1000	R = 8.
[10:9]	PLLx_X[1:0]		APLL input clock divider. The two bits are stored in Register 0x2D for PLLA (Bits[2:1]) and Register 0x34 for PLLB (Bits[2:1]).
		00	X = 1 (default).
		01	X = 2.
		10	X = 3.
		11	X = 4.
8	PLLx_TYPE		APLL operation mode. This bit is stored in Register 0x2D for PLLA (Bit 0) and Register 0x34 for PLLB (Bit 0).
		0	Integer mode (default).
		1	Fractional mode.
[7:4]	Reserved		Reserved.

Bits	Bit Name	Settings	Description
3	DPLLx_LOCKED		DPLLx lock (read-only bit). This bit is stored in Register 0x2E for PLLA (Bit 3) and Register 0x35 for PLLB (Bit 3). 0: DPLLx unlocked (default). 1: DPLLx locked.
2	PLLx_LOCKED		APLL lock (read-only bit). This bit is stored in Register 0x2E for PLLA (Bit 2) and Register 0x35 for PLLB (Bit 2). 0: APLL unlocked (default). 1: APLL locked.
1	DPLLx_BYPASS		DPLL bypass bit. This bit is stored in Register 0x2E for PLLA (Bit 1) and Register 0x35 for PLLB (Bit 1). 0: DPLLx not bypassed (default). 1: DPLLx bypassed.
0	PLLx_EN		APLL enable bit. This bit is stored in Register 0x2E for PLLA (Bit 0) and Register 0x35 for PLLB (Bit 0). 0: APLL disabled (default). 1: APLL enabled.

DIGITAL MICROPHONE INPUT INTERFACE

The ADAU1373 supports the digital microphone inputs. The digital microphone output data can be connected at the DMIC1_2_DATA and DMIC3_4_DATA pins (Ball B4 and Ball C6, respectively). The bit clock for the digital microphone is available at the DMIC_CLK pin (Ball A4). The bit clock is fixed at $64 \times f_S$ (see Figure 5 for the waveforms).

Four digital microphones or two stereo pairs of digital microphones can be connected to the ADAU1373 (see Figure 95 and Figure 96). The single pair of digital microphones shares the decimator with ADC; therefore, when using DMIC1_2_DATA, the ADC is not available. However, DMIC3_4_DATA has a separate decimator and, therefore, can be used independently.

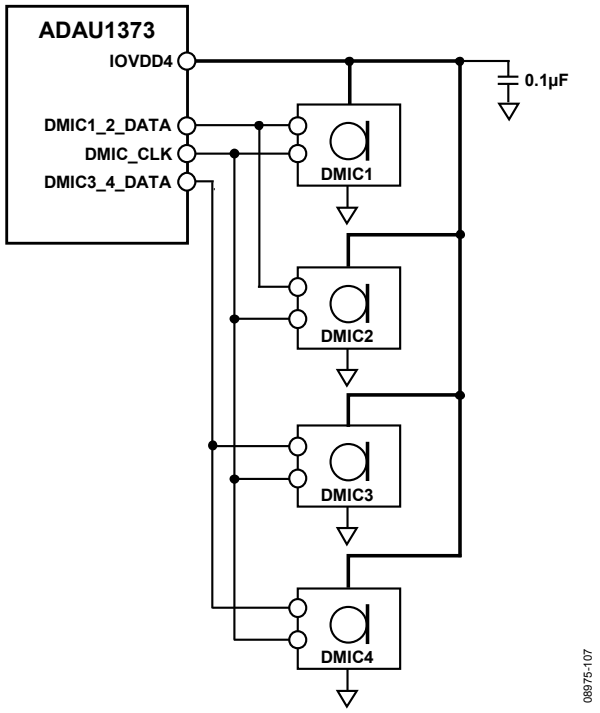


Figure 95. Digital Microphone Connection Diagram for Four Microphones

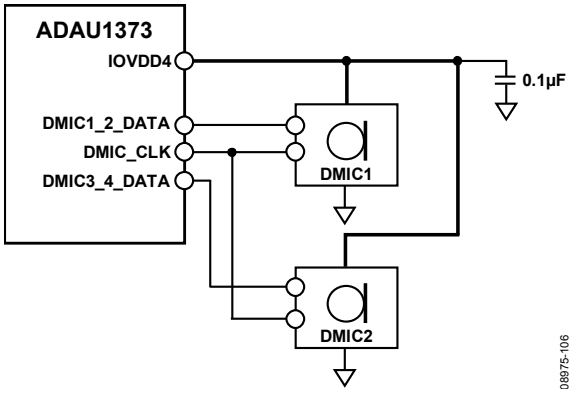


Figure 96. Digital Microphone Connection Diagram for Two Microphones

To enable digital microphone support, the digital recording engine must be enabled first, using Register 0xEB. The Digital Microphone 1/Digital Microphone 2 engine can be enabled using Bit 2 of Register 0xEB, and the Digital Microphone Input 3/Digital Microphone 4 engine can be enabled using Bit 3 of Register 0xEB.

After the recording engine is enabled, the digital microphone input block can be enabled using Register 0xE2, Bit 0 for Input 1/Input 2 (DMIC1_2_DATA) and Bit 2 for Input 3/Input 4 (DMIC3_4_DATA). The digital microphone data input is then routed through the decimator and the recording engine to digital mix/mux.

By default, the digital microphone inputs are configured as a stereo pair. If using only one microphone, use Register 0xE2, Bit 7, to set it as mono input.

The bit clock required for the digital microphone is available at the DMIC_CLK pin (Ball A4), and the drive capability can be set using Register 0xE9, Bit 3.

DIGITAL AUDIO INTERFACE

The ADAU1373 provides three digital audio interface ports: Digital Audio Interface A, Digital Audio Interface B, and Digital Audio Interface C. Each port can receive and transmit audio data in various serial formats. The ports can be configured as master or slave, accommodating many possible system design combinations. Each port has a frame clock (LRCLKA to LRCLKC), a bit clock (BCLKA to BCLKC), and data receive and data transmit pins (SDATAINA to SDATAINC and SDATAOUTA to SDATAOUTC) available. The possible serial audio data formats are right justified, left justified, I²S, and DSP mode. The format for the ports can be set using Register 0x44 for Digital Audio Interface A, Register 0x45 for Digital Audio Interface B, and Register 0x46 for Digital Audio Interface C. The serial data is received or transmitted MSB first, followed by the remaining data bits. For more information about the serial data input/output formats, see Figure 98 to Figure 100. The registers allow each port to be set independently, as either master or slave. In addition, these registers provide controls for bit clock polarity, swapping left/right data, inverting the frame clock, and adjusting data width. Figure 97 shows the audio interface and ASRC block diagram.

Digital Audio Interface A, Digital Audio Interface B, and Digital Audio Interface C can go through the ASRC or directly to the internal digital engine. The ASRCs on each port allow system design flexibility to accommodate sample rates at the ports that are different from those accommodated by the internal DSP.

The digital audio interface ports can be independently configured as master or slave by using the MSx bit (Bit 6) in Register 0x44, Register 0x45, and Register 0x46 for Digital Audio Interface A, Digital Audio Interface B, and Digital Audio Interface C, respectively. This allows a number of different options for using the three ports.

When the ports are configured in master mode, the ports derive the bit clock and frame clock using either AIFCLKA or AIFCLKB, which are derived from PLLA and PLLB, respectively. The sample rate can be selected using Bits[4:2] in Register 0x47, Register 0x48, and Register 0x49 for Digital Audio Interface A, Digital Audio Interface B, and Digital Audio Interface C, respectively.

In slave mode, the port accepts the bit clock and the frame clock from the master in the system. If the ASRCs are enabled, the port is not required to be synchronous to the master clock. However, if the ASRCs are disabled, ensure that the port is synchronous to the master in the system by providing the master clock from the respective master.

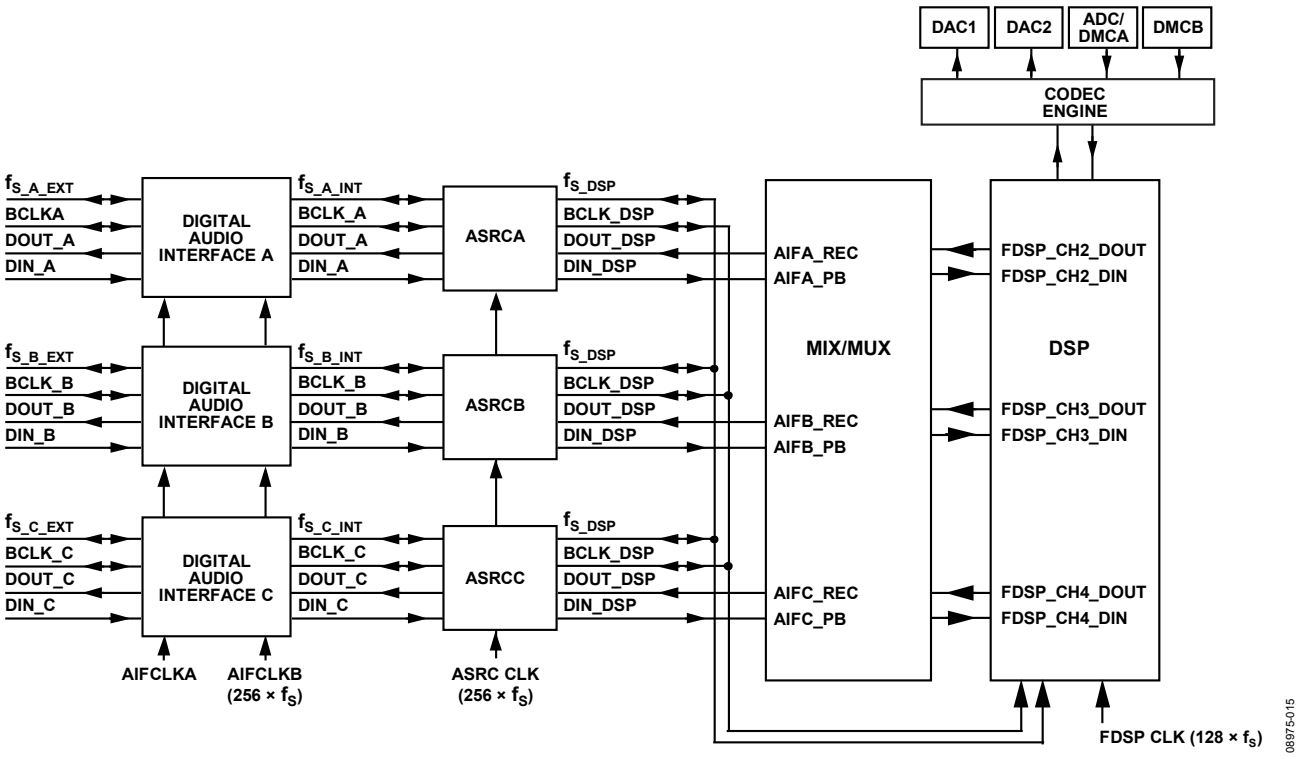


Figure 97. Digital Audio Interface and ASRC Block Diagram

SERIAL DATA INPUT/OUTPUT FORMATS

The flexible serial data input and output ports of the ADAU1373 can be set to accept or transmit data in 2-channel format. Data is processed in twos complement, MSB first format. The left channel data field always precedes the right channel data field in 2-channel streams. The digital audio input can support the following audio formats:

- I²S mode
- Left justified
- Right justified
- Digital signal processor (DSP) mode

The mode selection is performed by writing to the FORMATx bits (Bits[1:0]) of the digital audio interface settings registers (Register 0x44, Register 0x45, and Register 0x46). All modes are MSB first and operate with data of 16 bits to 32 bits.

The serial data clocks must be synchronous with the ADAU1373 master clock input. The LRCLKx (Ball D3, Ball E2, and Ball F1) and BCLKx (Ball D2, Ball E4, and Ball F2) pins are used to clock both the serial input and output ports. The ADAU1373 can be set as the master or the slave in a system. See Figure 98 to Figure 102 for the proper configurations for standard audio data formats.

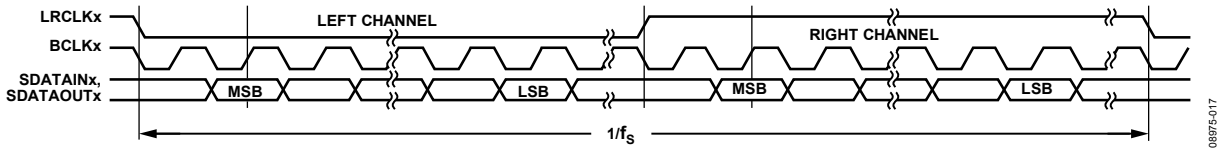


Figure 98. I²S Mode—16 Bits to 24 Bits per Channel

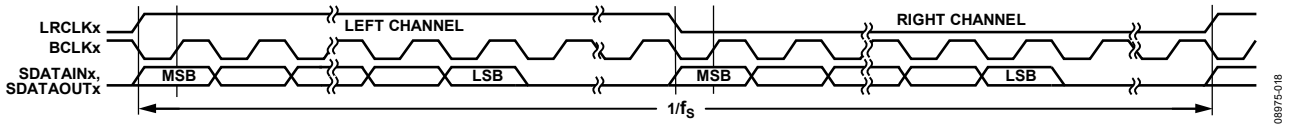


Figure 99. Left-Justified Mode—16 Bits to 24 Bits per Channel

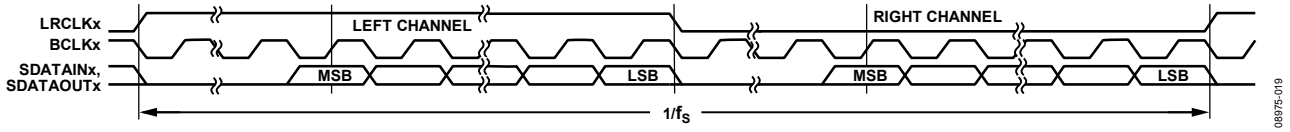


Figure 100. Right-Justified Mode—16 Bits to 24 Bits per Channel

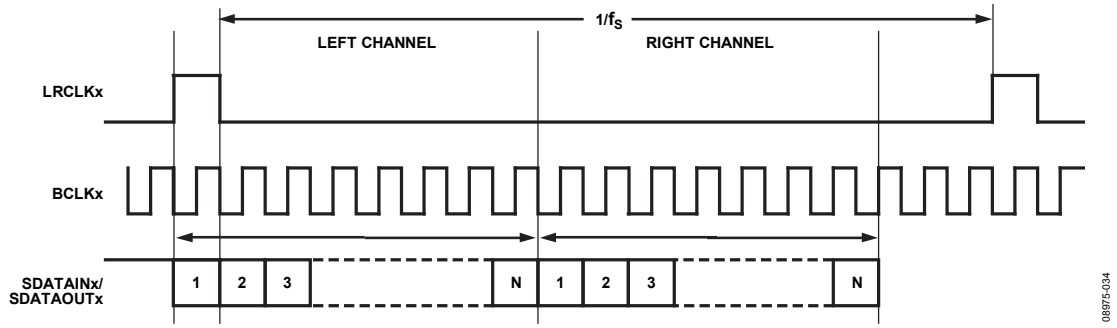


Figure 101. DSP/Pulse Code Modulation (PCM) Mode Audio Interface Submode 1 (SM1), Register 0x44 to Register 0x46, Bit LRPx = 0

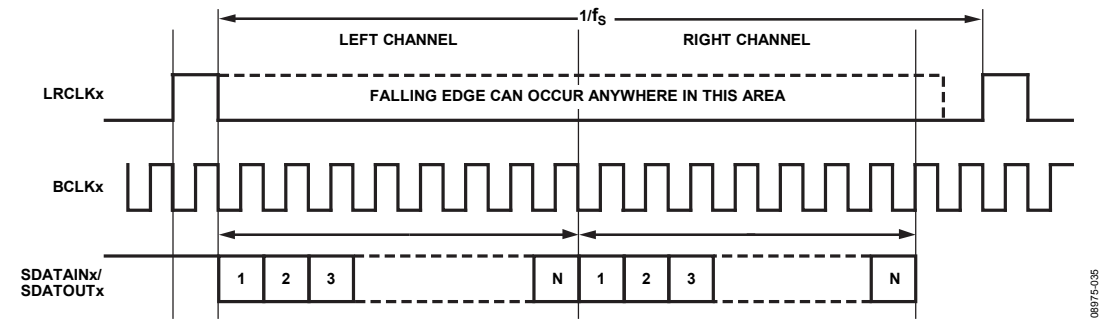


Figure 102. DSP/PCM Mode Audio Interface Submode 2 (SM2), Register 0x44 to Register 0x46, Bit LRPx = 1

ASYNCHRONOUS SAMPLE RATE CONVERTER

The ADAU1373 includes three bidirectional ASRCs to convert the sample rate for the selected digital audio interface port. The ASRCs can be set in automatic ratio detect mode to calculate the required ratio between the input and internal sample rate. This mode writes the value in Register 0x4A and Register 0x4B for Digital Audio Interface A, Register 0x4C and Register 0x4D for Digital Audio Interface B, and Register 0x4E and Register 0x4F for Digital Audio Interface C. The automatic ratio detect can be disabled, and the fractional value can be written into the same registers for manual setting. The maximum sample rate is 48 kHz for the ASRC, as well as for the internal DSP. This sets the limitation on the ASRC such that the interface port sample rate must be equal to or less than the internal core sample rate.

The output-to-input sample rate ratio number is split into the integer part and the fractional part. The integer part is three bits wide, and the fractional part is 12 bits wide. The total available range is 1:8 to 8:1.

The ASRC is bidirectional and converts the sample rate at the port side to the DSP side and vice versa. The DSP side of the ASRC always works at the core sample rate and should be the highest sample rate of all the ports.

Register 0x4A to Register 0x4F can be used to set the ASRC ratio manually for ASRCA, ASRCB, and ASRCC. The following section explains the manual setting of the sample rate conversion ratio.

Manual Setting of Sample Rate Conversion Ratio

Bits[6:4] in Register 0x4A contain the SRCAINT bits for the integer portion; and the SRCARFRE_HI bits (Bits[3:0]), along with the SRCAFRE_LOW bits (Bits[7:0] in Register 0x4B), form the total 12-bit fractional portion.

Bits[6:4] in Register 0x4C contain the SRCBINT bits for the integer portion; and the SRCBRFRE_HI bits (Bits[3:0]), along with the SRCBRFRE_LOW bits (Bits[7:0] in Register 0x4D), form the total 12-bit fractional portion.

Bits[6:4] in Register 0x4E contain the SRCCINT bits for the integer portion; and the SRCCRFRE_HI bits (Bits[3:0]), along with the SRCCRFRE_LOW bits (Bits[7:0] in Register 0x4F), form the total 12-bit fractional portion.

The ratio can be calculated using the following steps:

1. Calculate the ratio.
2. Split the ratio number into integer and fractional parts. Set M as the integer part of $f_{S_DSP}/f_{S_x_INT}$ or $f_{S_DSP}/f_{S_x_EXT}$, and set N as the fractional part.
3. Integer Part M can be set from 1 to 8 using Register 0x4A, Register 0x4C, and Register 0x4E, Bits[6:4] (SRCxINT), for ASRCA, ASRCB, and ASRCC, respectively.
4. Round Fractional Part N, using the following equation:

   ROUND ($N \times 2^{12}$) = ROUND ($N \times 4096$)

5. Convert the number to hexadecimal format.

The fractional part is 12 bits wide with an upper nibble (Bits[11:8]) and a lower byte (Bits[7:0]). The upper bits are set using Register 0x4A, Register 0x4C, and Register 0x4E, Bits[3:0] (SRCxRFRE_HI) and the lower byte is set using Register 0x4B, Register 0x4D, and Register 0x4F, Bits[7:0] (SRCxRFRE_LOW) for Digital Audio Interface A, Digital Audio Interface B, and Digital Audio Interface C, respectively.

Example A

If the target sample rate is 48 kHz and the source sample rate is 44.1 kHz, then

48/44.1 = 1.088435

Separate the integer portion, which is 1, and the fractional portion, which is 0.088435.

For the integer value of the ratio in hexadecimal format, set SRCxINT, Bits[2:0] = 0x1 (hexadecimal).

Next, to enter the fractional value, first convert the number to a 12-bit integer and then to hexadecimal format.

0.088435 × 4096 = 362.231 ≈ 362 = 0x16A (hex)

The upper nibble is 0x1 (hexadecimal), whereas the lower byte is 0x6A (hexadecimal).

That is, SRCxRFRE_HI, Bits[3:0] = 0x1, and SRCxRFRE_LOW, Bits[7:0] = 0x6A.

Example B

If the target sample rate is 44.1 kHz and the source sample rate is 8 kHz, then

44.1/8 = 5.5125

Separate the integer portion, which is 5, and the fractional portion, which is 0.5125.

For the integer value of the ratio in hexadecimal format, set SRCxINT, Bits[2:0] = 0x5 (hexadecimal).

Next, to enter the fractional value, first convert the number to a 12-bit integer and then to hexadecimal format.

0.5125 × 4096 = 2099.2 ≈ 131 = 0x83 (hex)

The upper nibble is 0x0 (hexadecimal), whereas the lower byte is 0x83 (hexadecimal).That is, SRCxRFRE_HI, Bits[3:0] = 0x0, and SRCxRFRE_LOW, Bits[7:0] = 0x83.

MIX/MUX

The ADAU1373 provides very flexible mixing and multiplexing of the digital signals to and from the DSP and to and from the codec/Digital Audio Interface A/Digital Audio Interface B/ Digital Audio Interface C.

The input mixing and routing matrix allows the digital data from Digital Audio Interface A, Digital Audio Interface B, and Digital Audio Interface C, as well as the ADC and digital microphone, to be selected or mixed to any of the DSP input channels (that is, DSP Channel 0 to DSP Channel 4). Similarly, the output mixing and routing matrix allows the data from DSP Channel 0 to DSP Channel 4 to be mixed and routed to Digital Audio Interface A, Digital Audio Interface B, and Digital Audio Interface C, as well as DAC1 and DAC2. The digital volume controls on each of the inputs, as well as the outputs, can be used to adjust the levels. The soft mode allows the volume to be updated for clickless operation.

The routing matrix also allows the data to be looped back from the internal ADC to the DACs or from Digital Audio Interface A to Digital Audio Interface B or Digital Audio Interface C.

For recording purposes, the data from the ADC or the digital microphone can be sent to Digital Audio Interface A, Digital Audio Interface B, and Digital Audio Interface C. Similarly, for playback, the data from the ports can be sent to the DACs and then to the analog outputs. The mixing block allows complete record and playback datapaths.

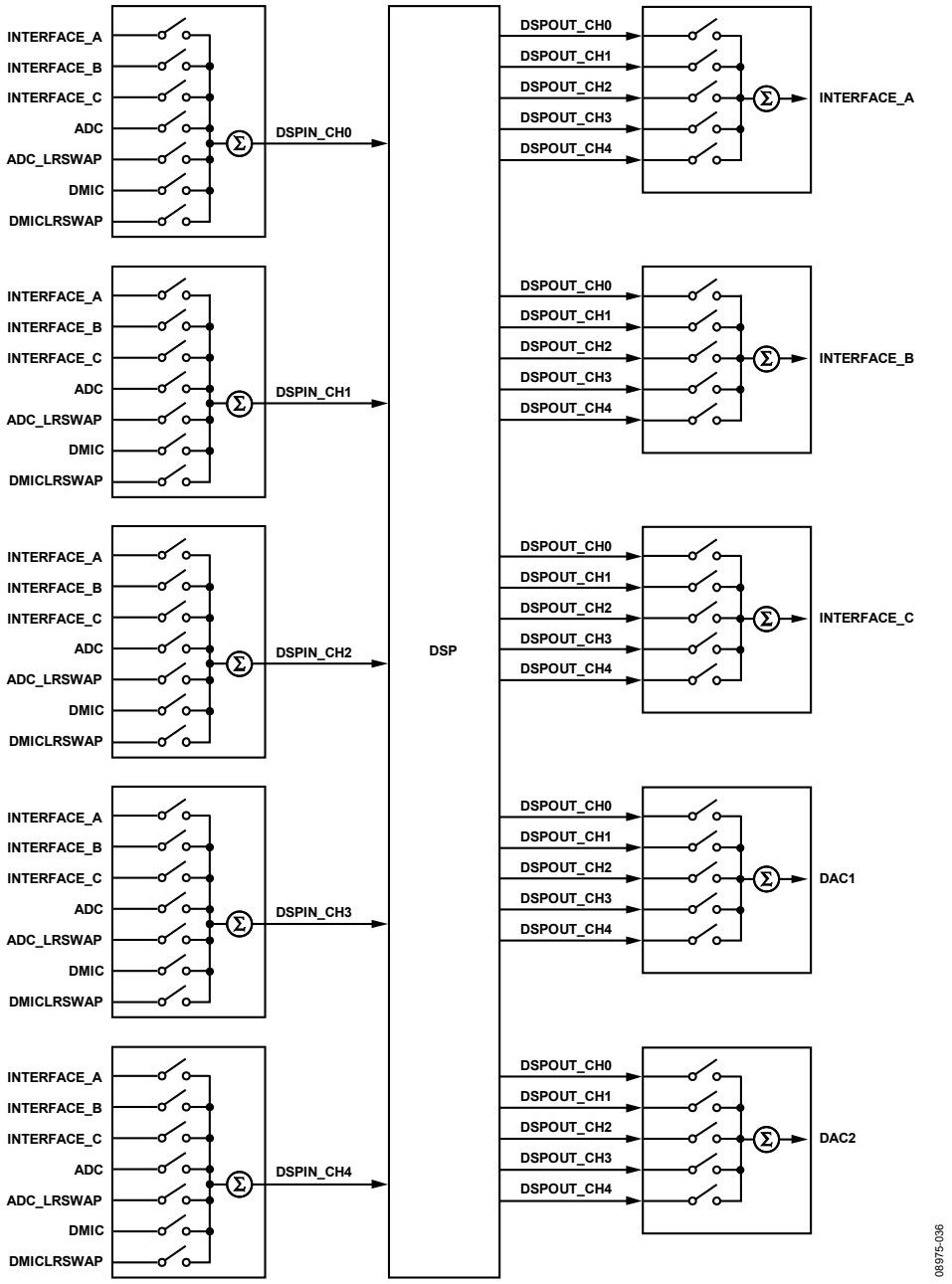


Figure 103. Digital Mix/Mux Block

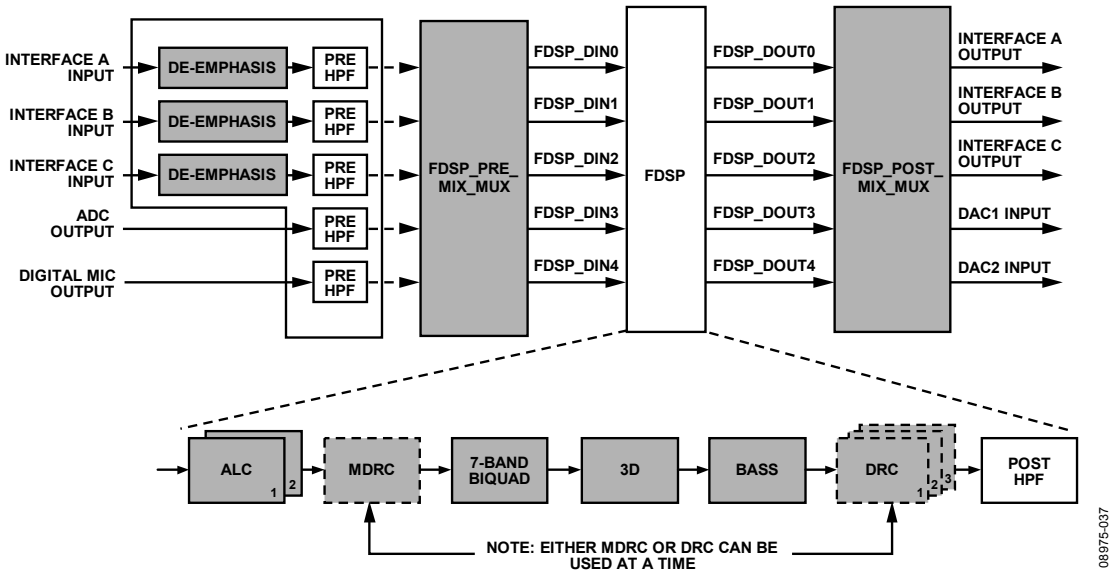


Figure 104. Fixed Function DSP (FDSP) Input and Output Connections and Available Processing Blocks

FIXED FUNCTION DSP (FDSP)

Figure 104 shows the fixed function DSP input and output connections, as well as the available processing blocks. The FDSP works at a 128 × f_S clock rate and has five input and output channels.

The five high-pass filters are available at the input channels to help remove the dc offset. In addition, the following blocks are provided to enhance the signal:

- ALC
- MDRC or three full-band DRCs
- Seven-band EQ
- 3D enhancement
- Bass enhancement
- High-pass filter

HIGH-PASS FILTERS (HPFs)

The ADAU1373 provides five fully programmable HPFs in front of the data path and one configurable HPF following the FDSP blocks.

The five fully programmable HPFs (called pre-HPFs) are used to remove the dc content or the low frequency components from the input signals. An additional HPF, located at the end of the FDSP chain and called the post-HPF, is designed to remove dc or low frequency components that may be introduced by the nonlinear processing in the FDSP blocks. All of these HPFs are first-order IIR with changeable 3 dB cutoff frequencies.

Pre-HPFs

All coefficients of the five pre-HPFs are in 11-bit format and fully programmable. Each coefficient takes up two register addresses, from Register 0xB3 to Register 0xBC. For each coefficient, the first register is the first eight MSB bits, and the second register is the last three LSB bits. Register 0xBD provides an individual control bit for each filter enable or disable.

The pre-HPF frequency transfer function is as follows:

$$H(z) = \frac{1+a}{2} \times \frac{1-z^{-1}}{1-a \times z^{-1}}$$

where Parameter *a* is determined by the cutoff frequency, f_C, and related to the sample rate, f_S. Use the following equations to calculate Parameter a:

$$W_C = 2 \times \pi \times f_C/f_S$$

$$a = \frac{1-\sin w_c}{\cos w_c}$$

For the pre-HPF, the coefficients are quantized to 10 bits, so that the decimal integer values of these coefficients are as follows:

$$a_{INT} = round(a \times 2048)$$

Pre-HPF Working Example

If the required cutoff frequency for the first pre-HPF is 900 Hz and the sampling rate is 48 kHz, then

$$w_C = 2 \times \pi \times f_C/f_S = 0.1178097$$

$$a = \frac{1-\sin w_c}{\cos w_c} = 0.8886221$$

$$a_{INT} = round(a \times 2048) = 1820$$

$$a_{HEX} = 71C$$

Therefore, set Bits[7:0] in Register 0xB3, Register 0xB5, Register 0xB7, Register 0xB9, and Register 0xBB as the MSBs and Bits[2:0] in Register 0xB4, Register 0xB6, Register 0xB8, Register 0xBA, and Register 0xBC as the LSBs for the pre-HPFs.

Post-HPFs

The post-HPF cutoff frequency is selectable via Register 0x7D, Bits[7:3] as 3.7 Hz for dc removal or from 50 Hz up to 800 Hz, with a 50 Hz step for low frequency component filtering. This HPF block can be enabled or disabled for the left or right channel, controlled by Register 0x7D, Bits[1:0]. The HPF calculates the dc value of the signal, which is subtracted from the signal when enabled. When the HPF block is disabled, Bit 2 of Register 0x7D determines whether the calculated dc value is maintained and subtracted from the input signal or cleared to 0.

Figure 105 shows the post-HPF frequency response plots for various cutoff frequency settings.

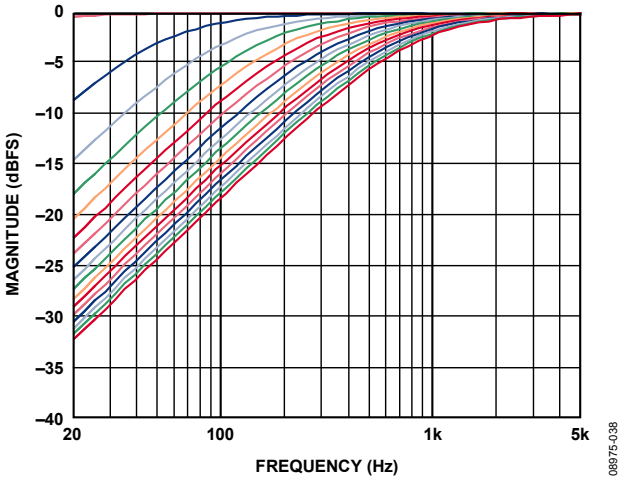


Figure 105. Post-HPF Frequency Response

DYNAMIC RANGE CONTROL (DRC)

The DRC is used to control the dynamic range of the signal. It provides the capability to match the dynamic range of the incoming signal with the dynamic range of the signal fed to the next block or device without losing the signal-to-noise ratio.

The ADAU1373 provides three full-band DRCs or one multiband DRC (MDRC). However, at any given time, either the three full-band DRCs or the MDRC can be used. Register 0x80 through Register 0xB2 are used for setting the MDRC or full-band DRCs. The MDRC and the seven-band EQ share the same register addresses (Register 0x80 through Register 0xBD). Therefore, for the MDRC, ensure that the EQ coefficient writing enable bit (EQ_WR_EN, Bit 0 in Register 0xBE) = 0; whereas for the seven-band EQ, the EQ_WR_EN bit = 1.

MDRC

The MDRC provides a multiband dynamic range control by splitting the signal into three bands, depending on the frequency: low, mid, and high. Each of the bands is processed separately, and individual controls are provided for each band DRC. The MDRC can be enabled or disabled by the MDRC_EN bit (Register 0xB2, Bit 0) (see the MDRC block diagram in Figure 106).

The 3-band MDRC is composed of a second-order high-pass IIR filter, a second-order low-pass IIR filter, the frequency splitter, and three individual DRCs for low, mid, and high bands.

The 3 dB cutoff frequency of the HPF can be set from 50 Hz to 800 Hz in 50 Hz steps, configured using the MDRC_HPF bits (Register 0xB0, Bits[5:2]).

The LPF cutoff frequency can be set to 4 kHz, 8 kHz, or 20 kHz via the MDRC_LPF bits (Register 0xB0, Bits[1:0]).

The HPF and LFP can be enabled or disabled by using the MDRC_LPFEN and MDRC_HPFEN bits in Register 0xB2.

The crossover frequencies between the low band and high band are defined in Register 0xB1 by the MDRC_CROSS_LOW bits (Bits[3:0]) and the MDRC_CROSS_HIGH bits (Bits[7:4]). The crossover frequency between low band and mid band can be varied from 100 Hz to 1600 Hz in steps of 100 Hz. The crossover frequency for the mid-to-high bands can be varied from 1 kHz to 16 kHz in steps of 1 kHz.

All of the previous frequency values are based on a 48 kHz sampling rate. If the input signals are of a different sampling rate, the values should be scaled accordingly.

Using the DRC

The ADAU1373 provides three DRCs that can be used as full band. The DRCs are shared between full-band DRC or MDRC. When the full-band DRCs are in use, the MDRC is not available. For full-band DRC, the crossover filters can be disabled in Register 0xB2 via the MDRC_HPFEN bit (Bit 1) and the MDRC_LPFEN bit (Bit 2). Each of the three DRCs has its own registers: Register 0x80 to Register 0x8F for DRC1, Register 0x90 to Register 0x9F for DRC2, and Register 0xA0 to Register 0xAF for DRC3, plus enable or disable bits, which are set by the DRCEN bits (Bits[1:0]) in Register 0x8D, Register 0x9D, and Register 0xAD.

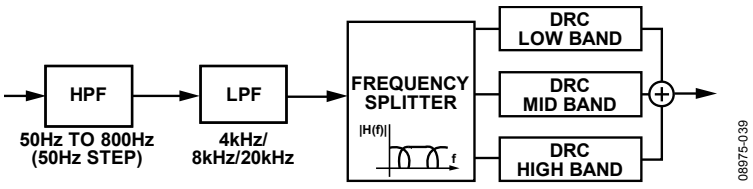


Figure 106. MDRC Block Diagram

The DRCs consist of both peak and rms signal detectors. Either the peak or the rms detector can be assigned for noise gate, compressor/expander, and limiter. Bits[5:3] in Register 0x8D, Register 0x9D, and Register 0xAD are provided for selecting the detectors, as follows:

- The DRCNGSRC bit (Bit 5) can be used for selecting the noise gate detector.
- The DRCCESRC bit (Bit 4) can be used for selecting the compressor/expander detector.
- The DRCLMSRC bit (Bit 3) can be used for selecting the limiter detector.

The DRC can be set to function as limiter, compressor, expander, or noise gate. See Figure 107 for the input/output plot showing the various modes of operation of the DRC.

The DRC allows flexibility in setting up the thresholds, as well as attack and release time controls. The DRC allows independent adjustment of the thresholds by providing control of the x-axis and y-axis using Register 0x82 to Register 0x89 for DRC1, Register 0x92 to Register 0x99 for DRC2, and Register 0xA2 to Register 0xA9 for DRC3. Bit DRCTHX1 to Bit DRCTHX4 in these registers can be used to set the input level threshold point on the x-axis, and Bit DRCTHY1 to Bit DRCTHY4 can be used to set the output level point on the y-axis. The available range is −96 dB to 0 dB for each threshold.

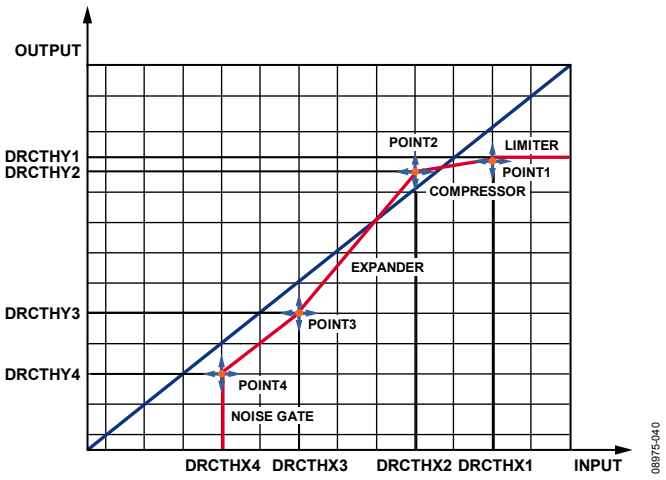


Figure 107. DRC Output vs. Input Plot

The DRC gain can be set using the DRCG bits (Bits[5:2]) in Register 0x8C, Register 0x9C, and Register 0xAC. The range available is −24 dB to +21 dB. See Table 19 for a listing of the DRC detector selection registers and bits and their functions.

Table 20 lists the registers and bits that control the dynamic behavior of the DRC.

Table 19. DRC Setting Bits and Functions

Register Address	Bits	Bit Name	Description
0x8C, 0x9C, 0xAC	[5:2]	DRCG	Sets the DRC gain; available range is from −24 dB to +21 dB.
0x8D, 0x9D, 0xAD	7	DRCNGTGT	Sets the DRC noise gate target.
0x8D, 0x9D, 0xAD	6	DRCNGHDEN	Enables or disables the DRC noise gate recovery hold.
0x8D, 0x9D, 0xAD	5	DRCNGSRC	Selects the DRC noise gate level detector; selects either rms or peak detector.
0x8D, 0x9D, 0xAD	4	DRCCESRC	Selects the DRC compressor/expander level detector; selects either rms or peak detector.
0x8D, 0x9D, 0xAD	3	DRCLMSRC	Selects the DRC limiter level detector; selects either rms or peak detector.
0x8D, 0x9D, 0xAD	2	DRCNGEN	Noise gate enable control; provides independent noise gate control.
0x8D, 0x9D, 0xAD	[1:0]	DRCEN	DRC enable control; enables or disables the DRC. The input source for the DRC can be selected as left channel, right channel, or both.

Table 20. DRC Dynamic Behavior Control

Register Address	Bits	Bit Name	Description
0x80, 0x90, 0xA0	[3:0]	DRCLELTAV	Sets rms signal detector averaging time. Available range is from 750 µs to 24.576 sec.
0x81, 0x91, 0xA1	[7:4]	DRCLELATT	Sets DRC attack time. Available range is 46.875 µs to 1.536 sec.
0x81, 0x91, 0xA1	[3:0]	DRCLELDEC	Sets DRC decay (release) time. Available range is 0.75 ms to 24.576 sec.
0x8A, 0x9A, 0xAA	[7:4]	DRCGSATT	Sets DRC gain smooth attack time. Available range is 46.875 µs to 1.536 sec.
0x8A, 0x9A, 0xAA	[3:0]	DRCGSDEC	Sets DRC gain smooth decay time. Available range is 0.75 ms to 24.576 sec.
0x8B, 0x9B, 0xAB	[7:4]	DRCHTNOR	Sets DRC normal operation hold time. Available range is from 0 ms up to 1.37 sec; value increments by 2× the previous value, beginning with 0.67 ms.
0x8B, 0x9B, 0xAB	[3:0]	DRCHTNG	Sets DRC noise gate hold time. Available range is from 0 ms up to 1.37 sec; value increments by 2× the previous value, beginning with 0.67 ms.

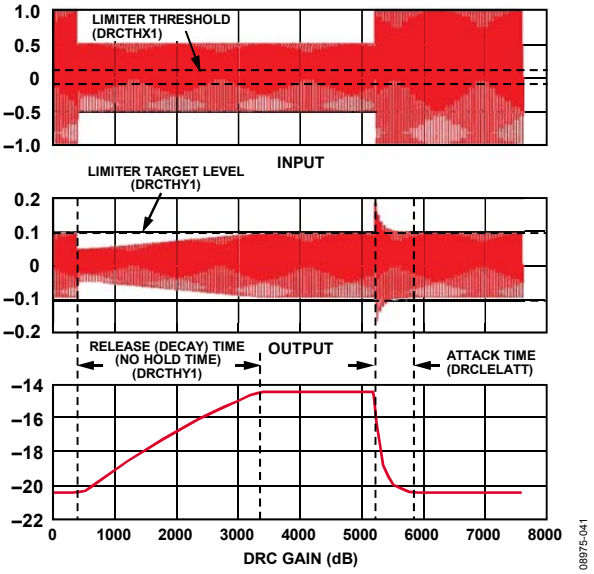


Figure 108. Limiter Dynamic Behavior—Working Example

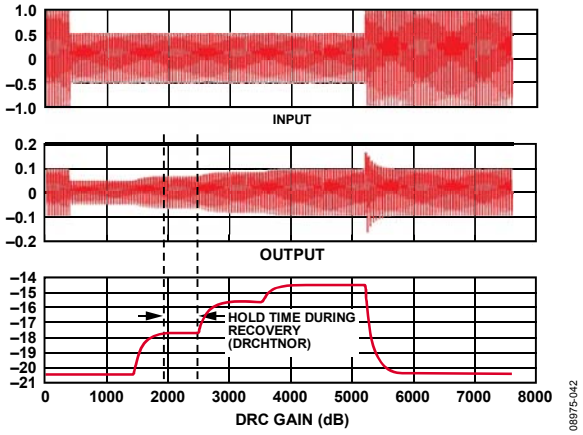


Figure 109. Limiter Dynamic—Working Example Showing Hold Time

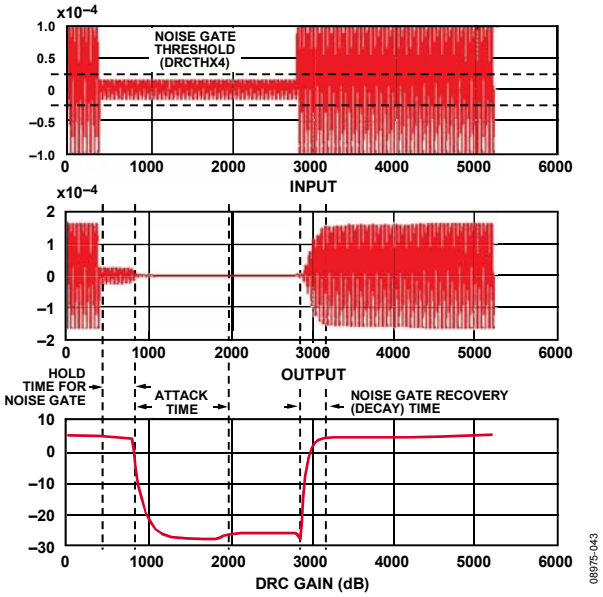


Figure 110. Noise Gate Dynamic—Working Example

Working Example

If the required LPF cutoff frequency is 20 kHz, the HPF cutoff frequency is 350 Hz, low band crossover frequency is 1 kHz, and high band crossover frequency is 8 kHz, as shown in Figure 111.

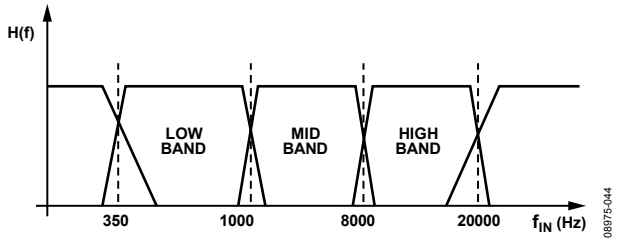


Figure 111. MDRC Example

The DRC can generate an interrupt request when enabled. See Table 21 for a listing of the interrupt request register and bit controls.

- To configure MDRC HPF and LPF, set Register 0xB0 to 0x1A.
- To configure MDRC crossover frequencies, set Register 0xB1 to 0x79.
- To enable MDRC HPF and LPF, set Register 0xB2 to 0x07.

Table 21. Interrupt Request Register and Bit Controls

Register Address	Bits	Bit Name	Function
0x8F, 0x9F, 0xAF	1	DRCIRQ_MODE	DRC interrupt mode. 0: selects the input signal rms value as the interrupt source; 1: selects the ratio between the peak and rms signal of the input signal.
0x8F, 0x9F, 0xAF	0	DRCIRQ_EN	DRC interrupt enable.
0x8E, 0x9E, 0xAE	[6:2]	SIG_DET_RMS	RMS detector level. Defines the rms value above which the IRQ circuits send out the interruption signal when the DRCIRQ_MODE bit = 0. Available range: −76.5 dB to −30 dB.
0x8E, 0x9E, 0xAE	[1:0]	SIG_DET_PK	Peak to rms detector ratio. Defines the peak to rms value above which the IRQ circuits send out the interruption signal when the DRCIRQ_MODE bit = 1. Available range: 12 dB to 30 dB.

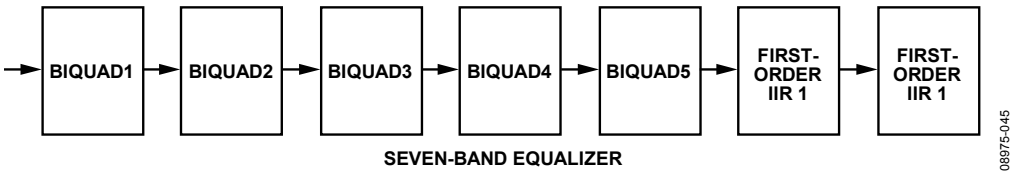


Figure 112. Seven-Band Equalizer Block Diagram

PROGRAMMABLE SEVEN-BAND EQUALIZER

The programmable seven-band equalizer is composed of five biquad filters (Band 1 to Band 5) and two first-order IIR filters (Band 6 and Band 7). See Figure 112 for a system block diagram.

The EQ shares Register 0x80 through Register 0xBD with the MDRC. All the filter coefficients are programmable via the corresponding registers. The filter bank can also be configured as some other filters, including de-emphasis and notch filter, when all five midfrequency bands are not needed.

Table 22. Register 0x80 to Register 0xBD EQ Coefficients

Register Address	Bit Name	Descripton
0x80	EQ1_COEF0_HI[15:8]	EQ Band 1, Coefficient 0 MSB
0x81	EQ1_COEF0_LO[7:0]	EQ Band 1, Coefficient 0 LSB
0x82	EQ1_COEF1_HI[15:8]	EQ Band 1, Coefficient 1 MSB
0x83	EQ1_COEF1_LO[7:0]	EQ Band 1, Coefficient 1 LSB
0x84	EQ1_COEF2_HI[15:8]	EQ Band 1, Coefficient 2 MSB
0x85	EQ1_COEF2_LO[7:0]	EQ Band 1, Coefficient 2 LSB
...	...	...
0xBC	EQ7_COEF2_HI[15:8]	EQ Band 7, Coefficient 2 MSB
0xBD	EQ7_COEF2_LO[7:0]	EQ Band 7, Coefficient 2 LSB

To operate as a seven-band equalizer, the two first-order IIR filters are usually configured as one low-pass shelving filter and one high-pass shelving filter, and the biquad filters are configured as peak filters.

The first-order IIR filter cutoff frequency and gain are adjustable using the filter coefficient registers. In addition, the five biquad filters have adjustable gain, the center frequency for the peak filters, or cutoff frequency for shelving filters. For a frequency band that is <200 Hz, the low-pass shelving filter is recommended instead of a peak filter.

The biquad common peaking filter transfer function for Band 1 through Band 5 is as follows:

$$H(z) = \frac{p0 + p1 \times z^{-1} + p2 \times z^{-2}}{1 - d1 \times z^{-1} - d2 \times z^{-2}}$$

The shelving filter transfer function for Band 6 and Band 7 is

$$H(z) = \frac{p0 + p1 \times z^{-1}}{1 - d1 \times z^{-1}}$$

The filter coefficients can be calculated using the previous two equations or by using the GUI provided. See the Register Map—EQ Coefficients section for register addresses.

Register 0xBE and Register 0xBF are used for EQ control. The EQ_FORMAT bit (Register 0xBE, Bit 2) defines the coefficient bit format. The default setting is 0, and the corresponding format is Q3.13. In this default mode, the supported coefficients range from −4 ~ +4. For equalization, this range means that the cutoff/center frequencies can vary from 40 Hz to 12 kHz when the input sampling rate is 48 kHz, and peak gain varies from −18 dB to +18 dB. When Register 0xBE, Bit 2 = 1, the EQ format changes to Q4.12 to achieve a larger coefficient range (from −8 ~ +8). This mode enables larger gain boost or cut range.

On-the-fly coefficient updates are supported. If the filter bank coefficients are updated in this mode, the EQ_UPD bit (Bit 1, Register 0xBE) should be set to 1 after the I²C coefficient write finishes. This setting updates the filter coefficients for the filter desired. The coefficient update procedure takes about 0.05 ms.

The EQ_UPDING bit (Bit 4, Register 0xBE) is a read-only bit that represents the coefficient update status. This bit should be read to check the status of the coefficient update process. When the EQ_UPDING bit is set to 1, the update is in process; when the EQ_UPDING bit is set to 0, the update is complete.

If the system clock is lost during the updating period, the update procedure cannot be completed and, in such a case, it is recommended that the EQ_UPD_CLR bit (Bit 3, Register 0xBE) be set to 1 to cancel the update.

Register 0x80 to Register 0xBD make up the EQ coefficient address. These addresses are also used by other registers. Therefore, when the EQ coefficient read/write access is required, the write/read enable bit, EQ_WR_EN (Register 0xBE, Bit 0), should be set to 1.

Register 0xBF is used for EQ enable/disable control. To save power, the filter bank can be disabled, and all of the seven bands can be bypassed. Bit EQEN and Bit EQBP7 to Bit EQBP1 in Register 0xBF can be used to enable or disable the desired EQ band.

Table 23. Bit Map of Register 0xBE, EQ_CTRL1

D7	D6	D5	D4	D3	D2	D1	D0
RESERVED			EQ_UPDING	EQ_UPD_CLR	EQ_FORMAT	EQ_UPD	EQ_WR_EN

Table 24. Bit Descriptions for Register 0xBE, EQCTRL1

Bit Name	Description	Bit Settings
EQ_UPDING	EQ coefficient update status	0: EQ coefficient update is complete or no update 1: EQ coefficient updating
EQ_UPD_CLR	EQ coefficient update cancel	0: normal operation 1: cancel/interrupt EQ coefficient update
EQ_FORMAT	EQ coefficient format selection	0: normal operation 1: large gain
EQ_UPD	EQ coefficient registers update flag	1: update 0: no update
EQ_WR_EN	EQ coefficient read/write enable	1: EQ coefficient read/write enable 0: EQ coefficient read/write disable

Table 25. Bit Map of Register 0xBF, EQ_CTRL2

D7	D6	D5	D4	D3	D2	D1	D0
EQEN	EQBP7	EQBP6	EQBP5	EQBP4	EQBP3	EQBP2	EQBP1

Table 26. Bit Descriptions for Register 0xBF, EQCTRL2

Bit Name	Description	Bit Settings
EQEN	EQ enable	1: EQ enabled 0: EQ disabled
EQBP7	EQ Band 7 bypass when EQ enabled	1: bypass EQ Band 7 0: no bypass
EQBP6	EQ Band 6 bypass when EQ enabled	1: bypass EQ Band 6 0: no bypass
EQBP5	EQ Band 5 bypass when EQ enabled	1: bypass EQ Band 5 0: no bypass
EQBP4	EQ Band 4 bypass when EQ enabled	1: bypass EQ Band 4 0: no bypass
EQBP3	EQ Band 3 bypass when EQ enabled	1: bypass EQ Band 3 0: no bypass
EQBP2	EQ Band 2 bypass when EQ enabled	1: bypass EQ Band 2 0: no bypass
EQBP1	EQ Band 1 bypass when EQ enabled	1: bypass EQ Band 1 0: no bypass

COEFFICIENT CALCULATIONS

Peak Filter Setting

With f_S as the input signal sampling frequency, f_C as the required peak filter center frequency, BW as the bandwidth, and G (dB) as the gain, use the following steps for coefficient calculation:

1. Transfer the gain in decibels (dB) to decimal domain.

$$k = 10^{\frac{G}{20}}$$

2. Calculate the double precision coefficients.

$$\alpha = \frac{(1 - \sin(\frac{BW}{f_S} \times 2\pi))}{\cos(\frac{BW}{f_S} \times 2\pi)}$$

$$\beta = \cos(\frac{f_C}{f_S} \times 2\pi)$$

$$p0 = \frac{(1+k) + (1-k) \times \alpha}{2}$$

$$p1 = -(1+\alpha) \times \beta$$

$$p2 = \frac{(1-k) + (1+k) \times \alpha}{2}$$

$$d1 = (1+\alpha) \times \beta$$

$$d2 = -\alpha$$

3. Transfer the double precision coefficients to integer values represented by registers.

$p0 = round(p0 \times 8192)$
$p1 = round(p1 \times 8192)$
$p2 = round(p2 \times 8192)$
$d1 = round(d1 \times 8192)$
$d2 = round(d2 \times 8192)$

4. Transfer the decimal integer values to 16-bit, twos complement hexadecimal values.

Low-Pass Shelving Filter

The low-pass shelving filter transfer function is

$$H(z) = \frac{p0 + p1 \times z^{-1}}{1 - d1 \times z^{-1}}$$

With f_S as the input signal sampling frequency, f_C as the required filter cutoff frequency, and G (dB) as the gain, use the following steps for coefficient calculation:

1. Transfer the gain in decibels (dB) to decimal domain.

$$k = 10^{\frac{G}{20}}$$

2. Calculate the double precision coefficients.

$$\alpha = \frac{(1 - \sin(\frac{f_C}{f_S} \times 2\pi))}{\cos(\frac{f_C}{f_S} \times 2\pi)}$$

$$p0 = \frac{(1+k) + (1-k) \times \alpha}{2}$$

$$p1 = \frac{(k-1) + (1+k) \times \alpha}{2}$$

$$d1 = \alpha$$

3. Transfer the double precision coefficients to integer values represented by registers.

$p0 = round(p0 \times 8192)$
$p1 = round(p1 \times 8192)$
$d1 = round(d1 \times 8192)$

4. Transfer the decimal integer values to twos complement hexadecimal values.

High-Pass Shelving Filter

The high-pass shelving filter transfer function is

$$H(z) = \frac{p0 + p1 \times z^{-1}}{1 - d1 \times z^{-1}}$$

With f_S as the input signal sampling frequency, f_C as the required filter cutoff frequency, and G (dB) as the gain, use the following steps for coefficient calculation:

1. Transfer the gain in decibels (dB) to decimal domain.

$$k = 10^{\frac{G}{20}}$$

2. Calculate the double precision coefficients.

$$\alpha = \frac{(1 - \sin(\frac{f_C}{f_S} \times 2\pi))}{\cos(\frac{f_C}{f_S} \times 2\pi)}$$

$$p0 = \frac{(1+k) - (1-k) \times \alpha}{2}$$

$$p1 = \frac{(1-k) - (1+k) \times \alpha}{2}$$

$$d1 = \alpha$$

3. Transfer the double precision coefficients to integer values represented by registers.

$p0 = round(p0 \times 8192)$

$p1 = round(p1 \times 8192)$

$d1 = round(d1 \times 8192)$

4. Transfer the decimal integer values to twos complement hexadecimal values.

Worked Examples

The following examples illustrate how to calculate the coefficients for the desired peak and low-pass/high-pass shelving filter.

Low-Pass Shelving Filter

If Band 6 is intended to operate as a low-pass shelving filter and the cutoff frequency of the filter is 80 Hz, peak gain is 6 dB, and input signal sampling frequency is 48 kHz, the coefficients are as follows:

$$k = 10^{(\frac{6}{20})} = 1.995262314968880$$

$$\alpha = \frac{(1 - \sin(\frac{80}{48000} \times 2\pi))}{\cos(\frac{80}{48000} \times 2\pi)} = 0.989582475318754$$

$$p0 = \frac{(1 + k) + (1 - k) \times \alpha}{2} = 1.005184084865251$$

$$p1 = \frac{(k - 1) - (1 + k) \times \alpha}{2} = -0.984398390453503$$

$$p2 = 0$$

$$d1 = \alpha = 0.989582475318754$$

$$d2 = 0$$

1. Transfer the coefficients to integer numbers:

   $p0 = round(1.005184084865251 \times 8192) = 8234$
   $p1 = round(-0.984398390453503 \times 8192) = -8064$
   $p2 = 0$
   $d1 = round(0.989582475318754 \times 8192) = 8107$
   $d2 = 0$

2. Represent the integer coefficients by 16-bit, twos complement hexadecimal values:

   p0 = 16-bit 0x202A
   p1 = 16-bit 0xE080
   p2 = 16-bit 0x0000
   d1 = 16-bit 0x1FAB
   d2 = 16-bit 0x0000

3. Therefore, the registers representing EQ1 coefficients should be set as follows:

   EQ6 COEF0M = 8'0x20, EQ6 COEF0L = 8'0x2A;
   EQ6 COEF1M = 8'0xE0, EQ6 COEF1L = 8'0x80;
   EQ6 COEF2M = 8'0x1F, EQ6 COEF2L = 8'0xAB

Peak Filter

If Band 1 is intended to operate as a peak filter with a filter center frequency of 240 Hz, the bandwidth is 120 Hz, peak gain is 6 dB, and the input signal sampling frequency is 48KHz, then the coefficients are as follows:

$$k = 10^{(\frac{6}{20})} = 1.995262314968880$$

$$\alpha = \frac{(1 - \sin(\frac{120}{48000} \times 2\pi))}{\cos(\frac{120}{4800} \times 2\pi)} = 0.984414127416097$$

$$\beta = \cos(\frac{240}{48000} \times 2\pi) = 0.999506560365732$$

$$p0 = \frac{(1 + k) + (1 - k) \times \alpha}{2} = 1.007756015814333$$

$$p1 = -(1 + \alpha) \times \beta = -1.983434938834828$$

$$p2 = \frac{(1 - k) + (1 + k) \times \alpha}{2} = 0.976658111601764$$

$$d1 = (1 + \alpha) \times \beta = 1.983434938834828$$

$$d2 = -\alpha = -0.984414127416097$$

1. Transfer the coefficients to integer numbers:

   $p0 = round(1.007756015814333 \times 8192) = 8256$
   $p1 = round(-1.983434938834828 \times 8192) = -16248$
   $p2 = round(0.976658111601764 \times 8192) = 8000$
   $d1 = round(1.983434938834828 \times 8192) = 16248$
   $d2 = round(-0.984414127416097 \times 8192) = -8064$

2. Represent the integer coefficients by 16-bit, twos complement hexadecimal values:

   p0 = 16-bit 0x2040
   p1 = 16-bit 0x1F40
   p2 = 16-bit 0x1F41
   d1 = 16-bit 0x3F78
   d2 = 16-bit 0xE080

3. Therefore, the registers representing EQ1 coefficients should be set as follows:

   EQ1 COEF0M = 8'0x20, EQ1 COEF0L = 8'0x40;
   EQ1 COEF1M = 8'0x1F, EQ1 COEF1L = 8'0x40;
   EQ1 COEF2M = 8'0x1F, EQ1 COEF2L = 8'0x41;
   EQ1 COEF3M = 8'0x3F, EQ1 COEF3L = 8'0x78;
   EQ1 COEF4M = 8'0xE0, EQ1 COEF4L = 8'0x80

High-Pass Shelving Filter

If Band 7 is intended to operate as a high-pass shelving filter and the cutoff frequency of the filter is 6 kHz, peak gain is 6 dB, and the input signal sampling frequency is 48 kHz, the coefficients are as follows:

$$k = 10^{(\frac{6}{20})} = 1.995262314968880$$

$$\alpha = \frac{(1 - \sin(\frac{6000}{48000} \times 2\pi))}{\cos(\frac{6000}{48000} \times 2\pi)} = 0.414213562373095$$

$$p0 = \frac{(1+k) - (1-k) \times \alpha}{2} = 1.703756731973916$$

$$p1 = \frac{(1-k) - (1+k) \times \alpha}{2} = -1.117970294347011$$

$p2 = 0$

$d1 = \alpha = 0.414213562373095$

$d2 = 0$

1. Transfer the coefficients to integer numbers:

   $p0 = round(1.703756731973916 \times 8192) = 13957$
   $p1 = round(-1.117970294347011 \times 8192) = -9158$
   $p2 = 0$
   $d1 = round(0.414213562373095 \times 8192) = 3393$
   $d2 = 0$

2. Represent the integer coefficients using 16-bit, twos complement hexadecimal values:

   p0 = 16-bit 0x3685
   p1 = 16-bit 0xDC3A
   p2 = 16-bit 0x0000
   d1 = 16-bit 0x0D41
   d2 = 16-bit 0x0000

3. Therefore, the registers representing the EQ7 coefficients should be set as follows:

   EQ7 COEF0M = 8'0x36, EQ7 COEF0L = 8'0x85;
   EQ7 COEF1M = 8'0xDC, EQ7 COEF1L =8'0x3A;
   EQ7 COEF2M = 8'0x0D, EQ7 COEF2L = 8'0x41

BASS ENHANCEMENT

The bass enhancement block can be used to increase the low frequency content of the stereo signal. Register 0x7E and Register 0x7F can be used to set the parameters of the block (see Table 27 and Table 28).

The left and right channels sum together to perform the bass enhancement algorithm. If only the left channel is selected, the left channel performs the desired flow alone. The input selection for the block is available via the BASS_SEL bits (Register 0x7F, Bits[1:0]). The input to the block is low-pass filtered. The cutoff frequency for the low-pass filter (LPF) can be set using the BASS_LPF bit (Register 0x7E, Bit 5). The signal is passed through the clipper, which generates the harmonics of the input signal. The clipper threshold can be set using the BASS_CUT bits (Register 0x7E, Bits[4:2]). The input signal that exceeds the clip threshold is clipped. The clipped signal is then passed through the band-pass filter, which removes the low and high frequency content. This bass-rich signal is then mixed with the high-pass filtered version of the input signal to form the final processed signal. The BASS_SPK bits (Register 0x7E, Bits[1:0]) can be used to set the low cutoff frequency of the speaker in the system to prevent overloading of the speaker. The gain can be set using the BASS_GAIN bits (Register 0x7F, Bits[4:2]).

Table 27. Bit Map of Register 0x7E and Register 0x7F

Reg. Addr.	7	6	5	4	3	2	1	0
0x7E			BASS_LPF	BASS_CUT[2:0]			BASS_SPK[1:0]	
0x7F				BASS_GAIN[2:0]			BASS_SEL[1:0]	

Table 28. Register 0x7E and Register 0x7F Bit Descriptions

Reg. Addr.	Bits	Bit Name	Description
0x7E	[7:6]	RESERVED	Reserved
	5	BASS_LPF	Bass output frequency range 0: 801 Hz 1: 1001 Hz
	[4:2]	BASS_CUT	Bass signal extend density (clip level) 000: Reserved 001: 0.125 …: Step size of 0.125 111: 0.875
	[1:0]	BASS_SPK	Cutoff frequency setting 00: 158 Hz 01: 232 Hz 10: 347 Hz 11: 520 Hz
0x7F	[7:5]	RESERVED	Reserved
	[4:2]	BASS_GAIN	Bass enhancement gain 000: Reserved; not open to user 001: 0 dB 010: 6 dB 011: 9.5 dB 100: 12 dB 101: 14 dB 110: 15.5 dB 111: 17 dB
	[1:0]	BASS_SEL	Left/right channel selection 00: both channels off 01: left channel on 10: right channel on 11: both channels on

3D ENHANCEMENT

The 3D enhancement block can be used to widen the stereo separation between the left and right signals.

Table 29 and Table 30 show the two 3D enhancement registers, E3D_CTRL1 and E3D_CTRL2 (Address 0xC0 and Address 0xC1, respectively). These registers provide control to enhance the depth and level of the signal. The low-pass filter cutoff frequency determines the frequency at which the effect begins to occur. The 3D enhancement increases the gain of the signal, which can be controlled by the E3D_GAIN bits (Register 0xC1, Bits[3:1]). In addition, the depth of the 3D effect can be adjusted using the E3D_ALPHA bits (Register 0xC0, Bits[3:0]). The depth must be set to the desired effect based on the signal and setup.

Table 29. Bit Descriptions for Register 0xC0, E3D Enhancement Control 1 (E3D_CTRL1)

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	E3D_LEVEL		3D enhancement level control	0x0	RW
		0000	0%, no 3D effect		
		0001	6.67%		
		0010	13.33%		
		0011	20%		
		0100	26.67%		
		0101	33.33%		
		0110	40%		
		0111	46.67%		
		1000	53.33%		
		1001	60%		
		1010	66.67%		
		1011	73.33%		
		1100	80%		
		1101	86.67%		
		1110	93.33%		
		1111	100%		
[3:0]	E3D_ALPHA		3D separate filter cutoff frequency	0x0	RW
		0000	No 3D effect		
		0001	1.5 kHz at 48 kHz sampling rate		
		0010	2.2 kHz at 48 kHz sampling rate		
		0011	3.6 kHz at 48 kHz sampling rate		
		0100	5.5 kHz at 48 kHz sampling rate		
		0101	8.1 kHz at 48 kHz sampling rate		
		0110	13 kHz at 48 kHz sampling rate		

Table 30. Bit Descriptions for E3D Enhancement Control 2, Register 0xC1 (E3D_CTRL2)

Bits	Bit Name	Settings	Description	Reset	Access
[3:1]	E3D_GAIN		3D enhancement gain setting	0x0	RW
		000	E3D gain: 1		
		001	E3D gain: 0.125		
		010	E3D gain: 0.25		
		011	E3D gain: 0.375		
		100	E3D gain: 0.5		
		101	E3D gain: 0.625		
		110	E3D gain: 0.75		
		111	E3D gain: 0.875		
0	E3D_EN		3D enhancement enable control	0x0	RW
		0	Enhancement disable		
		1	Enhancement enable		

DIGITAL AUTOMATIC LEVEL CONTROL (ALC)

The automatic level control (ALC) provides continuous adjustment of the input PGA in response to the rms amplitude of the input signal to maintain it at a constant level, which is defined by the ALCREF bits (Register 0xC4, Bits[3:0]). A digital peak detector monitors the input signal amplitude and limits it to the register-defined threshold level, using the ALCLVL bits (Register 0xC4, Bits[7:4]).

The ALC provides control over analog PGA and digital PGA, which can be selected individually or together.

To reduce the gain during the silent portion of the speech or music signal, the ALC provides a noise gate that can be operated in four different modes, as defined by the NGMODE bits (Register 0xC8, Bits[5:4]).

- Noise Gate Mode 1. Maintains the gain at the level it was before the ALC entered into noise gate mode.
- Noise Gate Mode 2. Sets the PGA gain to 0 dB.
- Noise Gate Mode 3. Mutes the ALC output.
- Noise Gate Mode 4. Noise gate function is disabled.

The ALC can be enabled or disabled for the left or right channel or for both channels via the ALCEN bits (Register 0xC8, Bits[3:2]).

If the rms value of the signal falls below the ALC target threshold (as defined by the ALCREF bits), the ALC increases the gain of the PGA at the rate set by the ALCREC bits (Register 0xC3, Bits[3:0]). If the signal is above the threshold, the ALC reduces the gain of the PGA at a rate that is set by the ALCATT bits (Register 0xC3, Bits[7:4]).

Because the dc offset introduced by the analog circuits greatly influences ALC operation, it is recommended that the HPF included in the ALC block be enabled when the ALC is enabled.

Peak Limiter Level

To prevent clipping during high level signals, the ALC circuit includes a limiter function. If the ALC input signal exceeds the peak level threshold (as defined by the ALCLVL bits), the PGA gain is ramped down as per the attack time set by the ALCATT bits until the signal level falls below that threshold. This function is automatically enabled when the ALC is enabled. The peak limiter level can be set using the ALCLVL bits. The level can be set from −22.5 dBFs to 0 dBFS in 16 steps.

ALC Target level

When the signal level is below the peak limiter threshold, the ALC attempts to maintain a constant signal level by increasing or decreasing the gain of the PGA. That constant level is defined as the ALC target level, which is set by the ALCREF bits. The level can be set from −24 dBFS to −1.5 dBFS in 16 steps.

ALC Maximum Gain

The ALCMAX bits (Register 0xC5, Bits[3:0]) set the maximum gain value that the PGA can reach while under the control of the ALC. The available gain range is −12 dB to +60 dB in 13 steps.

RMS Average Time

The rms average time is the time taken for the rms value estimation. It is set by the ALCTAV bits (Register 0xC2, Bits[7:4]). The averaging time range is 1.5 ms to 6.144 sec in 13 steps.

Target Level Ripple Remove

The ALCRIP bits (Register 0xC5, Bits[7:4]) define the ALC target level ripple range. When the input signal rms level is within this range, the ALC gain does not change. The ripple range can be set from 0 dB to −7.5 dB in 16 steps.

For example, if the ALC target level is −6 dB, the ripple is defined as 0.5 dB, and the detected rms value of the input signal is between −6 dB and −6.5 dB, the ALC gain does not change.

Attack (Gain Ramp-Down) Time

Attack time, which is set by the ALCATT bits, is the time that is required for the PGA gain to ramp down through 90% of its range. Therefore, the time for the recording level to return to its target value (limit operation threshold) depends on both the attack time and the gain adjustment required. If the gain adjustment is small, the real adjustment time is less than the attack time. The attack time range is from 1.5 ms to 6.144 sec in 13 steps. In mute condition, this is the mute attack time.

Decay/Recovery (Gain Ramp-Up) Time

Decay time, which is set by the ALCREC bits, is the time that is required for the PGA gain to ramp up to 90% of its range. Therefore, the time required for the recording level to return to its target value (recovery threshold) depends on both the decay time and the gain adjustment required. If the gain adjustment is small, the real adjustment time is less than the decay time. The recovery time ranges from 6 ms to 24.576 sec in 16 steps.

Recovery Hold Time

Recovery hold time, set by the ALCHLD bits (Register 0xC2, Bits[3:0]), is the time delay between the detection of the signal level below the recovery threshold and the PGA gain beginning to ramp up. The hold time applies only to gain ramp-up; there is no delay before the gain ramping down when the signal level is above target. The hold time range is 0 ms to 5.468 sec in 13 steps.

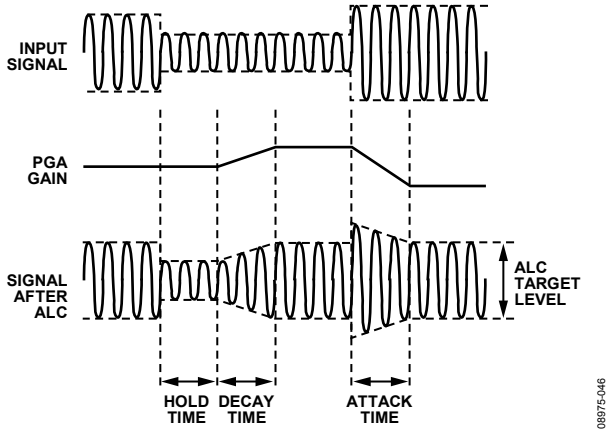


Figure 113. Digital PGA and ALC Decay Time, Hold Time, and Attack Time

Noise Gate Mode

When the signal is very quiet and consists mainly of noise, the ALC function may cause a phenomenon called noise pumping. The ALC, when disabled, treats the noise as a normal signal without any processing; when the ALC is enabled, the noise gate function is enabled. The noise gate prevents noise pumping by comparing the signal level at the input against a noise gate threshold. When the ALC noise gate function is enabled, there are three optional modes, as follows:

- Noise Gate Mode 1. Keeps the PGA gain as a constant when the ALC enters into noise gate.
- Noise Gate Mode 2. Sets the PGA gain to 0.
- Noise Gate Mode 3. Mutes the ALC output to −120 dB.

The noise gate mode is set by the NGMODE bits (Register 0xC8, Bits[5:4]). The ALCNGATT bits (Register 0xC7, Bits[7:4]) define the gain reduction rate for Noise Gate Mode 2 and Noise Gate Mode 3. In addition, when the ALC recovers from noise gate mode, the ALCNGREC bits (Register 0xC7, Bits[3:0]) set the PGA to increase to 0 dB at this rate at first; then the ALC enters the attack or recovery phase.

Before the ALC enters into recovery mode, the ALC gain can be held constant for some time. This hold time can be disabled or enabled by the HLDRST bit (Register 0xC8, Bit 7). For Noise Gate Mode 1, it is recommended that this bit be set to 1; for Noise Gate Mode 2 and Noise Gate Mode 3, this bit should be set to 0.

Noise Gate Attack Time

The noise gate attack time, which is set by the ALCNGATT bits, is the time constant used when the ALC begins its noise gate phase. This time constant is valid only in Noise Gate Mode 2 and Noise Gate Mode 3. The attack time ranges from 6 ms to 24.576 sec in 13 steps.

Noise Gate Recovery Time

The noise gate recovery time, which is set by the ALCNGREC bits (Register 0xC7, Bits[3:0]), is the time constant used when the ALC escapes from the noise gate. It is valid only in Noise Gate Mode 3. The recovery time ranges from 1.5 ms to 6.144 sec in 13 steps.

Noise Gate Hold Time

Noise gate hold time, which is set by the ALCNGHLD bits (Register 0xC6, Bits[3:0]), is the time between the detection of the signal level below the noise gate threshold and ALC entering into noise gate mode. The hold time range is 0 ms to 5.460 sec in 13 steps.

Noise Gate Threshold

The noise gate threshold, which is set by the ALCNGTH bits (Register 0xC6, Bits[7:4]), defines the noise level below which the signal is considered as noise. The noise gate threshold ranges from −81 dBFS to −36 dBFS in 16 steps.

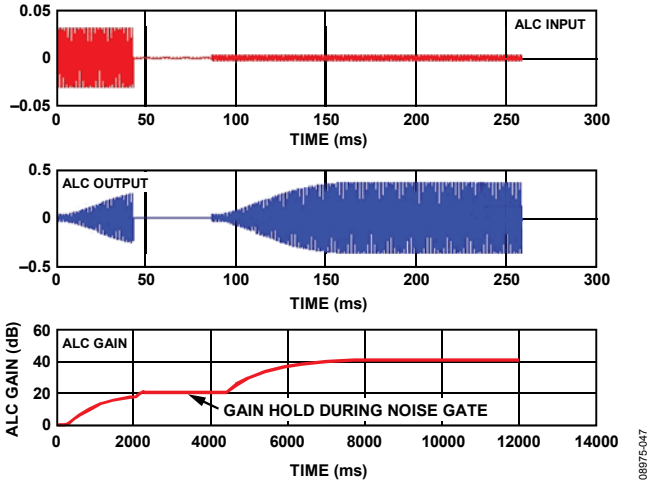


Figure 114. Noise Gate Mode 1

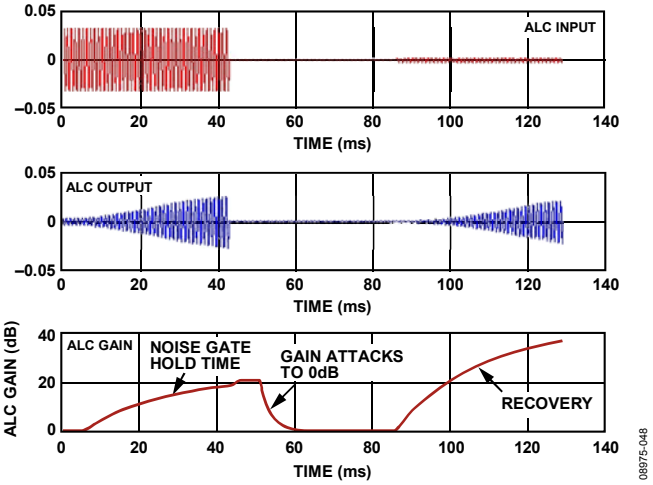


Figure 115. Noise Gate Mode 2

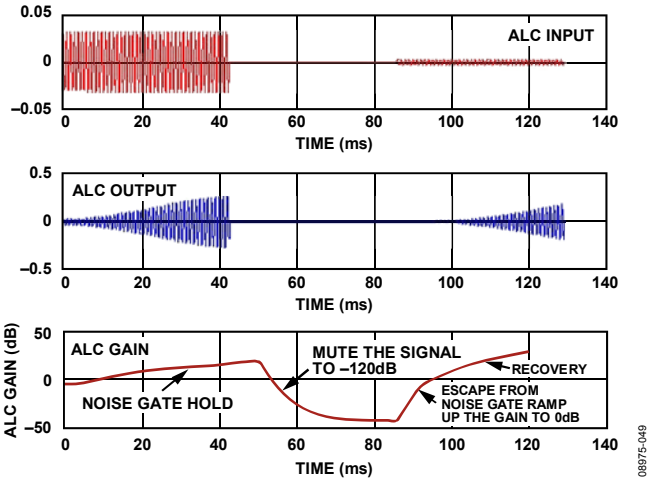


Figure 116. Noise Gate Mode 3

INTERRUPT REQUEST (IRQ)

The ADAU1373 can generate an interrupt request based on selected events from the various internal blocks. The interrupt controller receives inputs from the MICBIAS current detect, ASRC unlock detect, DRC signal activity detect, PLL unlock detect, jack detect, and analog fault detect. Three registers are provided for this function: Register 0xE5 can be used to set the mask for the interrupts, Register 0xE6 stores the raw status of the interrupts, and Register 0xE7 stores the status of the interrupts after mask. The generation of interrupts can be enabled or disabled using Register 0xE8, Bit 0.

The interrupts can be masked using the respective bits in Register 0xE5. A bit setting of 1 unmasks the faults and generates the interrupt request. The faults are reported in Register 0xE7. When faults are unmasked, the status bits in Register 0xE7 are latched until 1 is written to them. The raw status of the faults can be read in Register 0xE6.

In addition, any of the above interrupts can be used to initiate the IRQ (interrupt request) on the GPIOx pins. The four GPIO pins can be set for IRQ function using Register 0xE3 and Register 0xE4.

The following events are reported in the interrupt status register (Register 0xE6, IRQ_RAW):

- Unlocking of any of the three ASRCs. When either of the three ASRC loses lock, the respective ASRCx_IRQ_RAW_STATE bit is set.
- The DRC input level exceeding the threshold set in Register 0x8E, Register 0x9E, and Register 0xAE, which sets the DRC_IRQ_RAW_STATE.
- The on-chip PLL losing lock, which sets the PLL_UNLOCK_RAW_STATE bit.
- Any write to Register 0x36, Bits[1:0], which sets the HP_CFG_RAW_STATE bit.
- A change in the logic level at the JACKDET pin, which sets the HP_DECT_RAW_STATE bit.
- Occurrence of an analog fault, which sets the AFAULT_RAW_STATE bit.

The following analog faults can set the AFAULT_RAW_STATE bit:

- Earpiece amplifier overcurrent
- Speaker amplifier left channel overcurrent
- Speaker amplifier right channel overcurrent
- Headphone amplifier overcurrent or overtemperature

The overcurrent thresholds are fixed internally. The overtemperature fault is set when the die temperature exceeds 150°C ± 15°C.

The IRQs can be reported via GPIOx, or the IRQ_STATE register (Register 0xE7) can be read via the I^2C to determine which block is reporting a fault. The analog fault status in Register 0xE7 can be used in conjunction with Register 0x39 or Register 0x38 to differentiate among the analog faults.

Register 0x39 reports faults for an earpiece overcurrent, speaker amplifier overcurrent, headphone amplifier overcurrent, and die overtemperature.

In addition, Register 0x38 reports Microphone Bias 1 and Microphone Bias 2 current detect, as well as overcurrent and logic voltage changes at the JACKDET pin (Ball G5).

The MICB1THS and MICB2THS bits (Register 0x38, Bit 0 and Bit 2, respectively) can be used to detect the connection of the electret microphone at the MICBIASx pins (Ball C8 and Ball C9). When the electrets microphone is connected, the current flow from the MICBIASx pins to the microphone is detected. The current detection threshold can be set using Register 0x22. Four settings are provided: 150 μA (default), 330 μA, 510 μA, and 700 μA. Similarly, the overcurrent at the MICBIASx outputs can be detected. This allows for limiting the current drawn out of the internal microphone bias regulator in case of a short circuit at the MICBIASx pin. The overcurrent limit can be set to 330 μA, 700 μA, 1000 μA, or 1400 μA. The JACKDECT bit (Register 0x38, Bit 4) can be used to detect the insertion/ removal of the accessory at the headphone socket. When jack insertion is detected, the status bit is set to 1.

The ADC/DAC clock loss is reported in Register 0x37.

CONTROL PORTS

The ADAU1373 has a 2-wire I²C bus control port, which can be used to set the registers. The control port is capable of full read/write operation for all addressable registers. Operations such as mute and input/output mode control are programmed by writing to these registers.

All addresses can be accessed in either single-address mode or burst mode. The first byte (Byte 1) of a control port write contains the 7-bit chip address plus the R/$\overline{W}$ bit. The next byte (Byte 2) forms the subaddress of the register location within the ADAU1373. This subaddress must be a single byte long. All subsequent bytes (starting with Byte 3) contain the data to be written to the register. The number of bytes per word depends on the type of data that is being written.

The ADAU1373 provides several mechanisms for updating signal processing parameters in real time without causing pops or clicks.

The function of each of the two control port pins (SCL and SDA) is described in Table 31.

Table 31. Control Port Pin Functions

Pin Name	I²C Mode
SCL	Input clock
SDA	Open-collector input/output

I²C PORT

The ADAU1373 supports a 2-wire serial (I²C-compatible) microprocessor bus that drives multiple peripherals. Two pins, serial data (SDA) and serial clock (SCL), carry information between the ADAU1373 and the system I²C master controller. In I²C mode, the ADAU1373 is always a slave on the bus, meaning that it cannot initiate a data transfer. Each slave device is recognized by a unique address. The address and R/$\overline{W}$ byte format is shown in Table 32. The address resides in the first seven bits of the I²C write. The I²C address for the ADAU1373 is 0x1A. The LSB of the address (the R/$\overline{W}$ bit) specifies either a read or write operation. A Logic 1 corresponds to a read operation, and a Logic 0 corresponds to a write operation.

Burst mode addressing, where the subaddresses are automatically incremented at word boundaries, can be used for writing large amounts of data to contiguous registers. This increment happens automatically after a single word write unless a stop condition is encountered. A data transfer is always terminated by a stop condition.

The SDA and SCL pins should each have a 2 kΩ pull-up resistor to IOVDD5 (1.8 V to 3.3 V).

Table 32. I²C Address and Read/$\overline{\text{Write}}$ Byte Format

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	0	1	1	0	1	0	R/$\overline{W}$

Addressing

Initially, each device on the I²C bus is in an idle state and monitors the SDA and SCL lines for a start condition and the correct address. The I²C master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream follows. All devices on the bus respond to the start condition and shift the next eight bits (the 7-bit address plus the R/$\overline{W}$ bit), MSB first. The device that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This ninth bit is known as an acknowledge bit. All other devices withdraw from the bus at this point and return to the idle condition.

The R/$\overline{W}$ bit determines the direction of the data. A Logic 0 on the LSB of the first byte means that the master writes information to the peripheral, whereas a Logic 1 means that the master reads information from the peripheral after writing the subaddress and repeating the start address. A data transfer takes place until a stop condition is encountered. A stop condition occurs when SDA transitions from low to high while SCL is held high. Figure 117 shows the timing of an I²C single-byte write, and Figure 118 shows the timing of an I²C single-byte read.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, the ADAU1373 immediately jumps to the idle condition. During a given SCL high period, the user should issue only one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADAU1373 does not issue an acknowledge and returns to the idle condition.

If the user exceeds the highest subaddress while in autoincrement mode, one of two actions is taken. In read mode, the ADAU1373 outputs the highest subaddress register contents until the master device issues a no acknowledge, indicating the end of a read. In a no acknowledge condition, the SDA line is not pulled low on the ninth clock pulse on SCL. If the highest subaddress location is reached while in write mode, the data for the invalid byte is not loaded into any subaddress register, a no acknowledge is issued by the ADAU1373, and the part returns to the idle condition.

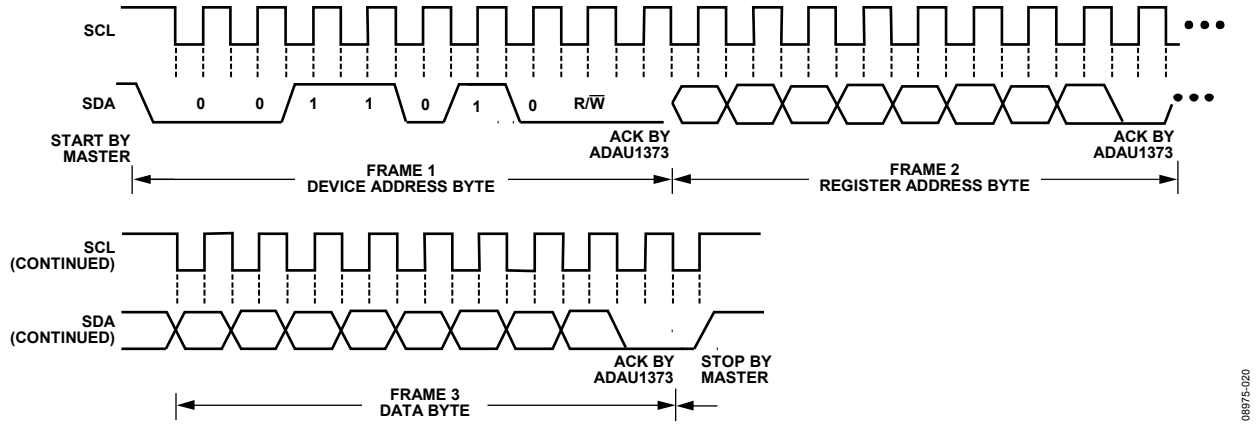


Figure 117. I²C Single Byte Write

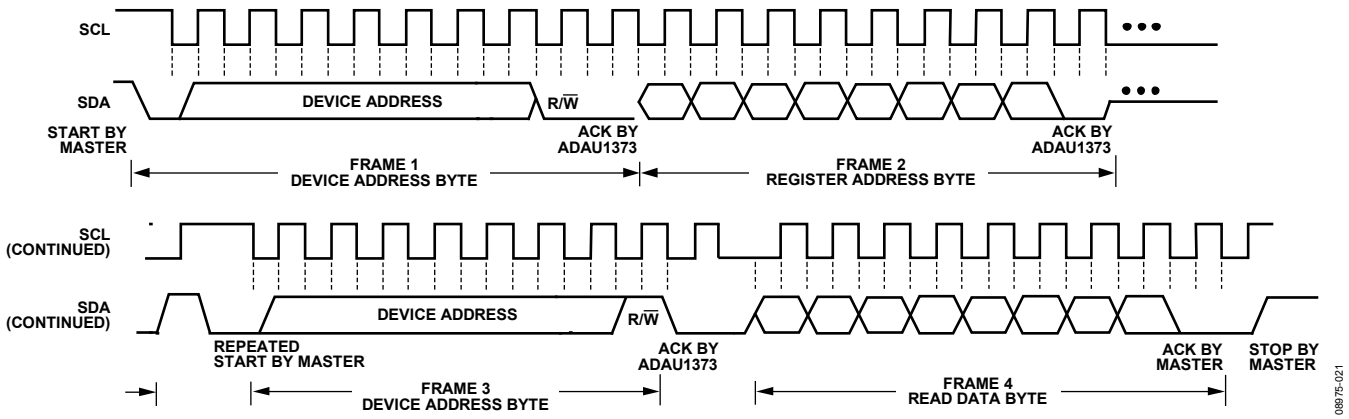


Figure 118. I²C Single Byte Read

I²C Read and Write Operations

Figure 119 shows the format of a single-word write operation. Every ninth clock pulse, the ADAU1373 issues an acknowledge by pulling SDA low.

Figure 120 shows the format of a burst mode write sequence. This figure shows an example of a write to sequential single-byte registers. The ADAU1373 increments its subaddress register after every byte because the requested subaddress corresponds to a register or memory area with a 1-byte word length.

Figure 121 shows the format of a single-word read operation. Note that the first R/$\overline{W}$ bit is set to 0, indicating a write operation. This is because the subaddress still needs to be written to set up the internal address. After the ADAU1373 acknowledges the receipt of the subaddress, the master must issue a repeated start command, followed by the chip address byte with the R/$\overline{W}$ bit set to 1 (read). This causes the ADAU1373 SDA to reverse and begin driving data back to the master. The master then responds every ninth pulse with an acknowledge pulse to the ADAU1373.

Figure 122 shows the format of a burst mode read sequence. This figure shows an example of a read from sequential single-byte registers. The ADAU1373 increments its subaddress register after every byte because the requested subaddress corresponds to a register or memory area with a 1-byte word length. The ADAU1373 always decodes the subaddress and sets the auto-increment circuit so that the address increments after the appropriate number of bytes.

Figure 119 to Figure 122 use the abbreviations shown in Table 33.

Table 33. Abbreviations for Read/Write Operations Format

Abbreviation	Description
S	Start bit
P	Stop bit
AM	Acknowledgment by master
AS	Acknowledgment by slave



Figure 119. Single-Word I²C Write Format

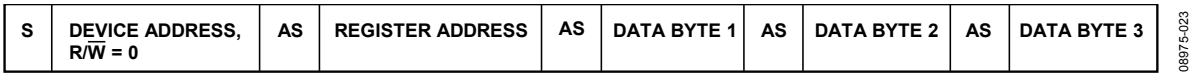


Figure 120. Burst Mode I²C Write Format

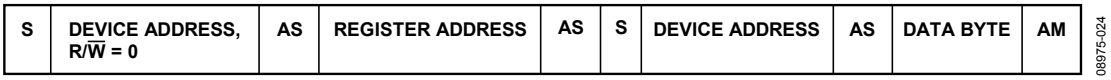


Figure 121. Single-Word I²C Read Format



Figure 122. Burst Mode I²C Read Format

REGISTER MAP SUMMARY (DEFAULT)

Table 34 is the summary of the control registers for the ADAU1373 in default mode using an MDRC, which can be accessed using an I²C port. Register 0x80 to Register 0xBD are shared with the seven-band EQ block. Refer to the EQ register map (see Table 245) for using the EQ function. Register addresses are in hexadecimal format.

Table 34. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
00	INPUT_MODE	[7:0]	GAINMODE3	GAINMODE2	GAINMODE1	GAINMODE0	INMODE3	INMODE2	INMODE1	INMODE0	0x00	RW
01	AIN1L_CTRL	[7:0]	RESERVED					AIN1LVOL			0x00	SRST
02	AIN1R_CTRL	[7:0]	RESERVED					AIN1RVOL			0x00	SRST
03	AIN2L_CTRL	[7:0]	RESERVED					AIN2LVOL			0x00	SRST
04	AIN2R_CTRL	[7:0]	RESERVED					AIN2RVOL			0x00	SRST
05	AIN3L_CTRL	[7:0]	RESERVED					AIN3LVOL			0x00	SRST
06	AIN3R_CTRL	[7:0]	RESERVED					AIN3RVOL			0x00	SRST
07	AIN4L_CTRL	[7:0]	RESERVED					AIN4LVOL			0x00	SRST
08	AIN4R_CTRL	[7:0]	RESERVED					AIN4RVOL			0x00	SRST
09	LLINE1_OUT	[7:0]	RESERVED					LLINE1			0x00	SRST
0A	RLINE1_OUT	[7:0]	RESERVED					RLINE1			0x00	SRST
0B	LLINE2_OUT	[7:0]	RESERVED					LLINE2			0x00	SRST
0C	RLINE2_OUT	[7:0]	RESERVED					RLINE2			0x00	SRST
0D	LCD_OUT	[7:0]	RESERVED					LCD			0x00	SRST
0E	RCD_OUT	[7:0]	RESERVED					RCD			0x00	SRST
0F	LHP_OUT	[7:0]	RESERVED					LHP			0x00	SRST
10	RHP_OUT	[7:0]	RESERVED					RHP			0x00	SRST
11	ADC_GAIN	[7:0]	ADCRGAIN3	ADCRGAIN2	ADCRGAIN1	ADCRGAIN0	ADCLGAIN3	ADCLGAIN2	ADCLGAIN1	ADCLGAIN0	0x00	RW
12	LADC_MIXER	[7:0]	RESERVED			ADCLMIX4	ADCLMIX3	ADCLMIX2	ADCLMIX1	ADCLMIX0	0x00	RW1C
13	RADC_MIXER	[7:0]	RESERVED			ADCRMIX4	ADCRMIX3	ADCRMIX2	ADCRMIX1	ADCRMIX0	0x00	RW1C
14	LLINE1MIX	[7:0]	LLINE1MIX7	LLINE1MIX6	LLINE1MIX5	LLINE1MIX4	LLINE1MIX3	LLINE1MIX2	LLINE1MIX1	LLINE1MIX0	0x00	RW1C
15	RLINE1MIX	[7:0]	RLINE1MIX7	RLINE1MIX6	RLINE1MIX5	RLINE1MIX4	RLINE1MIX3	RLINE1MIX2	RLINE1MIX1	RLINE1MIX0	0x00	RW1C
16	LLINE2MIX	[7:0]	LLINE2MIX7	LLINE2MIX6	LLINE2MIX5	LLINE2MIX4	LLINE2MIX3	LLINE2MIX2	LLINE2MIX1	LLINE2MIX0	0x00	RW1C
17	RLINE2MIX	[7:0]	RLINE2MIX7	RLINE2MIX6	RLINE2MIX5	RLINE2MIX4	RLINE2MIX3	RLINE2MIX2	RLINE2MIX1	RLINE2MIX0	0x00	RW1C
18	LCDMIX	[7:0]	CDLMIX7	CDLMIX6	CDLMIX5	CDLMIX4	CDLMIX3	CDLMIX2	CDLMIX1	CDLMIX0	0x00	RW1C
19	RCDMIX	[7:0]	CDRMIX7	CDRMIX6	CDRMIX5	CDRMIX4	CDRMIX3	CDRMIX2	CDRMIX1	CDRMIX0	0x00	RW1C
1A	LHPMIX	[7:0]	LHPMIX7	LHPMIX6	LHPMIX5	LHPMIX4	LHPMIX3	LHPMIX2	LHPMIX1	LHPMIX0	0x00	RW1C
1B	RHPMIX	[7:0]	RHPMIX7	RHPMIX6	RHPMIX5	RHPMIX4	RHPMIX3	RHPMIX2	RHPMIX1	RHPMIX0	0x00	RW1C
1C	EPMIX	[7:0]	EPMIX7	EPMIX6	EPMIX5	EPMIX4	EPMIX3	EPMIX2	EPMIX1	EPMIX0	0x00	RW1C
1D	HP_CTRL	[7:0]	RESERVED		POPTIME		HPMOD		HPOC		0x00	RW
1E	HP_CTRL2	[7:0]	RESERVED	LVL_THR		HIZ	VOLIM			RESERVED	0x00	RW
1F	LS_CTRL	[7:0]	CDDRIVE	DIRCD	CDSM		RCDBST	LCDBST	EDGE		0x00	RW
21	EPCONTROL	[7:0]	RESERVED		MICB2GAIN		MICB1GAIN		EPGAIN		0x00	RW
22	MICBIAS_CTRL1	[7:0]	VBATLOW	MICB1LIM	MICB1OCEN	MICB1CURDEN	MICB1SHT		MICB1CURD		0x00	RW
23	MICBIAS_CTRL2	[7:0]	RESERVED	MICB2LIM	MICB2OCEN	MICB2CURDEN	MICB2SHT		MICB2CURD		0x00	RW
24	OUTPUT_CONTROL	[7:0]	RNSM		LNSM		LDIFF	LNFBEN	ZCTO	VMID	0x00	RW
25	PWDN_CTRL1	[7:0]	LADCPDB	RADCPDB	MICB2PDB	MICB1PDB	AIN4PDB	AIN3PDB	AIN2PDB	AIN1PDB	0x00	RW
26	PWDN_CTRL2	[7:0]	LDAC2PDB	RADC2PDB	LDAC1PDB	RDAC1PDB	LLN2PDB	RLN2PDB	LLN1PDB	RLN1PDB	0x00	RW
27	PWDN_CTRL3	[7:0]	ZDPDB	VBATPWDB	RESERVED	EPPDB	LCDPDB	RCDPDB	HPPDB	PWDB	0x00	RW
28	DPLLA_CTRL	[7:0]	DPLLA_REF_SEL				DPLLA_NDIV				0x00	RW
29	PLLA_CTRL1	[7:0]	PLLA_M_HI								0x00	RW
2A	PLLA_CTRL2	[7:0]	PLLA_M_LO								0x00	RW
2B	PLLA_CTRL3	[7:0]	PLLA_N_HI								0x00	RW
2C	PLLA_CTRL4	[7:0]	PLLA_N_LO								0x00	RW
2D	PLLA_CTRL5	[7:0]	RESERVED	PLLA_R				PLLA_X		PLLA_TYPE	0x00	RW
2E	PLLA_CTRL6	[7:0]	RESERVED				DPLLA_LOCKED	PLLA_LOCKED	DPLLA_BYPASS	PLLA_EN	0x02	RW
2F	DPLLB_CTRL	[7:0]	DPLLB_REF_SEL				DPLLB_NDIV				0x00	RW
30	PLLB_CTRL1	[7:0]	PLLB_M_HI								0x00	RW
31	PLLB_CTRL2	[7:0]	PLLB_M_LO								0x00	RW
32	PLLB_CTRL3	[7:0]	PLLB_N_HI								0x00	RW
33	PLLB_CTRL4	[7:0]	PLLB_N_LO								0x00	RW
34	PLLB_CTRL5	[7:0]	RESERVED	PLLB_R				PLLB_X		PLLB_TYPE	0x00	RW
35	PLLB_CTRL6	[7:0]	RESERVED				DPLLB_LOCKED	PLLB_LOCKED	DPLLB_BYPASS	PLLB_EN	0x02	RW
36	HEADDECT	[7:0]	RESERVED						HEADSET		0x00	RW
37	ADC_DAC_STATUS	[7:0]	RESERVED	NOCLKDAC2	NOCLKDAC1	RESERVED				NOCLKADC	0x00	R

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
38	MIC_JACK_STATUS	[7:0]	RESERVED			JACKDECT	MICB2OC	MICB2THS	MICB1OC	MICB1THS	0x00	R
39	CHIP_FAULT_STATUS	[7:0]	RESERVED			OCEP	OCCDR	OCCDL	OCHP	OT	0x00	R
3C	ADC_SETTING	[7:0]	RESERVED					ADC_RESET_FORCE	ADC_RESET	PDETECT	0x00	RW
40	CLK1_SOURCE_DIV	[7:0]	COREN	CLK1S_SEL	CLK1SDIV			MCLK1DIV			0x00	MMRW
41	CLK1_OUTPUT_DIV	[7:0]	RESERVED		CLK1OEN	CLK1ODIV					0x00	RW
42	CLK2_SOURCE_DIV	[7:0]	CLK2EN	CLK2S_SEL	CLK2SDIV			MCLK2DIV			0x00	MMRW
43	CLK2_OUTPUT_DIV	[7:0]	RESERVED		CLK2OEN	CLK2ODIV					0x00	RW
44	DAIA	[7:0]	BCLKINVA	MSA	SWAPA	LRPA	WLA		FORMATA		0x0A	RW
45	DAIB	[7:0]	BCLKINVB	MSB	SWAPB	LRPB	WLB		FORMATB		0x0A	RW
46	DAIC	[7:0]	BCLKINVC	MSC	SWAPC	LRPC	WLC		FORMATC		0x0A	RW
47	BCLKDIVA	[7:0]	RESERVED		DAIA_SOURCE	DAIA_SR			BPFA		0x00	RW
48	BCLKDIVB	[7:0]	RESERVED		DAIB_SOURCE	DAIB_SR			BPFB		0x00	RW
49	BCLKDIVC	[7:0]	RESERVED		DAIC_SOURCE	DAIC_SR			BPFC		0x00	RW
4A	SRCA_RATIOA	[7:0]	SRCAMODE	SRCAINT			SRCARFRE_HI				0x00	RW
4B	SRCA_RATIOB	[7:0]	SRCARFRE_LOW								0x00	RW
4C	SRCB_RATIOA	[7:0]	SRCBMODE	SRCBINT			SRCBRFRE_HI				0x00	RW
4D	SRCB_RATIOB	[7:0]	SRCBRFRE_LOW								0x00	RW
4E	SRCC_RATIOA	[7:0]	SRCCMODE	SRCCINT			SRCCRFRE_HI				0x00	RW
4F	SRCC_RATIOB	[7:0]	SRCCRFRE_LOW								0x00	RW
50	DEEMP_CTRL	[7:0]	RESERVED			DEMPFS		DEMPCEN	DEMPBEN	DEMPAEN	0x00	RW
51	SRC_DAI_A_CTRL	[7:0]	RESERVED		SRCA_RECWRONG	SRCA_PBWRONG	SRCAUNLOCK	SRCAPBEN	SRCARECEN	DAIAEN	0x08	RW
52	SRC_DAI_B_CTRL	[7:0]	RESERVED		SRCB_RECWRONG	SRCB_PBWRONG	SRCBUNLOCK	SRCBPBEN	SRCBRECEN	DAIBEN	0x08	RW
53	SRC_DAI_C_CTRL	[7:0]	RESERVED		SRCC_RECWRONG	SRCC_PBWRONG	SRCCUNLOCK	SRCCPBEN	SRCCRECEN	DAICEN	0x08	RW
56	DIN_MIX_CTRL0	[7:0]	RESERVED	DIN_CHAN0_DMIC_SWAP	DIN_CHAN0_DMIC	DIN_CHAN0_ADC_SWAP	DIN_CHAN0_ADC	DIN_CHAN0_AIFC_PB	DIN_CHAN0_AIFB_PB	DIN_CHAN0_AIFA_PB	0x00	RW
57	DIN_MIX_CTRL1	[7:0]	RESERVED	DIN_CHAN1_DMIC_SWAP	DIN_CHAN1_DMIC	DIN_CHAN1_ADC_SWAP	DIN_CHAN1_ADC	DIN_CHAN1_AIFC_PB	DIN_CHAN1_AIFB_PB	DIN_CHAN1_AIFA_PB	0x00	RW
58	DIN_MIX_CTRL2	[7:0]	RESERVED	DIN_CHAN2_DMIC_SWAP	DIN_CHAN2_DMIC	DIN_CHAN2_ADC_SWAP	DIN_CHAN2_ADC	DIN_CHAN2_AIFC_PB	DIN_CHAN2_AIFB_PB	DIN_CHAN2_AIFA_PB	0x00	RW
59	DIN_MIX_CTRL3	[7:0]	RESERVED	DIN_CHAN3_DMIC_SWAP	DIN_CHAN3_DMIC	DIN_CHAN3_ADC_SWAP	DIN_CHAN3_ADC	DIN_CHAN3_AIFC_PB	DIN_CHAN3_AIFB_PB	DIN_CHAN3_AIFA_PB	0x00	RW
5A	DIN_MIX_CTRL4	[7:0]	RESERVED	DIN_CHAN4_DMIC_SWAP	DIN_CHAN4_DMIC	DIN_CHAN4_ADC_SWAP	DIN_CHAN4_ADC	DIN_CHAN4_AIFC_PB	DIN_CHAN4_AIFB_PB	DIN_CHAN4_AIFA_PB	0x00	RW
5B	DOUT_MIX_CTRL0	[7:0]	RESERVED			DOUT_CHAN4_AIFA_REC	DOUT_CHAN3_AIFA_REC	DOUT_CHAN2_AIFA_REC	DOUT_CHAN1_AIFA_REC	DOUT_CHAN0_AIFA_REC	0x00	RW
5C	DOUT_MIX_CTRL1	[7:0]	RESERVED			DOUT_CHAN4_AIFB_REC	DOUT_CHAN3_AIFB_REC	DOUT_CHAN2_AIFB_REC	DOUT_CHAN1_AIFB_REC	DOUT_CHAN0_AIFB_REC	0x00	RW
5D	DOUT_MIX_CTRL2	[7:0]	RESERVED			DOUT_CHAN4_AIFC_REC	DOUT_CHAN3_AIFC_REC	DOUT_CHAN2_AIFC_REC	DOUT_CHAN1_AIFC_REC	DOUT_CHAN0_AIFC_REC	0x00	RW
5E	DOUT_MIX_CTRL3	[7:0]	RESERVED			DOUT_CHAN4_DAC1	DOUT_CHAN3_DAC1	DOUT_CHAN2_DAC1	DOUT_CHAN1_DAC1	DOUT_CHAN0_DAC1	0x00	RW
5F	DOUT_MIX_CTRL4	[7:0]	RESERVED			DOUT_CHAN4_DAC2	DOUT_CHAN3_DAC2	DOUT_CHAN2_DAC2	DOUT_CHAN1_DAC2	DOUT_CHAN0_DAC2	0x00	RW
60	VOLMOD1	[7:0]	RESERVED		DAICRECVOLM	DAIBRECVOLM	DAIARECVOLM	DAICPBVOLM	DAIBPBVOLM	DAIAPBVOLM	0x00	RW
61	VOLMOD2	[7:0]	RESERVED				CODECDRECVOLM	CODECRECVOLM	CODECPBBVOLM	CODECPBAVOLM	0x00	RW
62	DAIA_PBL_VOL	[7:0]	DAIAPBLVOL								0x00	RW
63	DAIA_PBR_VOL	[7:0]	DAIAPBRVOL								0x00	RW
64	DAIB_PBL_VOL	[7:0]	DAIBPBLVOL								0x00	RW
65	DAIB_PBR_VOL	[7:0]	DAIBPBRVOL								0x00	RW
66	DAIC_PBL_VOL	[7:0]	DAICPBLVOL								0x00	RW
67	DAIC_PBR_VOL	[7:0]	DAICPBRVOL								0x00	RW
68	DAIA_RECL_VOL	[7:0]	DAIARECLVOL								0x00	RW
69	DAIA_RECR_VOL	[7:0]	DAIARECRVOL								0x00	RW

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
6A	DAIB_RECL_VOL	[7:0]	DAIBRECLVOL								0x00	RW
6B	DAIB_RECR_VOL	[7:0]	DAIBRECRVOL								0x00	RW
6C	DAIC_RECL_VOL	[7:0]	DAICRECLVOL								0x00	RW
6D	DAIC_RECR_VOL	[7:0]	DAICRECRVOL								0x00	RW
6E	PBAL_VOL	[7:0]	PBALVOL								0x00	RW
6F	PBAR_VOL	[7:0]	PBARVOL								0x00	RW
70	PBBL_VOL	[7:0]	PBBLVOL								0x00	RW
71	PBBR_VOL	[7:0]	PBBRVOL								0x00	RW
72	RECL_VOL	[7:0]	RECLVOL								0x00	RW
73	RECR_VOL	[7:0]	RECRVOL								0x00	RW
74	DRECL_VOL	[7:0]	DRECLVOL								0x00	RW
75	DRECR_VOL	[7:0]	DRECRVOL								0x00	RW
76	VOL_GAIN1	[7:0]	RESERVED		DAICPBRVOL_GAIN	DAICPBLVOL_GAIN	DAIBPBRVOL_GAIN	DAIBPBLVOL_GAIN	DAIAPBRVOL_GAIN	DAIAPBLVOL_GAIN	0x00	RW
77	VOL_GAIN2	[7:0]	RESERVED		DAICRECRVOL_GAIN	DAICRECLVOL_GAIN	DAIBRECRVOL_GAIN	DAIBRECLVOL_GAIN	DAIARECRVOL_GAIN	DAIARECLVOL_GAIN	0x00	RW
78	VOL_GAIN3	[7:0]	DRECRVOL_GAIN	DRECLVOL_GAIN	RECRVOL_GAIN	RECLVOL_GAIN	PBBRVOL_GAIN	PBBLVOL_GAIN	PBARVOL_GAIN	PBALVOL_GAIN	0x00	RW
7D	HPF_CTRL	[7:0]	HPFF					HPFOR	HPFEN		0x00	RW
7E	BASS1	[7:0]	RESERVED		BASS_LPF	BASS_CUT			BASS_SPK		0x00	RW
7F	BASS2	[7:0]	RESERVED			BASS_GAIN			BASS_SEL		0x00	RW
80	DRC1_CTRL1	[7:0]	DRCNGREC				DRCLELTAV				0x78	RW
81	DRC1_CTRL2	[7:0]	DRCLELATT				DRCLELDEC				0x18	RW
82	DRC1_CTRL3	[7:0]	DRCTHX1								0x00	RW
83	DRC1_CTRL4	[7:0]	DRCTHX2								0x00	RW
84	DRC1_CTRL5	[7:0]	DRCTHX3								0x00	RW
85	DRC1_CTRL6	[7:0]	DRCTHX4								0xC0	RW
86	DRC1_CTRL7	[7:0]	DRCTHY1								0x00	RW
87	DRC1_CTRL8	[7:0]	DRCTHY2								0x00	RW
88	DRC1_CTRL9	[7:0]	DRCTHY3								0x00	RW
89	DRC1_CTRL10	[7:0]	DRCTHY4								0xC0	RW
8A	DRC1_CTRL11	[7:0]	DRCGSATT				DRCGSDEC				0x88	RW
8B	DRC1_CTRL12	[7:0]	DRCHTNOR				DRCHTNG				0x7A	RW
8C	DRC1_CTRL13	[7:0]	RESERVED			DRCG			RESERVED		0xDF	RW
8D	DRC1_CTRL14	[7:0]	DRCNGTGT	DRCNGHDEN	DRCNGSRC	DRCCESRC	DRCLMSRC	DRCNGEN	DRCEN		0x20	RW
8E	DRC1_CTRL15	[7:0]	RESERVED	SIG_DET_RMS					SIG_DET_PK		0x00	RW
8F	DRC1_CTRL16	[7:0]	RESERVED					ALG_NGEN	DRCIRQ_MODE	DRCIRQ_EN	0x00	RW
90	DRC2_CTRL1	[7:0]	DRCNGREC				DRCLELTAV				0x78	RW
91	DRC2_CTRL2	[7:0]	DRCLELATT				DRCLELDEC				0x18	RW
92	DRC2_CTRL3	[7:0]	DRCTHX1								0x00	RW
93	DRC2_CTRL4	[7:0]	DRCTHX2								0x00	RW
94	DRC2_CTRL5	[7:0]	DRCTHX3								0x00	RW
95	DRC2_CTRL6	[7:0]	DRCTHX4								0xC0	RW
96	DRC2_CTRL7	[7:0]	DRCTHY1								0x00	RW
97	DRC2_CTRL8	[7:0]	DRCTHY2								0x00	RW
98	DRC2_CTRL9	[7:0]	DRCTHY3								0x00	RW
99	DRC2_CTRL10	[7:0]	DRCTHY4								0xC0	RW
9A	DRC2_CTRL11	[7:0]	DRCGSATT				DRCGSDEC				0x88	RW
9B	DRC2_CTRL12	[7:0]	DRCHTNOR				DRCHTNG				0x7A	RW
9C	DRC2_CTRL13	[7:0]	RESERVED			DRCG			RESERVED		0xDF	RW
9D	DRC2_CTRL14	[7:0]	DRCNGTGT	DRCNGHDEN	DRCNGSRC	DRCCESRC	DRCLMSRC	DRCNGEN	DRCEN		0x20	RW
9E	DRC2_CTRL15	[7:0]	RESERVED	SIG_DET_RMS					SIG_DET_PK		0x00	RW
9F	DRC2_CTRL16	[7:0]	RESERVED					ALG_NGEN	DRCIRQ_MODE	DRCIRQ_EN	0x00	RW
A0	DRC3_CTRL1	[7:0]	DRCNGREC				DRCLELTAV				0x78	RW
A1	DRC3_CTRL2	[7:0]	DRCLELATT				DRCLELDEC				0x18	RW
A2	DRC3_CTRL3	[7:0]	DRCTHX1								0x00	RW
A3	DRC3_CTRL4	[7:0]	DRCTHX2								0x00	RW
A4	DRC3_CTRL5	[7:0]	DRCTHX3								0x00	RW
A5	DRC3_CTRL6	[7:0]	DRCTHX4								0xC0	RW
A6	DRC3_CTRL7	[7:0]	DRCTHY1								0x00	RW
A7	DRC3_CTRL8	[7:0]	DRCTHY2								0x00	RW
A8	DRC3_CTRL9	[7:0]	DRCTHY3								0x00	RW
A9	DRC3_CTRL10	[7:0]	DRCTHY4								0xC0	RW

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
AA	DRC3_CTRL11	[7:0]	DRCGSATT				DRCGSDEC				0x88	RW
AB	DRC3_CTRL12	[7:0]	DRCHTNOR				DRCHTNG				0x7A	RW
AC	DRC3_CTRL13	[7:0]	RESERVED		DRCG				RESERVED		0xDF	RW
AD	DRC3_CTRL14	[7:0]	DRCNGTGT	DRCNGHDEN	DRCNGSRC	DRCCESRC	DRCLMSRC	DRCNGEN	DRCEN		0x20	RW
AE	DRC3_CTRL15	[7:0]	RESERVED	SIG_DET_RMS					SIG_DET_PK		0x00	RW
AF	DRC3_CTRL16	[7:0]	RESERVED					ALG_NGEN	DRCIRQ_MODE	DRCIRQ_EN	0x00	RW
B0	MDRC_PRE_FILTER	[7:0]	RESERVED		MDRC_HPF				MDRC_LPF		0x00	RW
B1	MDRC_SPL_CTRL	[7:0]	MDRC_CROSS_HIGH				MDRC_CROSS_LOW				0x00	RW
B2	MDRC_CTRL	[7:0]	RESERVED					MDRC_LPFEN	MDRC_HPFEN	MDRC_EN	0x00	RW
B3	PRE_HPF1_COEFH	[7:0]	PRE_HPF1_COEFH								0xFF	RW
B4	PRE_HPF1_COEFL	[7:0]	RESERVED					PRE_HPF_COEFL			0xFF	RW
B5	PRE_HPF2_COEFH	[7:0]	PRE_HPF2_COEFH								0xFF	RW
B6	PRE_HPF2_COEFL	[7:0]	RESERVED					PRE_HPF2_COEFL			0xFF	RW
B7	PRE_HPF3_COEFH	[7:0]	PRE_HPF3_COEFH								0xFF	RW
B8	PRE_HPF3_COEFL	[7:0]	RESERVED					PRE_HPF3_COEFL			0xFF	RW
B9	PRE_HPF4_COEFH	[7:0]	PRE_HPF4_COEFH								0xFF	RW
BA	PRE_HPF4_COEFL	[7:0]	RESERVED					PRE_HPF4_COEFL			0xFF	RW
BB	PRE_HPF5_COEFH	[7:0]	PRE_HPF5_COEFH								0xFF	RW
BC	PRE_HPF5_COEFL	[7:0]	RESERVED					PRE_HPF5_COEFL			0xFF	RW
BD	PRE_HPF_CTRL	[7:0]	RESERVED			PRE_HPF5_EN	PRE_HPF4_EN	PRE_HPF3_EN	PRE_HPF2_EN	PRE_HPF1_EN	0x1F	RW
BE	EQ_CTRL1	[7:0]	RESERVED			EQ_UPDING	EQ_UPD_CLR	EQ_FORMAT	EQ_UPD	EQ_WR_EN	0x00	RW
BF	EQ_CTRL2	[7:0]	EQEN	EQBP7	EQBP6	EQBP5	EQBP4	EQBP3	EQBP2	EQBP1	0x00	RW
C0	E3D_CTRL1	[7:0]	E3D_LEVEL				E3D_ALPHA				0x00	RW
C1	E3D_CTRL2	[7:0]	RESERVED				E3D_GAIN			E3D_EN	0x00	RW
C2	ALC_CTRL0	[7:0]	ALCTAV				ALCHLD				0x00	RW
C3	ALC_CTRL1	[7:0]	ALCATT				ALCREC				0x00	RW
C4	ALC_CTRL2	[7:0]	ALCLVL				ALCREF				0x00	RW
C5	ALC_CTRL3	[7:0]	ALCRIP				ALCMAX				0x00	RW
C6	ALC_CTRL4	[7:0]	ALCNGTH				ALCNGHLD				0x00	RW
C7	ALC_CTRL5	[7:0]	ALCNGATT				ALCNGREC				0x00	RW
C8	ALC_CTRL6	[7:0]	HLDRST	ALCHPF	NGMODE		ALCEN		ALCMODE		0x00	RW
DC	FDSP_SEL1	[7:0]	RESERVED	DRC3_SEL			RESERVED	DRC2_SEL			0x00	RW
DD	FDSP_SEL2	[7:0]	RESERVED	EQ_SEL			RESERVED	DRC1_SEL			0x00	RW
DE	FDSP_SEL3	[7:0]	RESERVED	E3D_SEL			RESERVED	HPF_SEL			0x00	RW
DF	FDSP_SEL4	[7:0]	RESERVED	BASS_EN_SEL			ALC_4CHEN	ALC_SEL			0x00	RW
E0	PBALPCTRL1	[7:0]	PBALPANA	PBALPWL				PBALPMODE		PBALPEN	0x00	RW
E1	PBBLPCTRL2	[7:0]	PBBLPANA	PBBLPWL				PBBLPMODE		PBBLPEN	0x00	RW
E2	DIGMICCTRL	[7:0]	MICLRMODE	DMICPOLSWAP			DMICBLRSWAP	DIGMICBEN	DMICALRSWAP	DIGMICAEN	0x00	RW
E3	GPIOSEL1	[7:0]	GPIO2SEL				GPIO1SEL				0x00	RW
E4	GPIOSEL2	[7:0]	GPIO4SEL				GPIO3SEL				0x00	RW
E5	IRQ_MASK	[7:0]	ASRCC_IRQ_MASK	ASRCB_IRQ_MASK	ASRCA_IRQ_MASK	DRC_IRQ_MASK	PLL_UNLOCK_MASK	HP_CFG_MASK	HP_DECT_MASK	AFAULT_MASK	0x00	RW
E6	IRQ_RAW	[7:0]	ASRCC_IRQ_RAW_STATE	ASRCB_IRQ_RAW_STATE	ASRCA_IRQ_RAW_STATE	DRC_IRQ_RAW_STATE	PLL_UNLOCK_RAW_STATE	HP_CFG_RAW_STATE	HP_DECT_RAW_STATE	AFAULT_RAW_STATE	02	R
E7	IRQ_STATE	[7:0]	ASRCC_IRQ_STATUS	ASRCB_IRQ_STATUS	ASRCA_IRQ_STATUS	DRC_IRQ_STATUS	PLL_UNLOCK_STATUS	HP_CFG_STATUS	HP_DECT_STATUS	AFAULT_STATUS	0x00	R
E8	IRQEN	[7:0]	RESERVED							IRQEN	0x00	RW
E9	PAD_CTRL1	[7:0]	RESERVED		I2CFILTER_BYPASS	I2CDRV	DMICCLKDRV	CDRV	BDRV	ADRV	1F	RW
EA	PAD_CTRL2	[7:0]	RESERVED				GPIO4DRV	GPIO3DRV	GPIO2DRV	GPIO1DRV	0F	RW
EB	DIGEN	[7:0]	RESERVED			FDSPEN	DRECEN	RECEN	PBBEN	PBAEN	0x00	RW
EC	LPCNTCTRL	[7:0]	LPC_B_CNT				LPC_A_CNT				0x00	RW
ED	CHIP_ID_HI	[7:0]	CHIP_ID_HI								13	R
EE	CHIP_ID_MID	[7:0]	CHIP_ID_MID								73	R
EF	CHIP_ID_LO	[7:0]	CHIP_ID_LOW								0B	R
FF	SOFT_RESET	[7:0]	SOFT_RST								0x00	MMRW

REGISTER BIT DESCRIPTIONS

INPUT_MODE REGISTER

Address: 0x00, Reset: 0x00, Name: INPUT_MODE

Sets the input mode to stereo (single-ended) or mono (differential).
Sets the input gain to either PGA or boost mode.

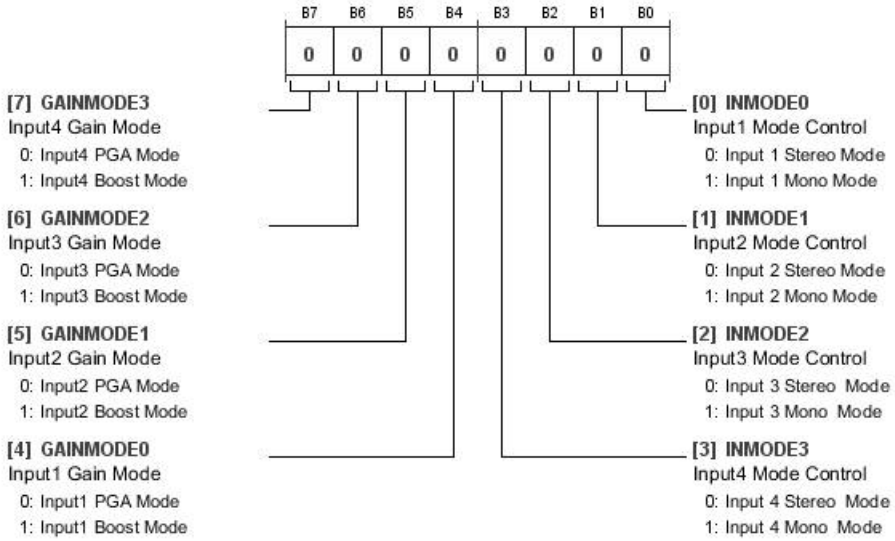


Table 35. Bit Descriptions for INPUT_MODE

Bits	Bit Name	Settings	Description	Reset	Access
7	GAINMODE3		Input 4 Gain Mode.	0x0	RW
		0	Input 4 PGA Mode		
		1	Input 4 Boost Mode		
6	GAINMODE2		Input 3 Gain Mode.	0x0	RW
		0	Input 3 PGA Mode		
		1	Input 3 Boost Mode		
5	GAINMODE1		Input 2 Gain Mode.	0x0	RW
		0	Input 2 PGA Mode		
		1	Input 2 Boost Mode		
4	GAINMODE0		Input 1 Gain Mode.	0x0	RW
		0	Input 1 PGA Mode		
		1	Input 1 Boost Mode		
3	INMODE3		Input 4 Mode Control.	0x0	RW
		0	Input 4 Stereo Mode		
		1	Input 4 Mono Mode		
2	INMODE2		Input 3 Mode Control.	0x0	RW
		0	Input 3 Stereo Mode		
		1	Input 3 Mono Mode		
1	INMODE1		Input 2 Mode Control.	0x0	RW
		0	Input 2 Stereo Mode		
		1	Input 2 Mono Mode		
0	INMODE0		Input 1 Mode Control.	0x0	RW
		0	Input 1 Stereo Mode		
		1	Input 1 Mono Mode		

AIN1L_CTRL REGISTER

Address: 0x01, Reset: 0x00, Name: AIN1L_CTRL

Input 1 Left Gain Setting
PGA Mode: −12 dB to +18 dB in 1 dB steps
Boost Mode: 0 dB/9 dB/20 dB in three steps

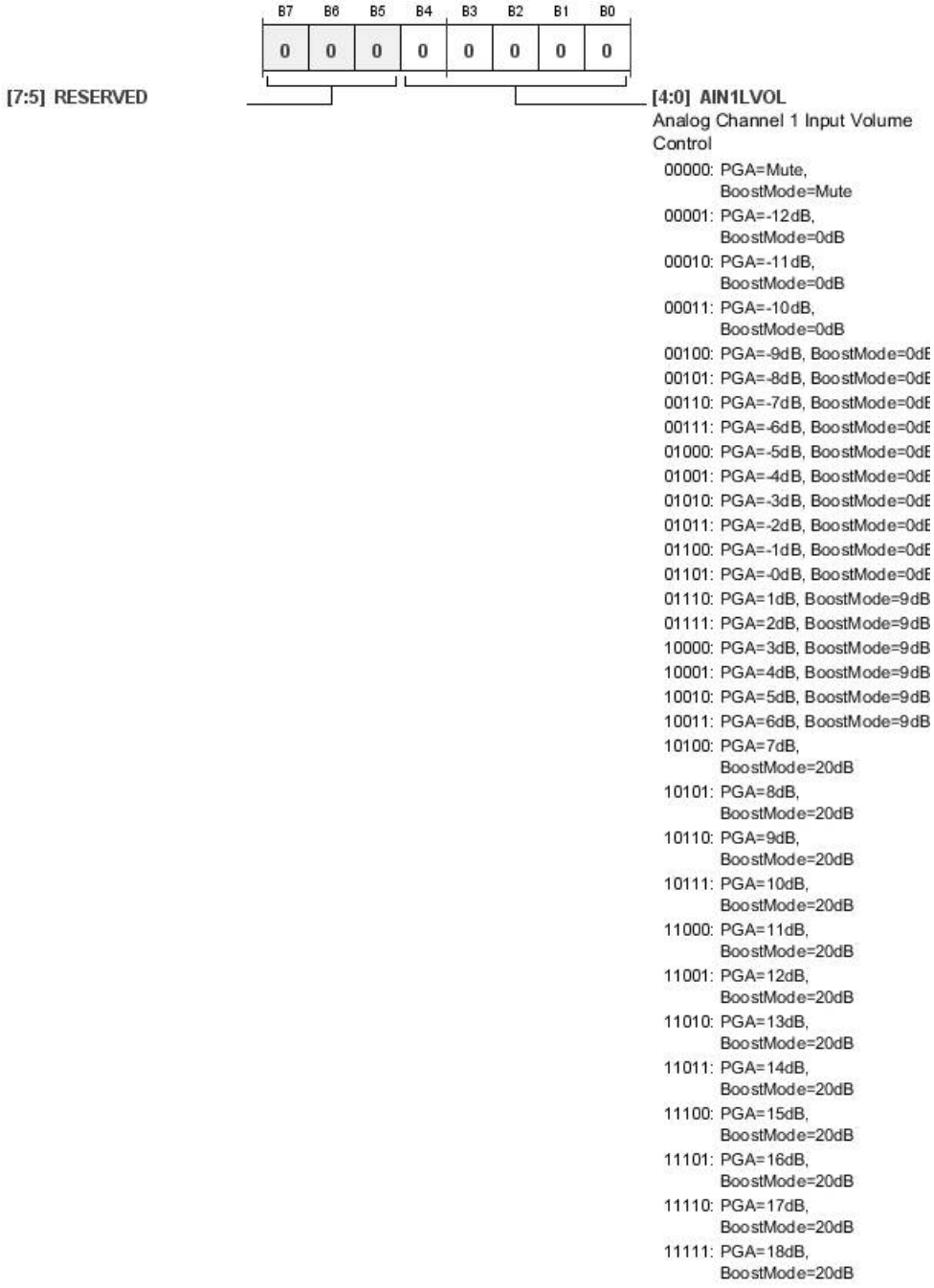


Table 36. Bit Descriptions for AIN1L_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
[4:0]	AIN1LVOL		Analog Channel 1 Input Volume Control.	0x00	RW
		00000	PGA = Mute, Boost Mode = Mute		
		00001	PGA = −12 dB, Boost Mode = 0 dB		
		00010	PGA = −11 dB, Boost Mode = 0 dB		
		00011	PGA = −10 dB, Boost Mode = 0 dB		
		00100	PGA = −9 dB, Boost Mode = 0 dB		
		00101	PGA = −8 dB, Boost Mode = 0 dB		
		00110	PGA = −7 dB, Boost Mode = 0 dB		
		00111	PGA = −6 dB, Boost Mode = 0 dB		
		01000	PGA = −5 dB, Boost Mode = 0 dB		
		01001	PGA = −4 dB, Boost Mode = 0 dB		
		01010	PGA = −3 dB, Boost Mode = 0 dB		
		01011	PGA = −2 dB, Boost Mode = 0 dB		
		01100	PGA = −1 dB, Boost Mode = 0 dB		
		01101	PGA = 0 dB, Boost Mode = 0 dB		
		01110	PGA = 1 dB, Boost Mode = 9 dB		
		01111	PGA = 2 dB, Boost Mode = 9 dB		
		10000	PGA = 3 dB, Boost Mode = 9 dB		
		10001	PGA = 4 dB, Boost Mode = 9 dB		
		10010	PGA = 5 dB, Boost Mode = 9 dB		
		10011	PGA = 6 dB, Boost Mode = 9 dB		
		10100	PGA = 7 dB, Boost Mode = 20 dB		
		10101	PGA = 8 dB, Boost Mode = 20 dB		
		10110	PGA = 9 dB, Boost Mode = 20 dB		
		10111	PGA = 10 dB, Boost Mode = 20 dB		
		11000	PGA = 11 dB, Boost Mode = 20 dB		
		11001	PGA = 12 dB, Boost Mode = 20 dB		
		11010	PGA = 13 dB, Boost Mode = 20 dB		
		11011	PGA = 14 dB, Boost Mode = 20 dB		
		11100	PGA = 15 dB, Boost Mode = 20 dB		
		11101	PGA = 16 dB, Boost Mode = 20 dB		
		11110	PGA = 17 dB, Boost Mode = 20 dB		
		11111	PGA = 18 dB, Boost Mode = 20 dB		

AIN1R_CTRL REGISTER

Address: 0x02, Reset: 0x00, Name: AIN1R_CTRL

Input 1 Right Gain Setting
PGA Mode: −12 dB to +18 dB in 1 dB steps
Boost Mode: 0 dB/9 dB/20 dB in three steps

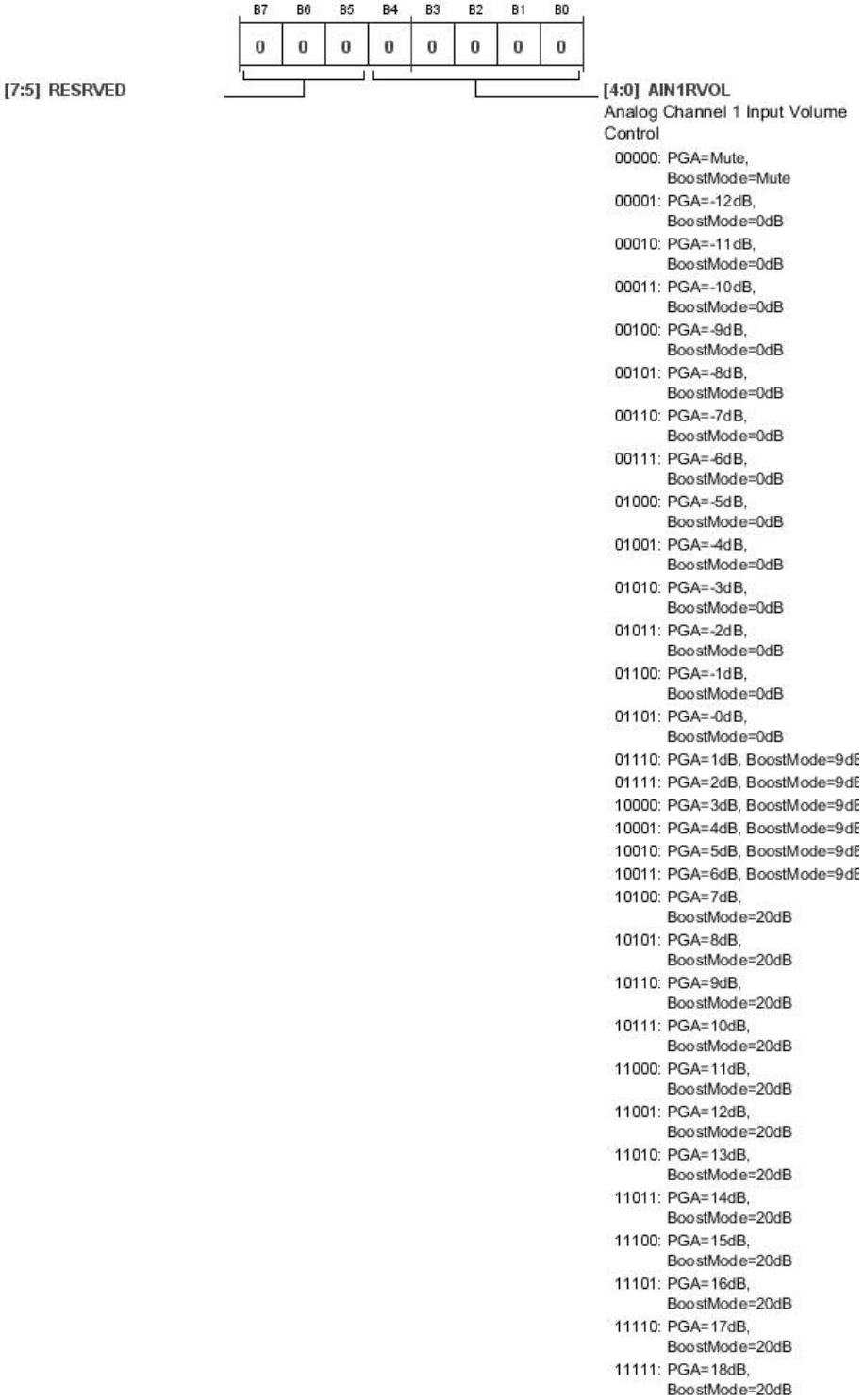


Table 37. Bit Descriptions for AIN1R_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
[4:0]	AIN1RVOL		Analog Channel 1 Input Volume Control.	0x00	RW
		00000	PGA = Mute, Boost Mode = Mute		
		00001	PGA = −12 dB, Boost Mode = 0 dB		
		00010	PGA = −11 dB, Boost Mode = 0 dB		
		00011	PGA = −10 dB, Boost Mode = 0 dB		
		00100	PGA = −9 dB, Boost Mode = 0 dB		
		00101	PGA = −8 dB, Boost Mode = 0 dB		
		00110	PGA = −7 dB, Boost Mode = 0 dB		
		00111	PGA = −6 dB, Boost Mode = 0 dB		
		01000	PGA = −5 dB, Boost Mode = 0 dB		
		01001	PGA = −4 dB, Boost Mode = 0 dB		
		01010	PGA = −3 dB, Boost Mode = 0 dB		
		01011	PGA = −2 dB, Boost Mode = 0 dB		
		01100	PGA = −1 dB, Boost Mode = 0 dB		
		01101	PGA = 0 dB, Boost Mode = 0 dB		
		01110	PGA = 1 dB, Boost Mode = 9 dB		
		01111	PGA = 2 dB, Boost Mode = 9 dB		
		10000	PGA = 3 dB, Boost Mode = 9 dB		
		10001	PGA = 4 dB, Boost Mode = 9 dB		
		10010	PGA = 5 dB, Boost Mode = 9 dB		
		10011	PGA = 6 dB, Boost Mode = 9 dB		
		10100	PGA = 7 dB, Boost Mode = 20 dB		
		10101	PGA = 8 dB, Boost Mode = 20 dB		
		10110	PGA = 9 dB, Boost Mode = 20 dB		
		10111	PGA = 10 dB, Boost Mode = 20 dB		
		11000	PGA = 11 dB, Boost Mode = 20 dB		
		11001	PGA = 12 dB, Boost Mode = 20 dB		
		11010	PGA = 13 dB, Boost Mode = 20 dB		
		11011	PGA = 14 dB, Boost Mode = 20 dB		
		11100	PGA = 15 dB, Boost Mode = 20 dB		
		11101	PGA = 16 dB, Boost Mode = 20 dB		
		11110	PGA = 17 dB, Boost Mode = 20 dB		
		11111	PGA = 18 dB, Boost Mode = 20 dB		

AIN2L_CTRL REGISTER

Address: 0x03, Reset: 0x00, Name: AIN2L_CTRL

Input 2 Left Gain Setting
PGA Mode: −12 dB to +18 dB in 1 dB steps
Boost Mode: 0 dB/9 dB/20 dB in three steps

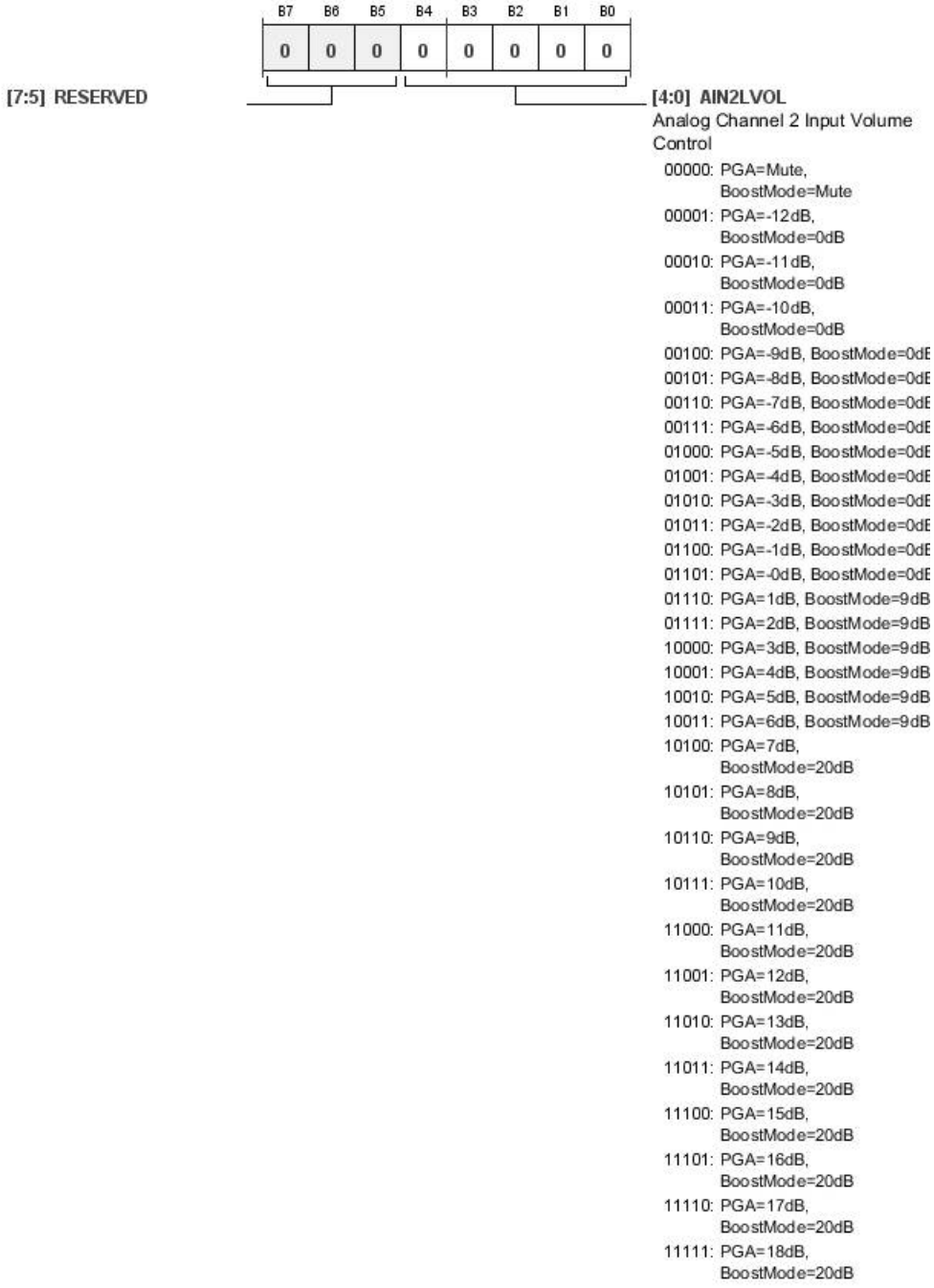


Table 38. Bit Descriptions for AIN2L_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
[4:0]	AIN2LVOL		Analog Channel 2 Input Volume Control.	0x00	RW
		00000	PGA = Mute, Boost Mode = Mute		
		00001	PGA = −12 dB, Boost Mode = 0 dB		
		00010	PGA = −11 dB, Boost Mode = 0 dB		
		00011	PGA = −10 dB, Boost Mode = 0 dB		
		00100	PGA = −9 dB, Boost Mode = 0 dB		
		00101	PGA = −8 dB, Boost Mode = 0 dB		
		00110	PGA = −7 dB, Boost Mode = 0 dB		
		00111	PGA = −6 dB, Boost Mode = 0 dB		
		01000	PGA = −5 dB, Boost Mode = 0 dB		
		01001	PGA = −4 dB, Boost Mode = 0 dB		
		01010	PGA = −3 dB, Boost Mode = 0 dB		
		01011	PGA = −2 dB, Boost Mode = 0 dB		
		01100	PGA = −1 dB, Boost Mode = 0 dB		
		01101	PGA = 0 dB, Boost Mode = 0 dB		
		01110	PGA = 1 dB, Boost Mode = 9 dB		
		01111	PGA = 2 dB, Boost Mode = 9 dB		
		10000	PGA = 3 dB, Boost Mode = 9 dB		
		10001	PGA = 4 dB, Boost Mode = 9 dB		
		10010	PGA = 5 dB, Boost Mode = 9 dB		
		10011	PGA = 6 dB, Boost Mode = 9 dB		
		10100	PGA = 7 dB, Boost Mode = 20 dB		
		10101	PGA = 8 dB, Boost Mode = 20 dB		
		10110	PGA = 9 dB, Boost Mode = 20 dB		
		10111	PGA = 10 dB, Boost Mode = 20 dB		
		11000	PGA = 11 dB, Boost Mode = 20 dB		
		11001	PGA = 12 dB, Boost Mode = 20 dB		
		11010	PGA = 13 dB, Boost Mode = 20 dB		
		11011	PGA = 14 dB, Boost Mode = 20 dB		
		11100	PGA = 15 dB, Boost Mode = 20 dB		
		11101	PGA = 16 dB, Boost Mode = 20 dB		
		11110	PGA = 17 dB, Boost Mode = 20 dB		
		11111	PGA = 18 dB, Boost Mode = 20 dB		

AIN2R_CTRL REGISTER

Address: 0x04, Reset: 0x00, Name: AIN2R_CTRL

Input 2 Right Gain Setting
PGA Mode: −12 dB to +18 dB in 1 dB steps
Boost Mode: 0 dB/9 dB/20 dB in three steps

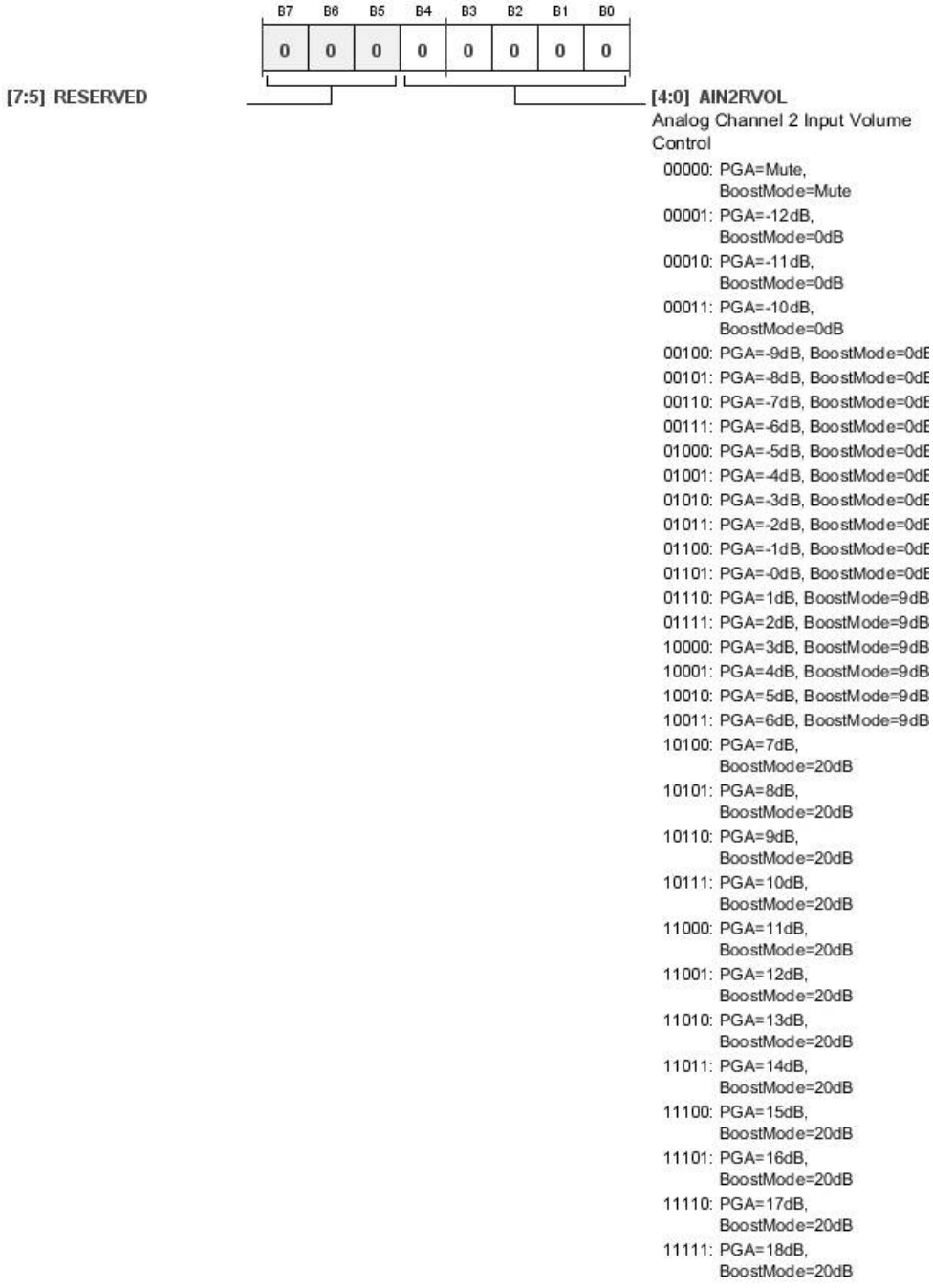


Table 39. Bit Descriptions for AIN2R_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
[4:0]	AIN2RVOL		Analog Channel 2 Input Volume Control.	0x00	RW
		00000	PGA = Mute, Boost Mode = Mute		
		00001	PGA = −12 dB, Boost Mode = 0 dB		
		00010	PGA = −11 dB, Boost Mode = 0 dB		
		00011	PGA = −10 dB, Boost Mode = 0 dB		
		00100	PGA = −9 dB, Boost Mode = 0 dB		
		00101	PGA = −8 dB, Boost Mode = 0 dB		
		00110	PGA = −7 dB, Boost Mode = 0 dB		
		00111	PGA = −6 dB, Boost Mode = 0 dB		
		01000	PGA = −5 dB, Boost Mode = 0 dB		
		01001	PGA = −4 dB, Boost Mode = 0 dB		
		01010	PGA = −3 dB, Boost Mode = 0 dB		
		01011	PGA = −2 dB, Boost Mode = 0 dB		
		01100	PGA = −1 dB, Boost Mode = 0 dB		
		01101	PGA = 0 dB, Boost Mode = 0 dB		
		01110	PGA = 1 dB, Boost Mode = 9 dB		
		01111	PGA = 2 dB, Boost Mode = 9 dB		
		10000	PGA = 3 dB, Boost Mode = 9 dB		
		10001	PGA = 4 dB, Boost Mode = 9 dB		
		10010	PGA = 5 dB, Boost Mode = 9 dB		
		10011	PGA = 6 dB, Boost Mode = 9 dB		
		10100	PGA = 7 dB, Boost Mode = 20 dB		
		10101	PGA = 8 dB, Boost Mode = 20 dB		
		10110	PGA = 9 dB, Boost Mode = 20 dB		
		10111	PGA = 10 dB, Boost Mode = 20 dB		
		11000	PGA = 11 dB, Boost Mode = 20 dB		
		11001	PGA = 12 dB, Boost Mode = 20 dB		
		11010	PGA = 13 dB, Boost Mode = 20 dB		
		11011	PGA = 14 dB, Boost Mode = 20 dB		
		11100	PGA = 15 dB, Boost Mode = 20 dB		
		11101	PGA = 16 dB, Boost Mode = 20 dB		
		11110	PGA = 17 dB, Boost Mode = 20 dB		
		11111	PGA = 18 dB, Boost Mode = 20 dB		

AIN3L_CTRL REGISTER

Address: 0x05, Reset: 0x00, Name: AIN3L_CTRL

Input 3 Left Gain Setting
PGA Mode: −12 dB to +18 dB in 1 dB steps
Boost Mode: 0 dB/9 dB/20 dB in three steps

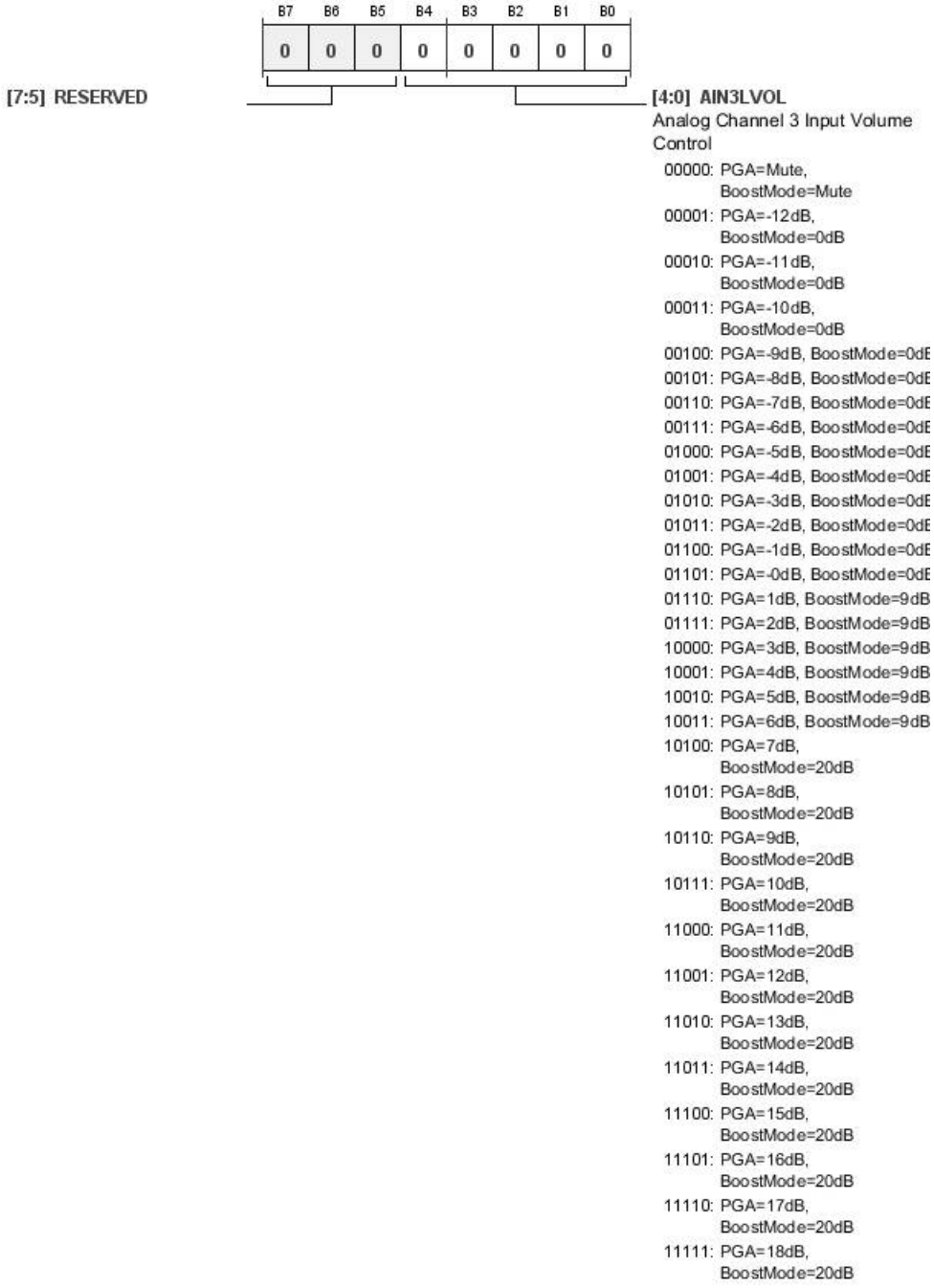


Table 40. Bit Descriptions for AIN3L_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
[4:0]	AIN3LVOL		Analog Channel 3 Input Volume Control.	0x00	RW
		00000	PGA = Mute, Boost Mode = Mute		
		00001	PGA = −12 dB, Boost Mode = 0 dB		
		00010	PGA = −11 dB, Boost Mode = 0 dB		
		00011	PGA = −10 dB, Boost Mode = 0 dB		
		00100	PGA = −9 dB, Boost Mode = 0 dB		
		00101	PGA = −8 dB, Boost Mode = 0 dB		
		00110	PGA = −7 dB, Boost Mode = 0 dB		
		00111	PGA = −6 dB, Boost Mode = 0 dB		
		01000	PGA = −5 dB, Boost Mode = 0 dB		
		01001	PGA = −4 dB, Boost Mode = 0 dB		
		01010	PGA = −3 dB, Boost Mode = 0 dB		
		01011	PGA = −2 dB, Boost Mode = 0 dB		
		01100	PGA = −1 dB, Boost Mode = 0 dB		
		01101	PGA = 0 dB, Boost Mode = 0 dB		
		01110	PGA = 1 dB, Boost Mode = 9 dB		
		01111	PGA = 2 dB, Boost Mode = 9 dB		
		10000	PGA = 3 dB, Boost Mode = 9 dB		
		10001	PGA = 4 dB, Boost Mode = 9 dB		
		10010	PGA = 5 dB, Boost Mode = 9 dB		
		10011	PGA = 6 dB, Boost Mode = 9 dB		
		10100	PGA = 7 dB, Boost Mode = 20 dB		
		10101	PGA = 8 dB, Boost Mode = 20 dB		
		10110	PGA = 9 dB, Boost Mode = 20 dB		
		10111	PGA = 10 dB, Boost Mode = 20 dB		
		11000	PGA = 11 dB, Boost Mode = 20 dB		
		11001	PGA = 12 dB, Boost Mode = 20 dB		
		11010	PGA = 13 dB, Boost Mode = 20 dB		
		11011	PGA = 14 dB, Boost Mode = 20 dB		
		11100	PGA = 15 dB, Boost Mode = 20 dB		
		11101	PGA = 16 dB, Boost Mode = 20 dB		
		11110	PGA = 17 dB, Boost Mode = 20 dB		
		11111	PGA = 18 dB, Boost Mode = 20 dB		

AIN3R_CTRL REGISTER

Address: 0x06, Reset: 0x00, Name: AIN3R_CTRL

Input 3 Right Gain Setting
PGA Mode: −12 dB to +18 dB in 1 dB steps
Boost Mode: 0 dB/9 dB/20 dB in three steps

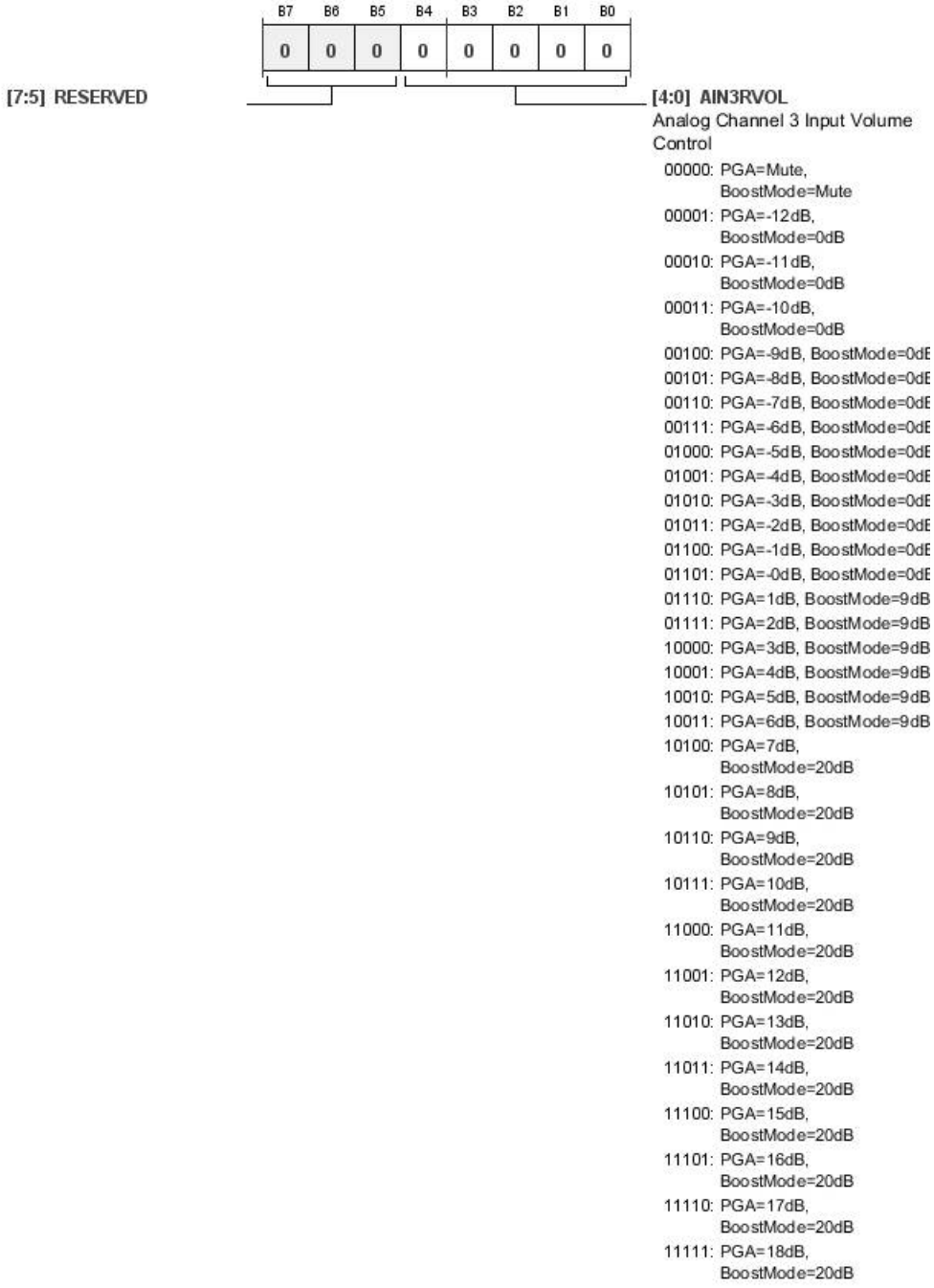


Table 41. Bit Descriptions for AIN3R_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
[4:0]	AIN3RVOL		Analog Channel 3 Input Volume Control.	0x00	RW
		00000	PGA = Mute, Boost Mode = Mute		
		00001	PGA = −12 dB, Boost Mode = 0 dB		
		00010	PGA = −11 dB, Boost Mode = 0 dB		
		00011	PGA = −10 dB, Boost Mode = 0 dB		
		00100	PGA = −9 dB, Boost Mode = 0 dB		
		00101	PGA = −8 dB, Boost Mode = 0 dB		
		00110	PGA = −7 dB, Boost Mode = 0 dB		
		00111	PGA = −6 dB, Boost Mode = 0 dB		
		01000	PGA = −5 dB, Boost Mode = 0 dB		
		01001	PGA = −4 dB, Boost Mode = 0 dB		
		01010	PGA = −3 dB, Boost Mode = 0 dB		
		01011	PGA = −2 dB, Boost Mode = 0 dB		
		01100	PGA = −1 dB, Boost Mode = 0 dB		
		01101	PGA = 0 dB, Boost Mode = 0 dB		
		01110	PGA = 1 dB, Boost Mode = 9 dB		
		01111	PGA = 2 dB, Boost Mode = 9 dB		
		10000	PGA = 3 dB, Boost Mode = 9 dB		
		10001	PGA = 4 dB, Boost Mode = 9 dB		
		10010	PGA = 5 dB, Boost Mode = 9 dB		
		10011	PGA = 6 dB, Boost Mode = 9 dB		
		10100	PGA = 7 dB, Boost Mode = 20 dB		
		10101	PGA = 8 dB, Boost Mode = 20 dB		
		10110	PGA = 9 dB, Boost Mode = 20 dB		
		10111	PGA = 10 dB, Boost Mode = 20 dB		
		11000	PGA = 11 dB, Boost Mode = 20 dB		
		11001	PGA = 12 dB, Boost Mode = 20 dB		
		11010	PGA = 13 dB, Boost Mode = 20 dB		
		11011	PGA = 14 dB, Boost Mode = 20 dB		
		11100	PGA = 15 dB, Boost Mode = 20 dB		
		11101	PGA = 16 dB, Boost Mode = 20 dB		
		11110	PGA = 17 dB, Boost Mode = 20 dB		
		11111	PGA = 18 dB, Boost Mode = 20 dB		

AIN4L_CTRL REGISTER

Address: 0x07, Reset: 0x00, Name: AIN4L_CTRL

Input 4 Left Gain Setting
PGA Mode: −12 dB to +18 dB in 1 dB steps
Boost Mode: 0 dB/9 dB/20 dB in three steps

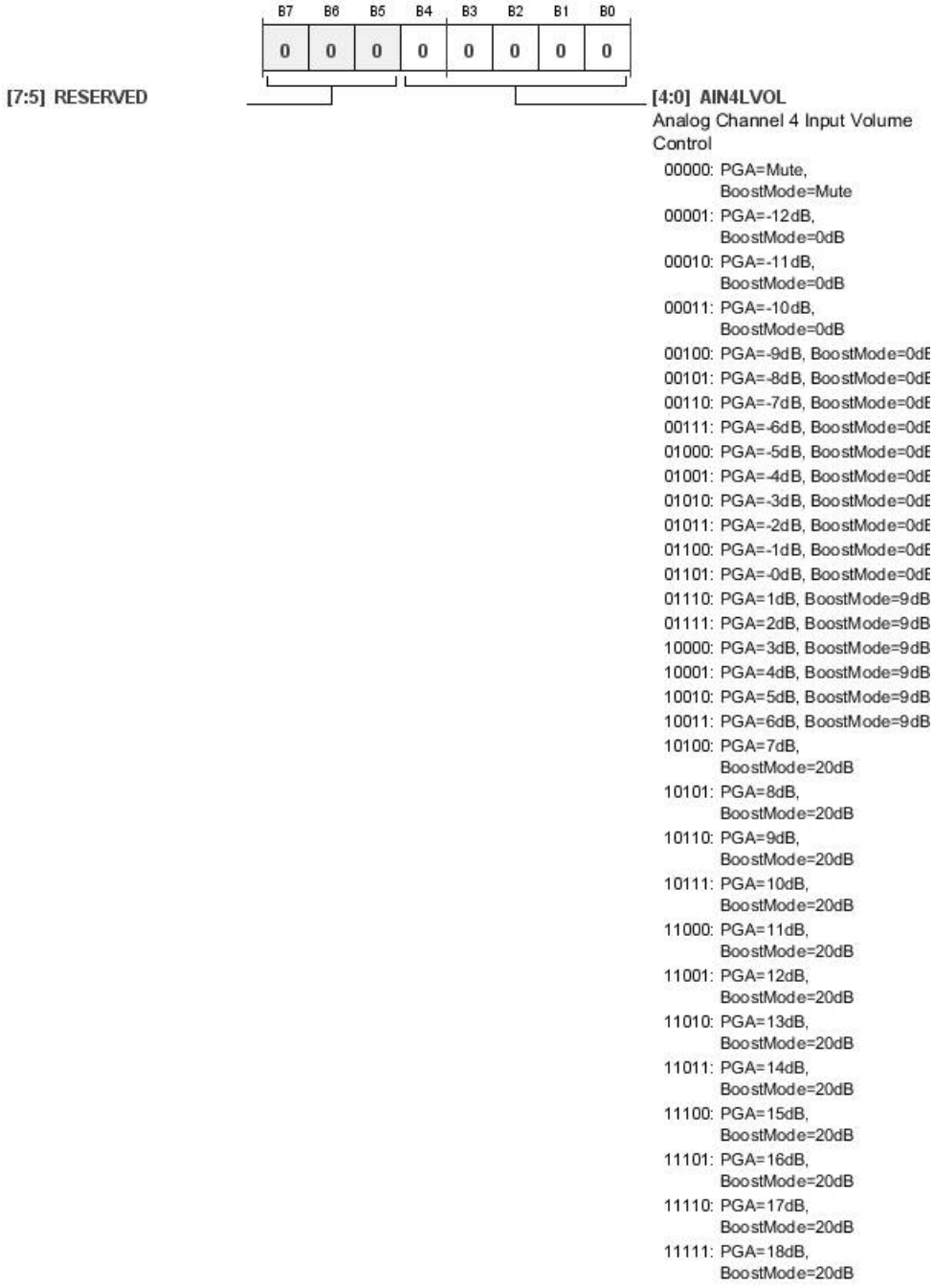


Table 42. Bit Descriptions for AIN4L_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
[4:0]	AIN4LVOL		Analog Channel 4 Input Volume Control.	0x00	RW
		00000	PGA = Mute, Boost Mode = Mute		
		00001	PGA = −12 dB, Boost Mode = 0 dB		
		00010	PGA = −11 dB, Boost Mode = 0 dB		
		00011	PGA = −10 dB, Boost Mode = 0 dB		
		00100	PGA = −9 dB, Boost Mode = 0 dB		
		00101	PGA = −8 dB, Boost Mode = 0 dB		
		00110	PGA = −7 dB, Boost Mode = 0 dB		
		00111	PGA = −6 dB, Boost Mode = 0 dB		
		01000	PGA = −5 dB, Boost Mode = 0 dB		
		01001	PGA = −4 dB, Boost Mode = 0 dB		
		01010	PGA = −3 dB, Boost Mode = 0 dB		
		01011	PGA = −2 dB, Boost Mode = 0 dB		
		01100	PGA = −1 dB, Boost Mode = 0 dB		
		01101	PGA = 0 dB, Boost Mode = 0 dB		
		01110	PGA = 1 dB, Boost Mode = 9 dB		
		01111	PGA = 2 dB, Boost Mode = 9 dB		
		10000	PGA = 3 dB, Boost Mode = 9 dB		
		10001	PGA = 4 dB, Boost Mode = 9 dB		
		10010	PGA = 5 dB, Boost Mode = 9 dB		
		10011	PGA = 6 dB, Boost Mode = 9 dB		
		10100	PGA = 7 dB, Boost Mode = 20 dB		
		10101	PGA = 8 dB, Boost Mode = 20 dB		
		10110	PGA = 9 dB, Boost Mode = 20 dB		
		10111	PGA = 10 dB, Boost Mode = 20 dB		
		11000	PGA = 11 dB, Boost Mode = 20 dB		
		11001	PGA = 12 dB, Boost Mode = 20 dB		
		11010	PGA = 13 dB, Boost Mode = 20 dB		
		11011	PGA = 14 dB, Boost Mode = 20 dB		
		11100	PGA = 15 dB, Boost Mode = 20 dB		
		11101	PGA = 16 dB, Boost Mode = 20 dB		
		11110	PGA = 17 dB, Boost Mode = 20 dB		
		11111	PGA = 18 dB, Boost Mode = 20 dB		

AIN4R_CTRL REGISTER

Address: 0x08, Reset: 0x00, Name: AIN4R_CTRL

Input 4 Right Gain Setting
PGA Mode: −12 dB to +18 dB in 1 dB steps
Boost Mode: 0 dB/9 dB/20 dB in three steps

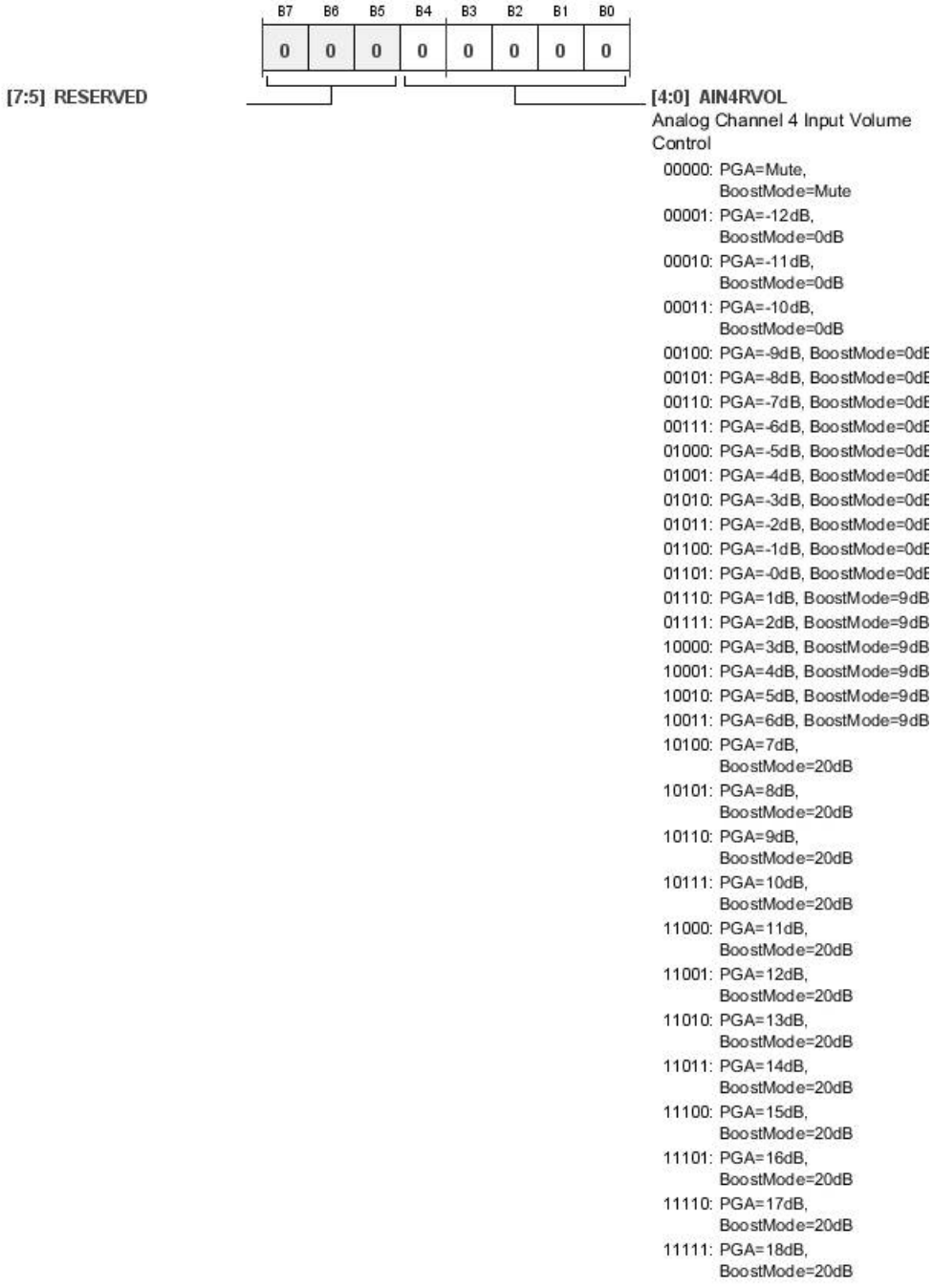


Table 43. Bit Descriptions for AIN4R_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
[4:0]	AIN4RVOL		Analog Channel 4 Input Volume Control.	0x00	RW
		00000	PGA = Mute, Boost Mode = Mute		
		00001	PGA = −12 dB, Boost Mode = 0 dB		
		00010	PGA = −11 dB, Boost Mode = 0 dB		
		00011	PGA = −10 dB, Boost Mode = 0 dB		
		00100	PGA = −9 dB, Boost Mode = 0 dB		
		00101	PGA = −8 dB, Boost Mode = 0 dB		
		00110	PGA = −7 dB, Boost Mode = 0 dB		
		00111	PGA = −6 dB, Boost Mode = 0 dB		
		01000	PGA = −5 dB, Boost Mode = 0 dB		
		01001	PGA = −4 dB, Boost Mode = 0 dB		
		01010	PGA = −3 dB, Boost Mode = 0 dB		
		01011	PGA = −2 dB, Boost Mode = 0 dB		
		01100	PGA = −1 dB, Boost Mode = 0 dB		
		01101	PGA = 0 dB, Boost Mode = 0 dB		
		01110	PGA = 1 dB, Boost Mode = 9 dB		
		01111	PGA = 2 dB, Boost Mode = 9 dB		
		10000	PGA = 3 dB, Boost Mode = 9 dB		
		10001	PGA = 4 dB, Boost Mode = 9 dB		
		10010	PGA = 5 dB, Boost Mode = 9 dB		
		10011	PGA = 6 dB, Boost Mode = 9 dB		
		10100	PGA = 7 dB, Boost Mode = 20 dB		
		10101	PGA = 8 dB, Boost Mode = 20 dB		
		10110	PGA = 9 dB, Boost Mode = 20 dB		
		10111	PGA = 10 dB, Boost Mode = 20 dB		
		11000	PGA = 11 dB, Boost Mode = 20 dB		
		11001	PGA = 12 dB, Boost Mode = 20 dB		
		11010	PGA = 13 dB, Boost Mode = 20 dB		
		11011	PGA = 14 dB, Boost Mode = 20 dB		
		11100	PGA = 15 dB, Boost Mode = 20 dB		
		11101	PGA = 16 dB, Boost Mode = 20 dB		
		11110	PGA = 17 dB, Boost Mode = 20 dB		
		11111	PGA = 18 dB, Boost Mode = 20 dB		

LLINE1_OUT REGISTER

Address: 0x09, Reset: 0x00, Name: LLINE1_OUT

Line Output 1 Left Gain Control

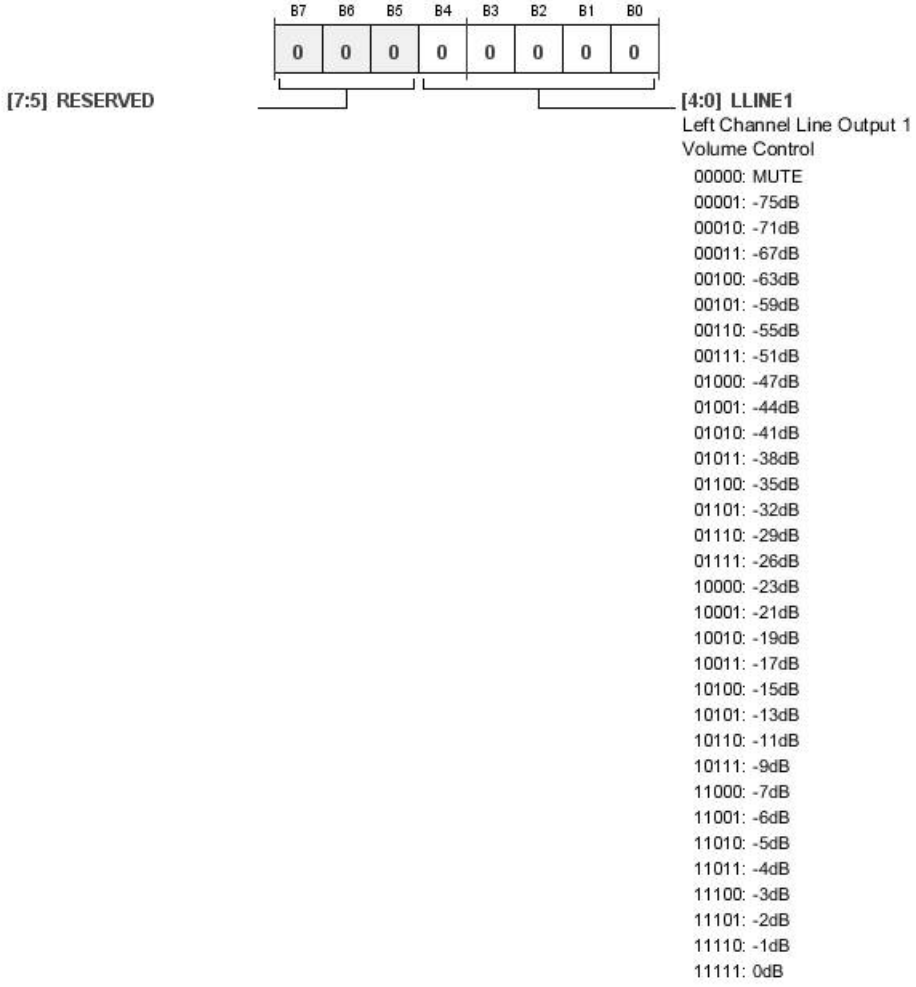


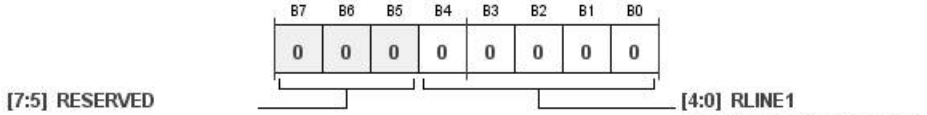
Table 44. Bit Descriptions for LLINE1_OUT

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
[4:0]	LLINE1		Left Channel Line Output 1 Volume Control.	0x00	RW
		00000	Mute		
		00001	−75 dB		
		00010	−71 dB		
		00011	−67 dB		
		00100	−63 dB		
		00101	−59 dB		
		00110	−55 dB		
		00111	−51 dB		
		01000	−47 dB		
		01001	−44 dB		
		01010	−41 dB		
		01011	−38 dB		
		01100	−35 dB		
		01101	−32 dB		
		01110	−29 dB		
		01111	−26 dB		
		10000	−23 dB		
		10001	−21 dB		
		10010	−19 dB		
		10011	−17 dB		
		10100	−15 dB		
		10101	−13 dB		
		10110	−11 dB		
		10111	−9 dB		
		11000	−7 dB		
		11001	−6 dB		
		11010	−5 dB		
		11011	−4 dB		
		11100	−3 dB		
		11101	−2 dB		
		11110	−1 dB		
		11111	0 dB		

RLINE1_OUT REGISTER

Address: 0x0A, Reset: 0x00, Name: RLINE1_OUT

Line Output 1 Right Gain Control



Right Channel Line Output 1 Volume Control

- 00000: MUTE
- 00001: -75dB
- 00010: -71dB
- 00011: -67dB
- 00100: -63dB
- 00101: -59dB
- 00110: -55dB
- 00111: -51dB
- 01000: -47dB
- 01001: -44dB
- 01010: -41dB
- 01011: -38dB
- 01100: -35dB
- 01101: -32dB
- 01110: -29dB
- 01111: -26dB
- 10000: -23dB
- 10001: -21dB
- 10010: -19dB
- 10011: -17dB
- 10100: -15dB
- 10101: -13dB
- 10110: -11dB
- 10111: -9dB
- 11000: -7dB
- 11001: -6dB
- 11010: -5dB
- 11011: -4dB
- 11100: -3dB
- 11101: -2dB
- 11110: -1dB
- 11111: 0dB

Table 45. Bit Descriptions for RLINE1_OUT

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
[4:0]	RLINE1		Right Channel Line Output 1 Volume Control.	0x00	RW
		00000	Mute		
		00001	−75 dB		
		00010	−71 dB		
		00011	−67 dB		
		00100	−63 dB		
		00101	−59 dB		
		00110	−55 dB		
		00111	−51 dB		
		01000	−47 dB		
		01001	−44 dB		
		01010	−41 dB		
		01011	−38 dB		
		01100	−35 dB		
		01101	−32 dB		
		01110	−29 dB		
		01111	−26 dB		
		10000	−23 dB		
		10001	−21 dB		
		10010	−19 dB		
		10011	−17 dB		
		10100	−15 dB		
		10101	−13 dB		
		10110	−11 dB		
		10111	−9 dB		
		11000	−7 dB		
		11001	−6 dB		
		11010	−5 dB		
		11011	−4 dB		
		11100	−3 dB		
		11101	−2 dB		
		11110	−1 dB		
		11111	0 dB		

LLINE2_OUT REGISTER

Address: 0x0B, Reset: 0x00, Name: LLINE2_OUT

Line Output 2 Left Gain Control

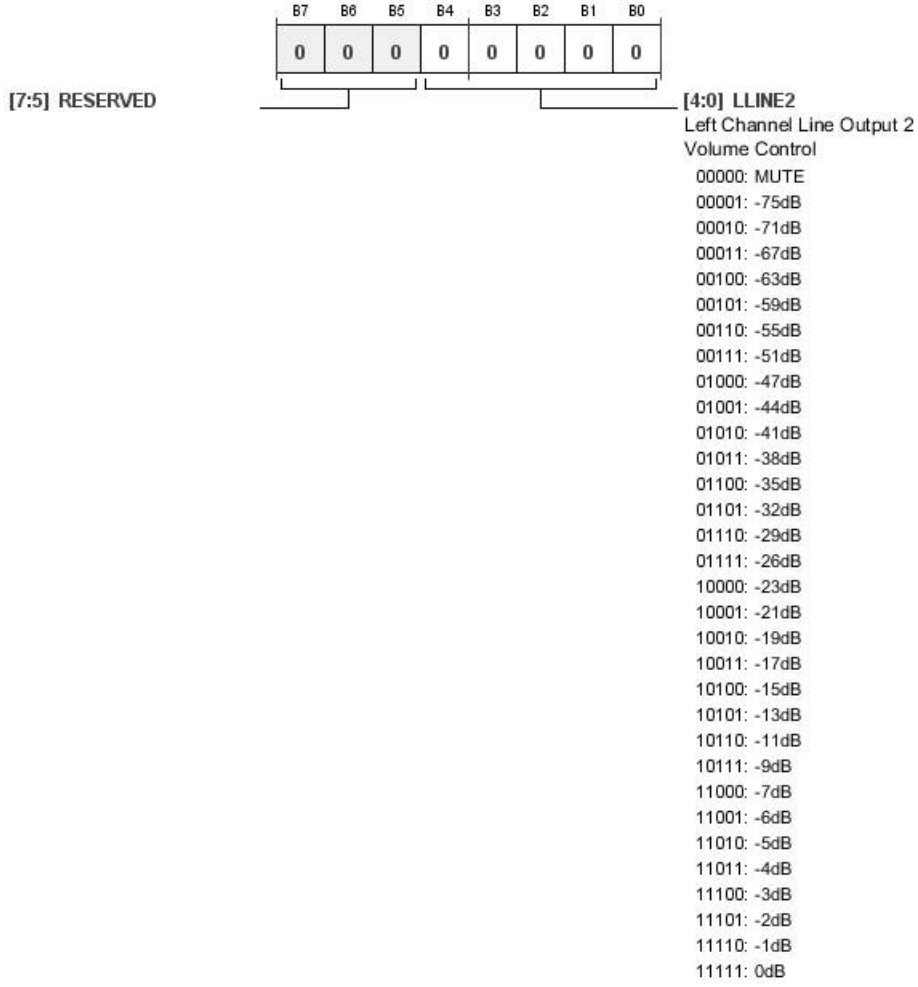


Table 46. Bit Descriptions for LLINE2_OUT

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
[4:0]	LLINE2		Left Channel Line Output 2 Volume Control.	0x00	RW
		00000	Mute		
		00001	−75 dB		
		00010	−71 dB		
		00011	−67 dB		
		00100	−63 dB		
		00101	−59 dB		
		00110	−55 dB		
		00111	−51 dB		
		01000	−47 dB		
		01001	−44 dB		
		01010	−41 dB		
		01011	−38 dB		
		01100	−35 dB		
		01101	−32 dB		
		01110	−29 dB		
		01111	−26 dB		
		10000	−23 dB		
		10001	−21 dB		
		10010	−19 dB		
		10011	−17 dB		
		10100	−15 dB		
		10101	−13 dB		
		10110	−11 dB		
		10111	−9 dB		
		11000	−7 dB		
		11001	−6 dB		
		11010	−5 dB		
		11011	−4 dB		
		11100	−3 dB		
		11101	−2 dB		
		11110	−1 dB		
		11111	0 dB		

RLINE2_OUT REGISTER

Address: 0x0C, Reset: 0x00, Name: RLINE2_OUT

Line Output 2 Right Gain Control

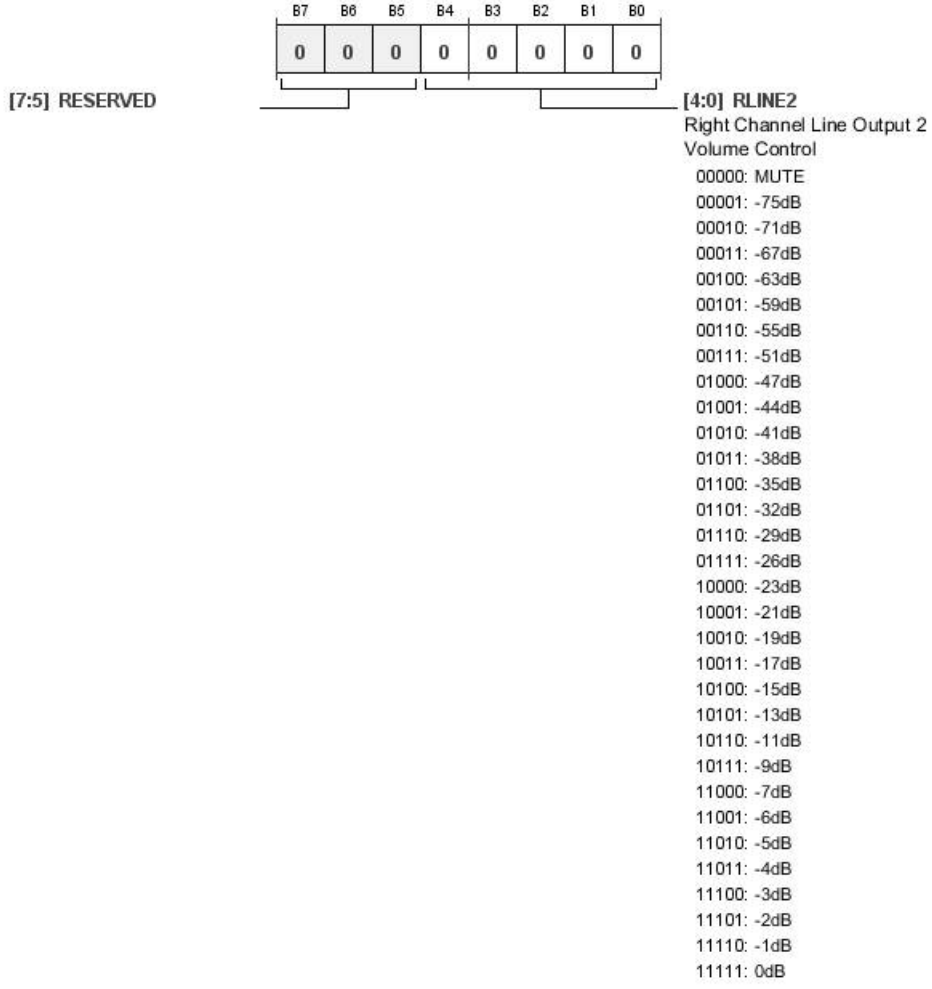


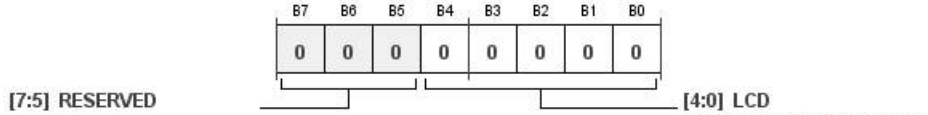
Table 47. Bit Descriptions for RLINE2_OUT

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
[4:0]	RLINE2		Right Channel Line Output 2 Volume Control.	0x00	RW
		00000	Mute		
		00001	−75 dB		
		00010	−71 dB		
		00011	−67 dB		
		00100	−63 dB		
		00101	−59 dB		
		00110	−55 dB		
		00111	−51 dB		
		01000	−47 dB		
		01001	−44 dB		
		01010	−41 dB		
		01011	−38 dB		
		01100	−35 dB		
		01101	−32 dB		
		01110	−29 dB		
		01111	−26 dB		
		10000	−23 dB		
		10001	−21 dB		
		10010	−19 dB		
		10011	−17 dB		
		10100	−15 dB		
		10101	−13 dB		
		10110	−11 dB		
		10111	−9 dB		
		11000	−7 dB		
		11001	−6 dB		
		11010	−5 dB		
		11011	−4 dB		
		11100	−3 dB		
		11101	−2 dB		
		11110	−1 dB		
		11111	0 dB		

LCD_OUT (SPEAKER) REGISTER

Address: 0x0D, Reset: 0x00, Name: LCD_OUT

Speaker Out Left Gain Control



Left Channel ClassD Output Volume Control

- 00000: MUTE
- 00001: -75dB
- 00010: -71dB
- 00011: -67dB
- 00100: -63dB
- 00101: -59dB
- 00110: -55dB
- 00111: -51dB
- 01000: -47dB
- 01001: -44dB
- 01010: -41dB
- 01011: -38dB
- 01100: -35dB
- 01101: -32dB
- 01110: -29dB
- 01111: -26dB
- 10000: -23dB
- 10001: -21dB
- 10010: -19dB
- 10011: -17dB
- 10100: -15dB
- 10101: -13dB
- 10110: -11dB
- 10111: -9dB
- 11000: -7dB
- 11001: -6dB
- 11010: -5dB
- 11011: -4dB
- 11100: -3dB
- 11101: -2dB
- 11110: -1dB
- 11111: 0dB

Table 48. Bit Descriptions for LCD_OUT

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
[4:0]	LCD		Left Channel Class-D Output Volume Control.	0x00	RW
		00000	Mute		
		00001	−75 dB		
		00010	−71 dB		
		00011	−67 dB		
		00100	−63 dB		
		00101	−59 dB		
		00110	−55 dB		
		00111	−51 dB		
		01000	−47 dB		
		01001	−44 dB		
		01010	−41 dB		
		01011	−38 dB		
		01100	−35 dB		
		01101	−32 dB		
		01110	−29 dB		
		01111	−26 dB		
		10000	−23 dB		
		10001	−21 dB		
		10010	−19 dB		
		10011	−17 dB		
		10100	−15 dB		
		10101	−13 dB		
		10110	−11 dB		
		10111	−9 dB		
		11000	−7 dB		
		11001	−6 dB		
		11010	−5 dB		
		11011	−4 dB		
		11100	−3 dB		
		11101	−2 dB		
		11110	−1 dB		
		11111	0 dB		

RCD_OUT (SPEAKER) REGISTER

Address: 0x0E, Reset: 0x00, Name: RCD_OUT

Speaker Out Right Gain Control

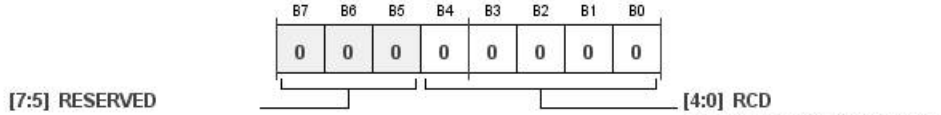


Table 49. Bit Descriptions for RCD_OUT

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
[4:0]	RCD		Right Channel Class-D Output Volume Control.	0x00	RW
		00000	Mute		
		00001	−75 dB		
		00010	−71 dB		
		00011	−67 dB		
		00100	−63 dB		
		00101	−59 dB		
		00110	−55 dB		
		00111	−51 dB		
		01000	−47 dB		
		01001	−44 dB		
		01010	−41 dB		
		01011	−38 dB		
		01100	−35 dB		
		01101	−32 dB		
		01110	−29 dB		
		01111	−26 dB		
		10000	−23 dB		
		10001	−21 dB		
		10010	−19 dB		
		10011	−17 dB		
		10100	−15 dB		
		10101	−13 dB		
		10110	−11 dB		
		10111	−9 dB		
		11000	−7 dB		
		11001	−6 dB		
		11010	−5 dB		
		11011	−4 dB		
		11100	−3 dB		
		11101	−2 dB		
		11110	−1 dB		
		11111	0 dB		

LHP_OUT REGISTER

Address: 0x0F, Reset: 0x00, Name: LHP_OUT

Headphone Out Left Gain Control

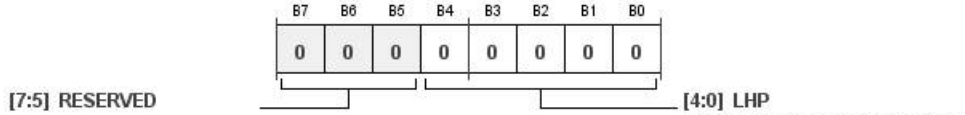


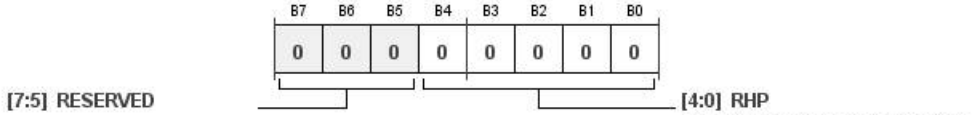
Table 50. Bit Descriptions for LHP_OUT

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
[4:0]	LHP		Left Channel Headphone Output Volume Control.	0x00	RW
		00000	Mute		
		00001	−75 dB		
		00010	−71 dB		
		00011	−67 dB		
		00100	−63 dB		
		00101	−59 dB		
		00110	−55 dB		
		00111	−51 dB		
		01000	−47 dB		
		01001	−44 dB		
		01010	−41 dB		
		01011	−38 dB		
		01100	−35 dB		
		01101	−32 dB		
		01110	−29 dB		
		01111	−26 dB		
		10000	−23 dB		
		10001	−21 dB		
		10010	−19 dB		
		10011	−17 dB		
		10100	−15 dB		
		10101	−13 dB		
		10110	−11 dB		
		10111	−9 dB		
		11000	−7 dB		
		11001	−6 dB		
		11010	−5 dB		
		11011	−4 dB		
		11100	−3 dB		
		11101	−2 dB		
		11110	−1 dB		
		11111	0 dB		

RHP_OUT REGISTER

Address: 0x10, Reset: 0x00, Name: RHP_OUT

Headphone Out Right Gain Control



Right Channel Headphone Output Volume Control

- 00000: MUTE
- 00001: -75dB
- 00010: -71dB
- 00011: -67dB
- 00100: -63dB
- 00101: -59dB
- 00110: -55dB
- 00111: -51dB
- 01000: -47dB
- 01001: -44dB
- 01010: -41dB
- 01011: -38dB
- 01100: -35dB
- 01101: -32dB
- 01110: -29dB
- 01111: -26dB
- 10000: -23dB
- 10001: -21dB
- 10010: -19dB
- 10011: -17dB
- 10100: -15dB
- 10101: -13dB
- 10110: -11dB
- 10111: -9dB
- 11000: -7dB
- 11001: -6dB
- 11010: -5dB
- 11011: -4dB
- 11100: -3dB
- 11101: -2dB
- 11110: -1dB
- 11111: 0dB

Table 51. Bit Descriptions for RHP_OUT

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
[4:0]	RHP		Right Channel Headphone Output Volume Control.	0x00	RW
		00000	Mute		
		00001	−75 dB		
		00010	−71 dB		
		00011	−67 dB		
		00100	−63 dB		
		00101	−59 dB		
		00110	−55 dB		
		00111	−51 dB		
		01000	−47 dB		
		01001	−44 dB		
		01010	−41 dB		
		01011	−38 dB		
		01100	−35 dB		
		01101	−32 dB		
		01110	−29 dB		
		01111	−26 dB		
		10000	−23 dB		
		10001	−21 dB		
		10010	−19 dB		
		10011	−17 dB		
		10100	−15 dB		
		10101	−13 dB		
		10110	−11 dB		
		10111	−9 dB		
		11000	−7 dB		
		11001	−6 dB		
		11010	−5 dB		
		11011	−4 dB		
		11100	−3 dB		
		11101	−2 dB		
		11110	−1 dB		
		11111	0 dB		

ADC_GAIN REGISTER

Address: 0x11, Reset: 0x00, Name: ADC_GAIN

20 dB Boost Gain Control, Pre-ADC

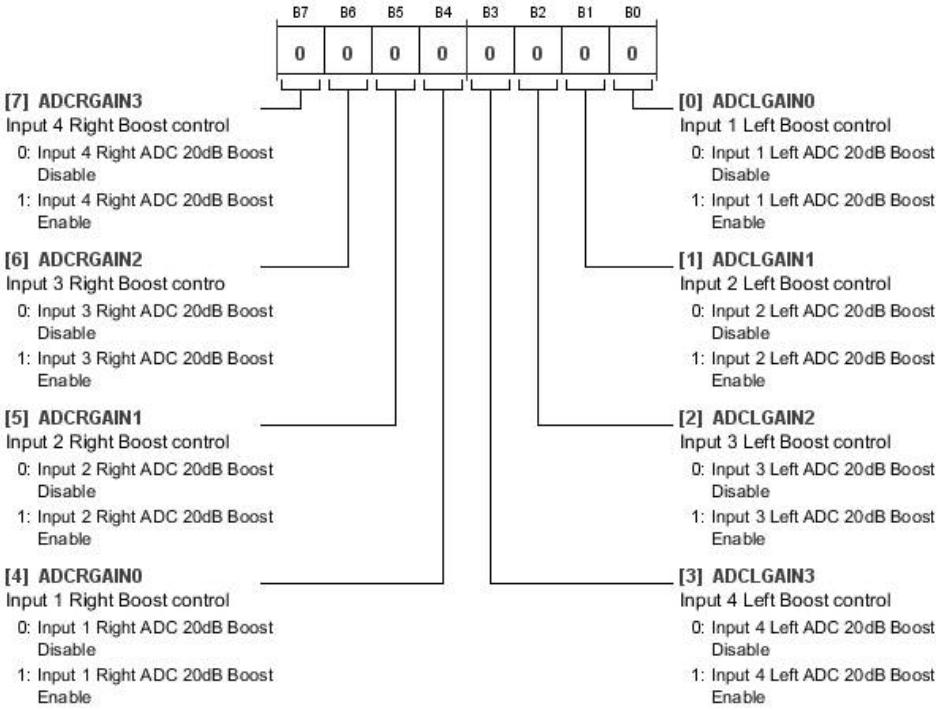


Table 52. Bit Descriptions for ADC_GAIN

Bits	Bit Name	Settings	Description	Reset	Access
7	ADCRGAIN3		Input 4 Right Boost Control.	0x0	RW
		0	Input 4 Right ADC, 20 dB Boost Disable		
		1	Input 4 Right ADC, 20 dB Boost Enable		
6	ADCRGAIN2		Input 3 Right Boost Control.	0x0	RW
		0	Input 3 Right ADC, 20 dB Boost Disable		
		1	Input 3 Right ADC, 20 dB Boost Enable		
5	ADCRGAIN1		Input 2 Right Boost Control.	0x0	RW
		0	Input 2 Right ADC, 20 dB Boost Disable		
		1	Input 2 Right ADC, 20 dB Boost Enable		
4	ADCRGAIN0		Input 1 Right Boost Control.	0x0	RW
		0	Input 1 Right ADC, 20 dB Boost Disable		
		1	Input 1 Right ADC, 20 dB Boost Enable		
3	ADCLGAIN3		Input 4 Left Boost Control.	0x0	RW
		0	Input 4 left ADC, 20 dB Boost Disable		
		1	Input 4 left ADC, 20 dB Boost Enable		
2	ADCLGAIN2		Input 3 Left Boost Control.	0x0	RW
		0	Input 3 left ADC, 20 dB Boost Disable		
		1	Input 3 left ADC, 20 dB Boost Enable		
1	ADCLGAIN1		Input 2 Left Boost Control.	0x0	RW
		0	Input 2 left ADC, 20 dB Boost Disable		
		1	Input 2 left ADC, 20 dB Boost Enable		
0	ADCLGAIN0		Input 1 Left Boost Control.	0x0	RW
		0	Input 1 left ADC, 20 dB Boost Disable		
		1	Input 1 left ADC, 20 dB Boost Enable		

LADC_MIXER REGISTER

Address: 0x12, Reset: 0x00, Name: LADC_MIXER

Left ADC Mixer Control

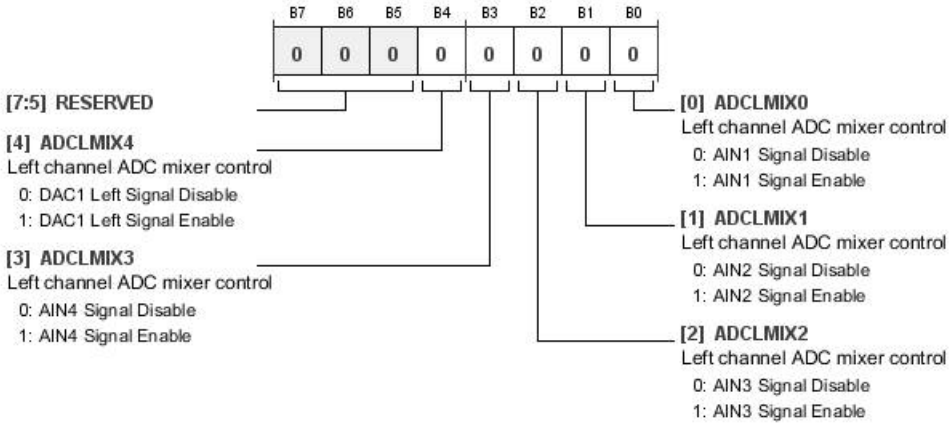


Table 53. Bit Descriptions for LADC_MIXER

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
4	ADCLMIX4		Left Channel ADC Mixer Control.	0x0	RW
		0	DAC1 Left Signal Disable		
		1	DAC1 Left Signal Enable		
3	ADCLMIX3		Left Channel ADC Mixer Control.	0x0	RW
		0	AIN4 Signal Disable		
		1	AIN4 Signal Enable		
2	ADCLMIX2		Left Channel ADC Mixer Control.	0x0	RW
		0	AIN3 Signal Disable		
		1	AIN3 Signal Enable		
1	ADCLMIX1		Left Channel ADC Mixer Control.	0x0	RW
		0	AIN2 Signal Disable		
		1	AIN2 Signal Enable		
0	ADCLMIX0		Left Channel ADC Mixer Control.	0x0	RW
		0	AIN1 Signal Disable		
		1	AIN1 Signal Enable		

RADC_MIXER REGISTER

Address: 0x13, Reset: 0x00, Name: RADC_MIXER

Right ADC Mixer Control

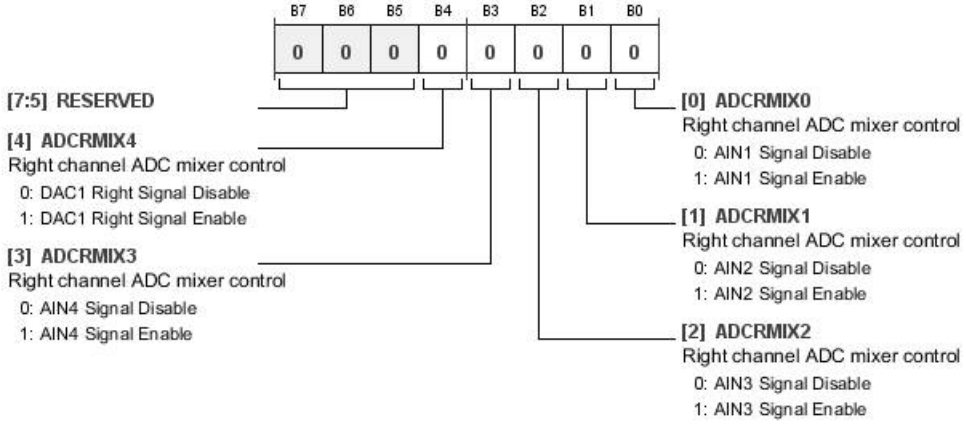


Table 54. Bit Descriptions for RADC_MIXER

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
4	ADCRMIX4		Right Channel ADC Mixer Control.	0x0	RW
		0	DAC1 Right Signal Disable		
		1	DAC1 Right Signal Enable		
3	ADCRMIX3		Right Channel ADC Mixer Control.	0x0	RW
		0	AIN4 Signal Disable		
		1	AIN4 Signal Enable		
2	ADCRMIX2		Right Channel ADC Mixer Control.	0x0	RW
		0	AIN3 Signal Disable		
		1	AIN3 Signal Enable		
1	ADCRMIX1		Right Channel ADC Mixer Control.	0x0	RW
		0	AIN2 Signal Disable		
		1	AIN2 Signal Enable		
0	ADCRMIX0		Right Channel ADC Mixer Control.	0x0	RW
		0	AIN1 Signal Disable		
		1	AIN1 Signal Enable		

LLINE1MIX REGISTER

Address: 0x14, Reset: 0x00, Name: LLINE1MIX

Lineout 1 Left Mixer Control

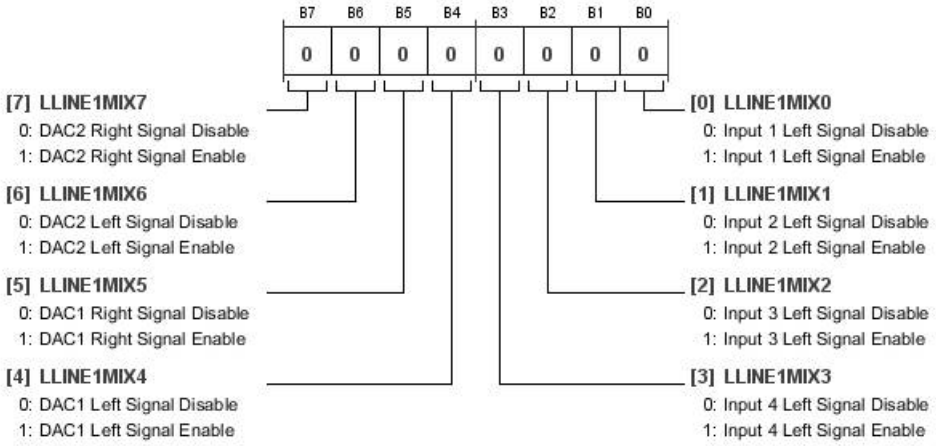


Table 55. Bit Descriptions for LLINE1MIX

Bits	Bit Name	Settings	Description	Reset	Access
7	LLINE1MIX7			0x0	RW
		0	DAC2 Right Signal Disable		
		1	DAC2 Right Signal Enable		
6	LLINE1MIX6			0x0	RW
		0	DAC2 Left Signal Disable		
		1	DAC2 Left Signal Enable		
5	LLINE1MIX5			0x0	RW
		0	DAC1 Right Signal Disable		
		1	DAC1 Right Signal Enable		
4	LLINE1MIX4			0x0	RW
		0	DAC1 Left Signal Disable		
		1	DAC1 Left Signal Enable		
3	LLINE1MIX3			0x0	RW
		0	Input 4 Left Signal Disable		
		1	Input 4 Left Signal Enable		
2	LLINE1MIX2			0x0	RW
		0	Input 3 Left Signal Disable		
		1	Input 3 Left Signal Enable		
1	LLINE1MIX1			0x0	RW
		0	Input 2 Left Signal Disable		
		1	Input 2 Left Signal Enable		
0	LLINE1MIX0			0x0	RW
		0	Input 1 Left Signal Disable		
		1	Input 1 Left Signal Enable		

RLINE1MIX REGISTER

Address: 0x15, Reset: 0x00, Name: RLINE1MIX

Lineout 1 Right Mixer Control

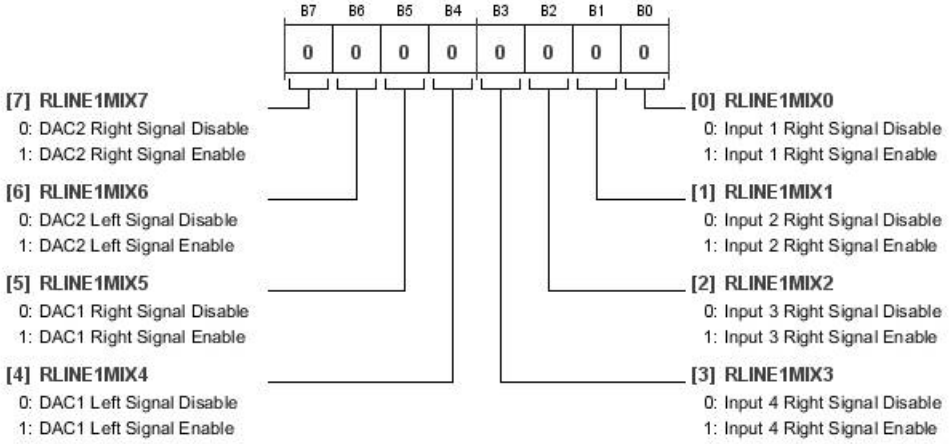


Table 56. Bit Descriptions for RLINE1MIX

Bits	Bit Name	Settings	Description	Reset	Access
7	RLINE1MIX7			0x0	RW
		0	DAC2 Right Signal Disable		
		1	DAC2 Right Signal Enable		
6	RLINE1MIX6			0x0	RW
		0	DAC2 Left Signal Disable		
		1	DAC2 Left Signal Enable		
5	RLINE1MIX5			0x0	RW
		0	DAC1 Right Signal Disable		
		1	DAC1 Right Signal Enable		
4	RLINE1MIX4			0x0	RW
		0	DAC1 Left Signal Disable		
		1	DAC1 Left Signal Enable		
3	RLINE1MIX3			0x0	RW
		0	Input 4 Right Signal Disable		
		1	Input 4 Right Signal Enable		
2	RLINE1MIX2			0x0	RW
		0	Input 3 Right Signal Disable		
		1	Input 3 Right Signal Enable		
1	RLINE1MIX1			0x0	RW
		0	Input 2 Right Signal Disable		
		1	Input 2 Right Signal Enable		
0	RLINE1MIX0			0x0	RW
		0	Input 1 Right Signal Disable		
		1	Input 1 Right Signal Enable		

LLINE2MIX REGISTER

Address: 0x16, Reset: 0x00, Name: LLINE2MIX

Lineout 2 Left Mixer Control

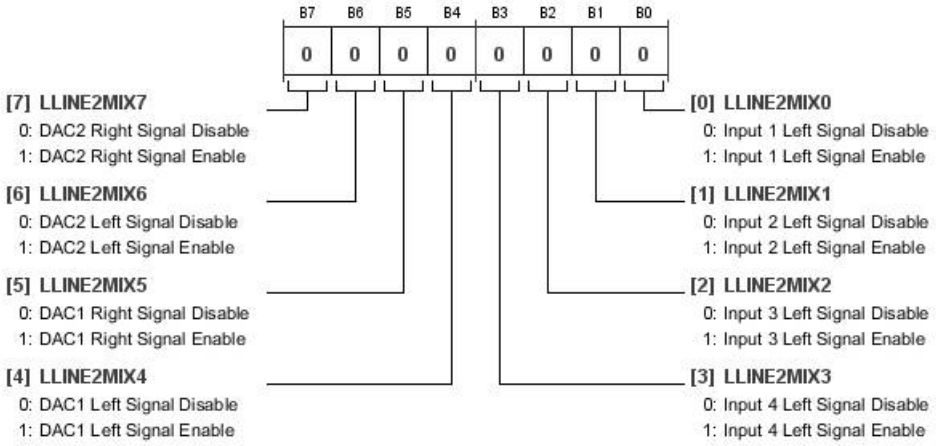


Table 57. Bit Descriptions for LLINE2MIX

Bits	Bit Name	Settings	Description	Reset	Access
7	LLINE2MIX7			0x0	RW
		0	DAC2 Right Signal Disable		
		1	DAC2 Right Signal Enable		
6	LLINE2MIX6			0x0	RW
		0	DAC2 Left Signal Disable		
		1	DAC2 Left Signal Enable		
5	LLINE2MIX5			0x0	RW
		0	DAC1 Right Signal Disable		
		1	DAC1 Right Signal Enable		
4	LLINE2MIX4			0x0	RW
		0	DAC1 Left Signal Disable		
		1	DAC1 Left Signal Enable		
3	LLINE2MIX3			0x0	RW
		0	Input 4 Left Signal Disable		
		1	Input 4 Left Signal Enable		
2	LLINE2MIX2			0x0	RW
		0	Input 3 Left Signal Disable		
		1	Input 3 Left Signal Enable		
1	LLINE2MIX1			0x0	RW
		0	Input 2 Left Signal Disable		
		1	Input 2 Left Signal Enable		
0	LLINE2MIX0			0x0	RW
		0	Input 1 Left Signal Disable		
		1	Input 1 Left Signal Enable		

RLINE2MIX REGISTER

Address: 0x17, Reset: 0x00, Name: RLINE2MIX

Lineout 2 Right Mixer Control

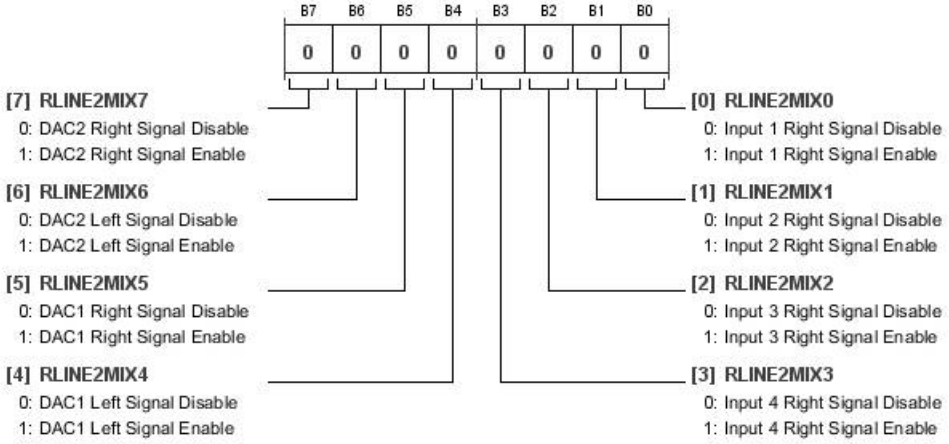


Table 58. Bit Descriptions for RLINE2MIX

Bits	Bit Name	Settings	Description	Reset	Access
7	RLINE2MIX7			0x0	RW
		0	DAC2 Right Signal Disable		
		1	DAC2 Right Signal Enable		
6	RLINE2MIX6			0x0	RW
		0	DAC2 Left Signal Disable		
		1	DAC2 Left Signal Enable		
5	RLINE2MIX5			0x0	RW
		0	DAC1 Right Signal Disable		
		1	DAC1 Right Signal Enable		
4	RLINE2MIX4			0x0	RW
		0	DAC1 Left Signal Disable		
		1	DAC1 Left Signal Enable		
3	RLINE2MIX3			0x0	RW
		0	Input 4 Right Signal Disable		
		1	Input 4 Right Signal Enable		
2	RLINE2MIX2			0x0	RW
		0	Input 3 Right Signal Disable		
		1	Input 3 Right Signal Enable		
1	RLINE2MIX1			0x0	RW
		0	Input 2 Right Signal Disable		
		1	Input 2 Right Signal Enable		
0	RLINE2MIX0			0x0	RW
		0	Input 1 Right Signal Disable		
		1	Input 1 Right Signal Enable		

LCDMIX (SPEAKER OUTPUT) REGISTER

Address: 0x18, Reset: 0x00, Name: LCDMIX

Speaker Out Left Mixer Control

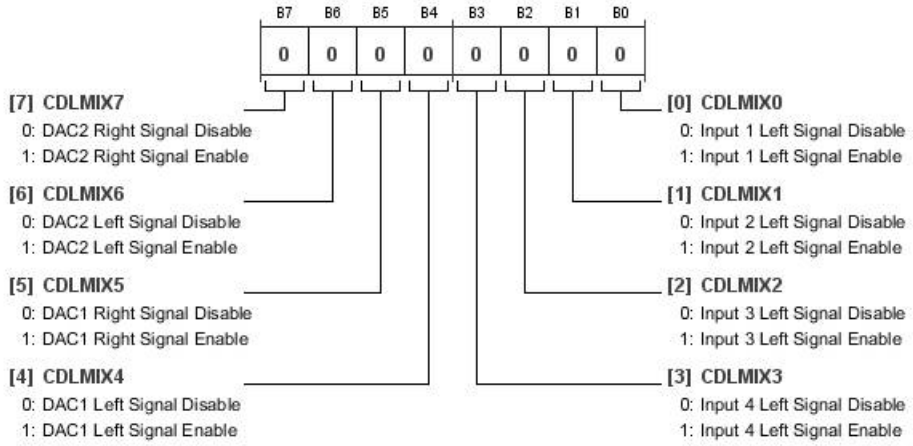


Table 59. Bit Descriptions for LCDMIX

Bits	Bit Name	Settings	Description	Reset	Access
7	CDLMIX7			0x0	RW
		0	DAC2 Right Signal Disable		
		1	DAC2 Right Signal Enable		
6	CDLMIX6			0x0	RW
		0	DAC2 Left Signal Disable		
		1	DAC2 Left Signal Enable		
5	CDLMIX5			0x0	RW
		0	DAC1 Right Signal Disable		
		1	DAC1 Right Signal Enable		
4	CDLMIX4			0x0	RW
		0	DAC1 Left Signal Disable		
		1	DAC1 Left Signal Enable		
3	CDLMIX3			0x0	RW
		0	Input 4 Left Signal Disable		
		1	Input 4 Left Signal Enable		
2	CDLMIX2			0x0	RW
		0	Input 3 Left Signal Disable		
		1	Input 3 Left Signal Enable		
1	CDLMIX1			0x0	RW
		0	Input 2 Left Signal Disable		
		1	Input 2 Left Signal Enable		
0	CDLMIX0			0x0	RW
		0	Input 1 Left Signal Disable		
		1	Input 1 Left Signal Enable		

RCDMIX (SPEAKER OUTPUT) REGISTER

Address: 0x19, Reset: 0x00, Name: RCDMIX

Speaker Out Right Mixer Control

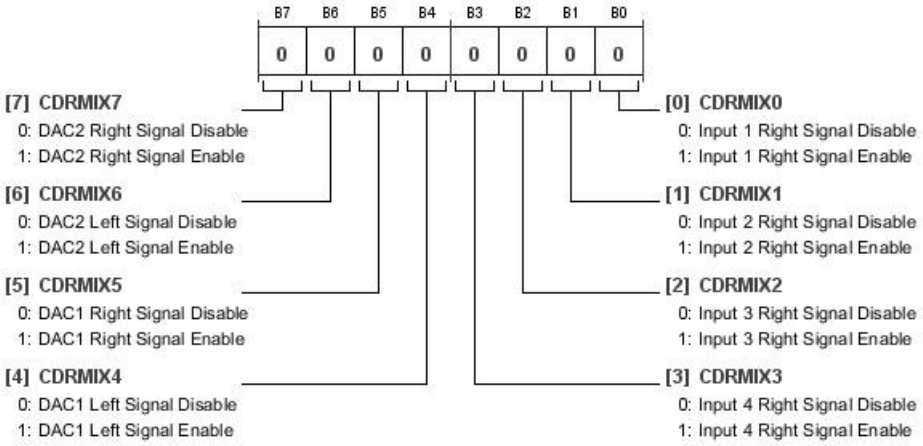


Table 60. Bit Descriptions for RCDMIX

Bits	Bit Name	Settings	Description	Reset	Access
7	CDRMIX7			0x0	RW
		0	DAC2 Right Signal Disable		
		1	DAC2 Right Signal Enable		
6	CDRMIX6			0x0	RW
		0	DAC2 Left Signal Disable		
		1	DAC2 Left Signal Enable		
5	CDRMIX5			0x0	RW
		0	DAC1 Right Signal Disable		
		1	DAC1 Right Signal Enable		
4	CDRMIX4			0x0	RW
		0	DAC1 Left Signal Disable		
		1	DAC1 Left Signal Enable		
3	CDRMIX3			0x0	RW
		0	Input 4 Right Signal Disable		
		1	Input 4 Right Signal Enable		
2	CDRMIX2			0x0	RW
		0	Input 3 Right Signal Disable		
		1	Input 3 Right Signal Enable		
1	CDRMIX1			0x0	RW
		0	Input 2 Right Signal Disable		
		1	Input 2 Right Signal Enable		
0	CDRMIX0			0x0	RW
		0	Input 1 Right Signal Disable		
		1	Input 1 Right Signal Enable		

LHPMIX REGISTER

Address: 0x1A, Reset: 0x00, Name: LHPMIX

Headphone Out Left Mixer Control

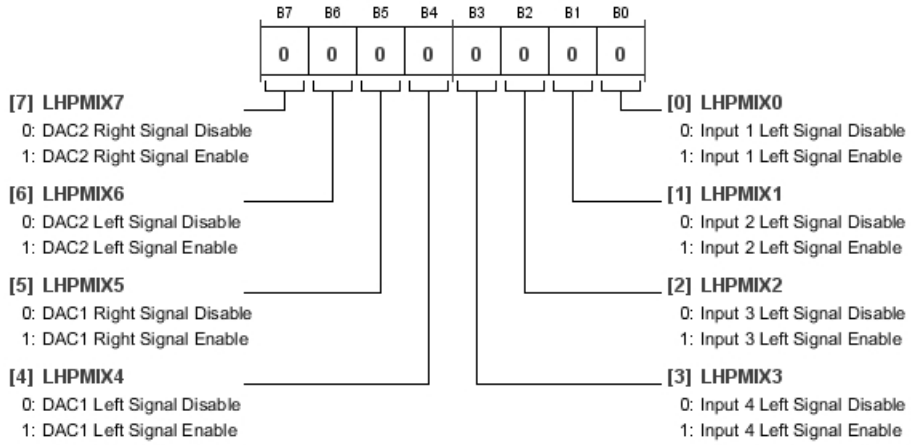


Table 61. Bit Descriptions for LHPMIX

Bits	Bit Name	Settings	Description	Reset	Access
7	LHPMIX7			0x0	RW
		0	DAC2 Right Signal Disable		
		1	DAC2 Right Signal Enable		
6	LHPMIX6			0x0	RW
		0	DAC2 Left Signal Disable		
		1	DAC2 Left Signal Enable		
5	LHPMIX5			0x0	RW
		0	DAC1 Right Signal Disable		
		1	DAC1 Right Signal Enable		
4	LHPMIX4			0x0	RW
		0	DAC1 Left Signal Disable		
		1	DAC1 Left Signal Enable		
3	LHPMIX3			0x0	RW
		0	Input 4 Left Signal Disable		
		1	Input 4 Left Signal Enable		
2	LHPMIX2			0x0	RW
		0	Input 3 Left Signal Disable		
		1	Input 3 Left Signal Enable		
1	LHPMIX1			0x0	RW
		0	Input 2 Left Signal Disable		
		1	Input 2 Left Signal Enable		
0	LHPMIX0			0x0	RW
		0	Input 1 Left Signal Disable		
		1	Input 1 Left Signal Enable		

RHPMIX REGISTER

Address: 0x1B, Reset: 0x00, Name: RHPMIX

Headphone Out Right Mixer Control

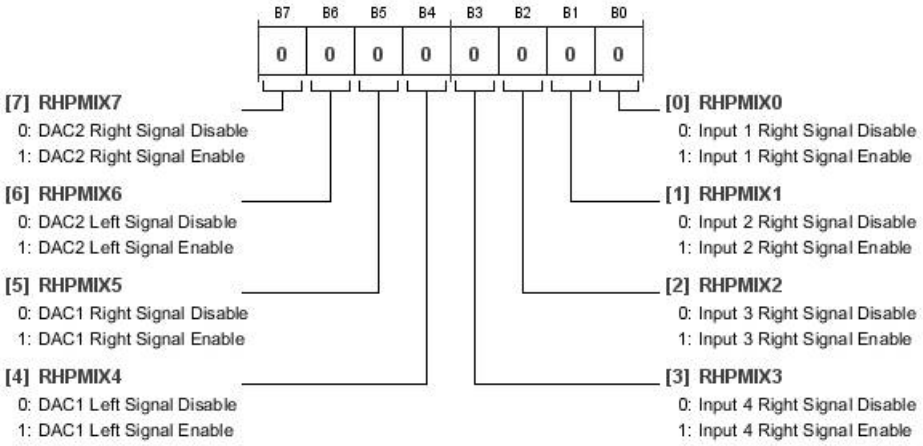


Table 62. Bit Descriptions for RHPMIX

Bits	Bit Name	Settings	Description	Reset	Access
7	RHPMIX7			0x0	RW
		0	DAC2 Right Signal Disable		
		1	DAC2 Right Signal Enable		
6	RHPMIX6			0x0	RW
		0	DAC2 Left Signal Disable		
		1	DAC2 Left Signal Enable		
5	RHPMIX5			0x0	RW
		0	DAC1 Right Signal Disable		
		1	DAC1 Right Signal Enable		
4	RHPMIX4			0x0	RW
		0	DAC1 Left Signal Disable		
		1	DAC1 Left Signal Enable		
3	RHPMIX3			0x0	RW
		0	Input 4 Right Signal Disable		
		1	Input 4 Right Signal Enable		
2	RHPMIX2			0x0	RW
		0	Input 3 Right Signal Disable		
		1	Input 3 Right Signal Enable		
1	RHPMIX1			0x0	RW
		0	Input 2 Right Signal Disable		
		1	Input 2 Right Signal Enable		
0	RHPMIX0			0x0	RW
		0	Input 1 Right Signal Disable		
		1	Input 1 Right Signal Enable		

EPMIX REGISTER

Address: 0x1C, Reset: 0x00, Name: EPMIX

Earpiece Out Mixer Control

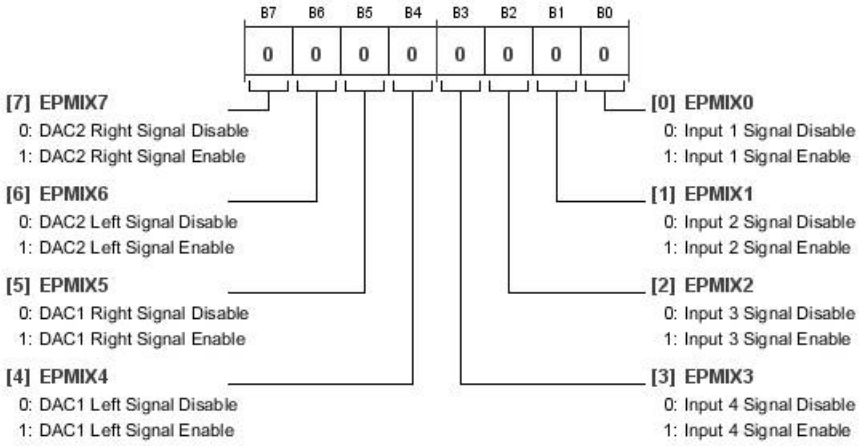


Table 63. Bit Descriptions for EPMIX

Bits	Bit Name	Settings	Description	Reset	Access
7	EPMIX7			0x0	RW
		0	DAC2 Right Signal Disable		
		1	DAC2 Right Signal Enable		
6	EPMIX6			0x0	RW
		0	DAC2 Left Signal Disable		
		1	DAC2 Left Signal Enable		
5	EPMIX5			0x0	RW
		0	DAC1 Right Signal Disable		
		1	DAC1 Right Signal Enable		
4	EPMIX4			0x0	RW
		0	DAC1 Left Signal Disable		
		1	DAC1 Left Signal Enable		
3	EPMIX3			0x0	RW
		0	Input 4 Signal Disable		
		1	Input 4 Signal Enable		
2	EPMIX2			0x0	RW
		0	Input 3 Signal Disable		
		1	Input 3 Signal Enable		
1	EPMIX1			0x0	RW
		0	Input 2 Signal Disable		
		1	Input 2 Signal Enable		
0	EPMIX0			0x0	RW
		0	Input 1 Signal Disable		
		1	Input 1 Signal Enable		

HP_CTRL REGISTER

Address: 0x1D, Reset: 0x00, Name: HP_CTRL

Headphone Amplifier Mode Control 1

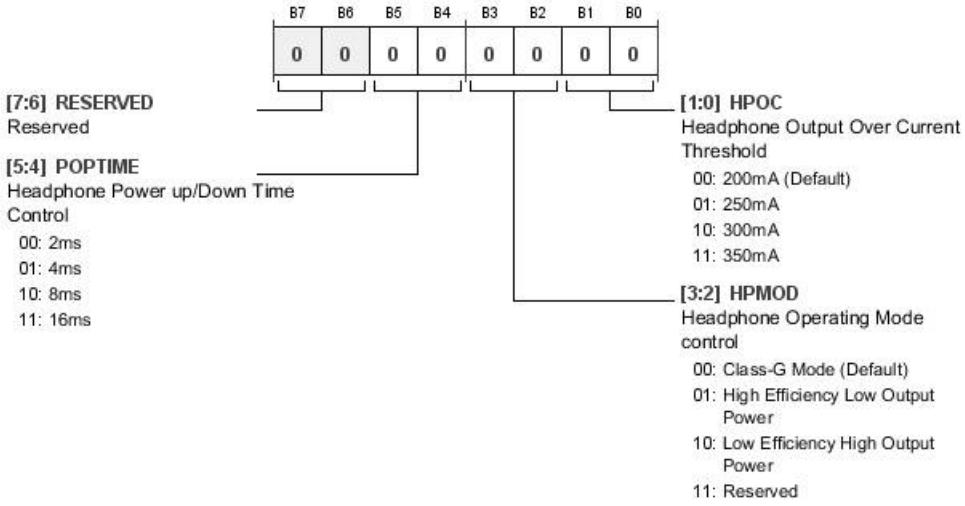


Table 64. Bit Descriptions for HP_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	RW
[5:4]	POPTIME		Headphone Power-Up/Power-Down Time Control. Headphone amplifier turn on time.	0x0	RW
		00	2 ms		
		01	4 ms		
		10	8 ms		
		11	16 ms		
[3:2]	HPMOD		Headphone Operating Mode Control. Headphone amplifier mode setting.	0x0	RW
		00	Class-G mode (default)		
		01	High efficiency low output power		
		10	Low efficiency high output power		
		11	Reserved		
[1:0]	HPOC		Headphone Output Overcurrent Threshold. Headphone amplifier overcurrent threshold setting.	0x0	RW
		00	200 mA (default)		
		01	250 mA		
		10	300 mA		
		11	350 mA		

HP_CTRL2 REGISTER

Address: 0x1E, Reset: 0x00, Name: HP_CTRL2

Headphone Amplifier Mode Control 2

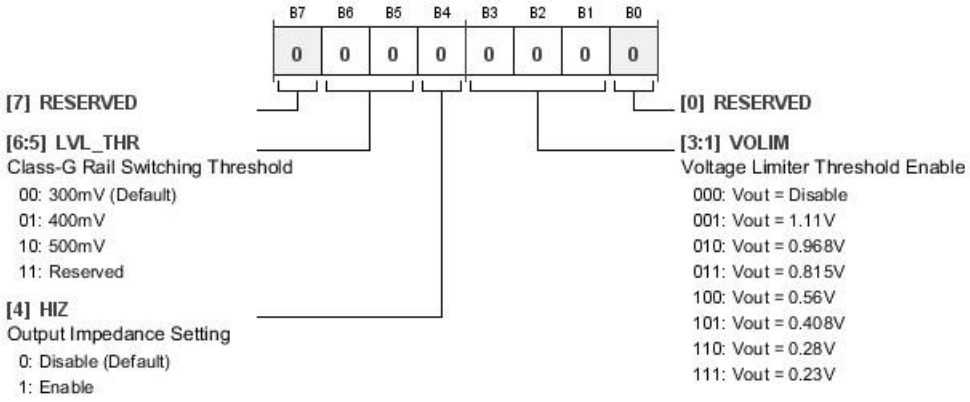


Table 65. Bit Descriptions for HP_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
[6:5]	LVL_THR		Class-G Rail Switching Threshold.	0x0	RW
		00	300 mV (Default)		
		01	400 mV		
		10	500 mV		
		11	Reserved		
4	HIZ		Output Impedance Setting.	0x0	RW
		0	Disable (Default)		
		1	Enable		
[3:1]	VOLIM		Voltage Limiter Threshold Enable.	0x0	RW
		000	V_{OUT} = Disable		
		001	V_{OUT} = 1.11 V		
		010	V_{OUT} = 0.968 V		
		011	V_{OUT} = 0.815 V		
		100	V_{OUT} = 0.56 V		
		101	V_{OUT} = 0.408 V		
		110	V_{OUT} = 0.28 V		
		111	V_{OUT} = 0.23 V		

LS_CTRL (SPEAKER) REGISTER

Address: 0x1F, Reset: 0x00, Name: LS_CTRL

Speaker Amplifier Mode Control

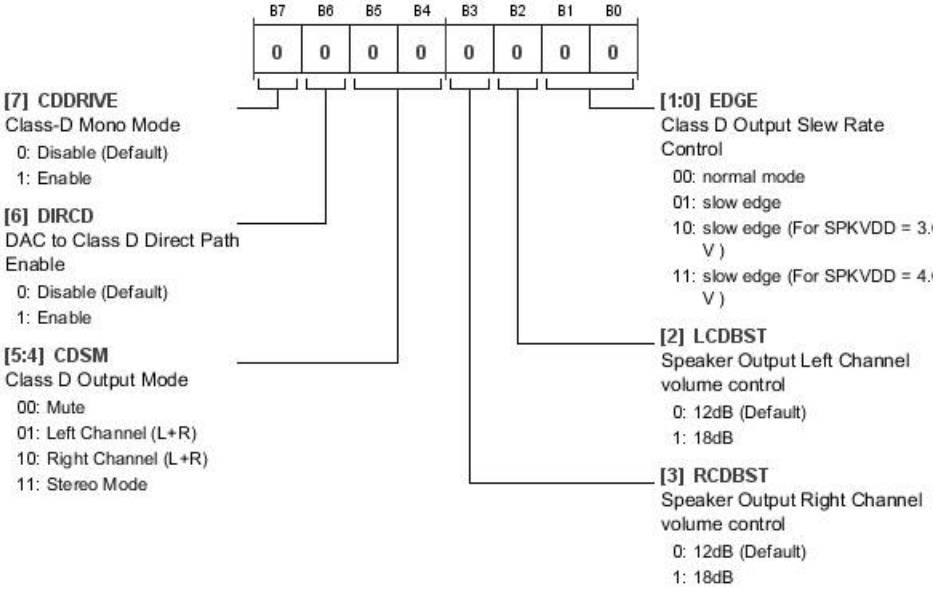


Table 66. Bit Descriptions for LS_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
7	CDDRIVE		Class-D Mono Mode.	0x0	RW
		0	Disable (default)		
		1	Enable		
6	DIRCD		DAC to Class-D Direct Path Enable. DAC direct couple to Class-D enable/disable control.	0x0	RW
		0	Disable (default)		
		1	Enable		
[5:4]	CDSM		Class-D Output Mode.	0x0	RW
		00	Mute		
		01	Left Channel (L + R)		
		10	Right Channel (L + R)		
		11	Stereo Mode		
3	RCDBST		Speaker Output Right Channel Volume Control.	0x0	RW
		0	12 dB (default)		
		1	18 dB		
2	LCDBST		Speaker Output Left Channel Volume Control.	0x0	RW
		0	12 dB (default)		
		1	18 dB		
[1:0]	EDGE		Class-D Output Slew Rate Control.	0x0	RW
		00	Normal mode		
		01	Slow edge		
		10	Slow edge (for SPKVDD = 3.0 V)		
		11	Slow edge (for SPKVDD = 4.0 V)		

EPCONTROL REGISTER

Address: 0x21, Reset: 0x00, Name: EPCONTROL

Earpiece Amplifier and Microphone Bias Output Control

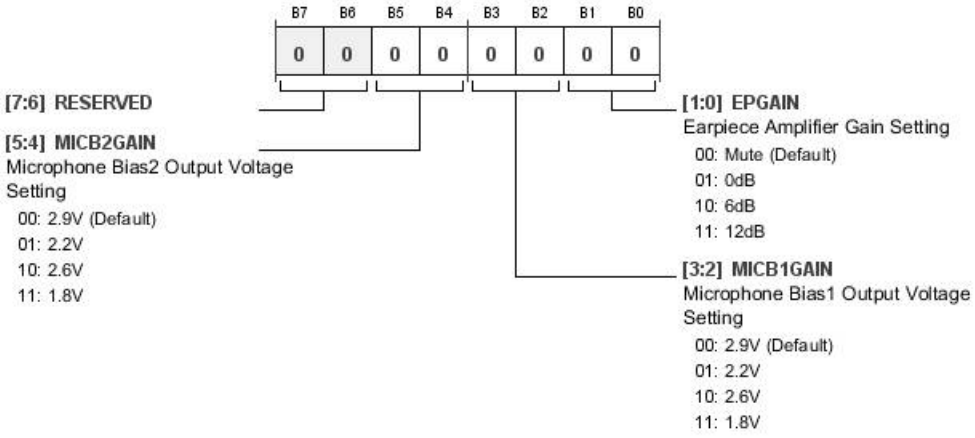


Table 67. Bit Descriptions for EPCONTROL

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	RW
[5:4]	MICB2GAIN		Microphone Bias 2 Output Voltage Setting.	0x0	RW
		00	2.9 V (default)		
		01	2.2 V		
		10	2.6 V		
		11	1.8 V		
[3:2]	MICB1GAIN		Microphone Bias 1 Output Voltage Setting.	0x0	RW
		00	2.9 V (default)		
		01	2.2 V		
		10	2.6 V		
		11	1.8 V		
[1:0]	EPGAIN		Earpiece Amplifier Gain Setting.	0x0	RW
		00	Mute (default)		
		01	0 dB		
		10	6 dB		
		11	12 dB		

MICBIAS_CTRL1 REGISTER

Address: 0x22, Reset: 0x00, Name: MICBIAS_CTRL1

Microphone Bias 1 Control

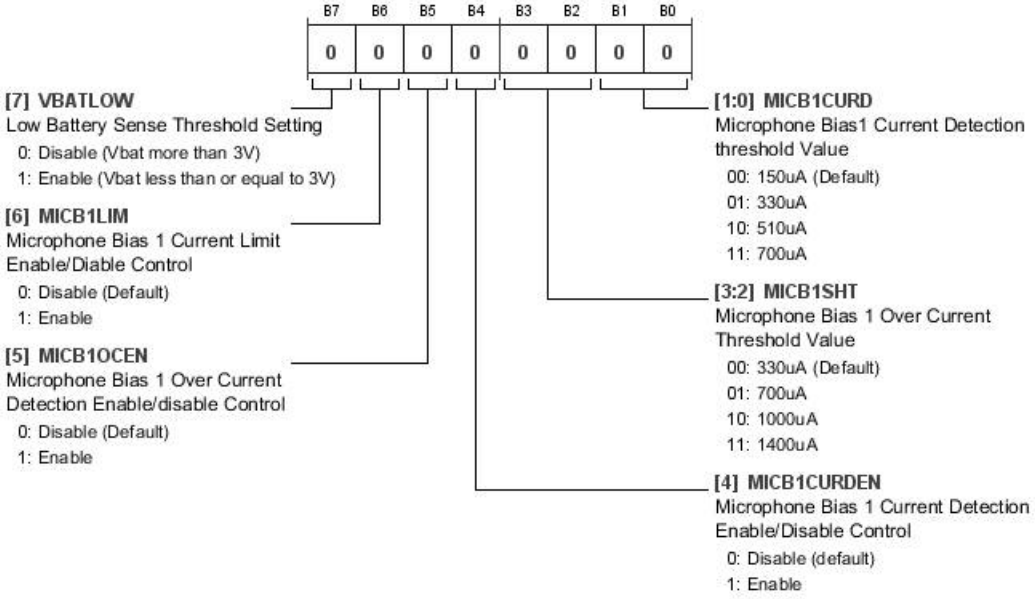


Table 68. Bit Descriptions for MICBIAS_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
7	VBATLOW		Low Battery Sense Threshold Setting.	0x0	RW
		0	Disable (V_{BAT} > 3 V)		
		1	Enable (V_{BAT} ≤ 3 V)		
6	MICB1LIM		Microphone Bias 1 Current Limit Enable/Disable Control.	0x0	RW
		0	Disable (default)		
		1	Enable		
5	MICB1OCEN		Microphone Bias 1 Overcurrent Detection Enable/disable Control.	0x0	RW
		0	Disable (default)		
		1	Enable		
4	MICB1CURDEN		Microphone Bias 1 Current Detection Enable/Disable Control.	0x0	RW
		0	Disable (default)		
		1	Enable		
[3:2]	MICB1SHT		Microphone Bias 1 Overcurrent Threshold Value.	0x0	RW
		00	330 µA (default)		
		01	700 µA		
		10	1000 µA		
		11	1400 µA		
[1:0]	MICB1CURD		Microphone Bias 1 Current Detection Threshold Value.	0x0	RW
		00	150 µA (default)		
		01	330 µA		
		10	510 µA		
		11	700 µA		

MICBIAS_CTRL2 REGISTER

Address: 0x23, Reset: 0x00, Name: MICBIAS_CTRL2

Microphone Bias 2 Control

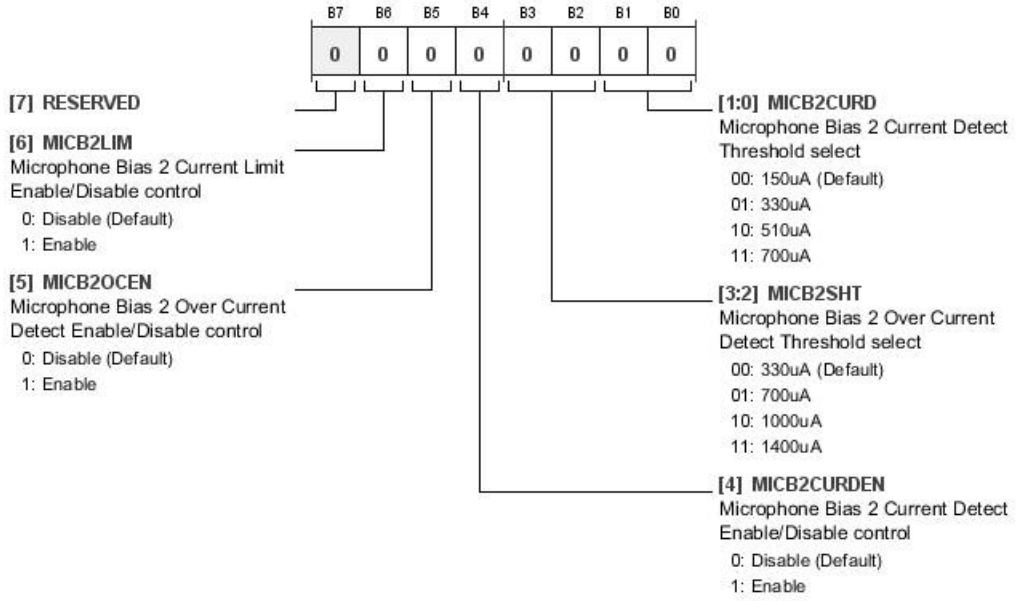


Table 69. Bit Descriptions for MICBIAS_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
6	MICB2LIM		Microphone Bias 2 Current Limit Enable/Disable Control.	0x0	RW
		0	Disable (default)		
		1	Enable		
5	MICB2OCEN		Microphone Bias 2 Overcurrent Detect Enable/Disable Control.	0x0	RW
		0	Disable (default)		
		1	Enable		
4	MICB2CURDEN		Microphone Bias 2 Current Detect Enable/Disable Control.	0x0	RW
		0	Disable (default)		
		1	Enable		
[3:2]	MICB2SHT		Microphone Bias 2 Overcurrent Detect Threshold Select.	0x0	RW
		00	330 µA (default)		
		01	700 µA		
		10	1000 µA		
		11	1400 µA		
[1:0]	MICB2CURD		Microphone Bias 2 Current Detect Threshold Select.	0x0	RW
		00	150 µA (default)		
		01	330 µA		
		10	510 µA		
		11	700 µA		

OUTPUT_CONTROL (LINE) REGISTER

Address: 0x24, Reset: 0x00, Name: OUTPUT_CONTROL

Line Output Mode Control

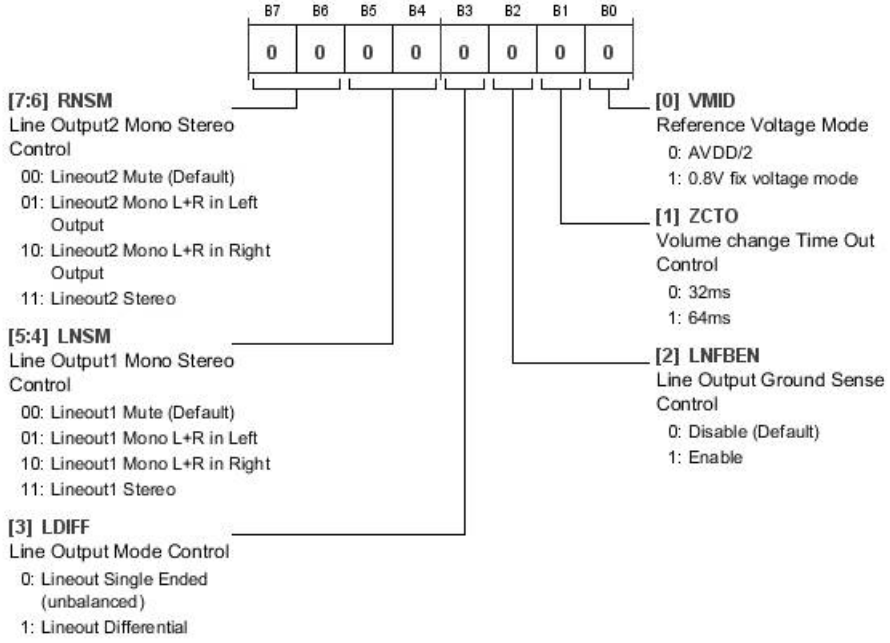


Table 70. Bit Descriptions for OUTPUT_CONTROL

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RNSM		Line Output 2 Mono Stereo Control.	0x0	RW
		00	Lineout 2 Mute (Default)		
		01	Lineout 2 Mono L + R in Left Output		
		10	Lineout 2 Mono L + R in Right Output		
		11	Lineout 2 Stereo		
[5:4]	LNSM		Line Output 1 Mono Stereo Control.	0x0	RW
		00	Lineout 1 Mute (Default)		
		01	Lineout 1 Mono L + R in Left Output		
		10	Lineout 1 Mono L + R in Right Output		
		11	Lineout 1 Stereo		
3	LDIFF		Line Output Mode Control.	0x0	RW
		0	Lineout Single-Ended (Unbalanced)		
		1	Lineout Differential		
2	LNFBEN		Line Output Ground Sense Control.	0x0	RW
		0	Disable (Default)		
		1	Enable		
1	ZCTO		Volume Change Timeout Control.	0x0	RW
		0	32 ms		
		1	64 ms		
0	VMID		Reference Voltage Mode.	0x0	RW
		0	AVDD/2		
		1	0.8 V Fix Voltage Mode		

PWDN_CTRL1 REGISTER

Address: 0x25, Reset: 0x00, Name: PWDN_CTRL1

Power-Down Block Control 1

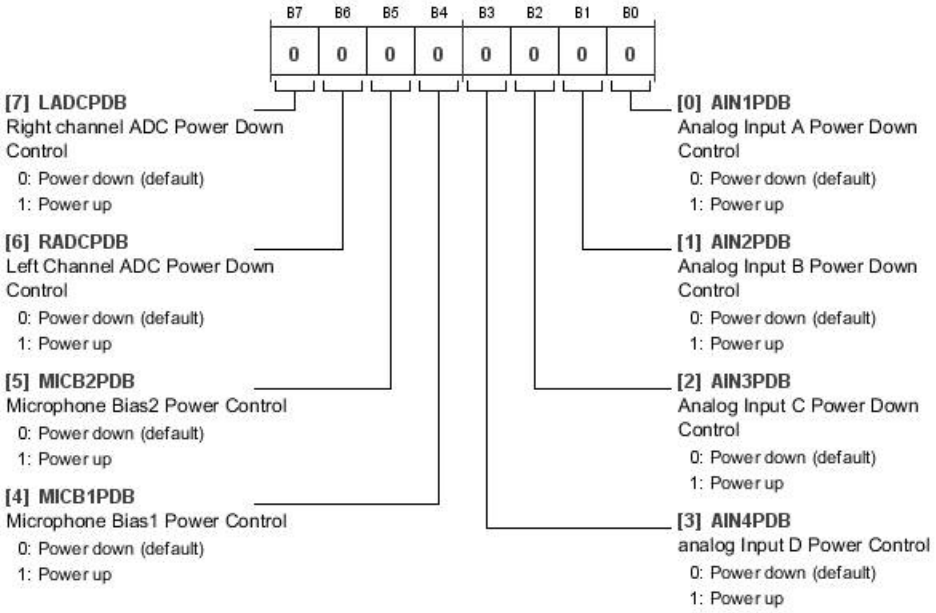


Table 71. Bit Descriptions for PWDN_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
7	LADCPDB		Right Channel ADC Power-Down Control.	0x0	RW
		0	Power down (default)		
		1	Power up		
6	RADCPDB		Left Channel ADC Power-Down Control.	0x0	RW
		0	Power down (default)		
		1	Power up		
5	MICB2PDB		Microphone Bias 2 Power-Down Control.	0x0	RW
		0	Power down (default)		
		1	Power up		
4	MICB1PDB		Microphone Bias 1 Power-Down Control.	0x0	RW
		0	Power down (default)		
		1	Power up		
3	AIN4PDB		Analog Input 4 Power-Down Control.	0x0	RW
		0	Power down (default)		
		1	Power up		
2	AIN3PDB		Analog Input 3 Power-Down Control.	0x0	RW
		0	Power down (default)		
		1	Power up		
1	AIN2PDB		Analog Input 2 Power-Down Control.	0x0	RW
		0	Power down (default)		
		1	Power up		
0	AIN1PDB		Analog Input 1 Power-Down Control.	0x0	RW
		0	Power down (default)		
		1	Power up		

PWDN_CTRL2 REGISTER

Address: 0x26, Reset: 0x00, Name: PWDN_CTRL2

Power-Down Block Control 2

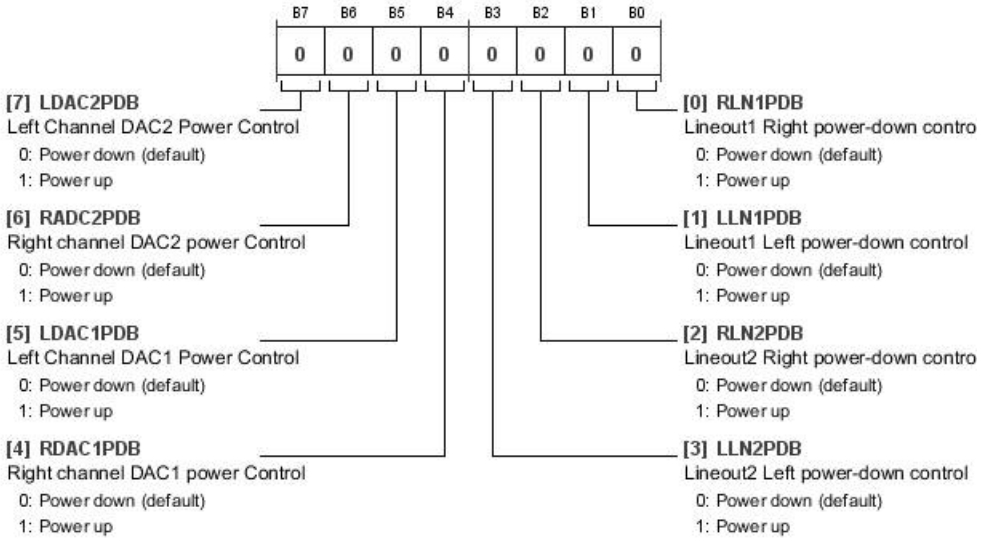


Table 72. Bit Descriptions for PWDN_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
7	LDAC2PDB		Left Channel DAC 2 Power-Down Control.	0x0	RW
		0	Power down (default)		
		1	Power up		
6	RADC2PDB		Right Channel DAC 2 Power-Down Control.	0x0	RW
		0	Power down (default)		
		1	Power up		
5	LDAC1PDB		Left Channel DAC1 Power-Down Control.	0x0	RW
		0	Power down (default)		
		1	Power up		
4	RDAC1PDB		Right Channel DAC1 Power-Down Control.	0x0	RW
		0	Power down (default)		
		1	Power up		
3	LLN2PDB		Lineout2 Left Power-Down Control.	0x0	RW
		0	Power down (default)		
		1	Power up		
2	RLN2PDB		Lineout2 Right Power-Down Control.	0x0	RW
		0	Power down (default)		
		1	Power up		
1	LLN1PDB		Lineout1 Left Power-Down Control.	0x0	RW
		0	Power down (default)		
		1	Power up		
0	RLN1PDB		Lineout1 Right Power-Down Control.	0x0	RW
		0	Power down (default)		
		1	Power up		

PWDN_CTRL3 REGISTER

Address: 0x27, Reset: 0x00, Name: PWDN_CTRL3

Power-Down Block Control 3

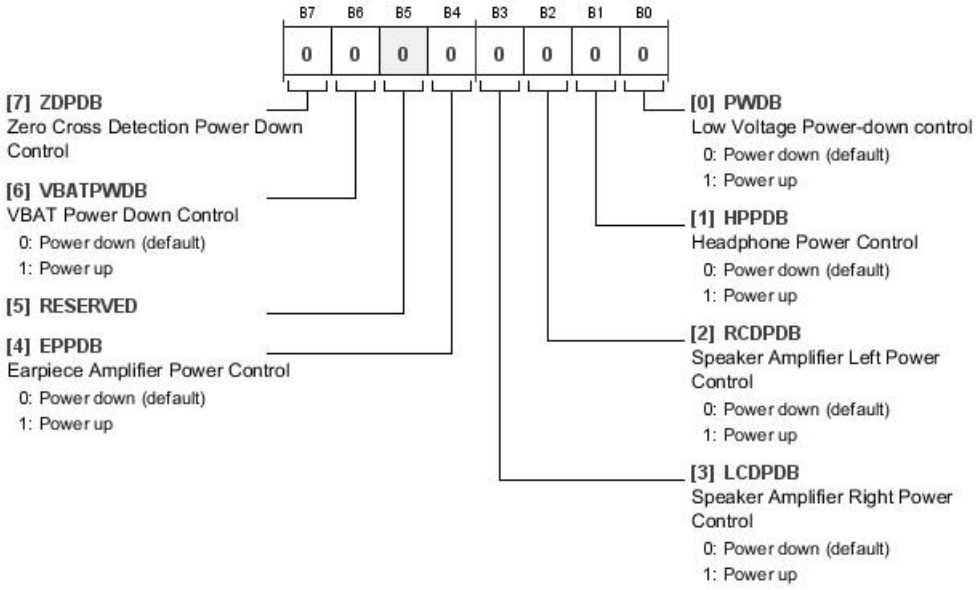


Table 73. Bit Descriptions for PWDN_CTRL3

Bits	Bit Name	Settings	Description	Reset	Access
7	ZDPDB		Zero Cross Detection Power-Down Control.	0x0	RW
6	VBATPWDB		VBAT Power-Down Control.	0x0	RW
		0	Power down (default)		
		1	Power up		
5	RESERVED		Reserved.	0x0	RW
4	EPPDB		Earpiece Amplifier Power Control.	0x0	RW
		0	Power down (default)		
		1	Power up		
3	LCDPDB		Speaker Amplifier Right Power Control.	0x0	RW
		0	Power down (default)		
		1	Power up		
2	RCDPDB		Speaker Amplifier Left Power Control.	0x0	RW
		0	Power down (default)		
		1	Power up		
1	HPPDB		Headphone Power Control.	0x0	RW
		0	Power down (default)		
		1	Power up		
0	PWDB		Low Voltage Power-Down Control.	0x0	RW
		0	Power down (default)		
		1	Power up		

DPLLA_CTRL REGISTER

Address: 0x28, Reset: 0x00, Name: DPLLA_CTRL

DPLLA Control

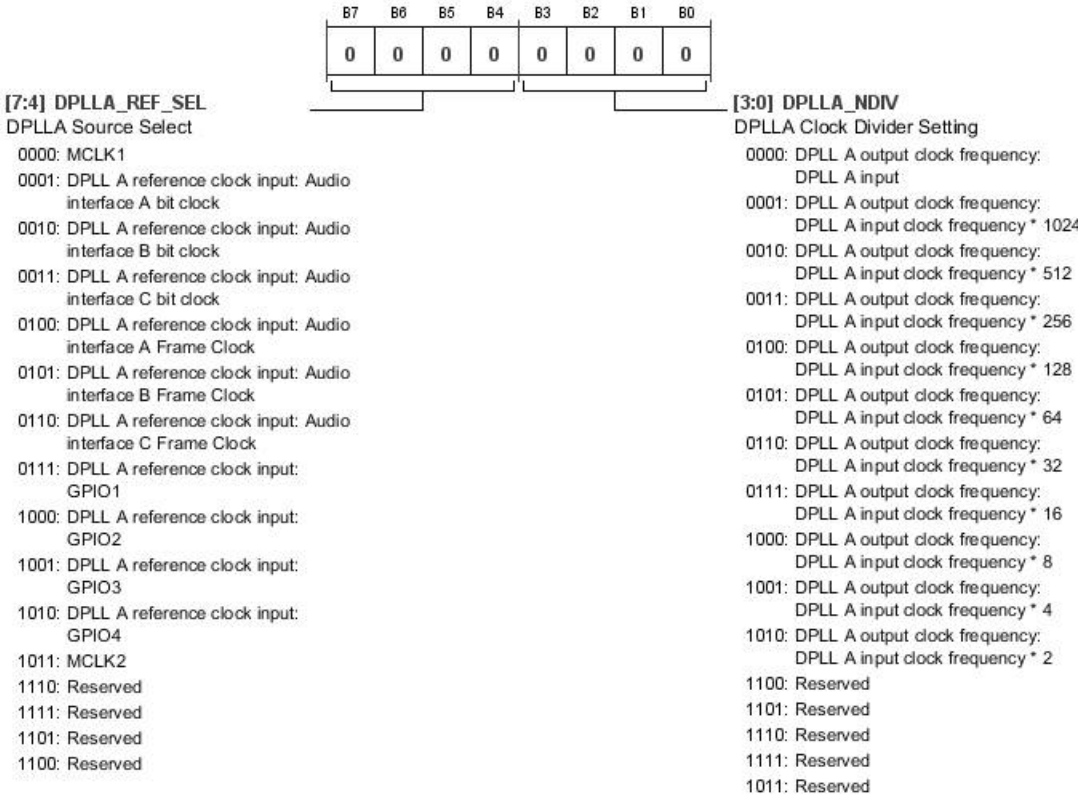


Table 74. Bit Descriptions for DPLLA_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DPLLA_REF_SEL		DPLLA Source Select. DPLLA source selection can be set to one of the following: Digital Audio Interface A/B/C bit clock/frame clock or GPIO1/2/3/4 or Master Clock Input 1/2.	0x0	RW
		0000	MCLK1		
		0001	DPLLA reference clock input: Digital Audio Interface A bit clock		
		0010	DPLLA reference clock input: Digital Audio Interface B bit clock		
		0011	DPLLA reference clock input: Digital Audio Interface C bit clock		
		0100	DPLLA reference clock input: Digital Audio Interface A frame clock		
		0101	DPLLA reference clock input: Digital Audio Interface B frame clock		
		0110	DPLLA reference clock input: Digital Audio Interface C frame clock		
		0111	DPLLA reference clock input: GPIO1		
		1000	DPLLA reference clock input: GPIO2		
		1001	DPLLA reference clock input: GPIO3		
		1010	DPLLA reference clock input: GPIO4		
		1011	MCLK2		
		1110	Reserved		
		1111	Reserved		
		1101	Reserved		
		1100	Reserved		

Bits	Bit Name	Settings	Description	Reset	Access
[3:0]	DPLLA_NDIV		DPLLA Clock Divider Setting. DPLLA clock divider settings from 1 to 1024 in 16 steps.	0x0	RW
		0000	DPLLA output clock frequency: DPLLA input		
		0001	DPLLA output clock frequency: DPLLA input clock frequency × 1024		
		0010	DPLLA output clock frequency: DPLLA input clock frequency × 512		
		0011	DPLLA output clock frequency: DPLLA input clock frequency × 256		
		0100	DPLLA output clock frequency: DPLLA input clock frequency × 128		
		0101	DPLLA output clock frequency: DPLLA input clock frequency × 64		
		0110	DPLLA output clock frequency: DPLLA input clock frequency × 32		
		0111	DPLLA output clock frequency: DPLLA input clock frequency × 16		
		1000	DPLLA output clock frequency: DPLLA input clock frequency × 8		
		1001	DPLLA output clock frequency: DPLLA input clock frequency × 4		
		1010	DPLLA output clock frequency: DPLLA input clock frequency × 2		
		1100	Reserved		
		1101	Reserved		
		1110	Reserved		
		1111	Reserved		
		1011	Reserved		

PLLA_CTRL1 REGISTER

Address: 0x29, Reset: 0x00, Name: PLLA_CTRL1

PLLA Fractional Mode Denominator M High Byte

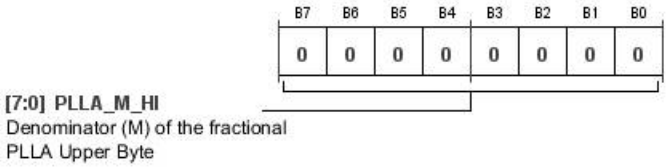


Table 75. Bit Descriptions for PLLA_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PLLA_M_HI		Denominator (M) of the Fractional PLLA Upper Byte. PLLA Fractional Mode Denominator M divider setting upper byte.	0x00	RW

PLLA_CTRL2 REGISTER

Address: 0x2A, Reset: 0x00, Name: PLLA_CTRL2

PLLA Fractional Mode Denominator M Lower Byte

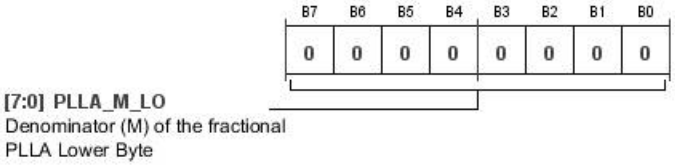


Table 76. Bit Descriptions for PLLA_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PLLA_M_LO		Denominator (M) of the Fractional PLLA Lower Byte. PLLA Fractional Mode Denominator M divider setting lower byte.	0x00	RW

PLLA_CTRL3 REGISTER

Address: 0x2B, Reset: 0x00, Name: PLLA_CTRL3

PLLA Fractional Mode N

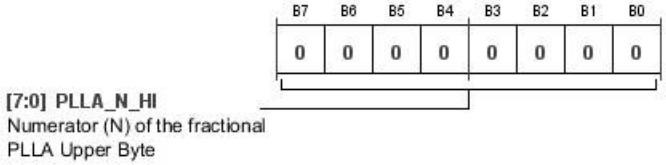


Table 77. Bit Descriptions for PLLA_CTRL3

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PLLA_N_HI		Numerator (N) of the Fractional PLLA Upper Byte. PLLA Fractional Mode Numerator N upper byte.	0x00	RW

PLLA_CTRL4 REGISTER

Address: 0x2C, Reset: 0x00, Name: PLLA_CTRL4

Numerator (N) of the Fractional PLLA Lower Byte

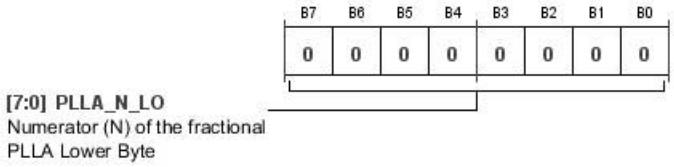


Table 78. Bit Descriptions for PLLA_CTRL4

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PLLA_N_LO		Numerator (N) of the Fractional PLLA Lower Byte. PLLA Fractional Mode Numerator N lower byte.	0x00	RW

PLLA_CTRL5 REGISTER

Address: 0x2D, Reset: 0x00, Name: PLLA_CTRL5

PLLA Type, X and R Value Setting

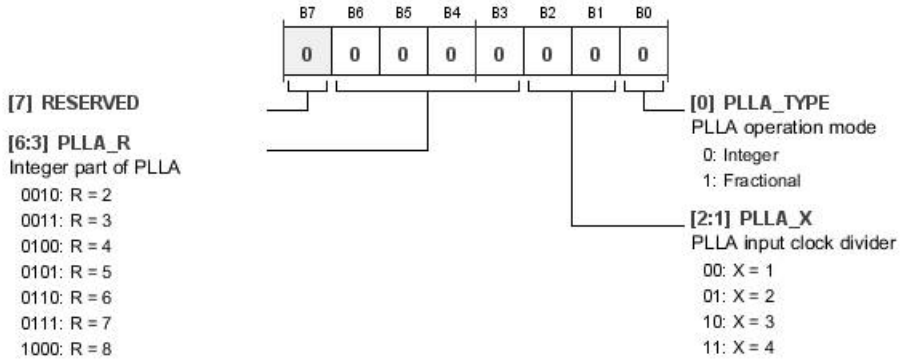


Table 79. Bit Descriptions for PLLA_CTRL5

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
[6:3]	PLLA_R		Integer Part of PLLA. Integer (R) of PLLA.	0x0	RW
		0010	R = 2		
		0011	R = 3		
		0100	R = 4		
		0101	R = 5		
		0110	R = 6		
		0111	R = 7		
		1000	R = 8		
[2:1]	PLLA_X		PLLA Input Clock Divider. PLLA input clock divider (X).	0x0	RW
		00	X = 1		
		01	X = 2		
		10	X = 3		
		11	X = 4		
0	PLLA_TYPE		PLLA Operation Mode. PLLA mode (fractional or integer).	0x0	RW
		0	Integer		
		1	Fractional		

PLLA_CTRL6 REGISTER

Address: 0x2E, Reset: 0x02, Name: PLLA_CTRL6

PLLA Control/Status

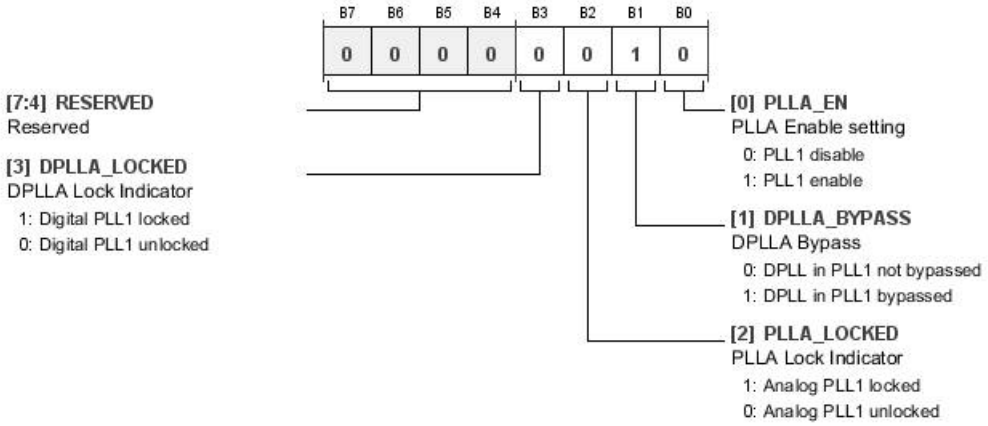


Table 80. Bit Descriptions for PLLA_CTRL6

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved.	0x0	RW
3	DPLLA_LOCKED		DPLLA Lock Indicator. DPLLA lock status indicator.	0x0	R
		1	Digital PLLA locked		
		0	Digital PLLA unlocked		
2	PLLA_LOCKED		PLLA Lock Indicator. PLLA lock status indicator.	0x0	R
		1	Analog PLLA locked		
		0	Analog PLLA unlocked		
1	DPLLA_BYPASS		DPLLA Bypass. DPLLA bypass select.	0x1	RW
		0	DPLL in PLLA not bypassed		
		1	DPLL in PLLA bypassed		
0	PLLA_EN		PLLA Enable Setting. PLLA enable/disable control.	0x0	RW
		0	PLLA disable		
		1	PLLA enable		

DPLLB_CTRL REGISTER

Address: 0x2F, Reset: 0x00, Name: DPLLB_CTRL

DPLLB Control

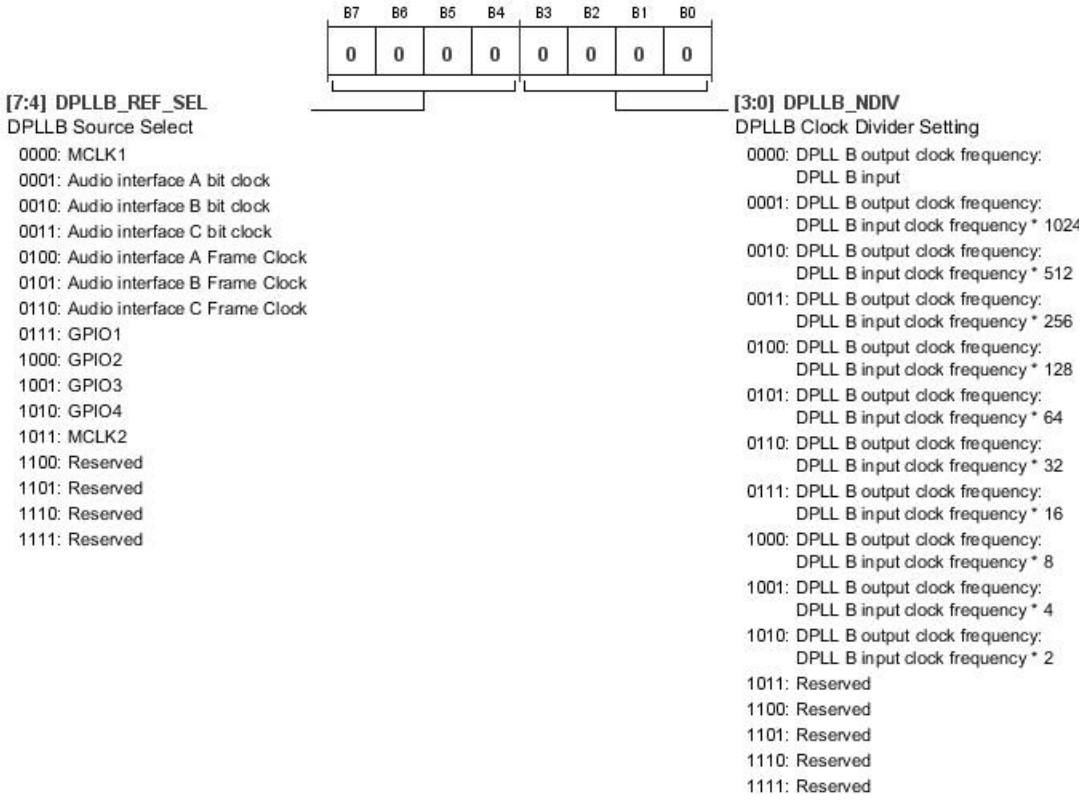


Table 81. Bit Descriptions for DPLLB_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DPLLB_REF_SEL		DPLLB Source Select. DPLLB clock divider settings from 1 to 1024 in 16 steps.	0x0	RW
		0000	MCLK1		
		0001	Audio Interface A bit clock		
		0010	Audio Interface B bit clock		
		0011	Audio Interface C bit clock		
		0100	Audio Interface A Frame Clock		
		0101	Audio Interface B Frame Clock		
		0110	Audio Interface C Frame Clock		
		0111	GPIO1		
		1000	GPIO2		
		1001	GPIO3		
		1010	GPIO4		
		1011	MCLK2		
		1100	Reserved		
		1101	Reserved		
		1110	Reserved		
		1111	Reserved		

Bits	Bit Name	Settings	Description	Reset	Access
[3:0]	DPLLB_NDIV		DPLLB Clock Divider Setting. DPLLB source selection can be set to one of the following: Digital Audio Interface A/B/C bit clock/frame clock or GPIO1/2/3/4 or Master Clock Input 1/2.	0x0	RW
		0000	DPLLB output clock frequency: DPLLB input		
		0001	DPLLB output clock frequency: DPLLB input clock frequency × 1024		
		0010	DPLLB output clock frequency: DPLLB input clock frequency × 512		
		0011	DPLLB output clock frequency: DPLLB input clock frequency × 256		
		0100	DPLLB output clock frequency: DPLLB input clock frequency × 128		
		0101	DPLLB output clock frequency: DPLLB input clock frequency × 64		
		0110	DPLLB output clock frequency: DPLLB input clock frequency × 32		
		0111	DPLLB output clock frequency: DPLLB input clock frequency × 16		
		1000	DPLLB output clock frequency: DPLLB input clock frequency × 8		
		1001	DPLLB output clock frequency: DPLLB input clock frequency × 4		
		1010	DPLLB output clock frequency: DPLLB input clock frequency × 2		
		1011	Reserved		
		1100	Reserved		
		1101	Reserved		
		1110	Reserved		
		1111	Reserved		

PLLB_CTRL1 REGISTER

Address: 0x30, Reset: 0x00, Name: PLLB_CTRL1

PLLB Fractional Mode Denominator M High Byte

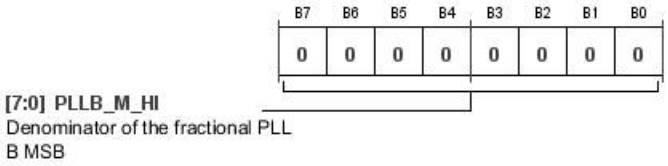


Table 82. Bit Descriptions for PLLB_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PLLB_M_HI		Denominator of the Fractional PLLB MSB. PLLB Fractional Mode Denominator M upper byte.	0x00	RW

PLLB CTRL2 REGISTER

Address: 0x31, Reset: 0x00, Name: PLLB_CTRL2

PLLB Fractional Mode Denominator M Lower Byte

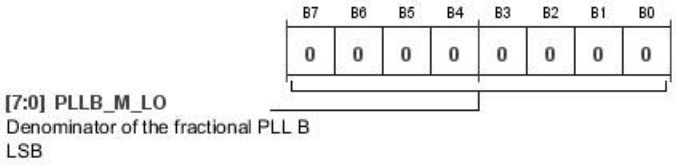


Table 83. Bit Descriptions for PLLB_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PLLB_M_LO		Denominator of the Fractional PLLB LSB. PLLB Fractional Mode Denominator M lower byte.	0x00	RW

PLLB_CTRL3 REGISTER

Address: 0x32, Reset: 0x00, Name: PLLB_CTRL3

PLLB Fractional Mode N

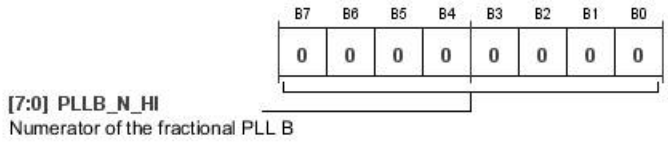


Table 84. Bit Descriptions for PLLB_CTRL3

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PLLB_N_HI		Numerator of the fractional PLLB. PLLB Fractional Mode Numerator N upper byte.	0x00	RW

PLLB_CTRL4 REGISTER

Address: 0x33, Reset: 0x00, Name: PLLB_CTRL4

Numerator (N) of the Fractional PLLB Lower Byte

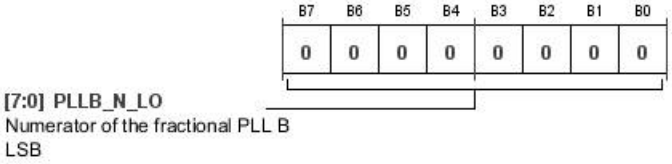


Table 85. Bit Descriptions for PLLB_CTRL4

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PLLB_N_LO		Numerator of the Fractional PLLB LSB. PLLB Fractional Mode Numerator N lower byte.	0x00	RW

PLLB_CTRL5 REGISTER

Address: 0x34, Reset: 0x00, Name: PLLB_CTRL5

PLLB Type, X and R Value Setting

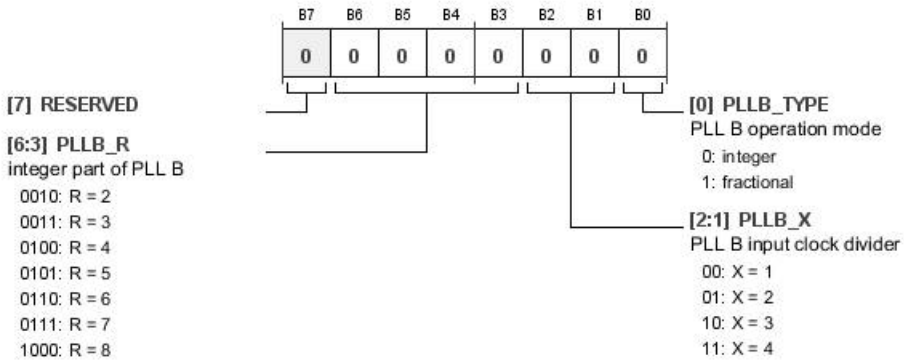


Table 86. Bit Descriptions for PLLB_CTRL5

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED			0x0	RW
[6:3]	PLLB_R		Integer Part of PLLB. Integer (R) of PLLB.	0x0	RW
		0010	R = 2		
		0011	R = 3		
		0100	R = 4		
		0101	R = 5		
		0110	R = 6		
		0111	R = 7		
		1000	R = 8		
[2:1]	PLLB_X		PLLB Input Clock Divider. PLLB input clock divider (X).	0x0	RW
		00	X = 1		
		01	X = 2		
		10	X = 3		
		11	X = 4		
0	PLLB_TYPE		PLLB Operation Mode. PLLB mode (fractional or integer).	0x0	RW
		0	Integer		
		1	Fractional		

PLLB_CTRL6 REGISTER

Address: 0x35, Reset: 0x02, Name: PLLB_CTRL6

PLLB Control/Status

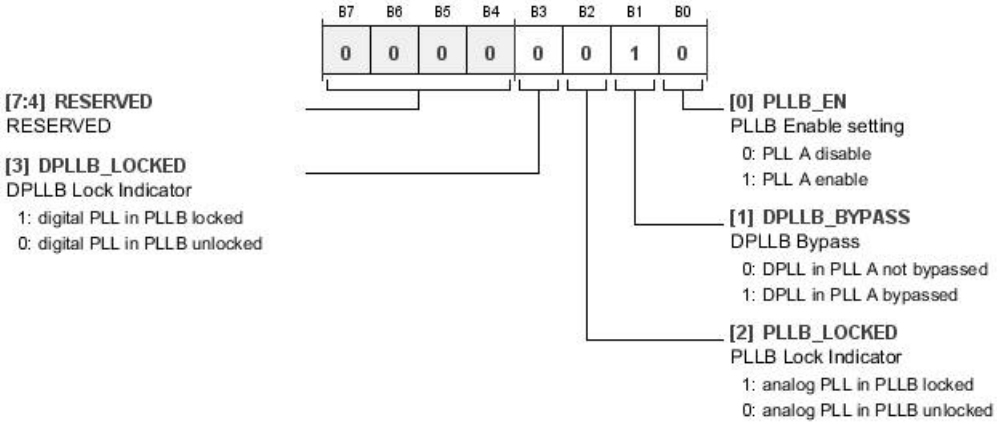


Table 87. Bit Descriptions for PLLB_CTRL6

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved.	0x0	RW
3	DPLLB_LOCKED		DPLLB Lock Indicator. DPLLB lock status indicator.	0x0	R
		1	Digital PLL in PLLB locked		
		0	Digital PLL in PLLB unlocked		
2	PLLB_LOCKED		PLLB Lock Indicator. PLLB lock status indicator.	0x0	R
		1	Analog PLL in PLLB locked		
		0	Analog PLL in PLLB unlocked		
1	DPLLB_BYPASS		DPLLB Bypass. DPLLB bypass select.	0x1	RW
		0	DPLL in PLLB not bypassed		
		1	DPLL in PLLB bypassed		
0	PLLB_EN		PLLB Enable Setting. PLLB enable/disable control.	0x0	RW
		0	PLLB disable		
		1	PLLB enable		

HEADDECT REGISTER

Address: 0x36, Reset: 0x00, Name: HEADDECT

Headphone Jack Detect Function Control.
Every write to these bits toggles the HP_CFG_RAW_STATE bit (Bit 2) in Register 0xE6.

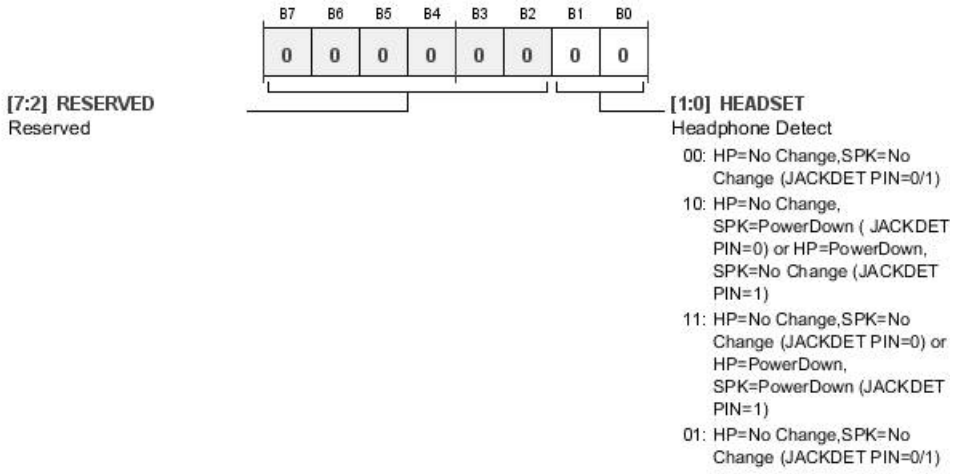


Table 88. Bit Descriptions for HEADDECT

Bits	Bit Name	Settings	Description	Reset	Access
[7:2]	RESERVED		Reserved.	0x0	RW
[1:0]	HEADSET		Headphone Detect. Headphone jack detect function control.	0x0	RW
		00	HP = no change, SPK = no change (JACKDET pin = 0/1)		
		10	HP = no change, SPK = power down (JACKDET pin = 0) or HP = power down, SPK = no change (JACKDET pin = 1)		
		11	HP = no change, SPK = no change (JACKDET pin = 0) or HP = power down, SPK = power down (JACKDET pin = 1)		
		01	HP = no change, SPK = no change (JACKDET pin = 0/1)		

ADC_DAC_STATUS REGISTER

Address: 0x37, Reset: 0x00, Name: ADC_DAC_STATUS

ADC/DAC Status

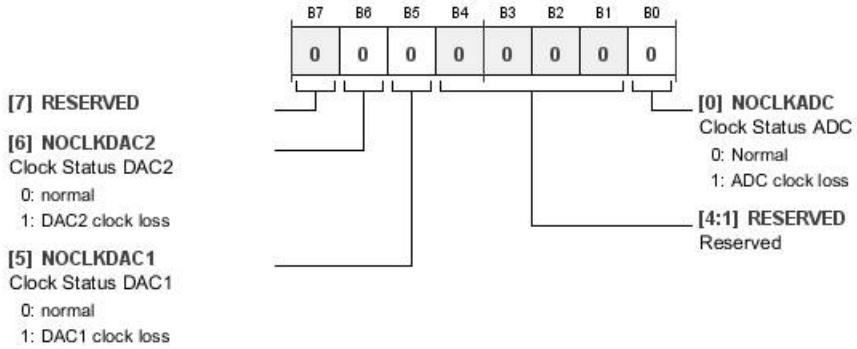


Table 89. Bit Descriptions for ADC_DAC_STATUS

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R
6	NOCLKDAC2		Clock Status DAC2.	0x0	R
		0	Normal		
		1	DAC2 clock loss		
5	NOCLKDAC1		Clock Status DAC1.	0x0	R
		0	Normal		
		1	DAC1 clock loss		
[4:1]	RESERVED		Reserved.	0x0	R
0	NOCLKADC		Clock Status ADC.	0x0	R
		0	Normal		
		1	ADC clock loss		

MIC_JACK_STATUS REGISTER

Address: 0x38, Reset: 0x00, Name: MIC_JACK_STATUS

Microphone/Jack Status

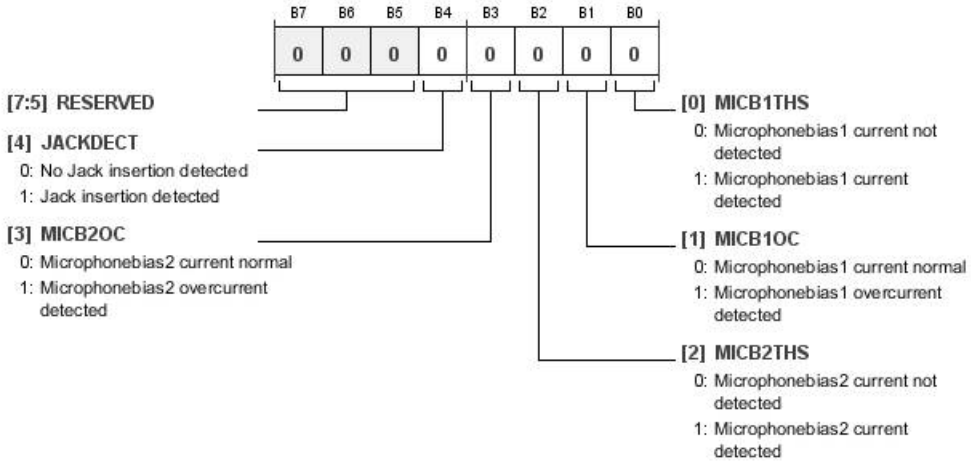


Table 90. Bit Descriptions for MIC_JACK_STATUS

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	R
4	JACKDECT			0x0	R
		0	No jack insertion detected		
		1	Jack insertion detected		
3	MICB2OC			0x0	R
		0	Microphone Bias 2 current normal		
		1	Microphone Bias 2 overcurrent detected		
2	MICB2THS			0x0	R
		0	Microphone Bias 2 current not detected		
		1	Microphone Bias 2 current detected		
1	MICB1OC			0x0	R
		0	Microphone Bias 1 current normal		
		1	Microphone Bias 1 overcurrent detected		
0	MICB1THS			0x0	R
		0	Microphone Bias 1 current not detected		
		1	Microphone Bias 1 current detected		

CHIP_FAULT_STATUS REGISTER

Address: 0x39, Reset: 0x00, Name: CHIP_FAULT_STATUS

Chip Status

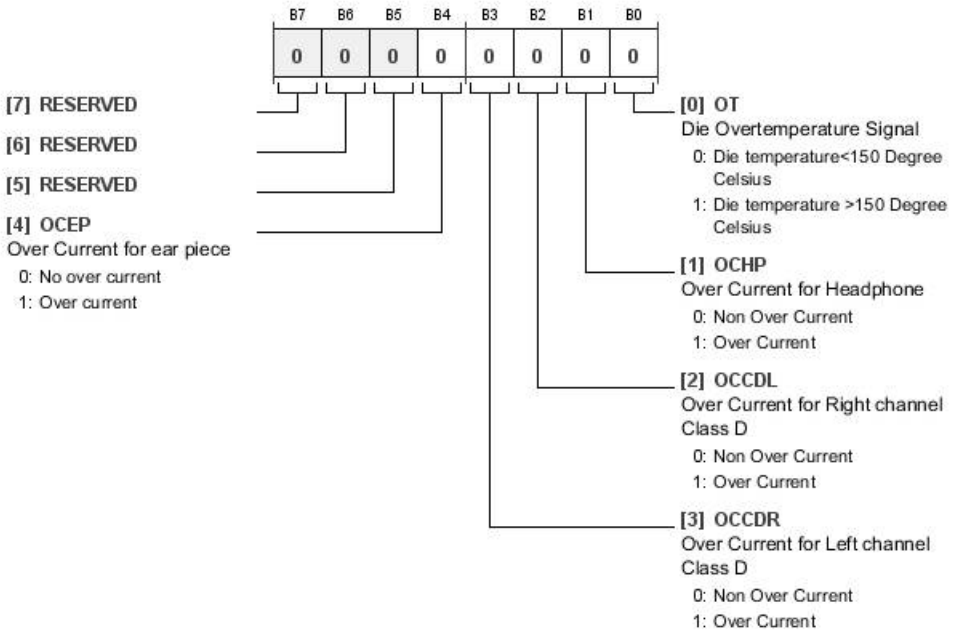


Table 91. Bit Descriptions for CHIP_FAULT_STATUS

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	R
4	OCEP		Overcurrent for Earpiece. Earpiece amplifier overcurrent indicator.	0x0	R
		0	No overcurrent		
		1	Overcurrent		
3	OCCDR		Overcurrent for Left Channel Class-D Speaker. Speaker amplifier left channel overcurrent indicator.	0x0	R
		0	No overcurrent		
		1	Overcurrent		
2	OCCDL		Overcurrent for Right Channel Class-D Speaker. Speaker amplifier right channel overcurrent indicator.	0x0	R
		0	No overcurrent		
		1	Overcurrent		
1	OCHP		Overcurrent for Headphone. Headphone amplifier overcurrent indicator.	0x0	R
		0	No overcurrent		
		1	Overcurrent		
0	OT		Die Overtemperature Signal. Junction overtemperature indicator.	0x0	R
		0	Die temperature < 150°C		
		1	Die temperature > 150°C		

ADC_SETTING REGISTER

Address: 0x3C, Reset: 0x00, Name: ADC_SETTING

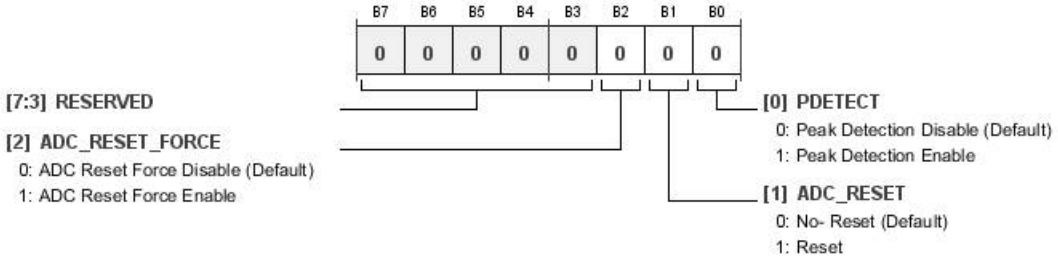


Table 92. Bit Descriptions for ADC_SETTING

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	RESERVED			0x00	RW
2	ADC_RESET_FORCE			0x0	RW
		0	ADC reset force disable (default)		
		1	ADC reset force enable		
1	ADC_RESET			0x0	RW
		0	No reset (default)		
		1	Reset		
0	PDETECT			0x0	RW
		0	Peak detection disable (default)		
		1	Peak detection enable		

CLK1_SOURCE_DIV REGISTER

Address: 0x40, Reset: 0x00, Name: CLK1_SOURCE_DIV

Clock 1 Divide and Core Clock Enable Control

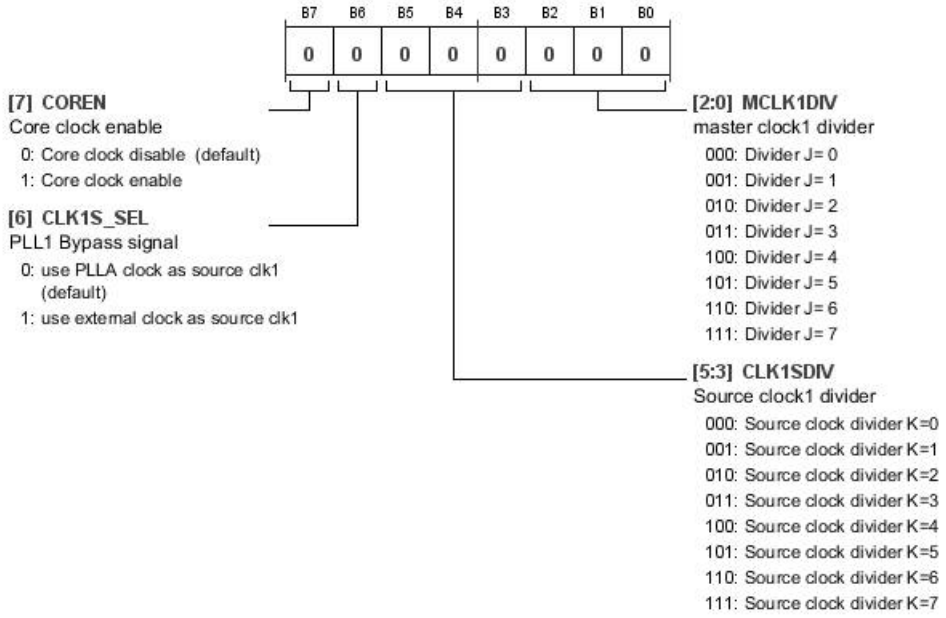


Table 93. Bit Descriptions for CLK1_SOURCE_DIV

Bits	Bit Name	Settings	Description	Reset	Access
7	COREN		Core Clock Enable. Core clock enable or disable control.	0x0	RW
		0	Core clock disable (default)		
		1	Core clock enable		
6	CLK1S_SEL		PLLA Bypass Signal. Clock source selection. Clock source can be set to either PLLA output or external input.	0x0	RW
		0	Use PLLA clock as Source Clock 1 (default)		
		1	Use external clock as Source Clock 1		
[5:3]	CLK1SDIV		Source Clock 1 Divider. Source Clock 1 divider settings, 0 through 7 in eight steps.	0x0	RW
		000	Source Clock Divider K = 0		
		001	Source Clock Divider K = 1		
		010	Source Clock Divider K = 2		
		011	Source Clock Divider K = 3		
		100	Source Clock Divider K = 4		
		101	Source Clock Divider K = 5		
		110	Source Clock Divider K = 6		
		111	Source Clock Divider K = 7		
[2:0]	MCLK1DIV		Master Clock 1 Divider. Master Clock 1 divider settings, 0 through 7 in eight steps.	0x0	RW
		000	Divider J = 0		
		001	Divider J = 1		
		010	Divider J = 2		
		011	Divider J = 3		
		100	Divider J = 4		
		101	Divider J = 5		
		110	Divider J = 6		
		111	Divider J = 7		

CLK1_OUTPUT_DIV REGISTER

Address: 0x41, Reset: 0x00, Name: CLK1_OUTPUT_DIV

Master Clock 1 Output Divider Control for PLLA

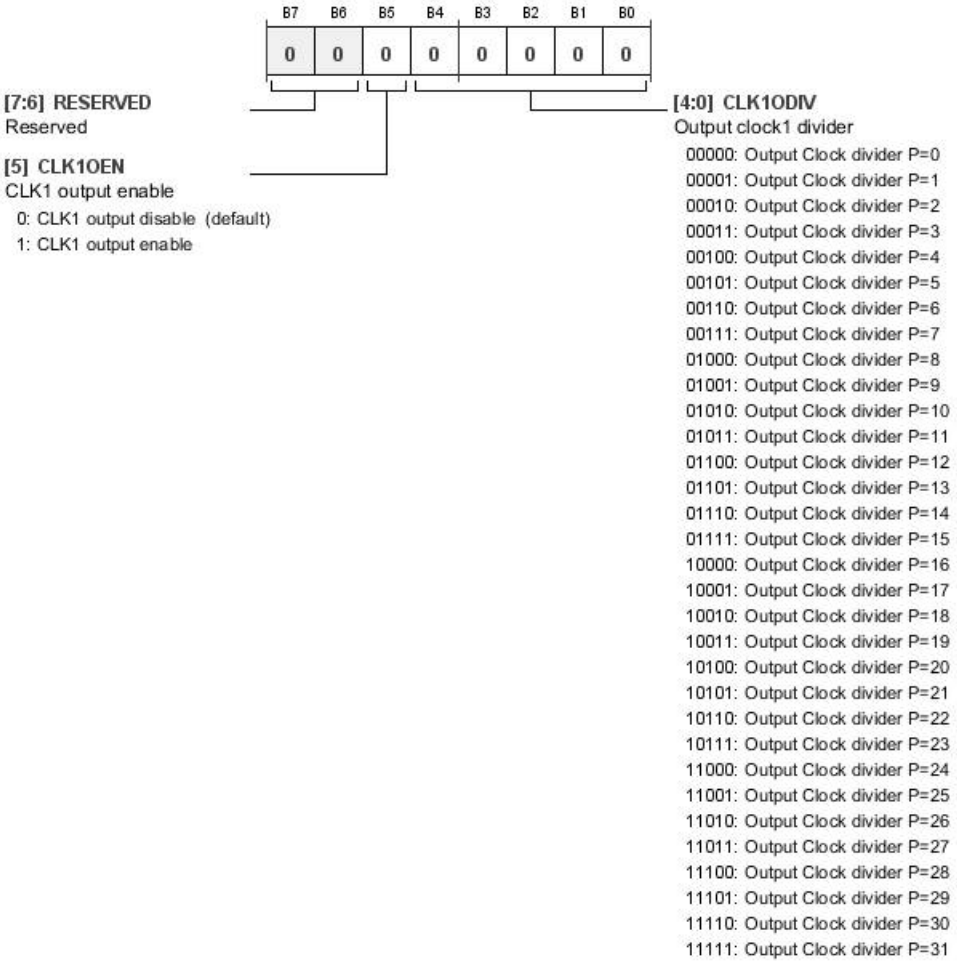


Table 94. Bit Descriptions for CLK1_OUTPUT_DIV

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	RW
5	CLK1OEN		CLK1 Output Enable. Output clock enable control.	0x0	RW
		0	CLK1 output disable (default)		
		1	CLK1 output enable		
[4:0]	CLK1ODIV		Output Clock 1 Divider. Output clock divider, settings 0 through 31.	0x00	RW
		00000	Output Clock Divider P = 0		
		00001	Output Clock Divider P = 1		
		00010	Output Clock Divider P = 2		
		00011	Output Clock Divider P = 3		
		00100	Output Clock Divider P = 4		
		00101	Output Clock Divider P = 5		
		00110	Output Clock Divider P = 6		
		00111	Output Clock Divider P = 7		
		01000	Output Clock Divider P = 8		
		01001	Output Clock Divider P = 9		
		01010	Output Clock Divider P = 10		

Bits	Bit Name	Settings	Description	Reset	Access
[4:0]	CLK1ODIV	01011	Output Clock Divider P = 11		
		01100	Output Clock Divider P = 12		
		01101	Output Clock Divider P = 13		
		01110	Output Clock Divider P = 14		
		01111	Output Clock Divider P = 15		
		10000	Output Clock Divider P = 16		
		10001	Output Clock Divider P = 17		
		10010	Output Clock Divider P = 18		
		10011	Output Clock Divider P = 19		
		10100	Output Clock Divider P = 20		
		10101	Output Clock Divider P = 21		
		10110	Output Clock Divider P = 22		
		10111	Output Clock Divider P = 23		
		11000	Output Clock Divider P = 24		
		11001	Output Clock Divider P = 25		
		11010	Output Clock Divider P = 26		
		11011	Output Clock Divider P = 27		
		11100	Output Clock Divider P = 28		
		11101	Output Clock Divider P = 29		
		11110	Output Clock Divider P = 30		
		11111	Output Clock Divider P = 31		

CLK2_SOURCE_DIV REGISTER

Address: 0x42, Reset: 0x00, Name: CLK2_SOURCE_DIV

Clock 2 Divide and Core Clock Enable Control

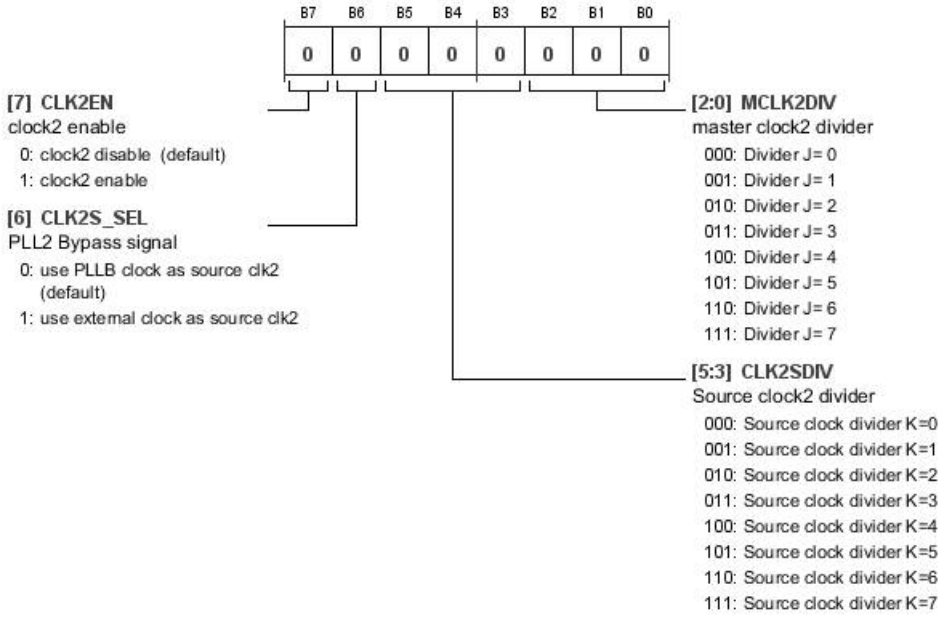


Table 95. Bit Descriptions for CLK2_SOURCE_DIV

Bits	Bit Name	Settings	Description	Reset	Access
7	CLK2EN		Clock 2 Enable. Core clock enable or disable control.	0x0	RW
		0	Clock 2 disable (default)		
		1	Clock 2 enable		
6	CLK2S_SEL		PLLB Bypass Signal. Clock source selection. Clock source can be set to either PLLB output or external input.	0x0	RW
		0	Use PLLB clock as Source Clock 2 (default)		
		1	Use external clock as Source Clock 2		
[5:3]	CLK2SDIV		Source Clock 2 Divider. Source Clock 2 divider settings, 0 through 7 in eight steps.	0x0	RW
		000	Source Clock Divider K = 0		
		001	Source Clock Divider K = 1		
		010	Source Clock Divider K = 2		
		011	Source Clock Divider K = 3		
		100	Source Clock Divider K = 4		
		101	Source Clock Divider K = 5		
		110	Source Clock Divider K = 6		
		111	Source Clock Divider K = 7		
[2:0]	MCLK2DIV		Master Clock 2 Divider. Master Clock 2 divider settings, 0 through 7 in eight steps.	0x0	RW
		000	Divider J = 0		
		001	Divider J = 1		
		010	Divider J = 2		
		011	Divider J = 3		
		100	Divider J = 4		
		101	Divider J = 5		
		110	Divider J = 6		
		111	Divider J = 7		

CLK2_OUTPUT_DIV REGISTER

Address: 0x43, Reset: 0x00, Name: CLK2_OUTPUT_DIV

Master Clock 2 Output Divider Control for PLLB

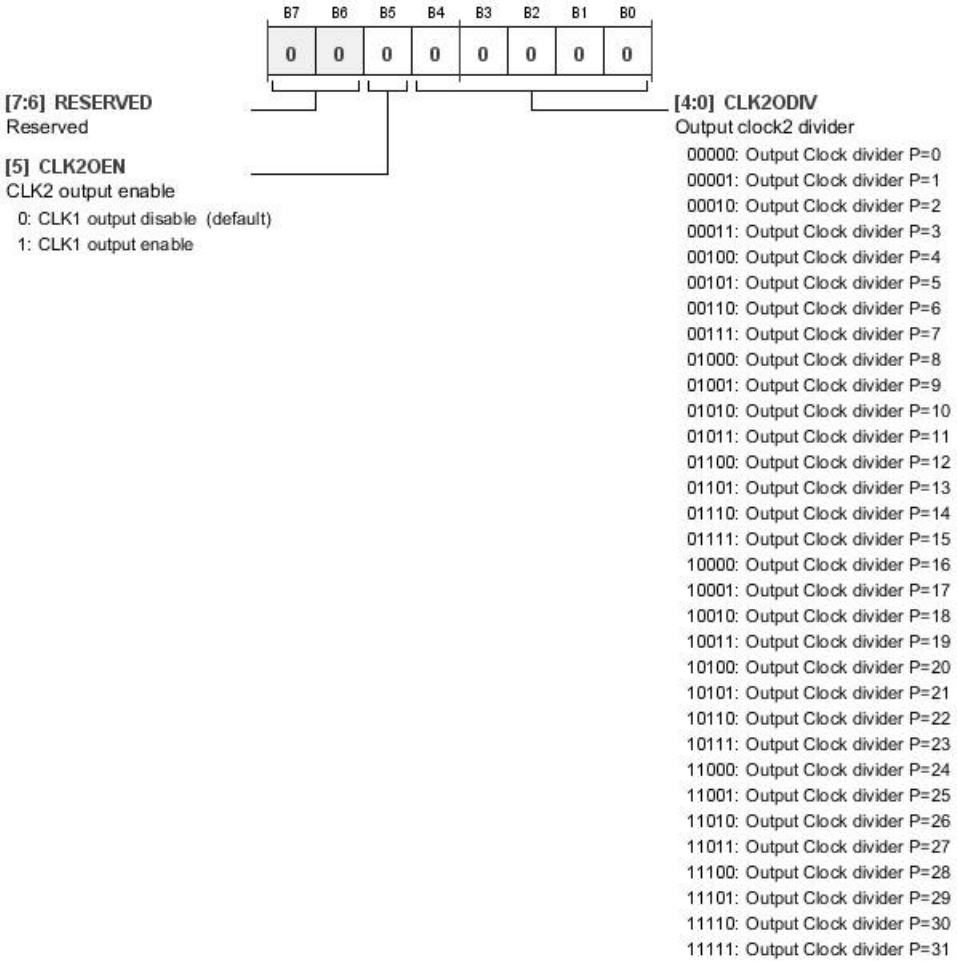


Table 96. Bit Descriptions for CLK2_OUTPUT_DIV

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	RW
5	CLK2OEN		CLK2 Output Enable. Output clock enable control.	0x0	RW
		0	CLK2 output disable (default)		
		1	CLK2 output enable		
[4:0]	CLK2ODIV		Output Clock 2 Divider. Output clock divider settings, 0 through 31.	0x00	RW
		00000	Output Clock Divider P = 0		
		00001	Output Clock Divider P = 1		
		00010	Output Clock Divider P = 2		
		00011	Output Clock Divider P = 3		
		00100	Output Clock Divider P = 4		
		00101	Output Clock Divider P = 5		
		00110	Output Clock Divider P = 6		
		00111	Output Clock Divider P = 7		
		01000	Output Clock Divider P = 8		
		01001	Output Clock Divider P = 9		
		01010	Output Clock Divider P = 10		

Bits	Bit Name	Settings	Description	Reset	Access
		01011	Output Clock Divider P = 11		
		01100	Output Clock Divider P = 12		
		01101	Output Clock Divider P = 13		
		01110	Output Clock Divider P = 14		
		01111	Output Clock Divider P = 15		
		10000	Output Clock Divider P = 16		
		10001	Output Clock Divider P = 17		
		10010	Output Clock Divider P = 18		
		10011	Output Clock Divider P = 19		
		10100	Output Clock Divider P = 20		
		10101	Output Clock Divider P = 21		
		10110	Output Clock Divider P = 22		
		10111	Output Clock Divider P = 23		
		11000	Output Clock Divider P = 24		
		11001	Output Clock Divider P = 25		
		11010	Output Clock Divider P = 26		
		11011	Output Clock Divider P = 27		
		11100	Output Clock Divider P = 28		
		11101	Output Clock Divider P = 29		
		11110	Output Clock Divider P = 30		
		11111	Output Clock Divider P = 31		

DAIA REGISTER

Address: 0x44, Reset: 0x0A, Name: DAIA

Digital Audio Interface A Settings 1

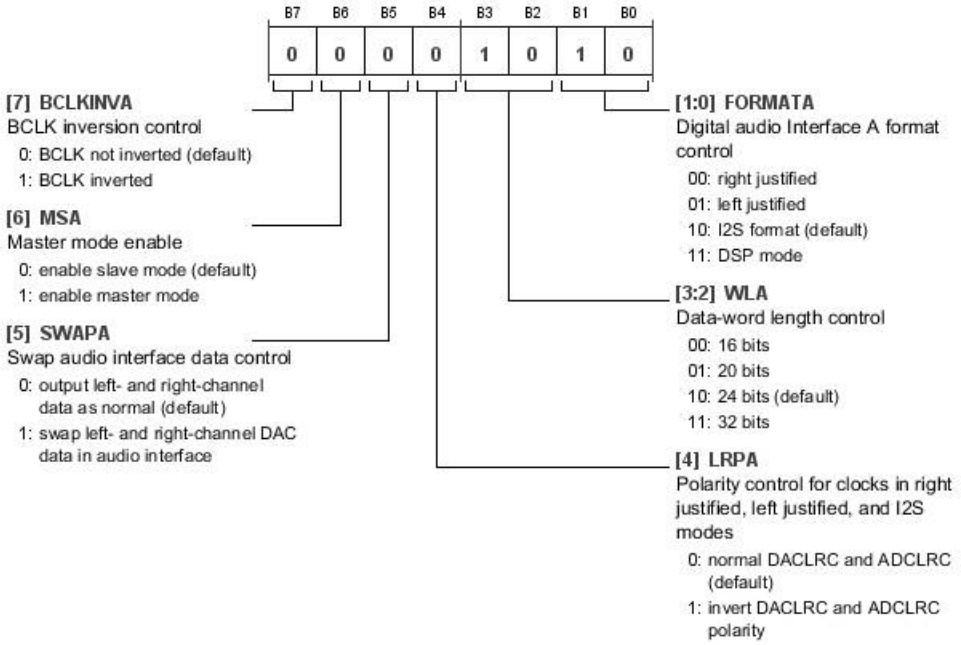


Table 97. Bit Descriptions for DAIA

Bits	Bit Name	Settings	Description	Reset	Access
7	BCLKINVA		BCLK Inversion Control. Bit clock polarity inversion setting.	0x0	RW
		0	BCLK not inverted (default)		
		1	BCLK inverted		
6	MSA		Master Mode Enable. Digital Audio Interface A master/slave setting.	0x0	RW
		0	Enable slave mode (default)		
		1	Enable master mode		
5	SWAPA		Swap Audio Interface Data Control. Left/right channel data swap setting.	0x0	RW
		0	Output left- and right-channel data as normal (default)		
		1	Swap left- and right-channel DAC data in audio interface		
4	LRPA		Polarity Control for Clocks in Right-Justified, Left-Justified, and I²S Modes. Polarity invert setting for frame clock.	0x0	RW
		0	Normal DACLRC and ADCLRC (default)		
		1	Invert DACLRC and ADCLRC polarity		
[3:2]	WLA		Data-Word Length Control. Digital Audio Interface A data-word length setting: 16/20/24/32 bits.	0x2	RW
		00	16 bits		
		01	20 bits		
		10	24 bits (default)		
		11	32 bits		
[1:0]	FORMATA		Digital Audio Interface A Format Control. Digital Audio Interface A serial format setting RJ/LJ/I2S/DSP mode.	0x2	RW
		00	Right justified		
		01	Left justified		
		10	I²S format (default)		
		11	DSP mode		

DAIB REGISTER

Address: 0x45, Reset: 0x0A, Name: DAIB

Digital Audio Interface B Settings 1

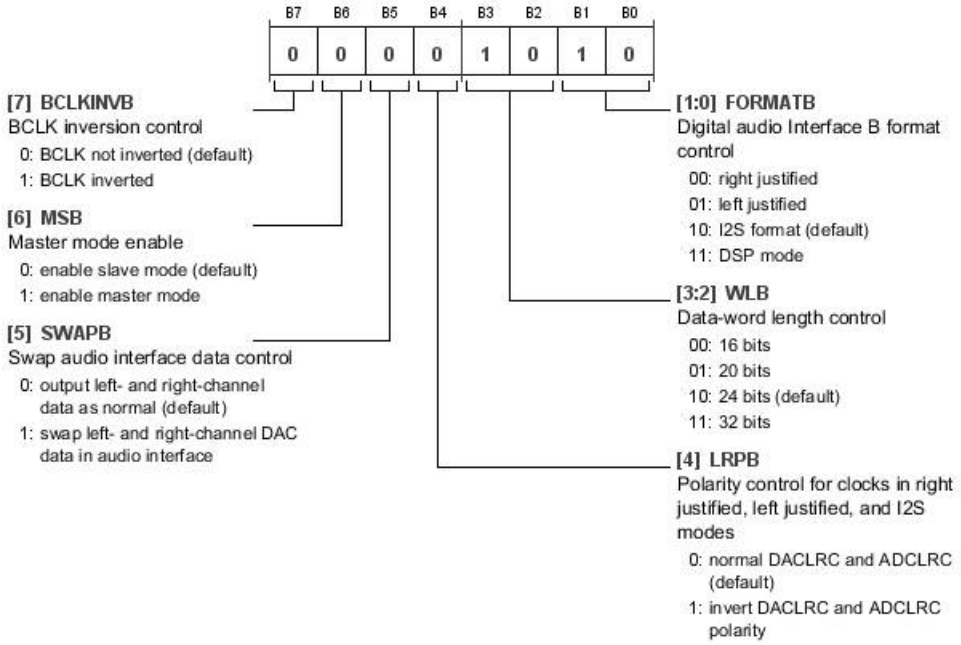


Table 98. Bit Descriptions for DAIB

Bits	Bit Name	Settings	Description	Reset	Access
7	BCLKINVB		BCLK Inversion Control. Bit clock polarity inversion setting.	0x0	RW
		0	BCLK not inverted (default)		
		1	BCLK inverted		
6	MSB		Master Mode Enable. Digital Audio Interface B master/slave setting.	0x0	RW
		0	Enable slave mode (default)		
		1	Enable master mode		
5	SWAPB		Swap Audio Interface Data Control. Left/right channel data swap setting.	0x0	RW
		0	Output left- and right-channel data as normal (default)		
		1	Swap left- and right-channel DAC data in audio interface		
4	LRPB		Polarity Control for Clocks in Right-Justified, Left-Justified, and I²S Modes. Polarity invert setting for frame clock.	0x0	RW
		0	Normal DACLRC and ADCLRC (default)		
		1	Invert DACLRC and ADCLRC polarity		
[3:2]	WLB		Data-Word Length Control. Digital Audio Interface B data-word length setting: 16/20/24/32 bits.	0x2	RW
		00	16 bits		
		01	20 bits		
		10	24 bits (default)		
		11	32 bits		
[1:0]	FORMATB		Digital Audio Interface B Format Control. Digital Audio Interface B serial format setting RJ/LJ/I²S/DSP mode.	0x2	RW
		00	Right justified		
		01	Left justified		
		10	I²S format (default)		
		11	DSP mode		

DAIC REGISTER

Address: 0x46, Reset: 0x0A, Name: DAIC

Digital Audio Interface C Settings 1

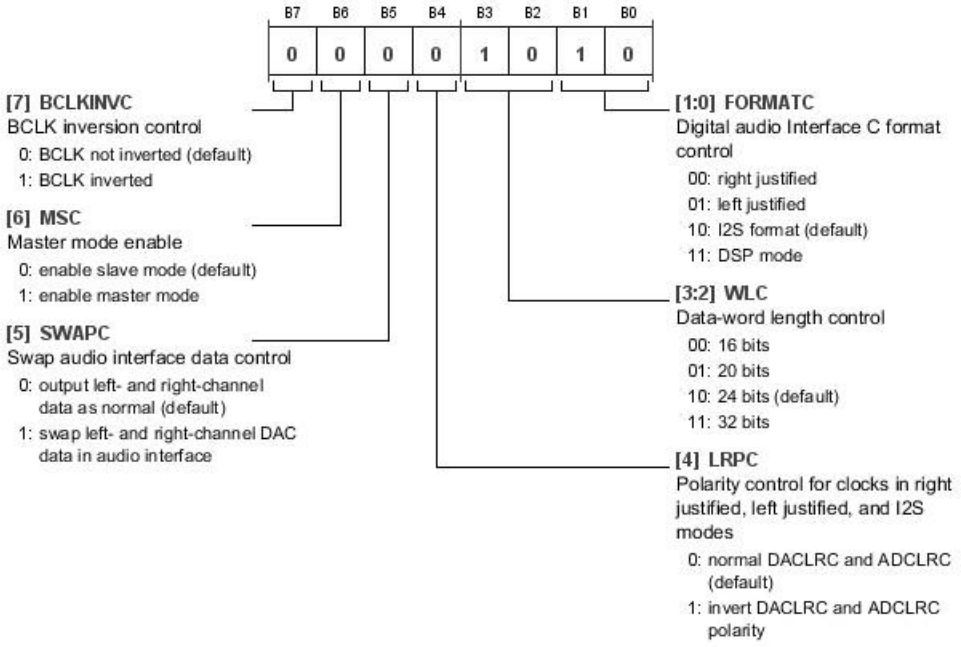


Table 99. Bit Descriptions for DAIC

Bits	Bit Name	Settings	Description	Reset	Access
7	BCLKINVC		BCLK Inversion Control. Bit clock polarity inversion setting.	0x0	RW
		0	BCLK not inverted (default)		
		1	BCLK inverted		
6	MSC		Master Mode Enable. Digital Audio Interface C master/slave setting.	0x0	RW
		0	Enable slave mode (default)		
		1	Enable master mode		
5	SWAPC		Swap Audio Interface Data Control. Left/right channel data swap setting.	0x0	RW
		0	Output left- and right-channel data as normal (default)		
		1	Swap left- and right-channel DAC data in audio interface		
4	LRPC		Polarity Control for Clocks in Right-Justified, Left-Justified, and I²S Modes. Polarity invert setting for frame clock.	0x0	RW
		0	Normal DACLRC and ADCLRC (default)		
		1	Invert DACLRC and ADCLRC polarity		
[3:2]	WLC		Data-Word Length Control. Digital Audio Interface C data-word length setting: 16/20/24/32 bits.	0x2	RW
		00	16 bits		
		01	20 bits		
		10	24 bits (default)		
		11	32 bits		
[1:0]	FORMATC		Digital Audio Interface C Format Control. Digital Audio Interface C serial format setting RJ/LJ/I²S/DSP mode.	0x2	RW
		00	Right justified		
		01	Left justified		
		10	I²S format (default)		
		11	DSP mode		

BCLKDIVA REGISTER

Address: 0x47, Reset: 0x00, Name: BCLKDIVA

Digital Audio Interface A Settings 2

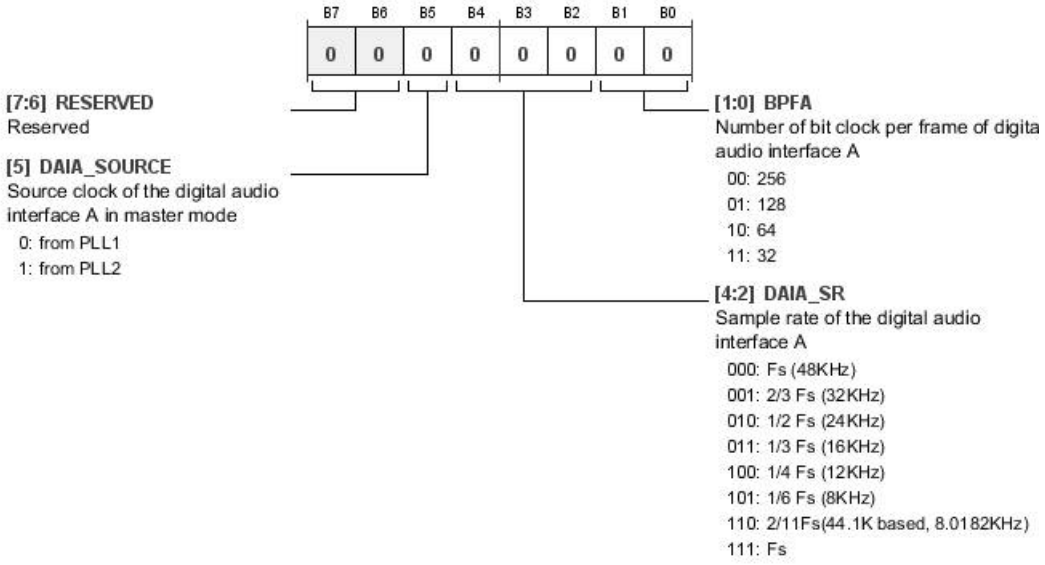


Table 100. Bit Descriptions for BCLKDIVA

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	RW
5	DAIA_SOURCE		Source Clock of the Digital Audio Interface A in Master Mode. Master clock source for Interface A can be set to either PLLA or PLLB.	0x0	RW
		0	From PLLA		
		1	From PLLB		
[4:2]	DAIA_SR		Sample Rate of Digital Audio Interface A. Sample rate for Interface A can be set to 32 kHz/24 kHz/16 kHz/12 kHz/8 kHz/8.0182 kHz.	0x0	RW
		000	f_S (48 kHz)		
		001	2/3 f_S (32 kHz)		
		010	1/2 f_S (24 kHz)		
		011	1/3 f_S (16 kHz)		
		100	1/4 f_S (12 kHz)		
		101	1/6 f_S (8 kHz)		
		110	2/11 f_S (44.1K based, 8.0182 kHz)		
		111	f_S		
[1:0]	BPFA		Number of Bit Clocks per Frame of Digital Audio Interface A. Number of bit clocks per frame can be set to 32/64/128/256.	0x0	RW
		00	256		
		01	128		
		10	64		
		11	32		

BCLKDIVB REGISTER

Address: 0x48, Reset: 0x00, Name: BCLKDIVB

Digital Audio Interface B Settings 2

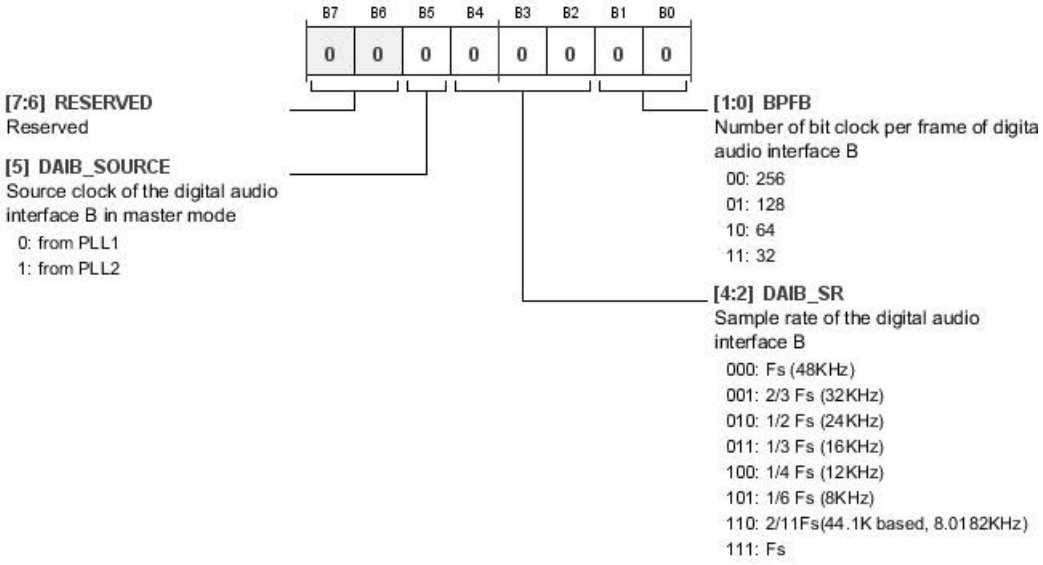


Table 101. Bit Descriptions for BCLKDIVB

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	RW
5	DAIB_SOURCE		Source Clock of the Digital Audio Interface B in Master Mode. Master clock source for Interface B can be set to either PLLA or PLLB.	0x0	RW
		0	From PLLA		
		1	From PLLB		
[4:2]	DAIB_SR		Sample Rate of Digital Audio Interface B. Sample rate for Interface B can be set to 32 kHz/24 kHz/16 kHz/12 kHz/8 kHz/8.0182 kHz.	0x0	RW
		000	f_S (48 kHz)		
		001	2/3 f_S (32 kHz)		
		010	1/2 f_S (24 kHz)		
		011	1/3 f_S (16 kHz)		
		100	1/4 f_S (12 kHz)		
		101	1/6 f_S (8 kHz)		
		110	2/11 f_S (44.1K based, 8.0182 kHz)		
		111	f_S		
[1:0]	BPFB		Number of Bit Clocks per Frame of Digital Audio Interface B. Number of bit clocks per frame can be set to 32/64/128/256.	0x0	RW
		00	256		
		01	128		
		10	64		
		11	32		

BCLKDIVC REGISTER

Address: 0x49, Reset: 0x00, Name: BCLKDIVC

Digital Audio Interface C Settings 2

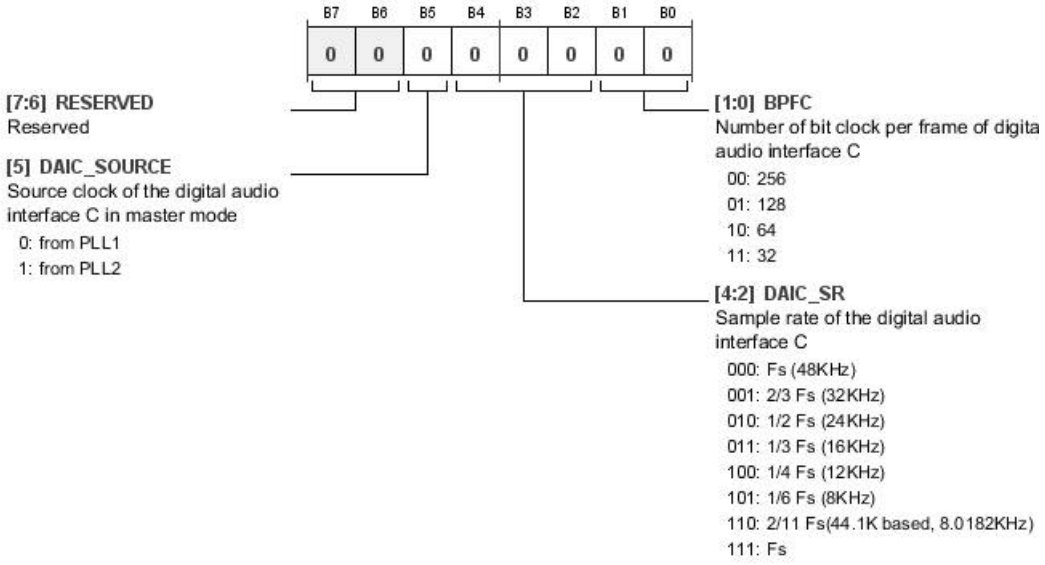


Table 102. Bit Descriptions for BCLKDIVC

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	RW
5	DAIC_SOURCE		Source Clock of Digital Audio Interface C in Master Mode. Master clock source for Interface C can be set to either PLLA or PLLB.	0x0	RW
		0	From PLLA		
		1	From PLLB		
[4:2]	DAIC_SR		Sample Rate of Digital Audio Interface C. Sample rate for Interface C can be set to 32 kHz/24 kHz/16 kHz/12 kHz/8 kHz/8.0182 kHz.	0x0	RW
		000	f_S (48 kHz)		
		001	2/3 f_S (32 kHz)		
		010	1/2 f_S (24 kHz)		
		011	1/3 f_S (16 kHz)		
		100	1/4 f_S (12 kHz)		
		101	1/6 f_S (8 kHz)		
		110	2/11 f_S (44.1K based, 8.0182 kHz)		
		111	f_S		
[1:0]	BPFC		Number of Bit Clocks per Frame of Digital Audio Interface C. Number of bit clocks per frame can be set to 32/64/128/256.	0x0	RW
		00	256		
		01	128		
		10	64		
		11	32		

SRCA_RATIOA REGISTER

Address: 0x4A, Reset: 0x00, Name: SRCA_RATIOA

Sample Rate Converter A Setting

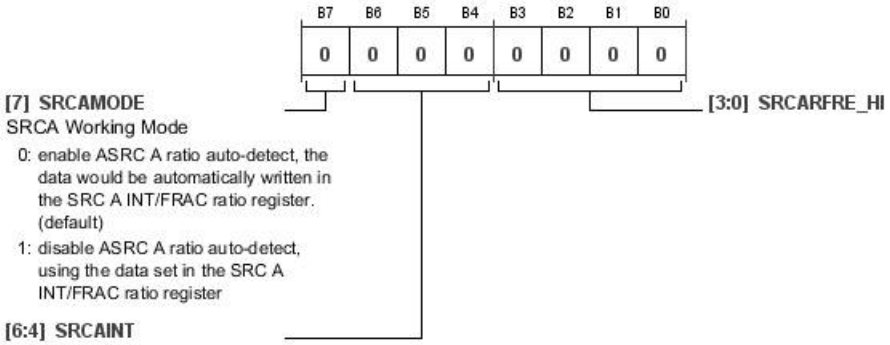


Table 103. Bit Descriptions for SRCA_RATIOA

Bits	Bit Name	Settings	Description	Reset	Access
7	SRCAMODE		SRCA Working Mode. SRCA ratio can be set to autodetect or manual mode. In manual mode the SRC ratio must be set using SRCAINT, SRCARFRE_HI, and SRCARFRE_LOW bits. The format is 3.12.	0x0	RW
		0	Enable ASRCA ratio autodetect; the data is automatically written in the SRCA INT/FRAC ratio register (default)		
		1	Disable ASRCA ratio autodetect, using the data set in the SRCA INT/FRAC ratio register		
[6:4]	SRCAINT		Integer Part of the SRCA Ratio Setting.	0x0	RW
[3:0]	SRCARFRE_HI		Upper Four Bits for the SRCA Ratio Setting.	0x0	RW

SRCA_RATIOB REGISTER

Address: 0x4B, Reset: 0x00, Name: SRCA_RATIOB

Sample Rate Converter A Setting

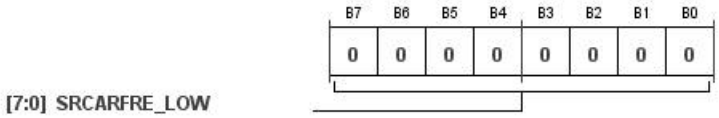


Table 104. Bit Descriptions for SRCA_RATIOB

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SRCARFRE_LOW		Lower Byte for the SRCA Ratio Setting.	0x00	RW

SRCB_RATIOA REGISTER

Address: 0x4C, Reset: 0x00, Name: SRCB_RATIOA

Sample Rate Converter B Setting

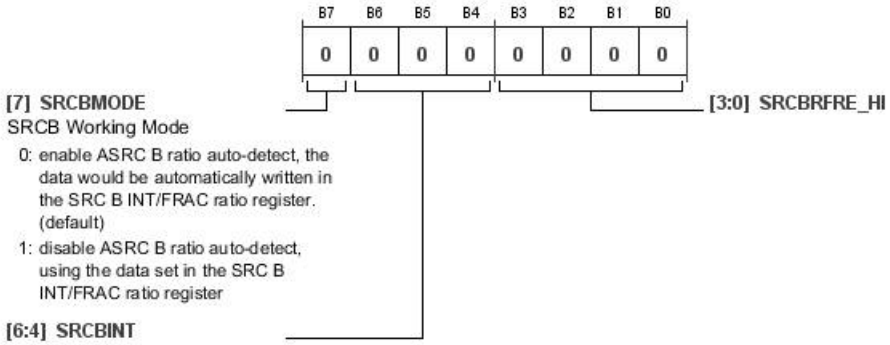


Table 105. Bit Descriptions for SRCB_RATIOA

Bits	Bit Name	Settings	Description	Reset	Access
7	SRCBMODE		SRCB Working Mode. SRCB ratio can be set to autodetect or manual mode. In manual mode the SRC ratio needs to be set using SRCBINT, SRCBRFRE_HI, and SRCBRFRE_LOW bits. The format is 3.12.	0x0	RW
		0	Enable ASRCB ratio autodetect; the data is automatically written in the SRCB INT/FRAC ratio register (default)		
		1	Disable ASRCB ratio autodetect, using the data set in the SRCB INT/FRAC ratio register		
[6:4]	SRCBINT		Integer Part of the SRCB Ratio Setting.	0x0	RW
[3:0]	SRCBRFRE_HI		Upper Four Bits for the SRCB Ratio Setting.	0x0	RW

SRCB_RATIOB REGISTER

Address: 0x4D, Reset: 0x00, Name: SRCB_RATIOB

Sample Rate Converter B Setting

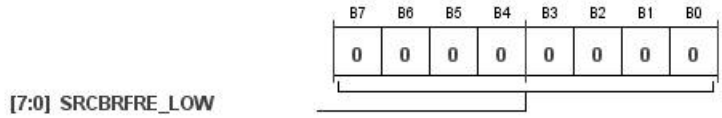


Table 106. Bit Descriptions for SRCB_RATIOB

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SRCBRFRE_LOW		Lower Byte for the SRCB Ratio Setting.	0x00	RW

SRCC_RATIOA REGISTER

Address: 0x4E, Reset: 0x00, Name: SRCC_RATIOA

Sample Rate Converter C Setting

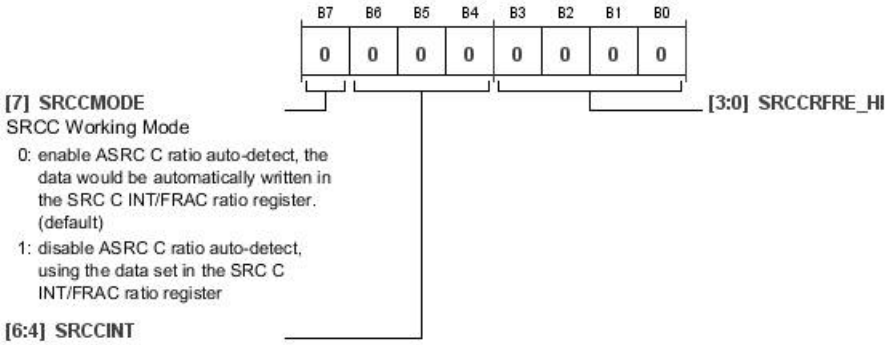


Table 107. Bit Descriptions for SRCC_RATIOA

Bits	Bit Name	Settings	Description	Reset	Access
7	SRCCMODE		SRCC Working Mode. SRCC ratio can be set to autodetect or manual mode. In manual mode, the SRCC ratio needs to be set using SRCCINT, SRCCRFRE_HI, and SRCCRFRE_LOW bits. The format is 3.12.	0x0	RW
		0	Enable ASRCC ratio autodetect; the data is automatically written in the SRCC INT/FRAC ratio register (default)		
		1	Disable ASRCC ratio autodetect, using the data set in the SRCC INT/FRAC ratio register		
[6:4]	SRCCINT		Integer Part of the SRCC Ratio Setting.	0x0	RW
[3:0]	SRCCRFRE_HI		Upper Four Bits for the SRCC Ratio Setting.	0x0	RW

SRCC_RATIOB REGISTER

Address: 0x4F, Reset: 0x00, Name: SRCC_RATIOB

Sample Rate Converter C Setting

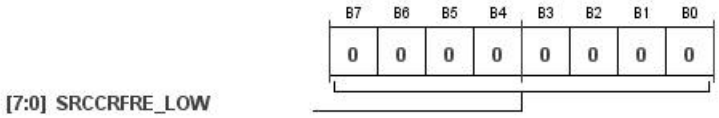


Table 108. Bit Descriptions for SRCC_RATIOB

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SRCCRFRE_LOW		Lower Byte for the SRCC Ratio Setting.	0x00	RW

DEEMP_CTRL REGISTER

Address: 0x50, Reset: 0x00, Name: DEEMP_CTRL

De-Emphasis Enable/Disable Control for Digital Audio Interface A/B/C

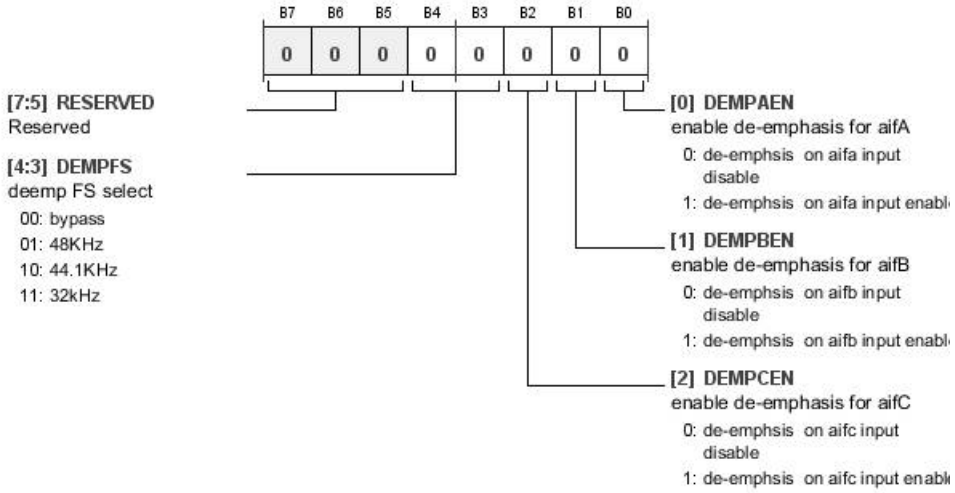


Table 109. Bit Descriptions for DEEMP_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
[4:3]	DEMPFS		De-Emphasis FS Select.	0x0	RW
		00	Bypass		
		01	48 kHz		
		10	44.1 kHz		
		11	32 kHz		
2	DEMPCEN		Enable De-Emphasis for AIFC. Digital Audio Interface C de-emphasis enable/disable.	0x0	RW
		0	De-emphasis on AIFC input disable		
		1	De-emphasis on AIFC input enable		
1	DEMPBEN		Enable De-Emphasis for AIFB. Digital Audio Interface B de-emphasis enable/disable.	0x0	RW
		0	De-emphasis on AIFB input disable		
		1	De-emphasis on AIFB input enable		
0	DEMPAEN		Enable De-Emphasis for AIFA. Digital Audio Interface A de-emphasis enable/disable.	0x0	RW
		0	De-emphasis on AIFA input disable		
		1	De-emphasis on AIFA input enable		

SRC_DAI_A_CTRL REGISTER

Address: 0x51, Reset: 0x08, Name: SRC_DAI_A_CTRL

SRCA and Digital Audio Interface A Control

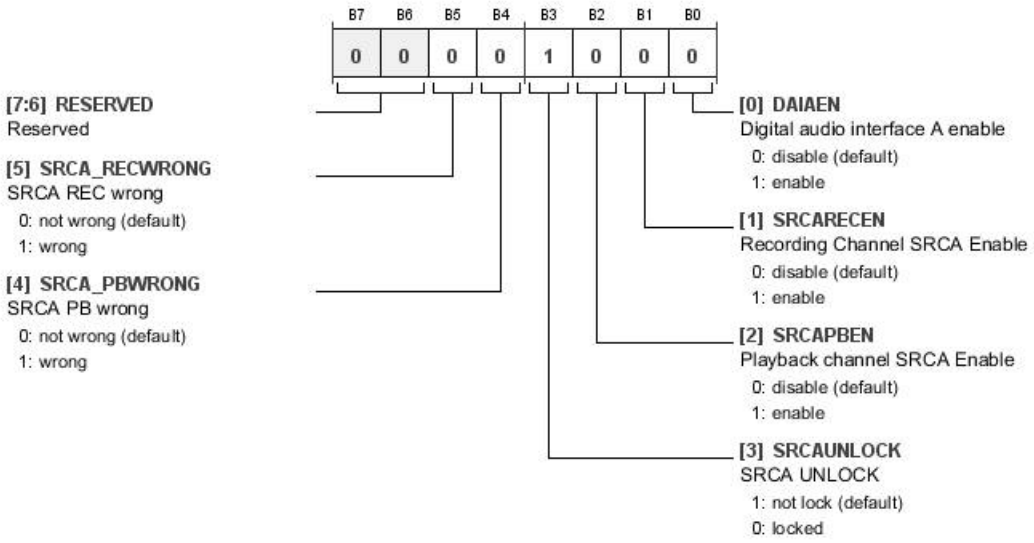


Table 110. Bit Descriptions for SRC_DAI_A_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	RW
5	SRCA_RECWRONG		SRCA Record Wrong. SRCA record status bit.	0x0	R
		0	Not wrong (default)		
		1	Wrong		
4	SRCA_PBWRONG		SRCA Playback Wrong. SRCA playback status bit.	0x0	R
		0	Not wrong (default)		
		1	Wrong		
3	SRCAUNLOCK		SRCA Unlock. SRCA lock status bit.	0x1	R
		1	Not locked (default)		
		0	Locked		
2	SRCAPBEN		Playback Channel SRCA Enable. Playback path SRCA enable/disable control.	0x0	RW
		0	Disable (default)		
		1	Enable		
1	SRCARECEN		Recording channel SRCA Enable. Record path SRCA enable/disable control.	0x0	RW
		0	Disable (default)		
		1	Enable		
0	DAIAEN		Digital Audio Interface A Enable. Digital Audio Interface A enable/disable control.	0x0	RW
		0	Disable (default)		
		1	Enable		

SRC_DAI_B_CTRL REGISTER

Address: 0x52, Reset: 0x08, Name: SRC_DAI_B_CTRL

SRCB and Digital Audio Interface B Control

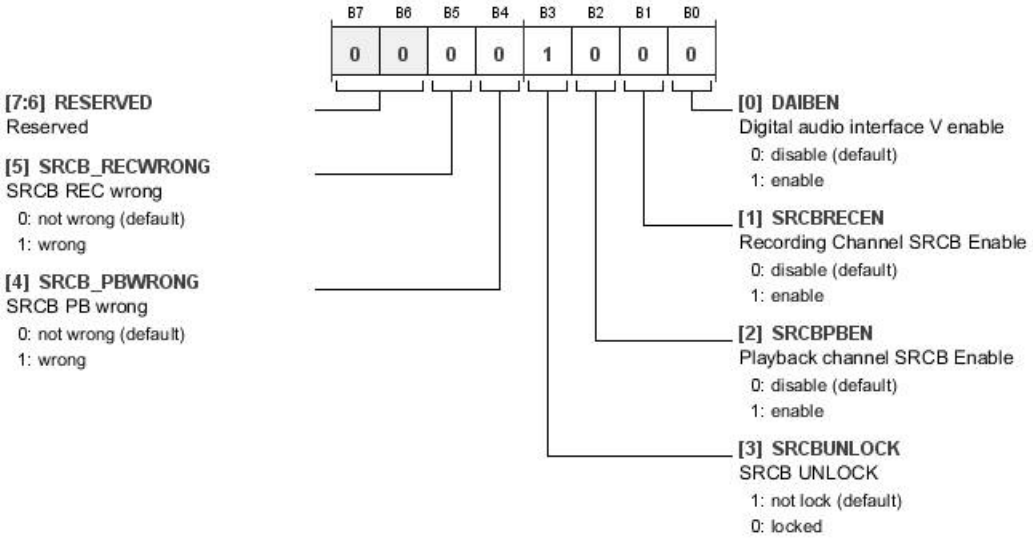


Table 111. Bit Descriptions for SRC_DAI_B_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	RW
5	SRCB_RECWRONG		SRCB Record Wrong. SRCB record status bit.	0x0	R
		0	Not wrong (default)		
		1	Wrong		
4	SRCB_PBWRONG		SRCB Playback Wrong. SRCB playback status bit.	0x0	R
		0	Not wrong (default)		
		1	Wrong		
3	SRCBUNLOCK		SRCB Unlock. SRCB lock status bit.	0x1	R
		1	Not lock (default)		
		0	Locked		
2	SRCBPBEN		Playback Channel SRCB Enable. Playback path SRCB enable/disable control.	0x0	RW
		0	Disable (default)		
		1	Enable		
1	SRCBRECEN		Recording Channel SRCB Enable. Record path SRCB enable/disable control.	0x0	RW
		0	Disable (default)		
		1	Enable		
0	DAIBEN		Digital Audio Interface B Enable. Digital Audio Interface B enable/disable control.	0x0	RW
		0	Disable (default)		
		1	Enable		

SRC_DAI_C_CTRL REGISTER

Address: 0x53, Reset: 0x08, Name: SRC_DAI_C_CTRL

SRCC and Digital Audio Interface C Control

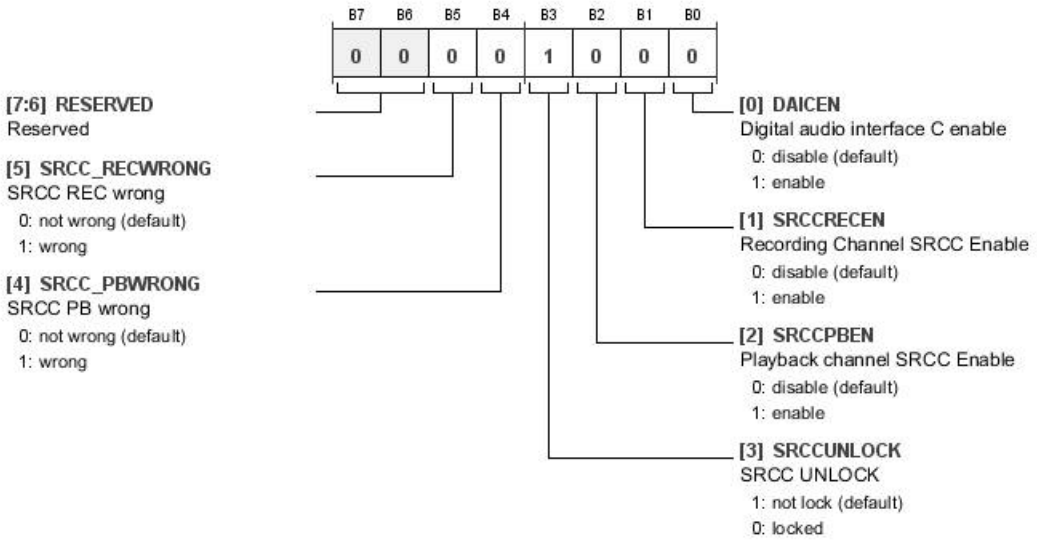


Table 112. Bit Descriptions for SRC_DAI_C_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	RW
5	SRCC_RECWRONG		SRCC Record Wrong. SRCC record status bit.	0x0	R
		0	Not wrong (default)		
		1	Wrong		
4	SRCC_PBWRONG		SRCC Playback Wrong. SRCC playback status bit.	0x0	R
		0	Not wrong (default)		
		1	Wrong		
3	SRCCUNLOCK		SRCC Unlock. SRCC lock status bit.	0x1	R
		1	Not lock (default)		
		0	Locked		
2	SRCCPBEN		Playback Channel SRCC Enable. Playback path SRCC enable/disable control.	0x0	RW
		0	Disable (default)		
		1	Enable		
1	SRCCRECEN		Recording Channel SRCC Enable. Record path SRCC enable/disable control.	0x0	RW
		0	Disable (default)		
		1	Enable		
0	DAICEN		Digital Audio Interface C Enable. Digital Audio Interface C enable/disable control.	0x0	RW
		0	Disable (default)		
		1	Enable		

DIN_MIX_CTRL0 (TO FDSP CHANNEL 0 INPUT) REGISTER

Address: 0x56, Reset: 0x00, Name: DIN_MIX_CTRL0

DSP Input Mixer Control Channel 0

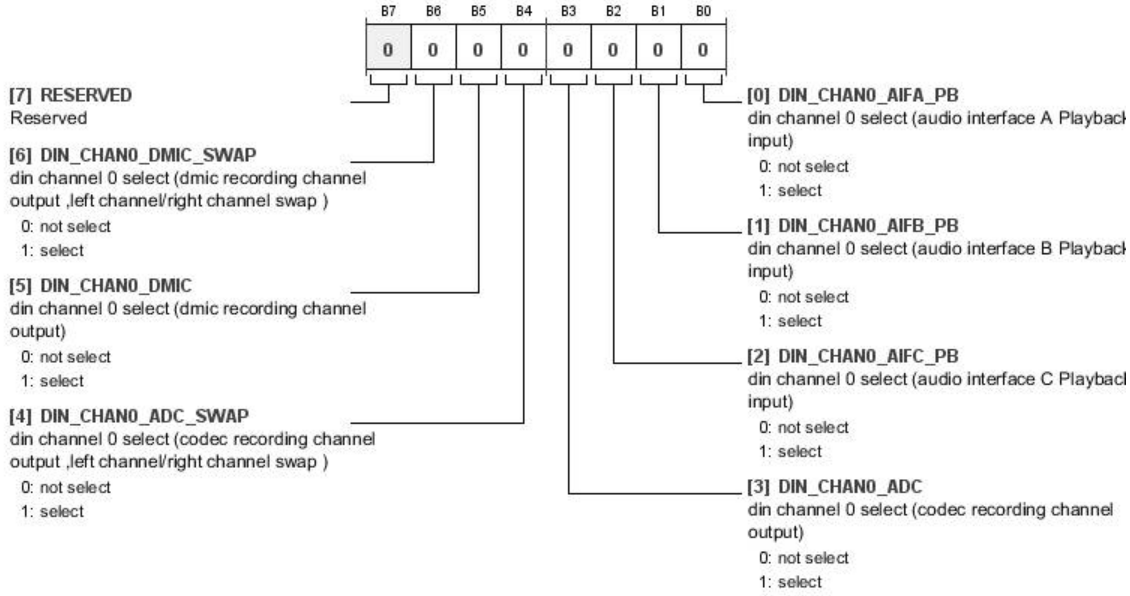


Table 113. Bit Descriptions for DIN_MIX_CTRL0

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
6	DIN_CHAN0_DMIC_SWAP		DIN Channel 0 Select (DMIC Recording Channel Output, Left Channel/Right Channel Swap). DSP data in Channel 0: DMIC (left/right swapped) select.	0x0	RW
		0	Not select		
		1	Select		
5	DIN_CHAN0_DMIC		DIN Channel 0 Select (DMIC Recording Channel Output). DSP data in Channel 0: DMIC select.	0x0	RW
		0	Not select		
		1	Select		
4	DIN_CHAN0_ADC_SWAP		DIN Channel 0 Select (Codec Recording Channel Output, Left Channel/ Right Channel Swap). DSP data in Channel 0: ADC select.	0x0	RW
		0	Not select		
		1	Select		
3	DIN_CHAN0_ADC		DIN Channel 0 Select (Codec Recording Channel Output). DSP data in Channel 0: ADC (left/right swapped) select.	0x0	RW
		0	Not select		
		1	Select		
2	DIN_CHAN0_AIFC_PB		DIN Channel 0 Select (Audio Interface C Playback Input). DSP data in Channel 0: Audio Interface C input select.	0x0	RW
		0	Not select		
		1	Select		
1	DIN_CHAN0_AIFB_PB		DIN Channel 0 Select (Audio Interface B Playback Input). DSP data in Channel 0: Audio Interface B input select.	0x0	RW
		0	Not select		
		1	Select		
0	DIN_CHAN0_AIFA_PB		DIN Channel 0 Select (Audio Interface A Playback Input). DSP data in Channel 0: Audio Interface A input select.	0x0	RW
		0	Not select		
		1	Select		

DIN_MIX_CTRL1 (TO FDSP CHANNEL 1 INPUT) REGISTER

Address: 0x57, Reset: 0x00, Name: DIN_MIX_CTRL1

DSP Input Mixer Control Channel 1

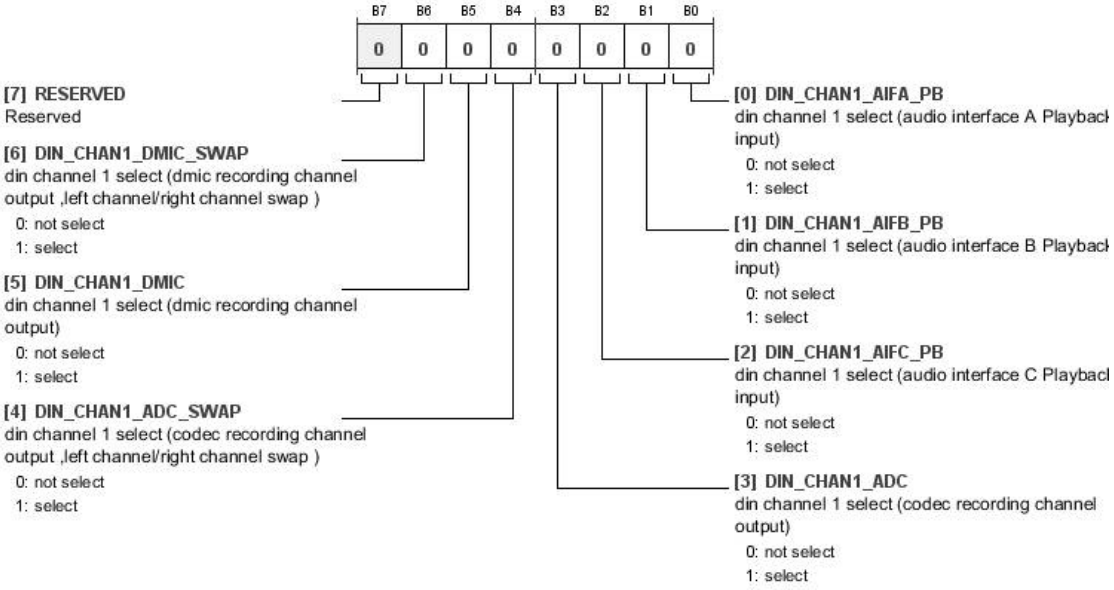


Table 114. Bit Descriptions for DIN_MIX_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
6	DIN_CHAN1_DMIC_SWAP		DIN Channel 1 Select (DMIC Recording Channel Output, Left Channel/Right Channel Swap). DSP data in Channel 1: DMIC (left/right swapped) select.	0x0	RW
		0	Not select		
		1	Select		
5	DIN_CHAN1_DMIC		DIN Channel 1 Select (DMIC Recording Channel Output). DSP data in Channel 1: DMIC select.	0x0	RW
		0	Not select		
		1	Select		
4	DIN_CHAN1_ADC_SWAP		DIN Channel 1 Select (Codec Recording Channel Output, Left Channel/ Right Channel Swap). DSP data in Channel 1: ADC select.	0x0	RW
		0	Not select		
		1	Select		
3	DIN_CHAN1_ADC		DIN Channel 1 Select (Codec Recording Channel Output). DSP data in Channel 1: ADC (left/right swapped) select.	0x0	RW
		0	Not select		
		1	Select		
2	DIN_CHAN1_AIFC_PB		DIN Channel 1 Select (Audio Interface C Playback Input). DSP data in Channel 1: Audio Interface C input select.	0x0	RW
		0	Not select		
		1	Select		
1	DIN_CHAN1_AIFB_PB		DIN Channel 1 Select (Audio Interface B Playback Input). DSP data in Channel 1: Audio Interface B input select.	0x0	RW
		0	Not select		
		1	Select		
0	DIN_CHAN1_AIFA_PB		DIN Channel 1 Select (Audio Interface A Playback Input). DSP data in Channel 1: Audio Interface A input select.	0x0	RW
		0	Not select		
		1	Select		

DIN_MIX_CTRL2 (TO FDSP CHANNEL 2 INPUT) REGISTER

Address: 0x58, Reset: 0x00, Name: DIN_MIX_CTRL2

DSP Input Mixer Control Channel 2

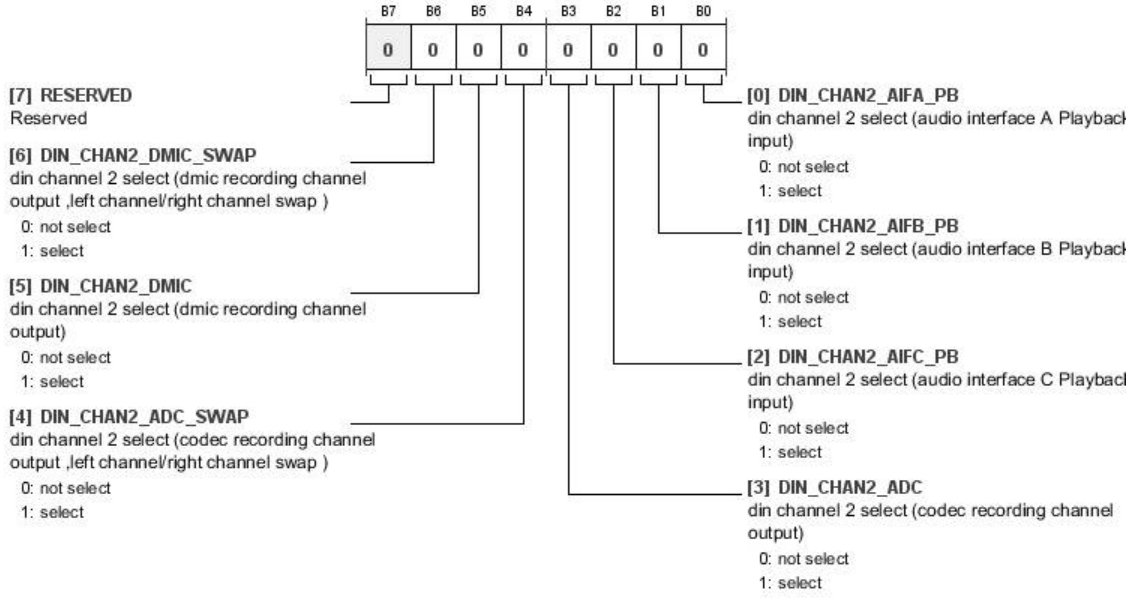


Table 115. Bit Descriptions for DIN_MIX_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
6	DIN_CHAN2_DMIC_SWAP		DIN Channel 2 Select (DMIC Recording Channel Output, Left Channel/Right Channel Swap). DSP data in Channel 2: DMIC (left/right swapped) select.	0x0	RW
		0	Not select		
		1	Select		
5	DIN_CHAN2_DMIC		DIN Channel 2 Select (DMIC Recording Channel Output). DSP data in Channel 2: DMIC select.	0x0	RW
		0	Not select		
		1	Select		
4	DIN_CHAN2_ADC_SWAP		DIN Channel 2 Select (Codec Recording Channel Output, Left Channel/ Right Channel Swap). DSP data in Channel 2: ADC select.	0x0	RW
		0	Not select		
		1	Select		
3	DIN_CHAN2_ADC		DIN Channel 2 Select (Codec Recording Channel Output). DSP data in Channel 2: ADC (left/right swapped) select.	0x0	RW
		0	Not select		
		1	Select		
2	DIN_CHAN2_AIFC_PB		DIN Channel 2 Select (Audio Interface C Playback Input). DSP data in Channel 2: Audio Interface C input select.	0x0	RW
		0	Not select		
		1	Select		
1	DIN_CHAN2_AIFB_PB		DIN Channel 2 Select (Audio Interface B Playback Input). DSP data in Channel 2: Audio Interface B input select.	0x0	RW
		0	Not select		
		1	Select		
0	DIN_CHAN2_AIFA_PB		DIN Channel 2 Select (Audio Interface A Playback Input). DSP data in Channel 2: Audio Interface A input select.	0x0	RW
		0	Not select		
		1	Select		

DIN_MIX_CTRL3 (TO FDSP CHANNEL 3 INPUT) REGISTER

Address: 0x59, Reset: 0x00, Name: DIN_MIX_CTRL3

DSP Input Mixer Control Channel 3

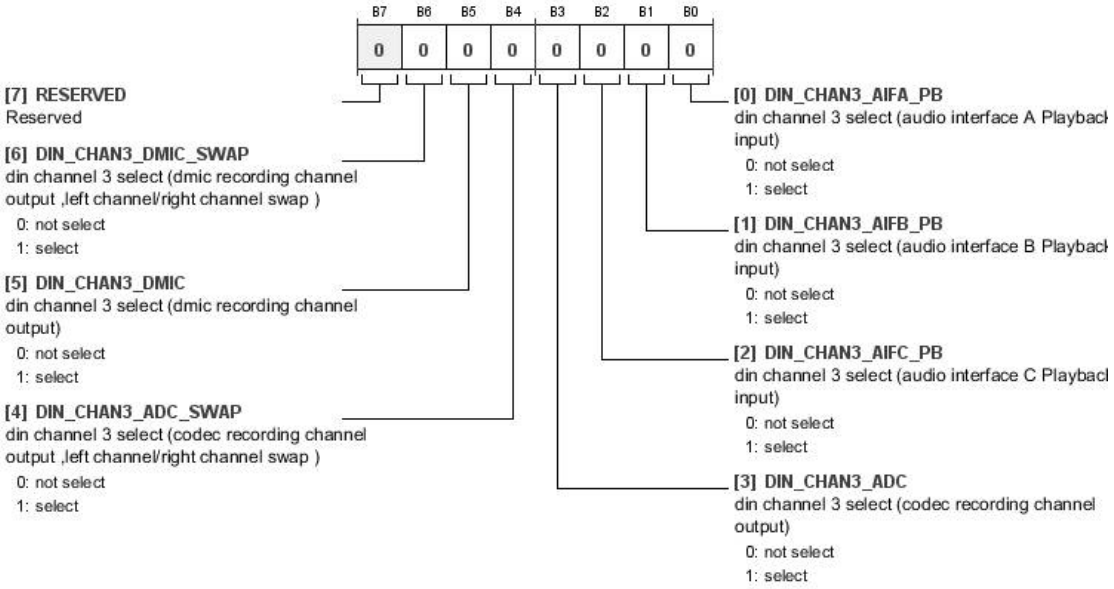


Table 116. Bit Descriptions for DIN_MIX_CTRL3

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
6	DIN_CHAN3_DMIC_SWAP		DIN Channel 3 Select (DMIC Recording Channel Output, Left Channel/Right Channel Swap). DSP data in Channel 3: DMIC (left/right swapped) select.	0x0	RW
		0	Not select		
		1	Select		
5	DIN_CHAN3_DMIC		DIN Channel 3 Select (DMIC Recording Channel Output). DSP data in Channel 3: DMIC Select.	0x0	RW
		0	Not select		
		1	Select		
4	DIN_CHAN3_ADC_SWAP		DIN Channel 3 Select (Codec Recording Channel Output, Left Channel/Right Channel Swap). DSP data in Channel 3: ADC select.	0x0	RW
		0	Not select		
		1	Select		
3	DIN_CHAN3_ADC		DIN Channel 3 Select (Codec Recording Channel Output). DSP data in Channel 3: ADC (left/right swapped) select.	0x0	RW
		0	Not select		
		1	Select		
2	DIN_CHAN3_AIFC_PB		DIN Channel 3 Select (Audio Interface C Playback Input). DSP data in Channel 3: Audio Interface C input select.	0x0	RW
		0	Not select		
		1	Select		
1	DIN_CHAN3_AIFB_PB		DIN Channel 3 Select (Audio Interface B Playback Input). DSP data in Channel 3: Audio Interface B input select.	0x0	RW
		0	Not select		
		1	Select		
0	DIN_CHAN3_AIFA_PB		DIN Channel 3 Select (Audio Interface A Playback Input). DSP data in Channel 3: Audio Interface A input select.	0x0	RW
		0	Not select		
		1	Select		

DIN_MIX_CTRL4 (TO FDSP CHANNEL 4 INPUT) REGISTER

Address: 0x5A, Reset: 0x00, Name: DIN_MIX_CTRL4

DSP Input Mixer Control Channel 4

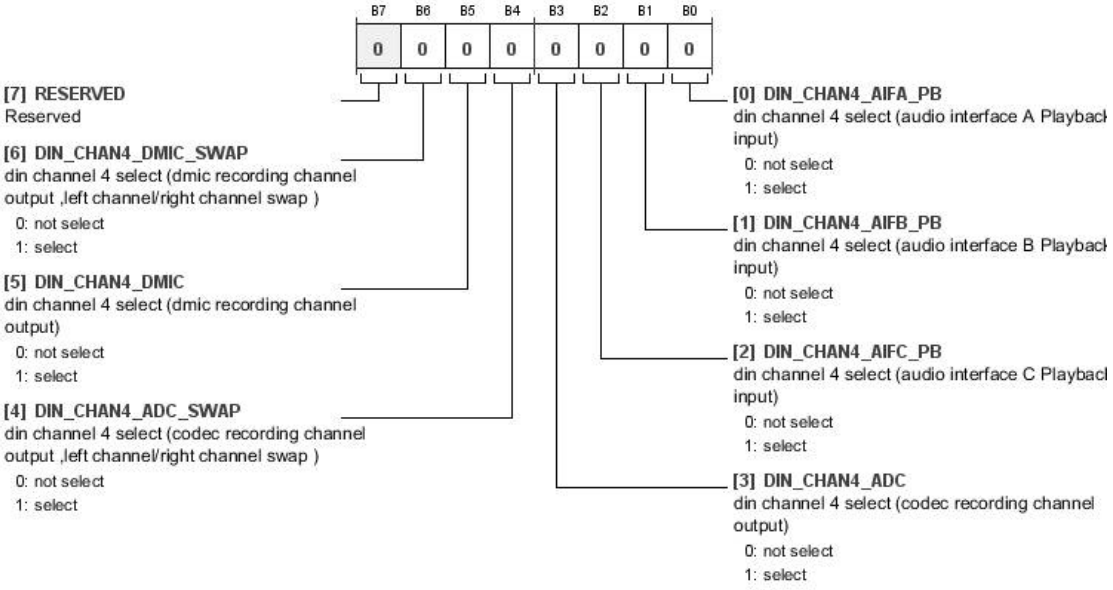


Table 117. Bit Descriptions for DIN_MIX_CTRL4

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
6	DIN_CHAN4_DMIC_SWAP		DIN Channel 4 Select (DMIC Recording Channel Output, Left Channel/Right Channel Swap). DSP data in Channel 4: DMIC (left/right swapped) select.	0x0	RW
		0	Not select		
		1	Select		
5	DIN_CHAN4_DMIC		DIN Channel 4 Select (DMIC Recording Channel Output). DSP data in Channel 4: DMIC select.	0x0	RW
		0	Not select		
		1	Select		
4	DIN_CHAN4_ADC_SWAP		DIN Channel 4 Select (Codec Recording Channel Output, Left Channel/Right Channel Swap). DSP data in Channel 4: ADC select.	0x0	RW
		0	Not select		
		1	Select		
3	DIN_CHAN4_ADC		DIN Channel 4 Select (Codec Recording Channel Output). DSP data in Channel 3: ADC (left/right swapped) select.	0x0	RW
		0	Not select		
		1	Select		
2	DIN_CHAN4_AIFC_PB		DIN Channel 4 Select (Audio Interface C Playback Input). DSP data in Channel 4: Audio Interface C input select.	0x0	RW
		0	Not select		
		1	Select		
1	DIN_CHAN4_AIFB_PB		DIN Channel 4 Select (Audio Interface B Playback Input). DSP data in Channel 4: Audio Interface B input select.	0x0	RW
		0	Not select		
		1	Select		
0	DIN_CHAN4_AIFA_PB		DIN Channel 4 Select (Audio Interface A Playback Input). DSP data in Channel 4: Audio Interface A input select.	0x0	RW
		0	Not select		
		1	Select		

DOUT_MIX_CTRL0 (TO DIGITAL AUDIO INTERFACE A RECORDING OUTPUT) REGISTER

Address: 0x5B, Reset: 0x00, Name: DOUT_MIX_CTRL0

DSP Output Mix Control Interface A

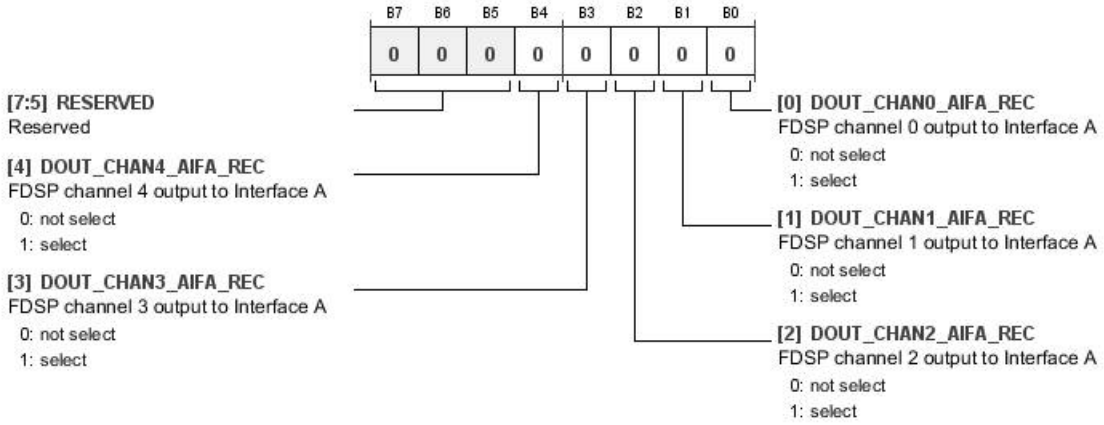


Table 118. Bit Descriptions for DOUT_MIX_CTRL0

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
4	DOUT_CHAN4_AIFA_REC		FDSP Channel 4 Output to Digital Audio Interface A. DSP output Channel 4 to Digital Audio Interface A enable/disable.	0x0	RW
		0	Not select		
		1	Select		
3	DOUT_CHAN3_AIFA_REC		FDSP Channel 3 Output to Digital Audio Interface A. DSP output Channel 3 to Digital Audio Interface A enable/disable.	0x0	RW
		0	Not select		
		1	Select		
2	DOUT_CHAN2_AIFA_REC		FDSP Channel 2 Output to Digital Audio Interface A. DSP output Channel 2 to Digital Audio Interface A enable/disable.	0x0	RW
		0	Not select		
		1	Select		
1	DOUT_CHAN1_AIFA_REC		FDSP Channel 1 Output to Digital Audio Interface A. DSP output Channel 1 to Digital Audio Interface A enable/disable.	0x0	RW
		0	Not select		
		1	Select		
0	DOUT_CHAN0_AIFA_REC		FDSP Channel 0 Output to Digital Audio Interface A. DSP output Channel 0 to Digital Audio Interface A enable/disable.	0x0	RW
		0	Not select		
		1	Select		

DOUT_MIX_CTRL1 (TO DIGITAL AUDIO INTERFACE B RECORDING OUTPUT) REGISTER

Address: 0x5C, Reset: 0x00, Name: DOUT_MIX_CTRL1

DSP Output Mix Control Interface B

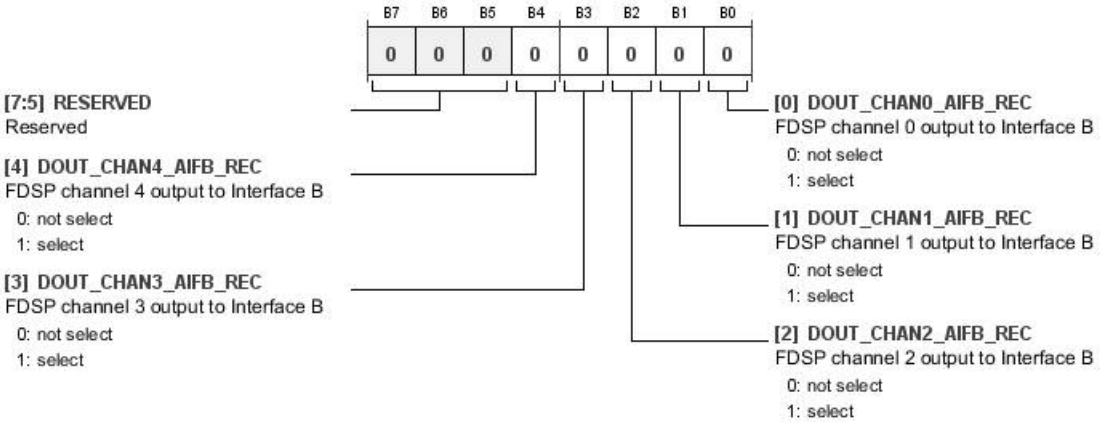


Table 119. Bit Descriptions for DOUT_MIX_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
4	DOUT_CHAN4_AIFB_REC		FDSP Channel 4 Output to Digital Audio Interface B. DSP output Channel 4 to Digital Audio Interface B enable/disable.	0x0	RW
		0	Not select		
		1	Select		
3	DOUT_CHAN3_AIFB_REC		FDSP Channel 3 Output to Digital Audio Interface B. DSP output Channel 3 to Digital Audio Interface B enable/disable.	0x0	RW
		0	Not select		
		1	Select		
2	DOUT_CHAN2_AIFB_REC		FDSP Channel 2 Output to Digital Audio Interface B. DSP output Channel 2 to Digital Audio Interface B enable/disable.	0x0	RW
		0	Not select		
		1	Select		
1	DOUT_CHAN1_AIFB_REC		FDSP Channel 1 Output to Digital Audio Interface B. DSP output Channel 1 to Digital Audio Interface B enable/disable.	0x0	RW
		0	Not select		
		1	Select		
0	DOUT_CHAN0_AIFB_REC		FDSP Channel 0 Output to Digital Audio Interface B. DSP output Channel 0 to Digital Audio Interface B enable/disable.	0x0	RW
		0	Not select		
		1	Select		

DOUT_MIX_CTRL2 (TO DIGITAL AUDIO INTERFACE C RECORDING OUTPUT) REGISTER

Address: 0x5D, Reset: 0x00, Name: DOUT_MIX_CTRL2

DSP Output Mix Control Interface C

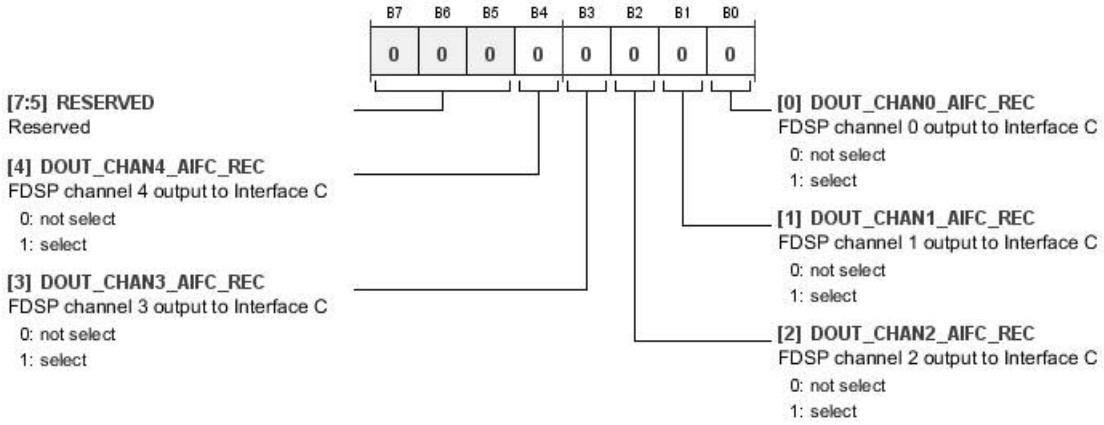


Table 120. Bit Descriptions for DOUT_MIX_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
4	DOUT_CHAN4_AIFC_REC		FDSP Channel 4 Output to Digital Audio Interface C. DSP output Channel 4 to Digital Audio Interface C enable/disable.	0x0	RW
		0	Not select		
		1	Select		
3	DOUT_CHAN3_AIFC_REC		FDSP Channel 3 Output to Digital Audio Interface C. DSP output Channel 3 to Digital Audio Interface C enable/disable.	0x0	RW
		0	Not select		
		1	Select		
2	DOUT_CHAN2_AIFC_REC		FDSP Channel 2 Output to Digital Audio Interface C. DSP output Channel 2 to Digital Audio Interface C enable/disable.	0x0	RW
		0	Not select		
		1	Select		
1	DOUT_CHAN1_AIFC_REC		FDSP Channel 1 Output to Digital Audio Interface C. DSP output Channel 1 to Digital Audio Interface C enable/disable.	0x0	RW
		0	Not select		
		1	Select		
0	DOUT_CHAN0_AIFC_REC		FDSP Channel 0 Output to Digital Audio Interface C. DSP output Channel 0 to Digital Audio Interface C enable/disable.	0x0	RW
		0	Not select		
		1	Select		

DOUT_MIX_CTRL3 (TO DAC1 PLAYBACK INPUT) REGISTER

Address: 0x5E, Reset: 0x00, Name: DOUT_MIX_CTRL3

DSP Output Mix Control DAC1

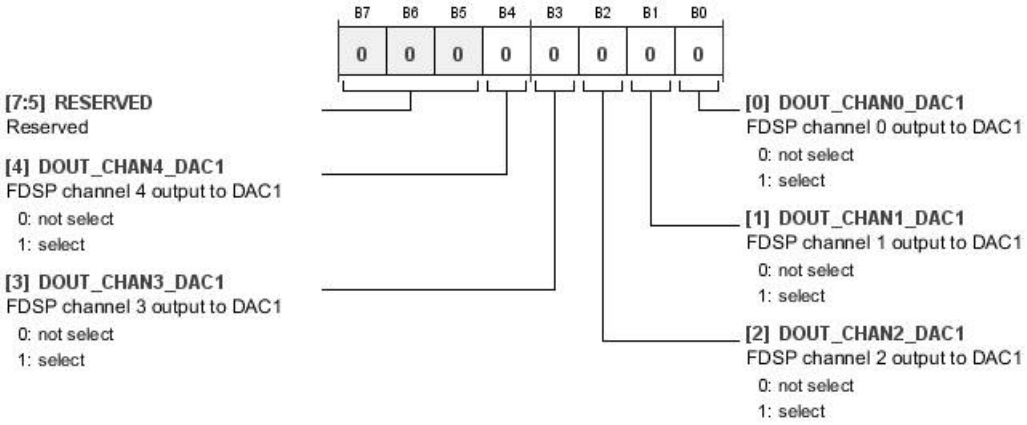


Table 121. Bit Descriptions for DOUT_MIX_CTRL3

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
4	DOUT_CHAN4_DAC1		FDSP Channel 4 Output to DAC1. DSP output Channel 4 to DAC1 enable/disable.	0x0	RW
		0	Not select		
		1	Select		
3	DOUT_CHAN3_DAC1		FDSP Channel 3 Output to DAC1. DSP output Channel 3 to DAC1 enable/disable.	0x0	RW
		0	Not select		
		1	Select		
2	DOUT_CHAN2_DAC1		FDSP Channel 2 Output to DAC1. DSP output Channel 2 to DAC1 enable/disable.	0x0	RW
		0	Not select		
		1	Select		
1	DOUT_CHAN1_DAC1		FDSP Channel 1 Output to DAC1. DSP output Channel 1 to DAC1 enable/disable.	0x0	RW
		0	Not select		
		1	Select		
0	DOUT_CHAN0_DAC1		FDSP Channel 0 Output to DAC1. DSP output Channel 0 to DAC1 enable/disable.	0x0	RW
		0	Not select		
		1	Select		

DOUT_MIX_CTRL4 (TO DAC2 PLAYBACK INPUT) REGISTER

Address: 0x5F, Reset: 0x00, Name: DOUT_MIX_CTRL4

DSP Output Mix Control DAC2

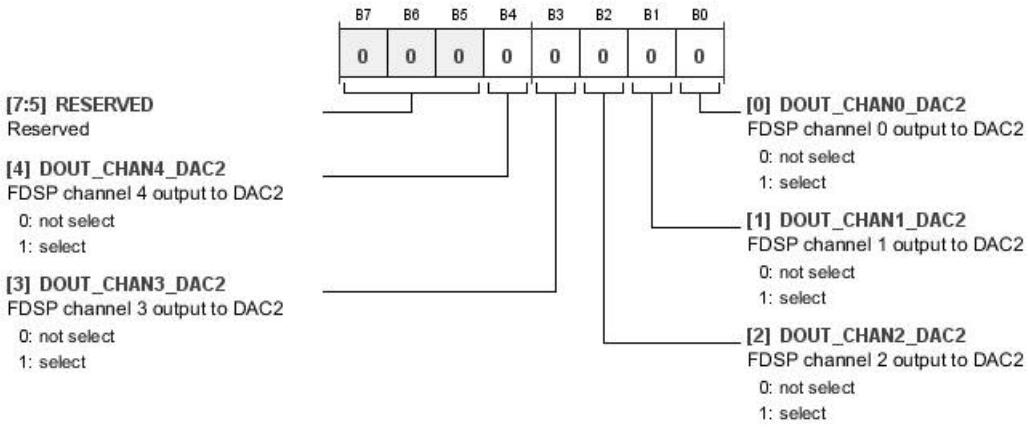


Table 122. Bit Descriptions for DOUT_MIX_CTRL4

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
4	DOUT_CHAN4_DAC2		FDSP Channel 4 Output to DAC2. DSP output Channel 4 to DAC2 enable/disable.	0x0	RW
		0	Not select		
		1	Select		
3	DOUT_CHAN3_DAC2		FDSP Channel 3 Output to DAC2. DSP output Channel 3 to DAC2 enable/disable.	0x0	RW
		0	Not select		
		1	Select		
2	DOUT_CHAN2_DAC2		FDSP Channel 2 Output to DAC2. DSP output Channel 2 to DAC2 enable/disable.	0x0	RW
		0	Not select		
		1	Select		
1	DOUT_CHAN1_DAC2		FDSP Channel 1 Output to DAC2. DSP output Channel 1 to DAC2 enable/disable.	0x0	RW
		0	Not select		
		1	Select		
0	DOUT_CHAN0_DAC2		FDSP Channel 0 Output to DAC2. DSP output Channel 0 to DAC2 enable/disable.	0x0	RW
		0	Not select		
		1	Select		

VOLMOD1 REGISTER

Address: 0x60, Reset: 0x00, Name: VOLMOD1

Digital Volume Change Selection Either Soft or Hard (Forced)

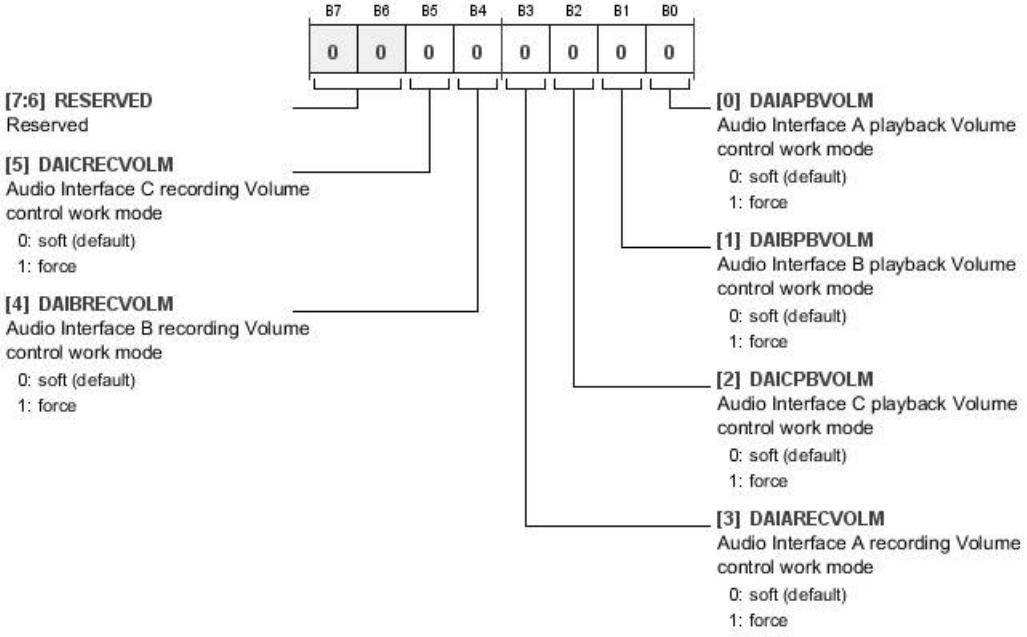


Table 123. Bit Descriptions for VOLMOD1

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	RW
5	DAICRECVOLM		Audio Interface C Recording Volume Control Work Mode. Audio Interface C recording volume control update mode.	0x0	RW
		0	Soft (default)		
		1	Force		
4	DAIBRECVOLM		Audio Interface B Recording Volume Control Work Mode. Audio Interface B recording volume control update mode.	0x0	RW
		0	Soft (default)		
		1	Force		
3	DAIARECVOLM		Audio Interface A Recording Volume Control Work Mode. Audio Interface A recording volume control update mode.	0x0	RW
		0	Soft (default)		
		1	Force		
2	DAICPBVOLM		Audio Interface C Playback Volume Control Work Mode. Audio Interface C playback volume control update mode.	0x0	RW
		0	Soft (default)		
		1	Force		
1	DAIBPBVOLM		Audio Interface B Playback Volume Control Work Mode. Audio Interface B playback volume control update mode.	0x0	RW
		0	Soft (default)		
		1	Force		
0	DAIAPBVOLM		Audio Interface A Playback Volume Control Work Mode. Audio Interface A playback volume control update mode.	0x0	RW
		0	Soft (default)		
		1	Force		

VOLMOD2 REGISTER

Address: 0x61, Reset: 0x00, Name: VOLMOD2

Digital Volume Change Selection, Either Soft or Hard (Forced)

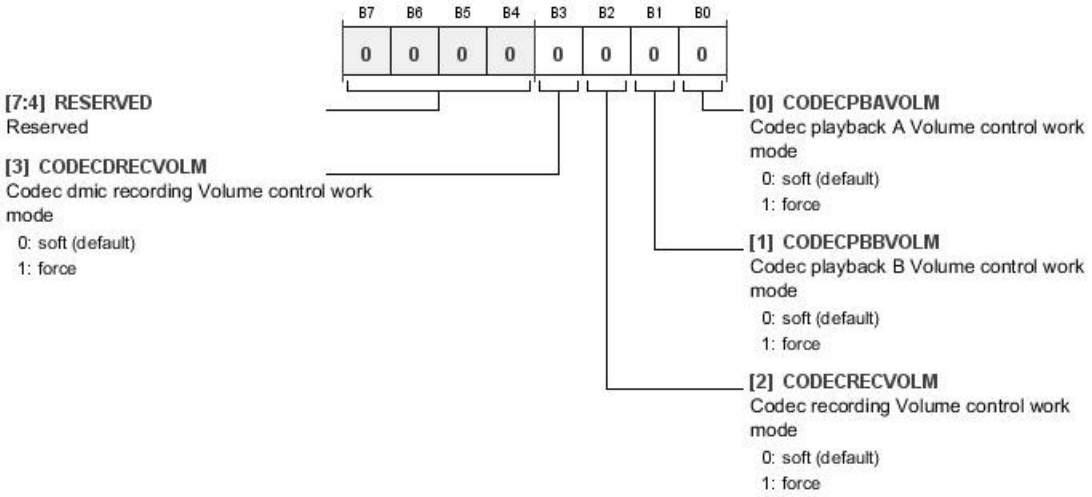


Table 124. Bit Descriptions for VOLMOD2

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved.	0x0	RW
3	CODECDRECVOLM		Codec DMIC Recording Volume Control Work Mode. Digital microphone playback volume control update mode.	0x0	RW
		0	Soft (default)		
		1	Force		
2	CODECRECVOLM		Codec Recording Volume Control Work Mode. ADC recording volume control update mode.	0x0	RW
		0	Soft (default)		
		1	Force		
1	CODECPBBVOLM		Codec Playback B Volume Control Work Mode. DAC2 playback volume control update mode.	0x0	RW
		0	Soft (default)		
		1	Force		
0	CODECPBAVOLM		Codec Playback A Volume Control Work Mode. DAC1 playback volume control update mode.	0x0	RW
		0	Soft (default)		
		1	Force		

DAIA_PBL_VOL REGISTER

Address: 0x62, Reset: 0x00, Name: DAIA_PBL_VOL

Digital Audio Interface A Left Channel Playback Volume Control

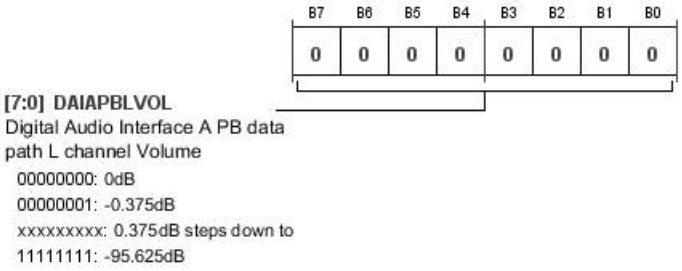


Table 125. Bit Descriptions for DAIA_PBL_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAIAPBLVOL		Digital Audio Interface A Playback Datapath Left Channel Volume. Interface A left channel playback volume control.	0x00	RW
		00000000	0 dB		
		00000001	−0.375 dB		
		xxxxxxxx	0.375 dB steps down to		
		11111111	−95.625 dB		

DAIA_PBR_VOL REGISTER

Address: 0x63, Reset: 0x00, Name: DAIA_PBR_VOL

Digital Audio Interface A Right Channel Playback Volume Control

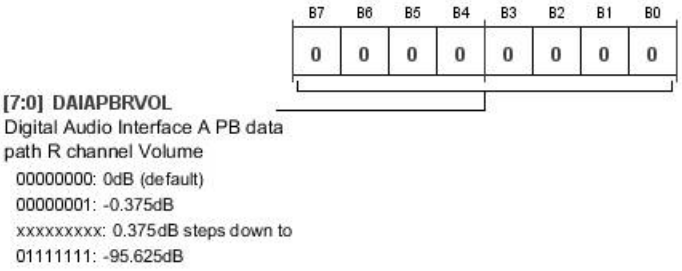


Table 126. Bit Descriptions for DAIA_PBR_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAIAPBRVOL		Digital Audio Interface A Playback Datapath Right Channel Volume. Interface A right channel playback volume control.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		xxxxxxxx	0.375 dB steps down to		
		11111111	−95.625 dB		

DAIB_PBL_VOL REGISTER

Address: 0x64, Reset: 0x00, Name: DAIB_PBL_VOL

Digital Audio Interface B Left Channel Playback Volume Control

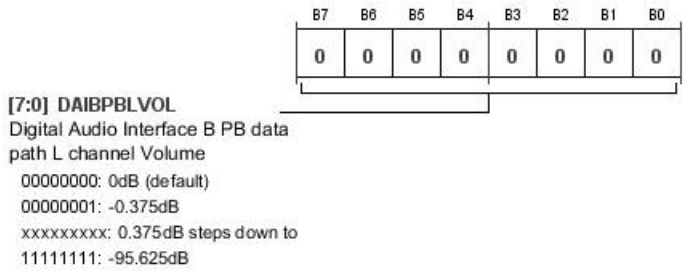


Table 127. Bit Descriptions for DAIB_PBL_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAIBPBLVOL		Digital Audio Interface B Playback Datapath Left Channel Volume. Interface B left channel playback volume control.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		xxxxxxxx	0.375 dB steps down to		
		11111111	−95.625 dB		

DAIB_PBR_VOL REGISTER

Address: 0x65, Reset: 0x00, Name: DAIB_PBR_VOL

Digital Audio Interface B Right Channel Playback Volume Control

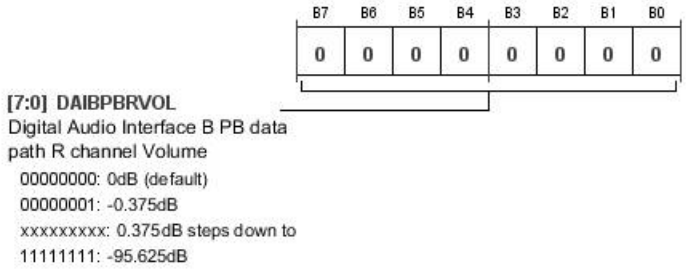


Table 128. Bit Descriptions for DAIB_PBR_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAIBPBRVOL		Digital Audio Interface B PB Datapath Right Channel Volume. Interface B right channel playback volume control.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		xxxxxxxx	0.375 dB steps down to		
		11111111	−95.625 dB		

DAIC_PBL_VOL REGISTER

Address: 0x66, Reset: 0x00, Name: DAIC_PBL_VOL

Digital Audio Interface C Left Channel Playback Volume Control

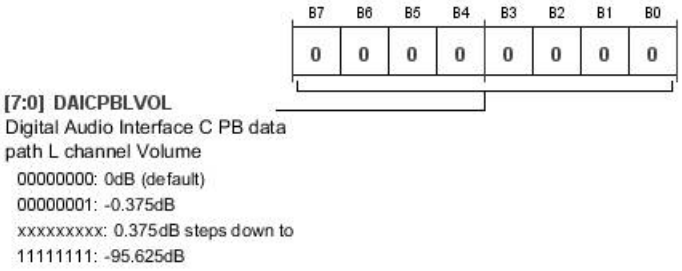


Table 129. Bit Descriptions for DAIC_PBL_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAICPBLVOL		Digital Audio Interface C Playback Datapath Left Channel Volume. Interface C left channel playback volume control.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		xxxxxxxx	0.375 dB steps down to		
		11111111	−95.625 dB		

DAIC_PBR_VOL REGISTER

Address: 0x67, Reset: 0x00, Name: DAIC_PBR_VOL

Digital Audio Interface C Right Channel Playback Volume Control

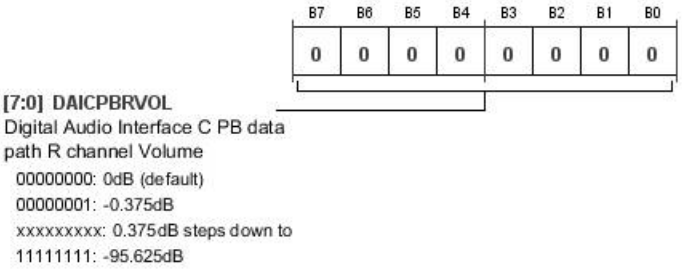


Table 130. Bit Descriptions for DAIC_PBR_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAICPBRVOL		Digital Audio Interface C Playback Datapath R Channel Volume. Interface C right channel playback volume control.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		xxxxxxxx	0.375 dB steps down to		
		11111111	−95.625 dB		

DAIA_RECL_VOL REGISTER

Address: 0x68, Reset: 0x00, Name: DAIA_RECL_VOL

Digital Audio Interface A Left Channel Recording Volume Control

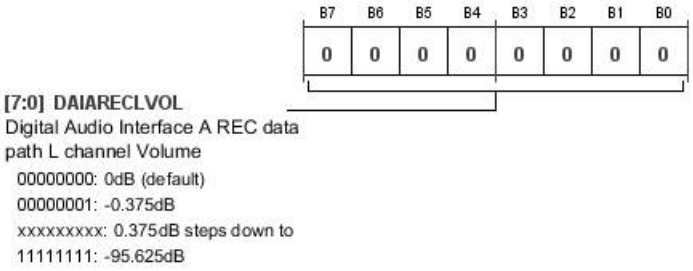


Table 131. Bit Descriptions for DAIA_RECL_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAIARECLVOL		Digital Audio Interface A Record Datapath Left Channel Volume. Interface A left channel recording volume control.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		xxxxxxxx	0.375 dB steps down to		
		11111111	−95.625 dB		

DAIA_RECR_VOL REGISTER

Address: 0x69, Reset: 0x00, Name: DAIA_RECR_VOL

Digital Audio Interface A Right Channel Recording Volume Control

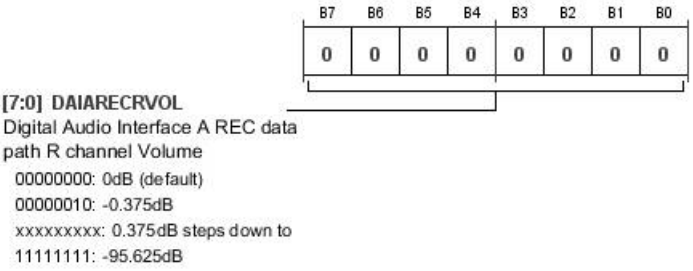


Table 132. Bit Descriptions for DAIA_RECR_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAIARECRVOL		Digital Audio Interface A Record Datapath Right Channel Volume. Interface A right channel recording volume control.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		xxxxxxxx	0.375 dB steps down to		
		11111111	−95.625 dB		

DAIB_RECL_VOL REGISTER

Address: 0x6A, Reset: 0x00, Name: DAIB_RECL_VOL

Digital Audio Interface B Left Channel Recording Volume Control

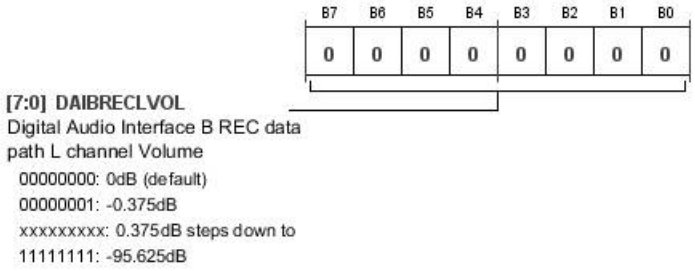


Table 133. Bit Descriptions for DAIB_RECL_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAIBRECLVOL		Digital Audio Interface B Record Datapath Left Channel Volume. Interface B left channel recording volume control.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		xxxxxxxx	0.375 dB steps down to		
		11111111	−95.625 dB		

DAIB_RECR_VOL REGISTER

Address: 0x6B, Reset: 0x00, Name: DAIB_RECR_VOL

Digital Audio Interface B Right Channel Recording Volume Control

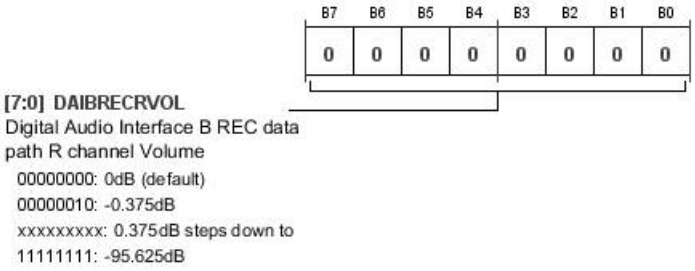


Table 134. Bit Descriptions for DAIB_RECR_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAIBRECRVOL		Digital Audio Interface B Record Datapath Right Channel Volume. Interface B right channel recording volume control.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		xxxxxxxx	0.375 dB steps down to		
		11111111	−95.625 dB		

DAIC_RECL_VOL REGISTER

Address: 0x6C, Reset: 0x00, Name: DAIC_RECL_VOL

Digital Audio Interface C Left Channel Recording Volume Control

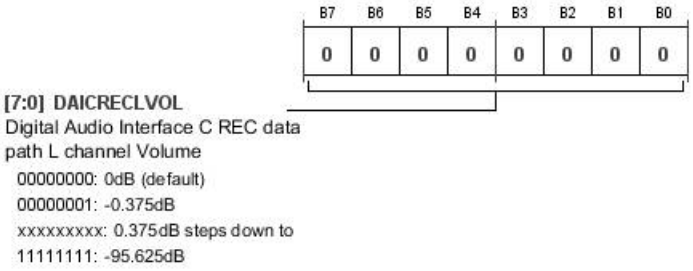


Table 135. Bit Descriptions for DAIC_RECL_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAICRECLVOL		Digital Audio Interface C Record Datapath Left Channel Volume. Interface C left channel recording volume control.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		xxxxxxxx	0.375 dB steps down to		
		11111111	−95.625 dB		

DAIC_RECR_VOL REGISTER

Address: 0x6D, Reset: 0x00, Name: DAIC_RECR_VOL

Digital Audio Interface C Right Channel Recording Volume Control

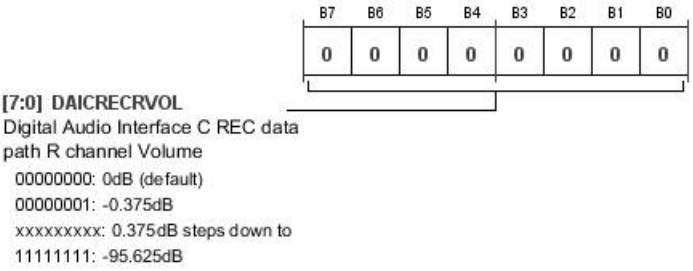


Table 136. Bit Descriptions for DAIC_RECR_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAICRECRVOL		Digital Audio Interface C Record Datapath Right Channel Volume. Interface C right channel recording volume control.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		xxxxxxxx	0.375 dB steps down to		
		11111111	−95.625 dB		

PBAL_VOL REGISTER

Address: 0x6E, Reset: 0x00, Name: PBAL_VOL

DAC1 Left Channel Playback Volume Control

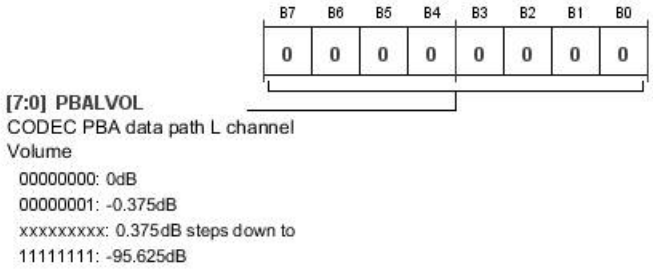


Table 137. Bit Descriptions for PBAL_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PBALVOL		Codec PBA Datapath Left Channel Volume. DAC1 left channel playback volume control.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		xxxxxxxx	0.375 dB steps down to		
		11111111	−95.625 dB		

PBAR_VOL REGISTER

Address: 0x6F, Reset: 0x00, Name: PBAR_VOL

DAC1 Right Channel Playback Volume Control

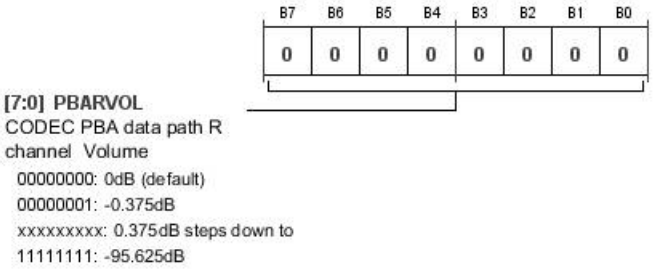


Table 138. Bit Descriptions for PBAR_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PBARVOL		Codec PBA Datapath Right Channel Volume. DAC1 right channel playback volume control.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		xxxxxxxx	0.375 dB steps down to		
		11111111	−95.625 dB		

PBBL_VOL REGISTER

Address: 0x70, Reset: 0x00, Name: PBBL_VOL

DAC2 Left Channel Playback Volume Control

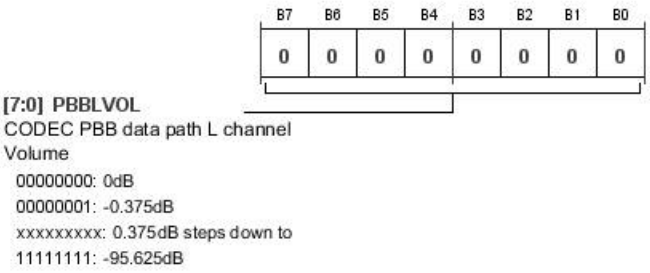


Table 139. Bit Descriptions for PBBL_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PBBLVOL		Codec PBB Datapath Left Channel Volume. DAC2 left channel playback volume control.	0x00	RW
		00000000	0 dB		
		00000001	−0.375 dB		
		xxxxxxxx	0.375 dB steps down to		
		11111111	−95.625 dB		

PBBR_VOL REGISTER

Address: 0x71, Reset: 0x00, Name: PBBR_VOL

DAC2 Right Channel Playback Volume Control

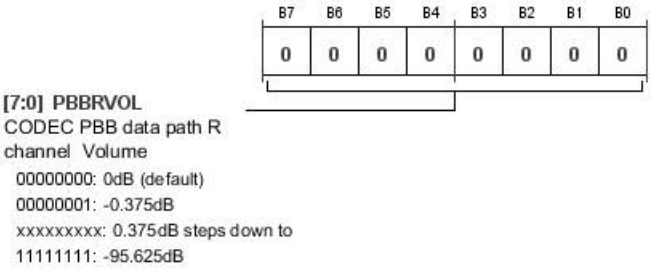


Table 140. Bit Descriptions for PBBR_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PBBRVOL		Codec PBB Datapath Right Channel Volume. DAC2 right channel playback volume control.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		xxxxxxxx	0.375 dB steps down to		
		11111111	−95.625 dB		

RECL_VOL REGISTER

Address: 0x72, Reset: 0x00, Name: RECL_VOL

ADC Left Channel Recording Volume Control

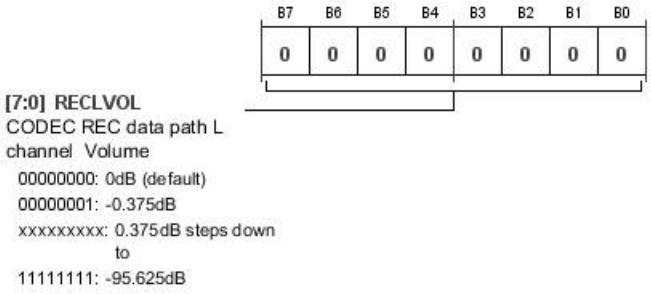


Table 141. Bit Descriptions for RECL_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	RECLVOL		Codec Record Datapath Left Channel Volume. ADC left channel recording volume control.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		xxxxxxxx	0.375 dB steps down to		
		11111111	−95.625 dB		

RECR_VOL REGISTER

Address: 0x73, Reset: 0x00, Name: RECR_VOL

ADC Right Channel Recording Volume Control

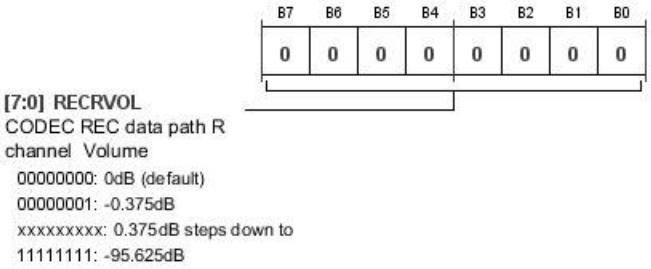


Table 142. Bit Descriptions for RECR_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	RECRVOL		Codec Record Datapath Right Channel Volume. ADC right channel recording volume control.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		xxxxxxxx	0.375 dB steps down to		
		11111111	−95.625 dB		

DRECL_VOL REGISTER

Address: 0x74, Reset: 0x00, Name: DRECL_VOL

Digital Microphone Left Channel Recording Volume Control

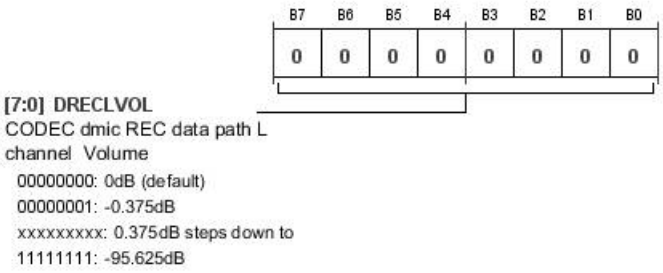


Table 143. Bit Descriptions for DRECL_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRECLVOL		Codec DMIC Record Datapath Left Channel Volume. Digital microphone left channel recording volume control.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		xxxxxxxx	0.375 dB steps down to		
		11111111	−95.625 dB		

DRECR_VOL REGISTER

Address: 0x75, Reset: 0x00, Name: DRECR_VOL

Digital Microphone Right Channel Recording Volume Control

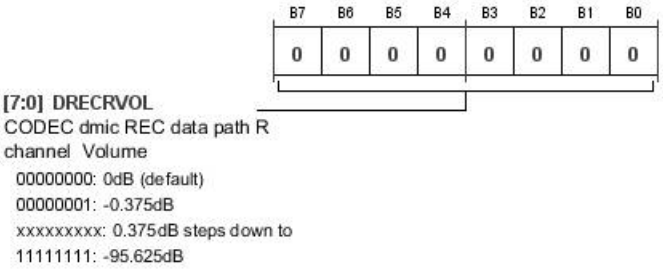


Table 144. Bit Descriptions for DRECR_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRECRVOL		Codec DMIC Record Datapath Right Channel Volume. Digital microphone right channel recording volume control.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		xxxxxxxx	0.375 dB steps down to		
		11111111	−95.625 dB		

VOL_GAIN1 (DAI PLAYBACK) REGISTER

Address: 0x76, Reset: 0x00, Name: VOL_GAIN1

Digital Audio Interface Playback Path Volume Control Gain

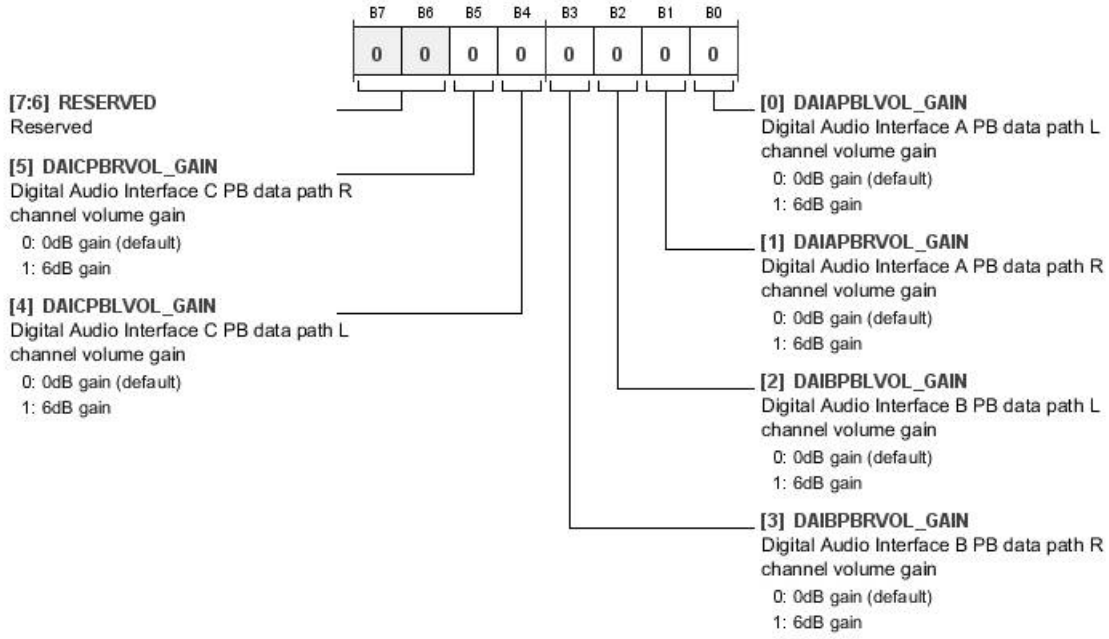


Table 145. Bit Descriptions for VOL_GAIN1

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	RW
5	DAICPBRVOL_GAIN		Digital Audio Interface C Playback Datapath Right Channel Volume Gain. Interface C right channel playback gain.	0x0	RW
		0	0 dB gain (default)		
		1	6 dB gain		
4	DAICPBLVOL_GAIN		Digital Audio Interface C Playback Datapath Left Channel Volume Gain. Interface C left channel playback gain.	0x0	RW
		0	0 dB gain (default)		
		1	6 dB gain		
3	DAIBPBRVOL_GAIN		Digital Audio Interface B Playback Datapath Right Channel Volume Gain. Interface B right channel playback gain.	0x0	RW
		0	0 dB gain (default)		
		1	6 dB gain		
2	DAIBPBLVOL_GAIN		Digital Audio Interface B Playback Datapath Left Channel Volume Gain. Interface B left channel playback gain.	0x0	RW
		0	0 dB gain (default)		
		1	6 dB gain		
1	DAIAPBRVOL_GAIN		Digital Audio Interface A Playback Datapath Right Channel Volume Gain. Interface A right channel playback gain.	0x0	RW
		0	0 dB gain (default)		
		1	6 dB gain		
0	DAIAPBLVOL_GAIN		Digital Audio Interface A Playback Datapath Left Channel Volume Gain. Interface A left channel playback gain.	0x0	RW
		0	0 dB gain (default)		
		1	6 dB gain		

VOL_GAIN2 (DAI RECORD) REGISTER

Address: 0x77, Reset: 0x00, Name: VOL_GAIN2

Digital Audio Interface Recording Path Volume Control Gain

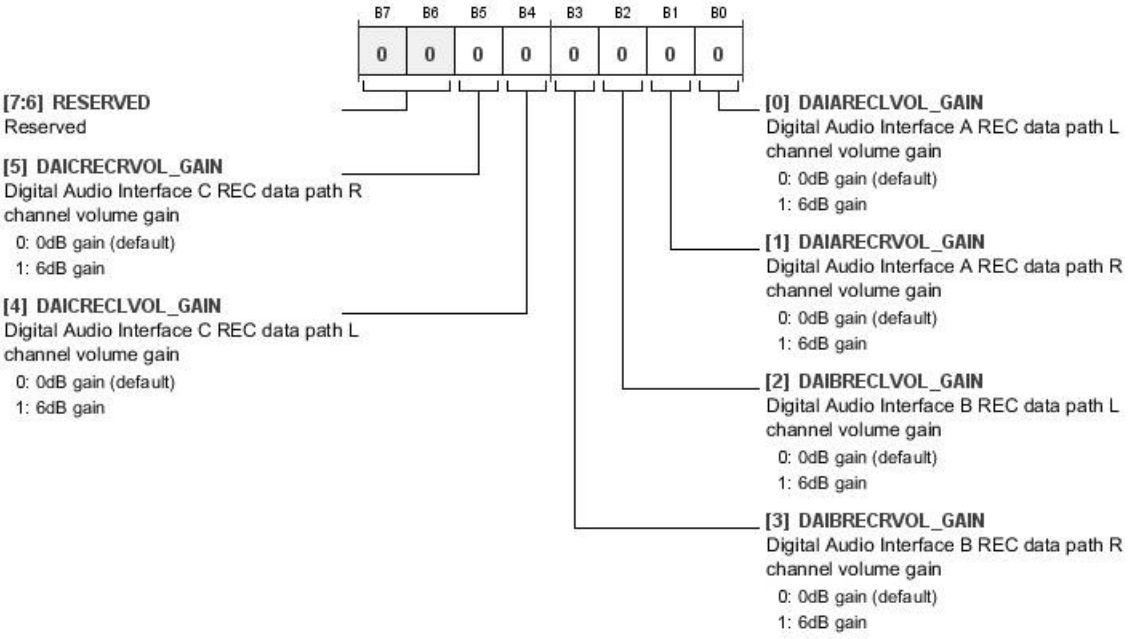


Table 146. Bit Descriptions for VOL_GAIN2

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	RW
5	DAICRECRVOL_GAIN		Digital Audio Interface C Record Datapath Right Channel Volume Gain. Interface C right channel recording gain.	0x0	RW
		0	0 dB gain (default)		
		1	6 dB gain		
4	DAICRECLVOL_GAIN		Digital Audio Interface C Record Datapath Left Channel Volume Gain. Interface C left channel recording gain.	0x0	RW
		0	0 dB gain (default)		
		1	6 dB gain		
3	DAIBRECRVOL_GAIN		Digital Audio Interface B Record Datapath Right Channel Volume Gain. Interface B right channel recording gain.	0x0	RW
		0	0 dB gain (default)		
		1	6 dB gain		
2	DAIBRECLVOL_GAIN		Digital Audio Interface B REC Datapath Left Channel Volume Gain. Interface B left channel recording gain.	0x0	RW
		0	0 dB gain (default)		
		1	6 dB gain		
1	DAIARECRVOL_GAIN		Digital Audio Interface A Record Datapath Right Channel Volume Gain. Interface A right channel recording gain.	0x0	RW
		0	0 dB gain (default)		
		1	6 dB gain		
0	DAIARECLVOL_GAIN		Digital Audio Interface A Record Datapath Left Channel Volume Gain. Interface A left channel recording gain.	0x0	RW
		0	0 dB gain (default)		
		1	6 dB gain		

VOL_GAIN3 (CODEC) REGISTER

Address: 0x78, Reset: 0x00, Name: VOL_GAIN3

Codec Playback/Recording Path Volume Control Gain

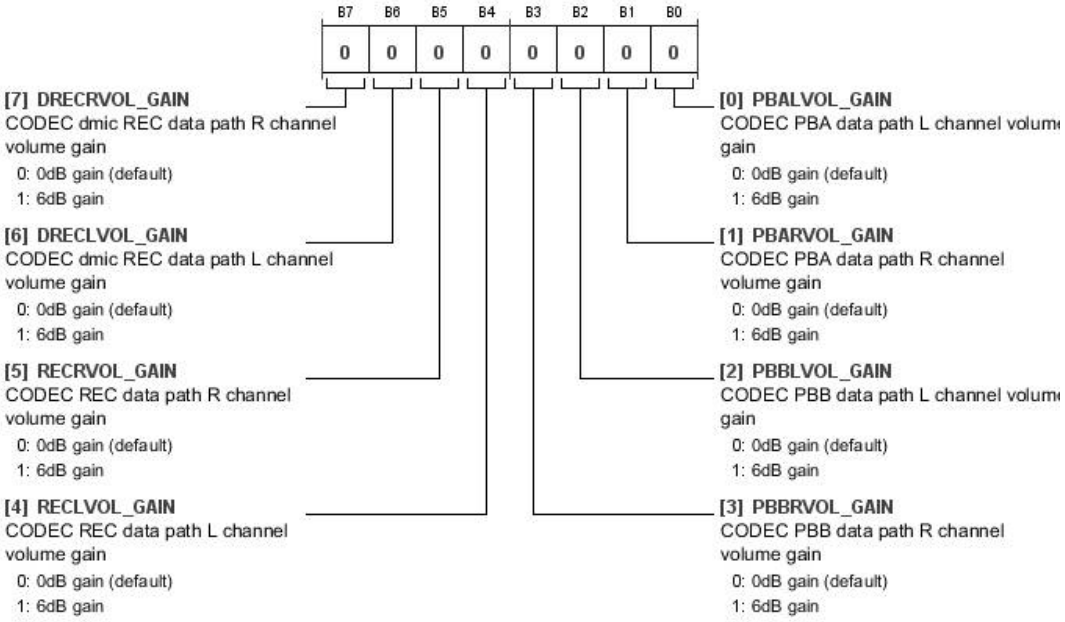


Table 147. Bit Descriptions for VOL_GAIN3

Bits	Bit Name	Settings	Description	Reset	Access
7	DRECRVOL_GAIN		Codec DMIC Record Datapath Right Channel Volume Gain. Digital microphone right channel recording volume gain.	0x0	RW
		0	0 dB gain (default)		
		1	6 dB gain		
6	DRECLVOL_GAIN		Codec DMIC Record Datapath Left Channel Volume Gain. Digital microphone left channel recording volume gain.	0x0	RW
		0	0 dB gain (default)		
		1	6 dB gain		
5	RECRVOL_GAIN		Codec Record Datapath Right Channel Volume Gain. ADC right channel recording volume gain.	0x0	RW
		0	0 dB gain (default)		
		1	6 dB gain		
4	RECLVOL_GAIN		Codec Record Datapath Left Channel Volume Gain. ADC left channel recording volume gain.	0x0	RW
		0	0 dB gain (default)		
		1	6 dB gain		
3	PBBRVOL_GAIN		Codec Playback B Datapath Right Channel Volume Gain. DAC2 right channel playback volume gain.	0x0	RW
		0	0 dB gain (default)		
		1	6 dB gain		
2	PBBLVOL_GAIN		Codec Playback B Datapath Left Channel Volume Gain. DAC2 left channel playback volume gain.	0x0	RW
		0	0 dB gain (default)		
		1	6 dB gain		
1	PBARVOL_GAIN		Codec Playback A Datapath Right Channel Volume Gain. DAC1 right channel playback volume gain.	0x0	RW
		0	0 dB gain (default)		
		1	6 dB gain		

Bits	Bit Name	Settings	Description	Reset	Access
0	PBALVOL_GAIN		Codec Playback A Datapath Left Channel Volume Gain. DAC1 left channel playback volume gain.	0x0	RW
		0	0 dB gain (default)		
		1	6 dB gain		

HPF_CTRL REGISTER

Address: 0x7D, Reset: 0x00, Name: HPF_CTRL

DSP High-Pass Filter Setting

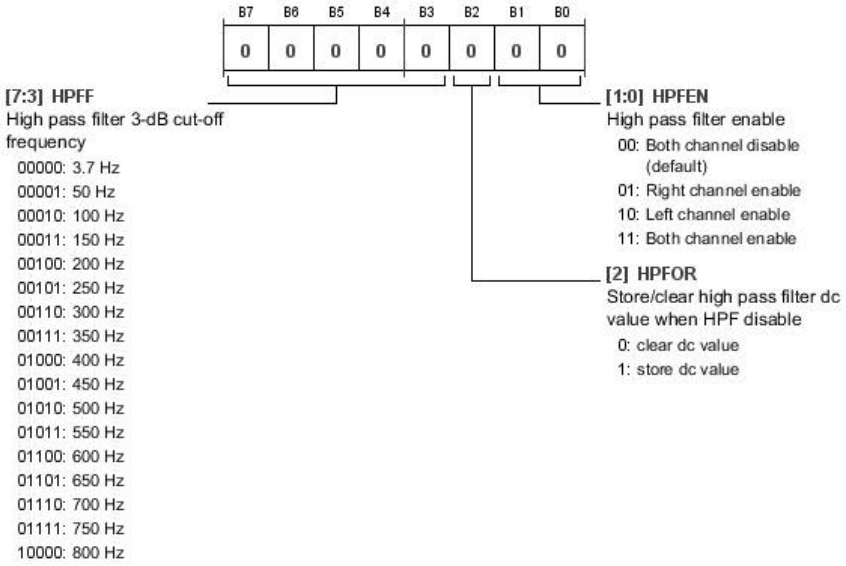


Table 148. Bit Descriptions for HPF_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	HPFF		High-Pass Filter 3 dB Cutoff Frequency. High-pass filter cutoff frequency selection: 3.7 Hz, 50 Hz to 800 Hz in 16 steps.	0x00	RW
		00000	3.7 Hz		
		00001	50 Hz		
		00010	100 Hz		
		00011	150 Hz		
		00100	200 Hz		
		00101	250 Hz		
		00110	300 Hz		
		00111	350 Hz		
		01000	400 Hz		
		01001	450 Hz		
		01010	500 Hz		
		01011	550 Hz		
		01100	600 Hz		
		01101	650 Hz		
		01110	700 Hz		
		01111	750 Hz		
		10000	800 Hz		
2	HPFOR		Store/Clear High-Pass Filter DC Value When HPF Disabled. High-pass filter dc value control.	0x0	RW
		0	Clear dc value		
		1	Store dc value		

Bits	Bit Name	Settings	Description	Reset	Access
[1:0]	HPFEN		High-Pass Filter Enable. High-pass filter enable/disable control.	0x0	RW
		00	Both channels disabled (default)		
		01	Right channel enabled		
		10	Left channel enabled		
		11	Both channels enabled		

BASS1 REGISTER

Address: 0x7E, Reset: 0x00, Name: BASS1

Bass Enhancement Control Register

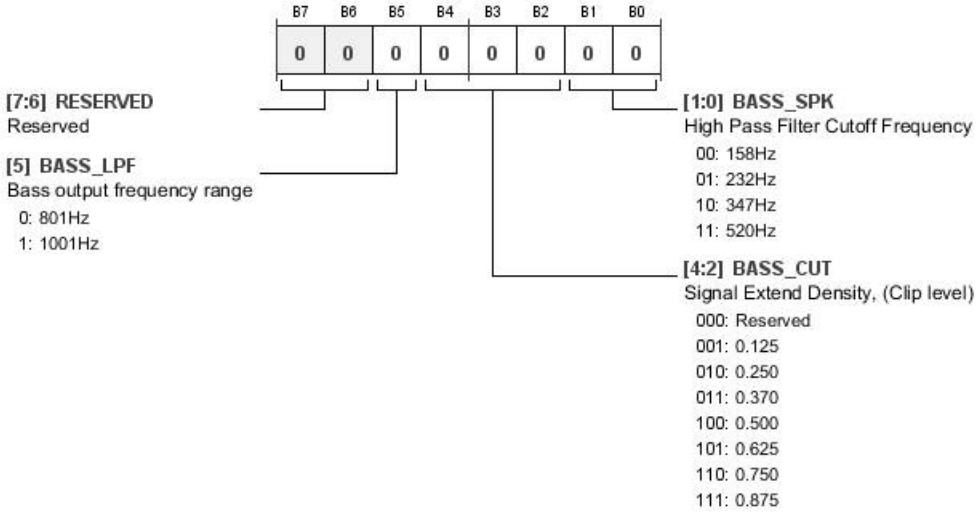


Table 149. Bit Descriptions for BASS1

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	RW
5	BASS_LPF		Bass Output Frequency Range. Cutoff frequency setting for low-pass filter bass enhancement.	0x0	RW
		0	801 Hz		
		1	1001 Hz		
[4:2]	BASS_CUT		Signal Extend Density (Clip Level). Overdrive level for bass enhancement.	0x0	RW
		000	Reserved		
		001	0.125		
		010	0.250		
		011	0.370		
		100	0.500		
		101	0.625		
		110	0.750		
		111	0.875		
[1:0]	BASS_SPK		High-Pass Filter Cutoff Frequency. Cutoff frequency setting for high-pass filter bass enhancement.	0x0	RW
		00	158 Hz		
		01	232 Hz		
		10	347 Hz		
		11	520 Hz		

BASS2 REGISTER

Address: 0x7F, Reset: 0x00, Name: BASS2

Bass Enhancement Control Register

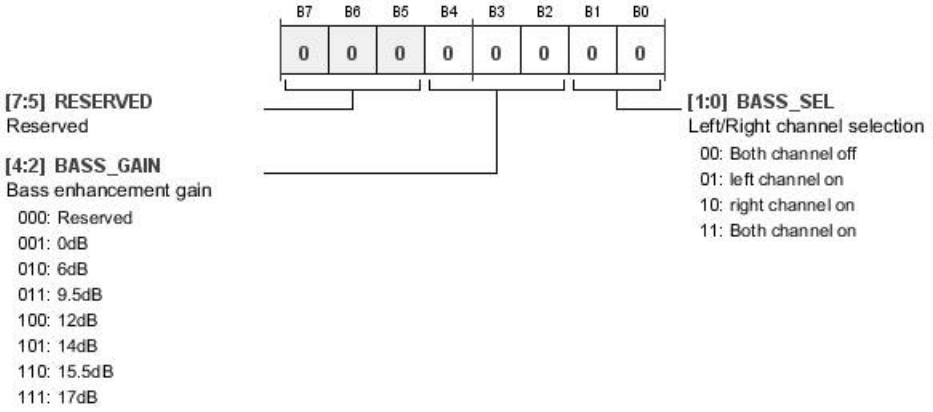


Table 150. Bit Descriptions for BASS2

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
[4:2]	BASS_GAIN		Bass Enhancement Gain. Gain control setting for bass enhancement.	0x0	RW
		000	Reserved		
		001	0 dB		
		010	6 dB		
		011	9.5 dB		
		100	12 dB		
		101	14 dB		
		110	15.5 dB		
		111	17 dB		
[1:0]	BASS_SEL		Left/Right Channel Selection. Channel selection for bass enhancement.	0x0	RW
		00	Both channels off		
		01	Left channel on		
		10	Right channel on		
		11	Both channels on		

DRC1_CTRL1 REGISTER

Address: 0x80, Reset: 0x78, Name: DRC1_CTRL1

DRC1 Level Detector Averaging Time and DRC Noise Gate Recovery Time Setting

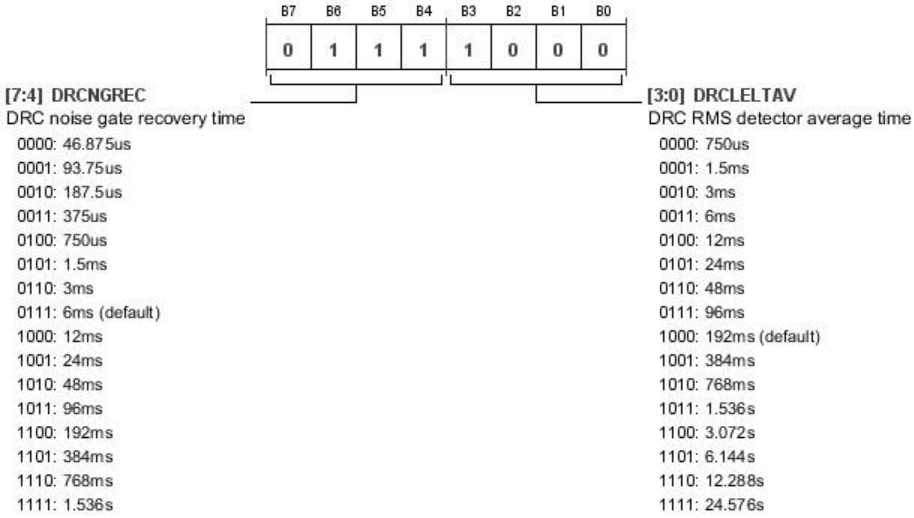


Table 151. Bit Descriptions for DRC1_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DRCNGREC		DRC1 Noise Gate Recovery Time.	0x7	RW
		0000	46.875 µs		
		0001	93.75 µs		
		0010	187.5 µs		
		0011	375 µs		
		0100	750 µs		
		0101	1.5 ms		
		0110	3 ms		
		0111	6 ms (default)		
		1000	12 ms		
		1001	24 ms		
		1010	48 ms		
		1011	96 ms		
		1100	192 ms		
		1101	384 ms		
		1110	768 ms		
		1111	1.536 sec		
[3:0]	DRCLELTAV		DRC1 RMS Detector Average Time.	0x8	RW
		0000	750 µs		
		0001	1.5 ms		
		0010	3 ms		
		0011	6 ms		
		0100	12 ms		
		0101	24 ms		
		0110	48 ms		
		0111	96 ms		
		1000	192 ms (default)		
		1001	384 ms		
		1010	768 ms		
		1011	1.536 sec		

Bits	Bit Name	Settings	Description	Reset	Access
		1100	3.072 sec		
		1101	6.144 sec		
		1110	12.288 sec		
		1111	24.576 sec		

DRC1_CTRL2 REGISTER

Address: 0x81, Reset: 0x18, Name: DRC1_CTRL2

DRC1 Attack and Decay Time Setting

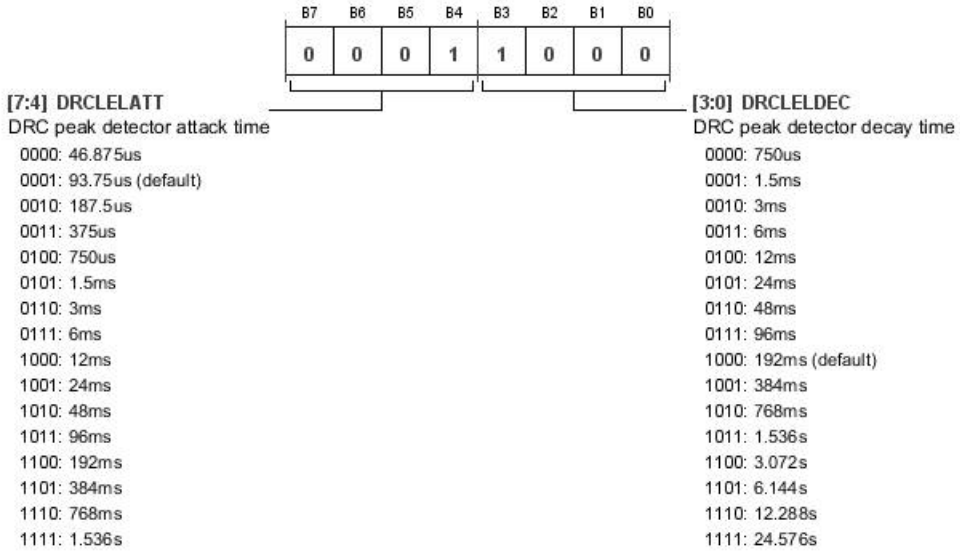


Table 152. Bit Descriptions for DRC1_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DRCLELATT		DRC1 Peak Detector Attack Time.	0x1	RW
		0000	46.875 µs		
		0001	93.75 µs (default)		
		0010	187.5 µs		
		0011	375 µs		
		0100	750 µs		
		0101	1.5 ms		
		0110	3 ms		
		0111	6 ms		
		1000	12 ms		
		1001	24 ms		
		1010	48 ms		
		1011	96 ms		
		1100	192 ms		
		1101	384 ms		
		1110	768 ms		
		1111	1.536 sec		

Bits	Bit Name	Settings	Description	Reset	Access
[3:0]	DRCLELDEC		DRC1 Peak Detector Decay Time.	0x8	RW
		0000	750 µs		
		0001	1.5 ms		
		0010	3 ms		
		0011	6 ms		
		0100	12 ms		
		0101	24 ms		
		0110	48 ms		
		0111	96 ms		
		1000	192 ms (default)		
		1001	384 ms		
		1010	768 ms		
		1011	1.536 sec		
		1100	3.072 sec		
		1101	6.144 sec		
		1110	12.288 sec		
		1111	24.576 sec		

DRC1_CTRL3 REGISTER

Address: 0x82, Reset: 0x00, Name: DRC1_CTRL3

DRC1 Threshold Point X1 on X-Axis (Input Level)

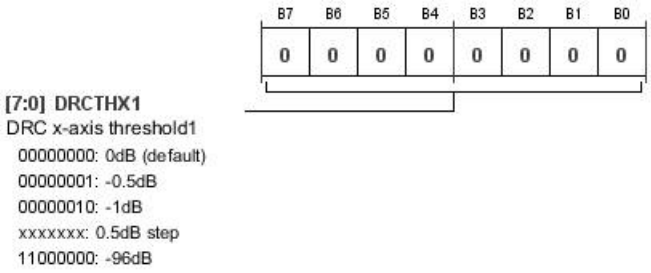


Table 153. Bit Descriptions for DRC1_CTRL3

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHX1		DRC1 X-Axis Threshold 1.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxx	0.5 dB step		
		11000000	−96 dB		

DRC1_CTRL4 REGISTER

Address: 0x83, Reset: 0x00, Name: DRC1_CTRL4

DRC1 Threshold Point X2 on X-Axis (Input Level)

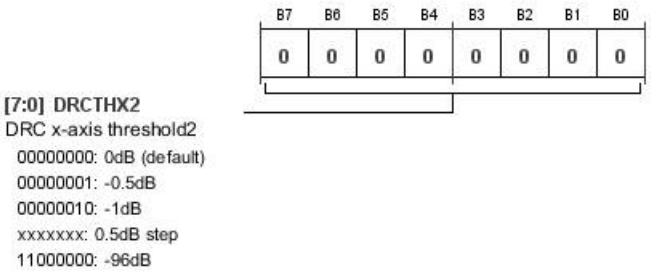


Table 154. Bit Descriptions for DRC1_CTRL4

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHX2		DRC1 X-Axis Threshold 2.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxx	0.5 dB step		
		11000000	−96 dB		

DRC1_CTRL5 REGISTER

Address: 0x84, Reset: 0x00, Name: DRC1_CTRL5

DRC1 Threshold Point X3 on X-Axis (Input Level)

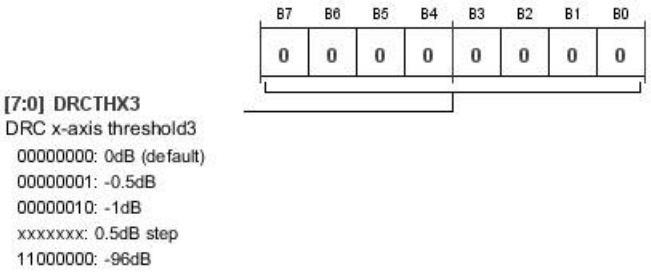


Table 155. Bit Descriptions for DRC1_CTRL5

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHX3		DRC1 X-Axis Threshold 3.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxx	0.5 dB step		
		11000000	−96 dB		

DRC1_CTRL6 REGISTER

Address: 0x85, Reset: 0xC0, Name: DRC1_CTRL6

DRC1 Threshold Point X4 on X-Axis (Input Level)

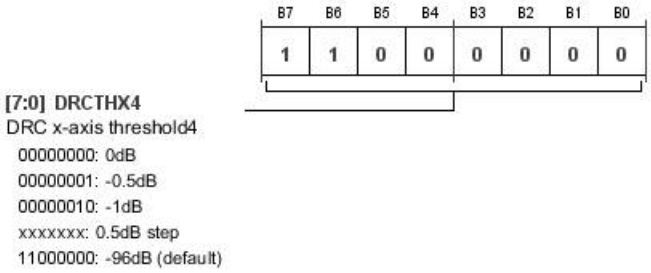


Table 156. Bit Descriptions for DRC1_CTRL6

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHX4		DRC1 X-Axis Threshold 4.	0xC0	RW
		00000000	0 dB		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxx	0.5 dB step		
		11000000	−96 dB (default)		

DRC1_CTRL7 REGISTER

Address: 0x86, Reset: 0x00, Name: DRC1_CTRL7

DRC1 Threshold Point Y1 on Y-Axis (Output Level)

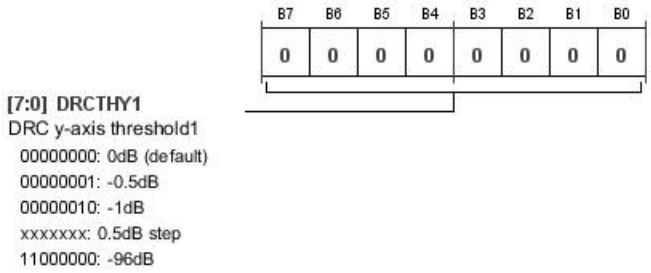


Table 157. Bit Descriptions for DRC1_CTRL7

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHY1		DRC1 Y-Axis Threshold 1.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxx	0.5 dB step		
		11000000	−96 dB		

DRC1_CTRL8 REGISTER

Address: 0x87, Reset: 0x00, Name: DRC1_CTRL8

DRC1 Threshold Point Y2 on Y-Axis (Output Level)

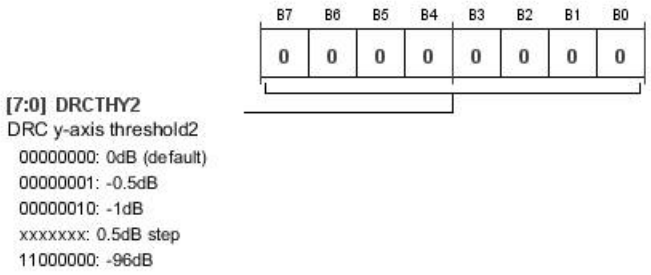


Table 158. Bit Descriptions for DRC1_CTRL8

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHY2		DRC1 Y-Axis Threshold 2.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxx	0.5 dB step		
		11000000	−96 dB		

DRC1_CTRL9 REGISTER

Address: 0x88, Reset: 0x00, Name: DRC1_CTRL9

DRC1 Threshold Point Y3 on Y-Axis (Output Level)

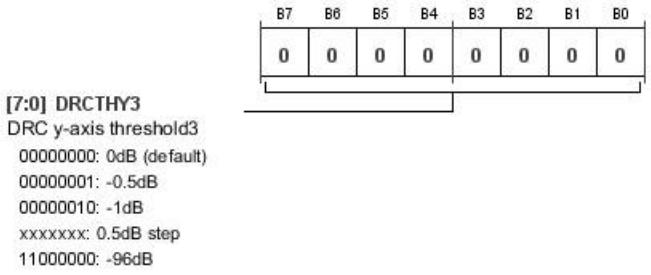


Table 159. Bit Descriptions for DRC1_CTRL9

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHY3		DRC1 Y-Axis Threshold 3.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxx	0.5 dB step		
		11000000	−96 dB		

DRC1_CTRL10 REGISTER

Address: 0x89, Reset: 0xC0, Name: DRC1_CTRL10

DRC1 Threshold Point Y4 on Y-Axis (Output Level).

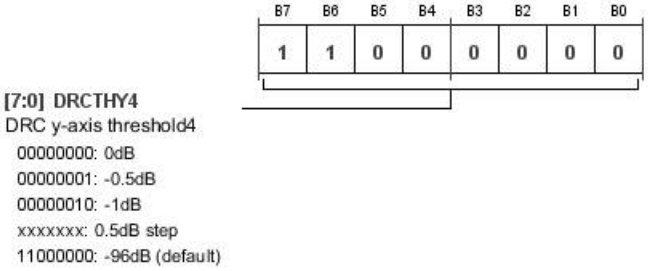


Table 160. Bit Descriptions for DRC1_CTRL10

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHY4		DRC1 Y-Axis Threshold 4.	0xC0	RW
		00000000	0 dB		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxx	0.5 dB step		
		11000000	−96 dB (default)		

DRC1_CTRL11 REGISTER

Address: 0x8A, Reset: 0x88, Name: DRC1_CTRL11

DRC1 Gain Smoothing Attack and Decay Time Setting

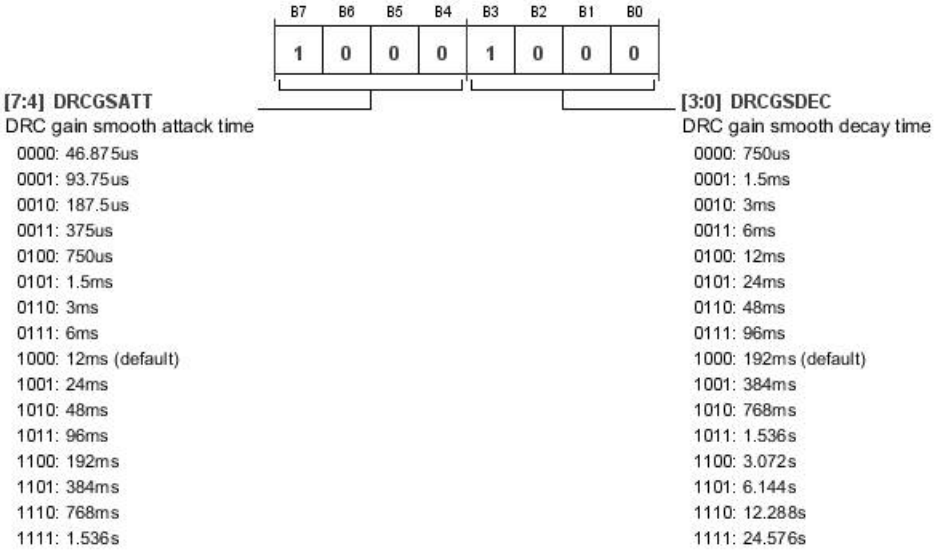


Table 161. Bit Descriptions for DRC1_CTRL11

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DRCGSATT		DRC1 Gain Smooth Attack Time.	0x8	RW
		0000	46.875 µs		
		0001	93.75 µs		
		0010	187.5 µs		
		0011	375 µs		
		0100	750 µs		
		0101	1.5 ms		
		0110	3 ms		
		0111	6 ms		
		1000	12 ms (default)		
		1001	24 ms		
		1010	48 ms		
		1011	96 ms		
		1100	192 ms		
		1101	384 ms		
		1110	768 ms		
		1111	1.536 sec		
[3:0]	DRCGSDEC		DRC1 Gain Smooth Decay Time.	0x8	RW
		0000	750 µs		
		0001	1.5 ms		
		0010	3 ms		
		0011	6 ms		
		0100	12 ms		
		0101	24 ms		
		0110	48 ms		
		0111	96 ms		
		1000	192 ms (default)		
		1001	384 ms		
		1010	768 ms		
		1011	1.536 sec		
		1100	3.072 sec		
		1101	6.144 sec		
		1110	12.288 sec		
		1111	24.576 sec		

DRC1_CTRL12 REGISTER

Address: 0x8B, Reset: 0x7A, Name: DRC1_CTRL12

DRC1 Noise Gate Hold Time and Normal Operation Hold Time Setting

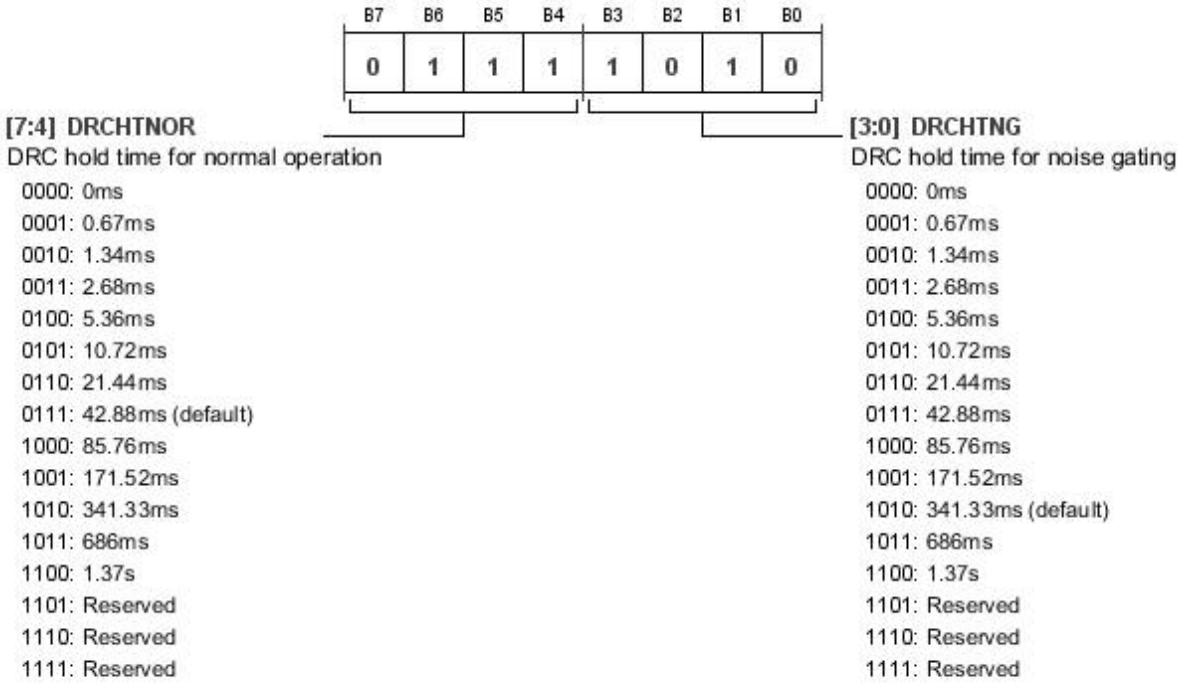


Table 162. Bit Descriptions for DRC1_CTRL12

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DRCHTNOR		DRC1 Hold Time for Normal Operation.	0x7	RW
		0000	0 ms		
		0001	0.67 ms		
		0010	1.34 ms		
		0011	2.68 ms		
		0100	5.36 ms		
		0101	10.72 ms		
		0110	21.44 ms		
		0111	42.88 ms (default)		
		1000	85.76 ms		
		1001	171.52 ms		
		1010	341.33 ms		
		1011	686 ms		
		1100	1.37 sec		
		1101	Reserved		
		1110	Reserved		
		1111	Reserved		
[3:0]	DRCHTNG		DRC1 Hold Time for Noise Gating.	0xA	RW
		0000	0 ms		
		0001	0.67 ms		
		0010	1.34 ms		
		0011	2.68 ms		
		0100	5.36 ms		
		0101	10.72 ms		

Bits	Bit Name	Settings	Description	Reset	Access
		0110	21.44 ms		
		0111	42.88 ms		
		1000	85.76 ms		
		1001	171.52 ms		
		1010	341.33 ms (default)		
		1011	686 ms		
		1100	1.37 sec		
		1101	Reserved		
		1110	Reserved		
		1111	Reserved		

DRC1_CTRL13 REGISTER

Address: 0x8C, Reset: 0xDF, Name: DRC1_CTRL13

DRC1 Gain Setting

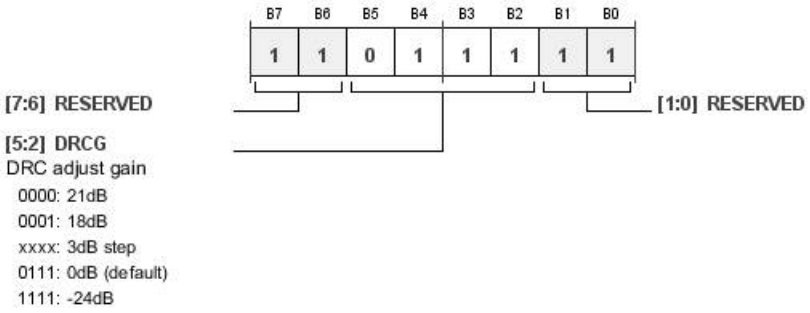


Table 163. Bit Descriptions for DRC1_CTRL13

Bits	Bit Name	Settings	Description	Reset	Access
[5:2]	DRCG		DRC1 Adjust Gain. DRC1 gain setting.	0x7	RW
		0000	21 dB		
		0001	18 dB		
		xxxx	3 dB step size		
		0111	0 dB (default)		
		1111	−24 dB		

DRC1_CTRL14 REGISTER

Address: 0x8D, Reset: 0x20, Name: DRC1_CTRL14

DRC1 Enable Control

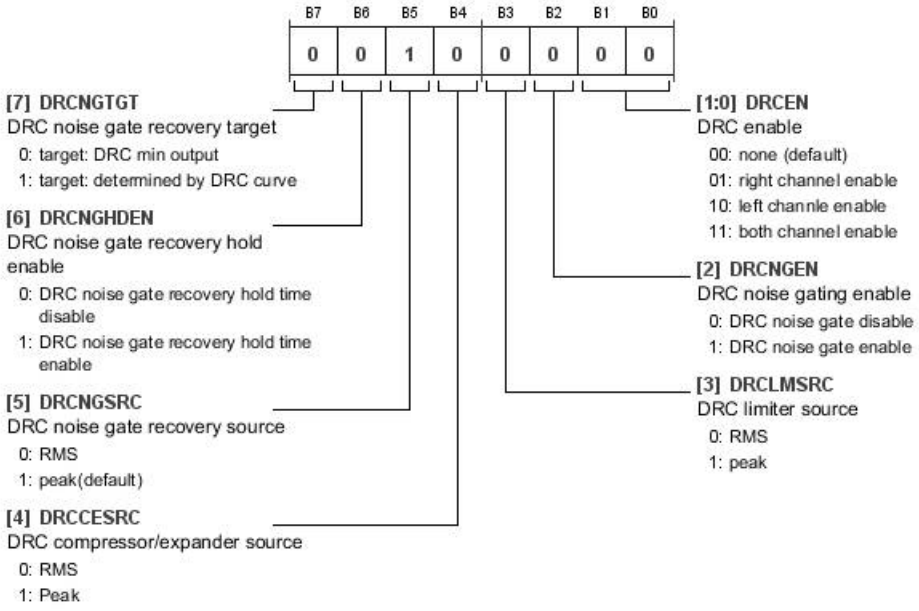


Table 164. Bit Descriptions for DRC1_CTRL14

Bits	Bit Name	Settings	Description	Reset	Access
7	DRCNGTGT		DRC1 Noise Gate Recovery Target.	0x0	RW
		0	Target: DRC minimum output		
		1	Target: determined by DRC curve		
6	DRCNGHDEN		DRC1 Noise Gate Recovery Hold Enable.	0x0	RW
		0	DRC noise gate recovery hold time disable		
		1	DRC noise gate recovery hold time enable		
5	DRCNGSRC		DRC1 Noise Gate Recovery Source.	0x1	RW
		0	RMS		
		1	Peak (default)		
4	DRCCESRC		DRC1 Compressor/Expander Source.	0x0	RW
		0	RMS		
		1	Peak		
3	DRCLMSRC		DRC1 Limiter Source.	0x0	RW
		0	RMS		
		1	Peak		
2	DRCNGEN		DRC1 Noise Gating Enable.	0x0	RW
		0	DRC noise gate disable		
		1	DRC noise gate enable		
[1:0]	DRCEN		DRC1 Enable.	0x0	RW
		00	None (default)		
		01	Right channel enable		
		10	Left channel enable		
		11	Both channels enable		

DRC1_CTRL15 REGISTER

Address: 0x8E, Reset: 0x00, Name: DRC1_CTRL15

DRC1 Peak to RMS Ratio and RMS Detector Setting Register

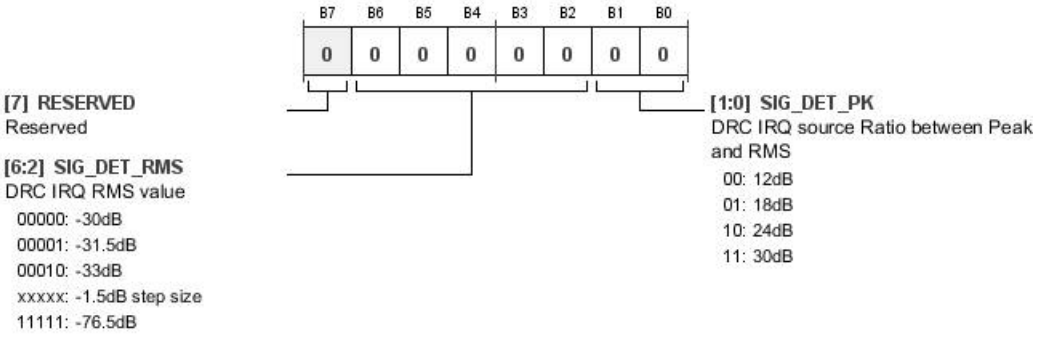


Table 165. Bit Descriptions for DRC1_CTRL15

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
[6:2]	SIG_DET_RMS		DRC1 IRQ RMS Value. DRC RMS detector setting.	0x00	RW
		00000	−30 dB		
		00001	−31.5 dB		
		00010	−33 dB		
		xxxxx	−1.5 dB step size		
		11111	−76.5 dB		
[1:0]	SIG_DET_PK		DRC1 IRQ Source Ratio Between Peak and RMS. DRC peak to rms ratio setting.	0x0	RW
		00	12 dB		
		01	18 dB		
		10	24 dB		
		11	30 dB		

DRC1_CTRL16 REGISTER

Address: 0x8F, Reset: 0x00, Name: DRC1_CTRL16

DRC1 IRQ Enable/Disable and IRQ Source Selection Setting Register

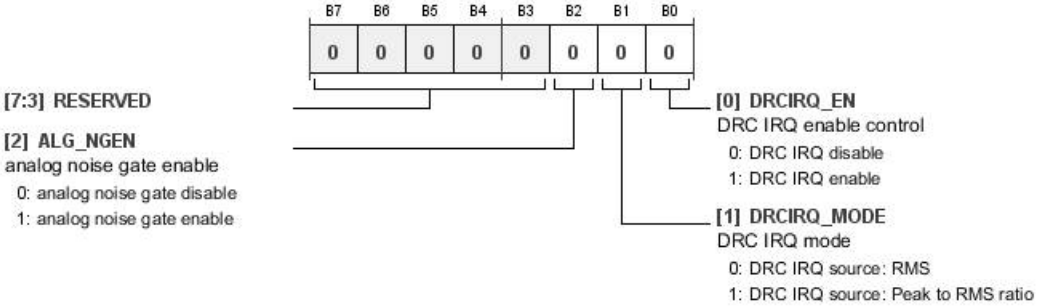


Table 166. Bit Descriptions for DRC1_CTRL16

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	RESERVED		Reserved.	0x00	RW
2	ALG_NGEN		Analog Noise Gate Enable.	0x0	RW
		0	Analog noise gate disable		
		1	Analog noise gate enable		
1	DRCIRQ_MODE		DRC1 IRQ Mode. DRC IRQ source selection setting.	0x0	RW
		0	DRC IRQ source: rms		
		1	DRC IRQ source: Peak to rms ratio		
0	DRCIRQ_EN		DRC1 IRQ Enable Control. DRC IRQ enable/disable control.	0x0	RW
		0	DRC IRQ disable		
		1	DRC IRQ enable		

DRC2_CTRL1 REGISTER

Address: 0x90, Reset: 0x78, Name: DRC2_CTRL1

DRC2 Level Detector Averaging Time and DRC Noise Gate Recovery Time Setting

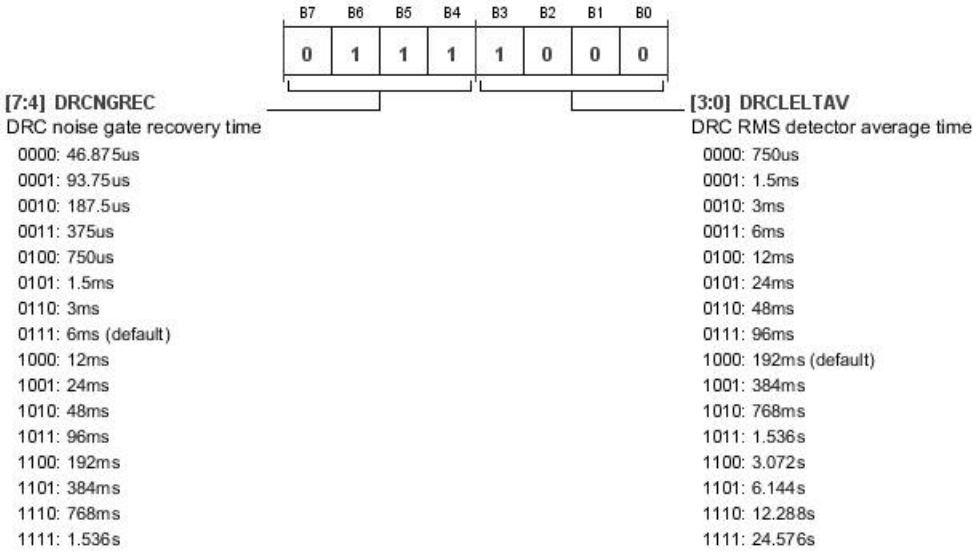


Table 167. Bit Descriptions for DRC2_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DRCNGREC		DRC2 Noise Gate Recovery Time.	0x7	RW
		0000	46.875 µs		
		0001	93.75 µs		
		0010	187.5 µs		
		0011	375 µs		
		0100	750 µs		
		0101	1.5 ms		
		0110	3 ms		
		0111	6 ms (default)		
		1000	12 ms		
		1001	24 ms		
		1010	48 ms		
		1011	96 ms		
		1100	192 ms		
		1101	384 ms		
		1110	768 ms		
		1111	1.536 sec		
[3:0]	DRCLELTAV		DRC2 RMS Detector Average Time.	0x8	RW
		0000	750 µs		
		0001	1.5 ms		
		0010	3 ms		
		0011	6 ms		
		0100	12 ms		
		0101	24 ms		
		0110	48 ms		
		0111	96 ms		
		1000	192 ms (default)		
		1001	384 ms		
		1010	768 ms		

Bits	Bit Name	Settings	Description	Reset	Access
		1011	1.536 sec		
		1100	3.072 sec		
		1101	6.144 sec		
		1110	12.288 sec		
		1111	24.576 sec		

DRC2_CTRL2 REGISTER

Address: 0x91, Reset: 0x18, Name: DRC2_CTRL2

DRC2 Attack and Decay Time Setting

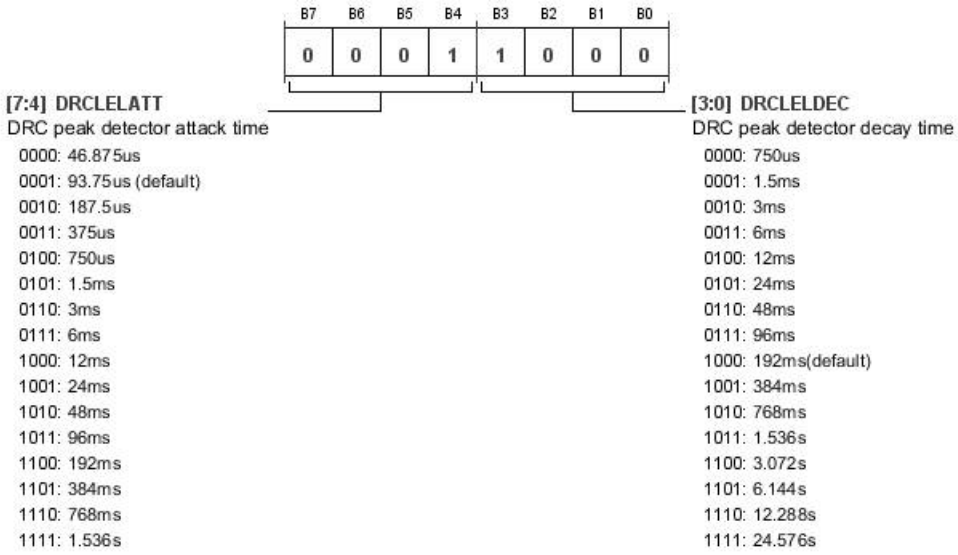


Table 168. Bit Descriptions for DRC2_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DRCLELATT		DRC2 Peak Detector Attack Time.	0x1	RW
		0000	46.875 µs		
		0001	93.75 µs (default)		
		0010	187.5 µs		
		0011	375 µs		
		0100	750 µs		
		0101	1.5 ms		
		0110	3 ms		
		0111	6 ms		
		1000	12 ms		
		1001	24 ms		
		1010	48 ms		
		1011	96 ms		
		1100	192 ms		
		1101	384 ms		
		1110	768 ms		
		1111	1.536 sec		

Bits	Bit Name	Settings	Description	Reset	Access
[3:0]	DRCLELDEC		DRC2 Peak Detector Decay Time.	0x8	RW
		0000	750 µs		
		0001	1.5 ms		
		0010	3 ms		
		0011	6 ms		
		0100	12 ms		
		0101	24 ms		
		0110	48 ms		
		0111	96 ms		
		1000	192 ms (default)		
		1001	384 ms		
		1010	768 ms		
		1011	1.536 sec		
		1100	3.072 sec		
		1101	6.144 sec		
		1110	12.288 sec		
		1111	24.576 sec		

DRC2_CTRL3 REGISTER

Address: 0x92, Reset: 0x00, Name: DRC2_CTRL3

DRC2 Threshold Point X1 on X-Axis (Input Level)

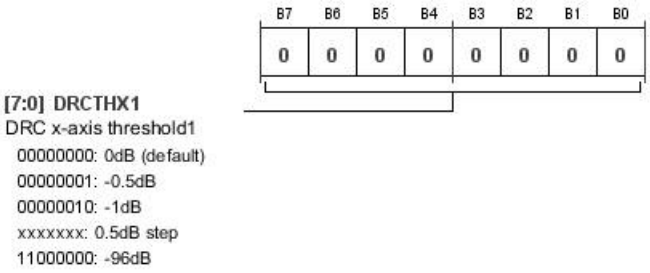


Table 169. Bit Descriptions for DRC2_CTRL3

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHX1		DRC2 X-Axis Threshold 1.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxxx	0.5 dB step size		
		11000000	−96 dB		

DRC2_CTRL4 REGISTER

Address: 0x93, Reset: 0x00, Name: DRC2_CTRL4

DRC2 Threshold Point X2 on X-Axis (Input Level)

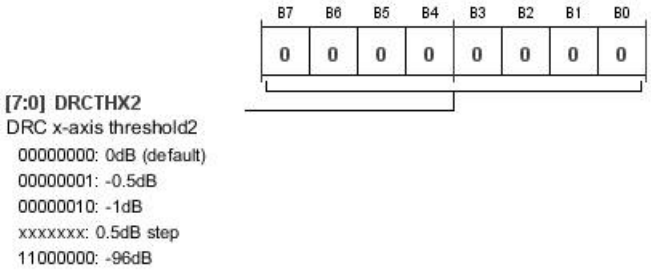


Table 170. Bit Descriptions for DRC2_CTRL4

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHX2		DRC2 X-Axis Threshold 2.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxxx	0.5 dB step size		
		11000000	−96 dB		

DRC2_CTRL5 REGISTER

Address: 0x94, Reset: 0x00, Name: DRC2_CTRL5

DRC2 Threshold Point X3 on X-Axis (Input Level)

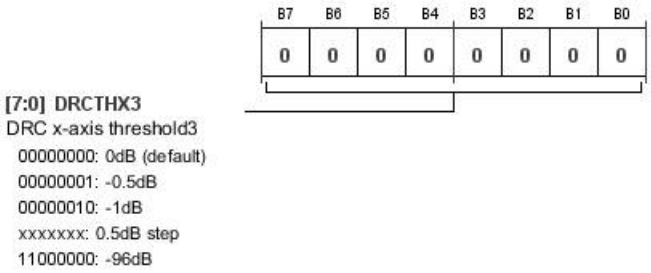


Table 171. Bit Descriptions for DRC2_CTRL5

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHX3		DRC2 X-Axis Threshold 3.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxxx	0.5 dB step size		
		11000000	−96 dB		

DRC2_CTRL6 REGISTER

Address: 0x95, Reset: 0xC0, Name: DRC2_CTRL6

DRC2 Threshold Point X4 on X-Axis (Input Level)

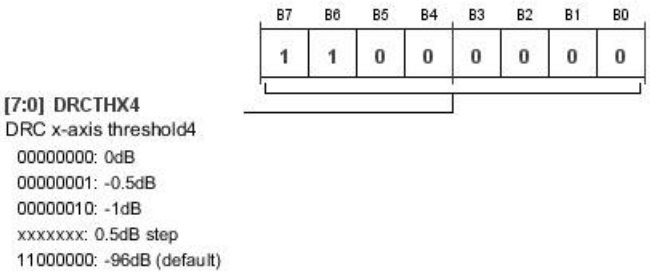


Table 172. Bit Descriptions for DRC2_CTRL6

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHX4		DRC2 X-Axis Threshold 4.	0xC0	RW
		00000000	0 dB		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxxx	0.5 dB step size		
		11000000	−96 dB (default)		

DRC2_CTRL7 REGISTER

Address: 0x96, Reset: 0x00, Name: DRC2_CTRL7

DRC2 Threshold Point Y1 on Y-Axis (Output Level)

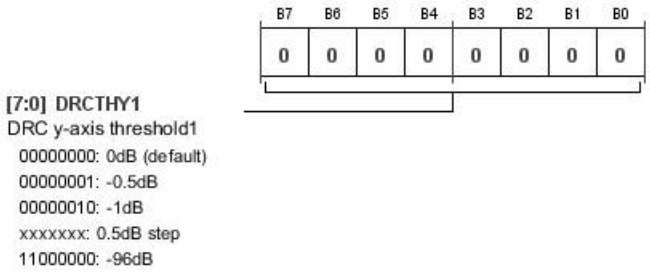


Table 173. Bit Descriptions for DRC2_CTRL7

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHY1		DRC2 Y-Axis Threshold 1.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxxx	0.5 dB step size		
		11000000	−96 dB		

DRC2_CTRL8 REGISTER

Address: 0x97, Reset: 0x00, Name: DRC2_CTRL8

DRC2 Threshold Point Y2 on Y-Axis (Output Level)

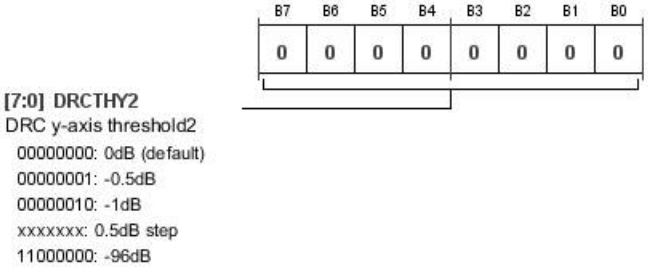


Table 174. Bit Descriptions for DRC2_CTRL8

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHY2		DRC2 Y-Axis Threshold 2.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxxx	0.5 dB step size		
		11000000	−96 dB		

DRC2_CTRL9 REGISTER

Address: 0x98, Reset: 0x00, Name: DRC2_CTRL9

DRC2 Threshold Point Y3 on Y-Axis (Output Level)

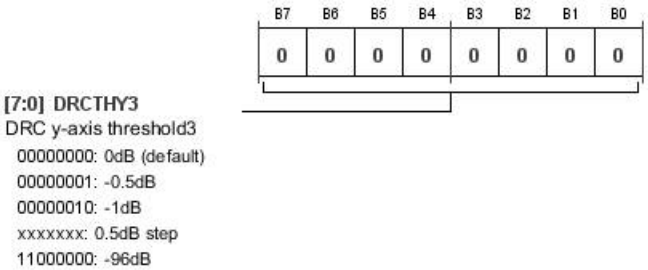


Table 175. Bit Descriptions for DRC2_CTRL9

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHY3		DRC2 Y-Axis Threshold 3.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxxx	0.5 dB step size		
		11000000	−96 dB		

DRC2_CTRL10 REGISTER

Address: 0x99, Reset: 0xC0, Name: DRC2_CTRL10

DRC2 Threshold Point Y4 on Y-Axis (Output Level)

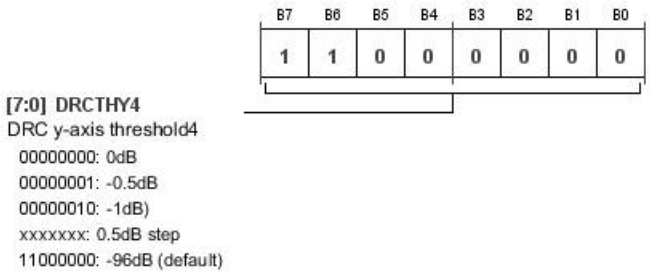


Table 176. Bit Descriptions for DRC2_CTRL10

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHY4		DRC2 Y-Axis Threshold 4.	0xC0	RW
		00000000	0 dB		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxxx	0.5 dB step size		
		11000000	−96 dB (default)		

DRC2_CTRL11 REGISTER

Address: 0x9A, Reset: 0x88, Name: DRC2_CTRL11

DRC2 Gain Smoothing Attack and Decay Time Setting

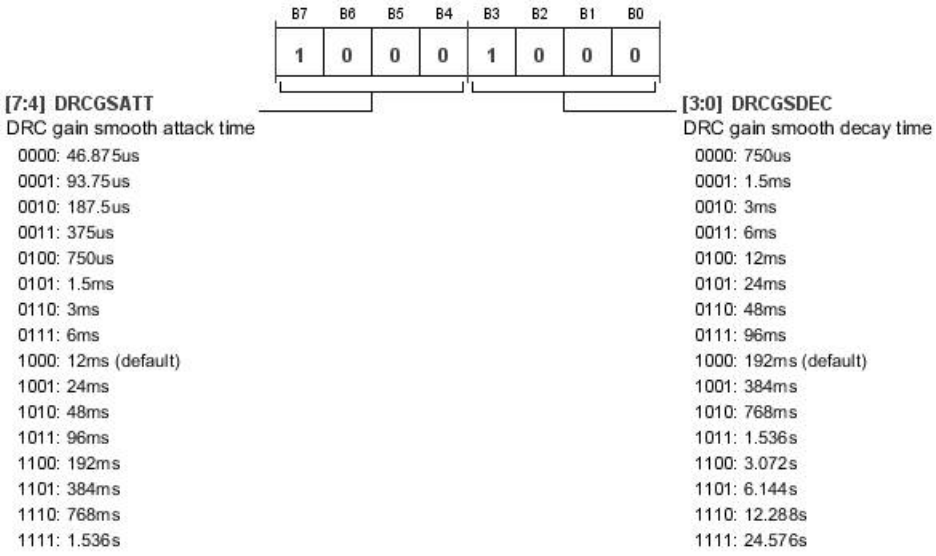


Table 177. Bit Descriptions for DRC2_CTRL11

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DRCGSATT		DRC2 Gain Smooth Attack Time.	0x8	RW
		0000	46.875 µs		
		0001	93.75 µs		
		0010	187.5 µs		
		0011	375 µs		
		0100	750 µs		
		0101	1.5 ms		
		0110	3 ms		
		0111	6 ms		
		1000	12 ms (default)		
		1001	24 ms		
		1010	48 ms		
		1011	96 ms		
		1100	192 ms		
		1101	384 ms		
		1110	768 ms		
		1111	1.536 sec		
[3:0]	DRCGSDEC		DRC Gain Smooth Decay Time.	0x8	RW
		0000	750 µs		
		0001	1.5 ms		
		0010	3 ms		
		0011	6 ms		
		0100	12 ms		
		0101	24 ms		
		0110	48 ms		
		0111	96 ms		
		1000	192 ms (default)		
		1001	384 ms		
		1010	768 ms		
		1011	1.536 sec		
		1100	3.072 sec		
		1101	6.144 sec		
		1110	12.288 sec		
		1111	24.576 sec		

DRC2_CTRL12 REGISTER

Address: 0x9B, Reset: 0x7A, Name: DRC2_CTRL12

DRC2 Noise Gate Hold Time and Normal Operation Hold Time Setting

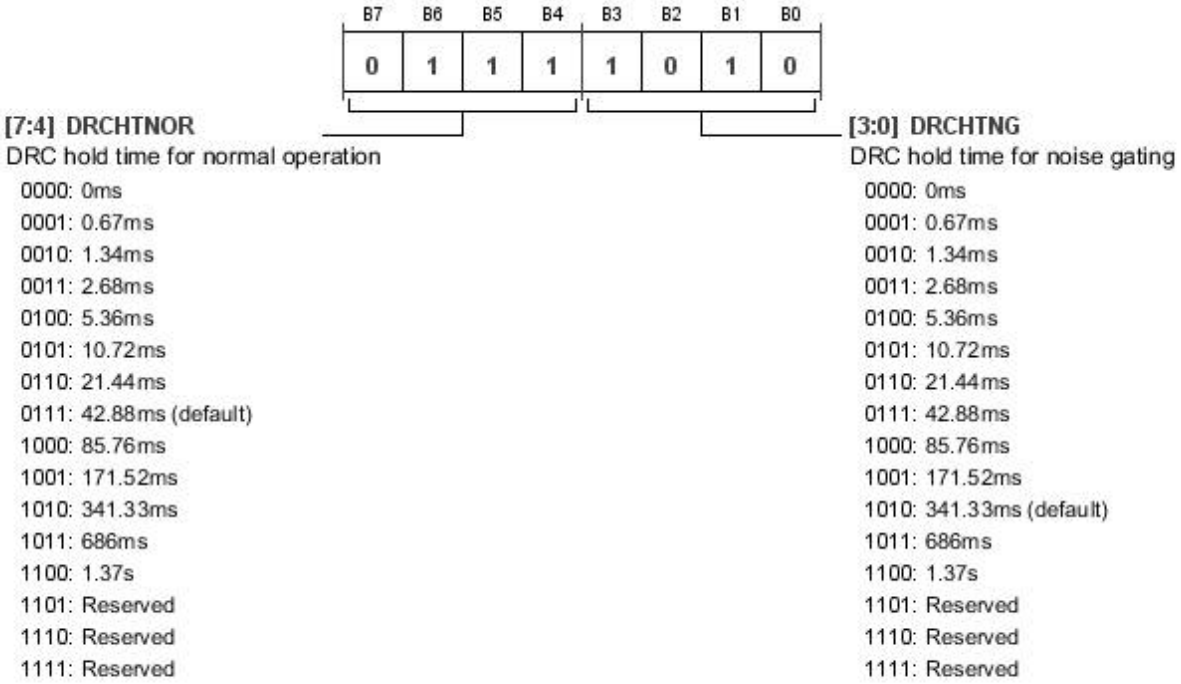


Table 178. Bit Descriptions for DRC2_CTRL12

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DRCHTNOR		DRC2 Hold Time for Normal Operation.	0x7	RW
		0000	0 ms		
		0001	0.67 ms		
		0010	1.34 ms		
		0011	2.68 ms		
		0100	5.36 ms		
		0101	10.72 ms		
		0110	21.44 ms		
		0111	42.88 ms (default)		
		1000	85.76 ms		
		1001	171.52 ms		
		1010	341.33 ms		
		1011	686 ms		
		1100	1.37 sec		
		1101	Reserved		
		1110	Reserved		
		1111	Reserved		
[3:0]	DRCHTNG		DRC2 Hold Time for Noise Gating.	0xA	RW
		0000	0 ms		
		0001	0.67 ms		
		0010	1.34 ms		
		0011	2.68 ms		
		0100	5.36 ms		
		0101	10.72 ms		

Bits	Bit Name	Settings	Description	Reset	Access
		0110	21.44 ms		
		0111	42.88 ms		
		1000	85.76 ms		
		1001	171.52 ms		
		1010	341.33 ms (default)		
		1011	686 ms		
		1100	1.37 sec		
		1101	Reserved		
		1110	Reserved		
		1111	Reserved		

DRC2_CTRL13 REGISTER

Address: 0x9C, Reset: 0xDF, Name: DRC2_CTRL13

DRC2 Gain Setting

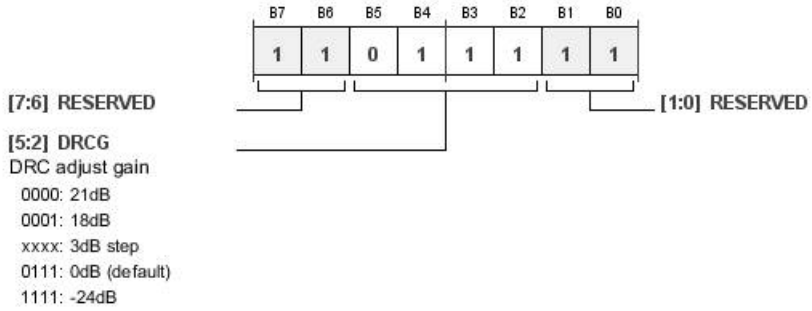


Table 179. Bit Descriptions for DRC2_CTRL13

Bits	Bit Name	Settings	Description	Reset	Access
[5:2]	DRCG		DRC2 Adjust Gain. DRC2 gain.	0x7	RW
		0000	21 dB		
		0001	18 dB		
		xxxx	3 dB step size		
		0111	0 dB (default)		
		1111	−24 dB		

DRC2_CTRL14 REGISTER

Address: 0x9D, Reset: 0x20, Name: DRC2_CTRL14

DRC2 Enable Control

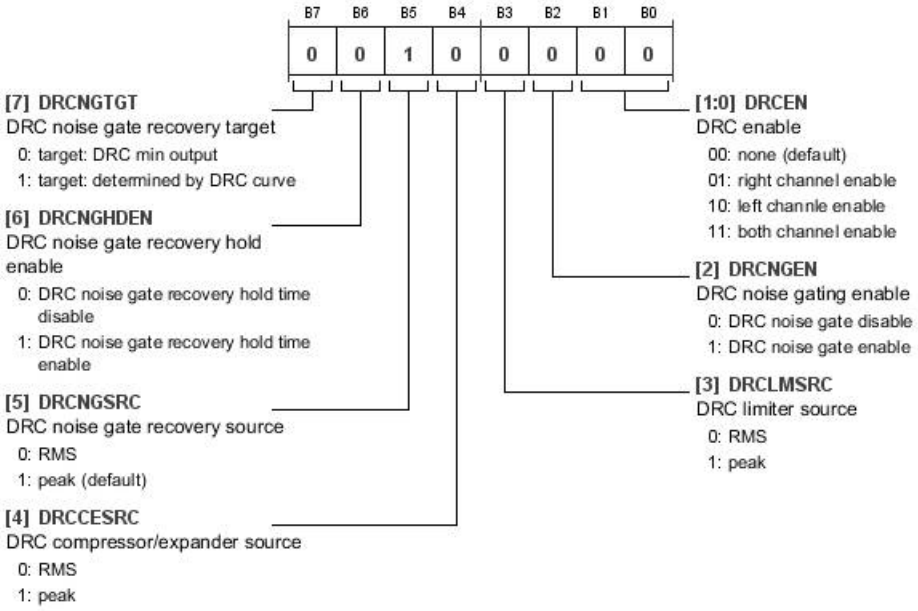


Table 180. Bit Descriptions for DRC2_CTRL14

Bits	Bit Name	Settings	Description	Reset	Access
7	DRCNGTGT		DRC2 Noise Gate Recovery Target.	0x0	RW
		0	Target: DRC minimum output		
		1	Target: determined by DRC curve		
6	DRCNGHDEN		DRC2 Noise Gate Recovery Hold Enable.	0x0	RW
		0	DRC noise gate recovery hold time disable		
		1	DRC noise gate recovery hold time enable		
5	DRCNGSRC		DRC2 Noise Gate Recovery Source.	0x1	RW
		0	RMS		
		1	Peak (default)		
4	DRCCESRC		DRC2 Compressor/Expander Source.	0x0	RW
		0	RMS		
		1	Peak		
3	DRCLMSRC		DRC2 Limiter Source.	0x0	RW
		0	RMS		
		1	Peak		
2	DRCNGEN		DRC2 Noise Gating Enable.	0x0	RW
		0	DRC noise gate disable		
		1	DRC noise gate enable		
[1:0]	DRCEN		DRC2 Enable.	0x0	RW
		00	None (default)		
		01	Right channel enable		
		10	Left channel enable		
		11	Both channels enable		

DRC2_CTRL15 REGISTER

Address: 0x9E, Reset: 0x00, Name: DRC2_CTRL15

DRC2 Peak to RMS Ratio and RMS Detector Setting Register

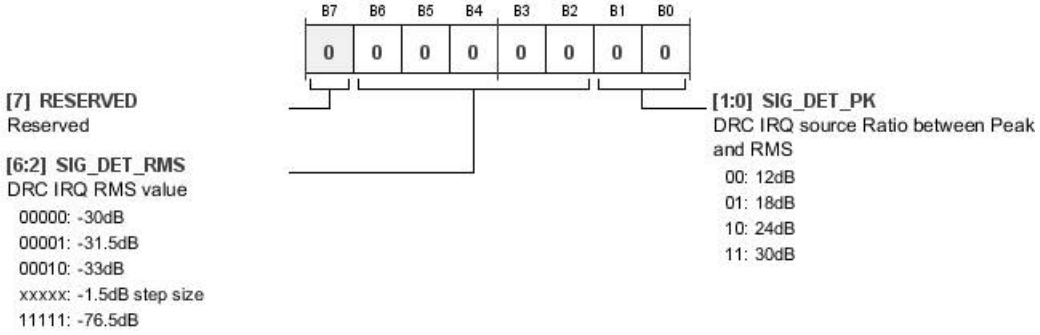


Table 181. Bit Descriptions for DRC2_CTRL15

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
[6:2]	SIG_DET_RMS		DRC2 IRQ RMS Value. DRC rms detector setting.	0x00	RW
		00000	−30 dB		
		00001	−31.5 dB		
		00010	−33 dB		
		xxxxx	−1.5 dB step size		
		11111	−76.5 dB		
[1:0]	SIG_DET_PK		DRC2 IRQ Source Ratio Between Peak and RMS. DRC peak to rms ratio setting.	0x0	RW
		00	12 dB		
		01	18 dB		
		10	24 dB		
		11	30 dB		

DRC2_CTRL16 REGISTER

Address: 0x9F, Reset: 0x00, Name: DRC2_CTRL16

DRC2 IRQ Enable/Disable and IRQ Source Selection Setting Register

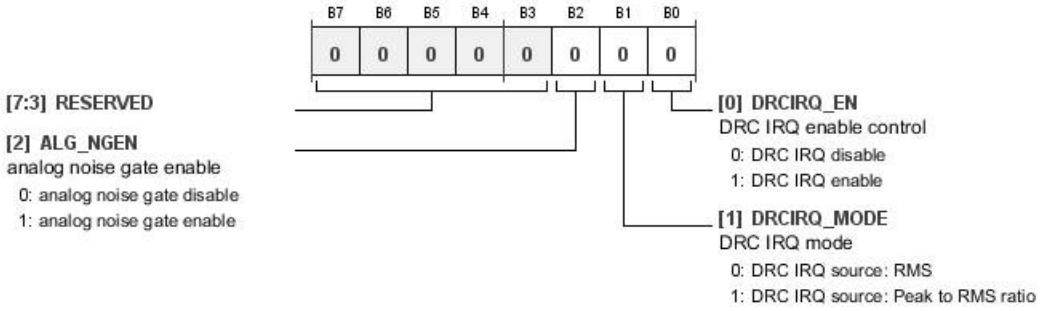


Table 182. Bit Descriptions for DRC2_CTRL16

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	RESERVED			0x00	RW
2	ALG_NGEN		Analog Noise Gate Enable.	0x0	RW
		0	Analog noise gate disable		
		1	Analog noise gate enable		
1	DRCIRQ_MODE		DRC2 IRQ Mode. DRC IRQ source selection setting.	0x0	RW
		0	DRC IRQ source: rms		
		1	DRC IRQ source: peak to rms ratio		
0	DRCIRQ_EN		DRC2 IRQ Enable Control. DRC IRQ enable/disable control.	0x0	RW
		0	DRC IRQ disable		
		1	DRC IRQ enable		

DRC3_CTRL1 REGISTER

Address: 0xA0, Reset: 0x78, Name: DRC3_CTRL1

DRC3 Level Detector Averaging Time and DRC Noise Gate Recovery Time Setting

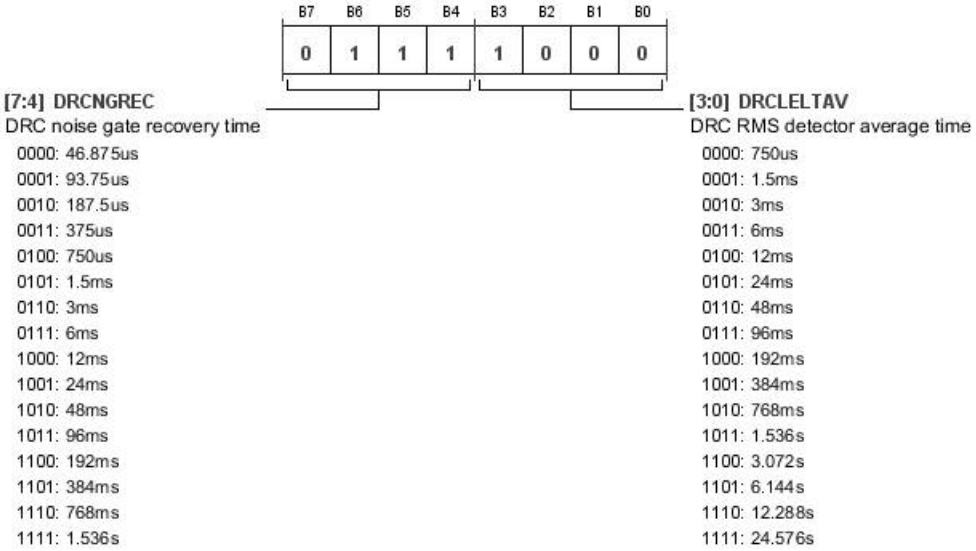


Table 183. Bit Descriptions for DRC3_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DRCNGREC		DRC3 Noise Gate Recovery Time.	0x7	RW
		0000	46.875 µs		
		0001	93.75 µs		
		0010	187.5 µs		
		0011	375 µs		
		0100	750 µs		
		0101	1.5 ms		
		0110	3 ms		
		0111	6 ms		
		1000	12 ms		
		1001	24 ms		
		1010	48 ms		
		1011	96 ms		
		1100	192 ms		
		1101	384 ms		
		1110	768 ms		
		1111	1.536 sec		
[3:0]	DRCLELTAV		DRC3 RMS Detector Average Time.	0x8	RW
		0000	750 µs		
		0001	1.5 ms		
		0010	3 ms		
		0011	6 ms		
		0100	12 ms		
		0101	24 ms		
		0110	48 ms		
		0111	96 ms		
		1000	192 ms		
		1001	384 ms		
		1010	768 ms		

Bits	Bit Name	Settings	Description	Reset	Access
		1011	1.536 sec		
		1100	3.072 sec		
		1101	6.144 sec		
		1110	12.288 sec		
		1111	24.576 sec		

DRC3_CTRL2 REGISTER

Address: 0xA1, Reset: 0x18, Name: DRC3_CTRL2

DRC3 Attack and Decay Time Setting

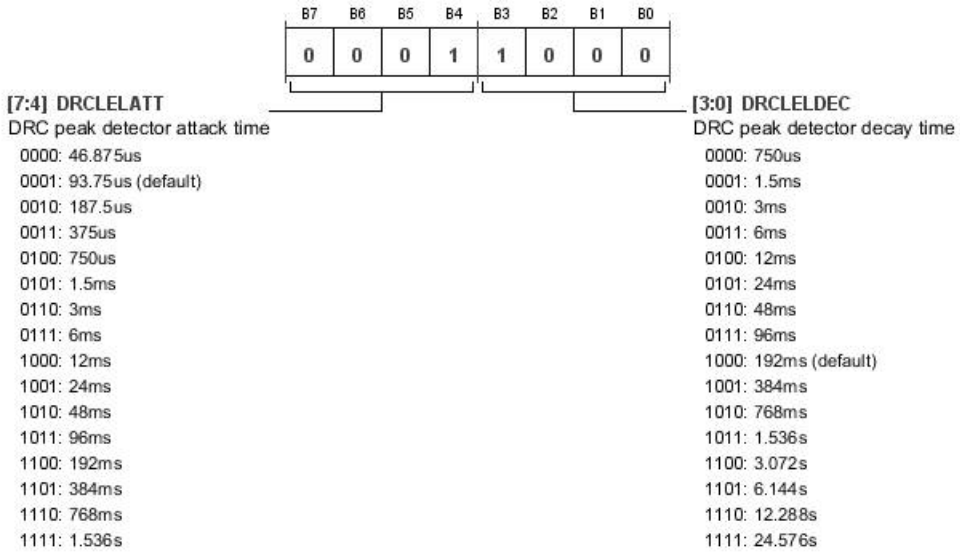


Table 184. Bit Descriptions for DRC3_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DRCLELATT		DRC3 Peak Detector Attack Time.	0x1	RW
		0000	46.875 µs		
		0001	93.75 µs (default)		
		0010	187.5 µs		
		0011	375 µs		
		0100	750 µs		
		0101	1.5 ms		
		0110	3 ms		
		0111	6 ms		
		1000	12 ms		
		1001	24 ms		
		1010	48 ms		
		1011	96 ms		
		1100	192 ms		
		1101	384 ms		
		1110	768 ms		
		1111	1.536 sec		

Bits	Bit Name	Settings	Description	Reset	Access
[3:0]	DRCLELDEC		DRC3 Peak Detector Decay Time.	0x8	RW
		0000	750 µs		
		0001	1.5 ms		
		0010	3 ms		
		0011	6 ms		
		0100	12 ms		
		0101	24 ms		
		0110	48 ms		
		0111	96 ms		
		1000	192 ms (default)		
		1001	384 ms		
		1010	768 ms		
		1011	1.536 sec		
		1100	3.072 sec		
		1101	6.144 sec		
		1110	12.288 sec		
		1111	24.576 sec		

DRC3_CTRL3 REGISTER

Address: 0xA2, Reset: 0x00, Name: DRC3_CTRL3

DRC3 Threshold Point X1 on X-Axis (Input Level)

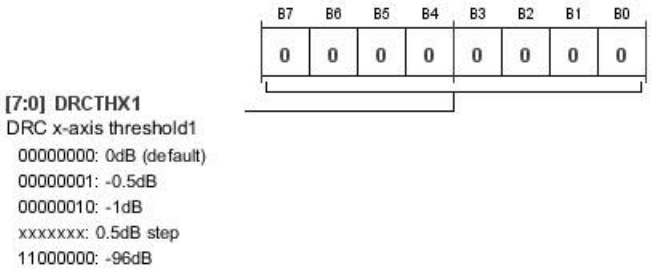


Table 185. Bit Descriptions for DRC3_CTRL3

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHX1		DRC3 X-Axis Threshold 1.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxxx	0.5 dB step		
		11000000	−96 dB		

DRC3_CTRL4 REGISTER

Address: 0xA3, Reset: 0x00, Name: DRC3_CTRL4

DRC3 Threshold Point X2 on X-Axis (Input Level)

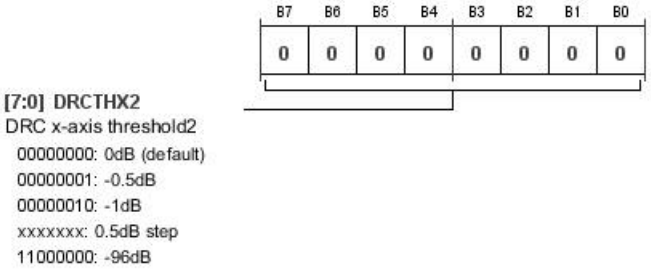


Table 186. Bit Descriptions for DRC3_CTRL4

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHX2		DRC3 X-Axis Threshold 2.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxxx	0.5 dB step		
		11000000	−96 dB		

DRC3_CTRL5 REGISTER

Address: 0xA4, Reset: 0x00, Name: DRC3_CTRL5

DRC3 Threshold Point X3 on X-Axis (Input Level)

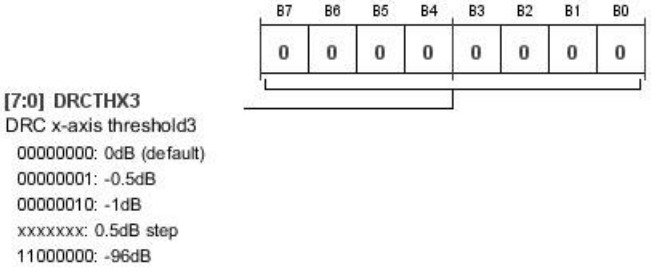


Table 187. Bit Descriptions for DRC3_CTRL5

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHX3		DRC3 X-Axis Threshold 3.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxxx	0.5 dB step		
		11000000	−96 dB		

DRC3_CTRL6 REGISTER

Address: 0xA5, Reset: 0xC0, Name: DRC3_CTRL6

DRC3 Threshold Point X4 on X-Axis (Input Level)

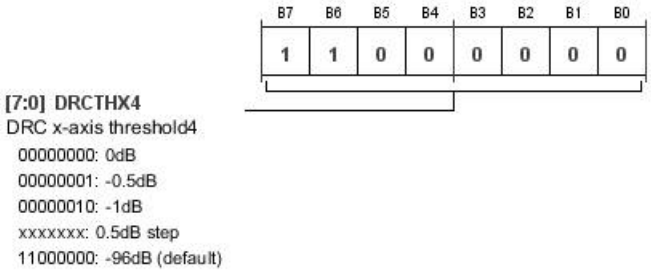


Table 188. Bit Descriptions for DRC3_CTRL6

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHX4		DRC3 X-Axis Threshold 4.	0xC0	RW
		00000000	0 dB		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxxx	0.5 dB step		
		11000000	−96 dB (default)		

DRC3_CTRL7 REGISTER

Address: 0xA6, Reset: 0x00, Name: DRC3_CTRL7

DRC3 Threshold Point Y1 on Y-Axis (Output Level)

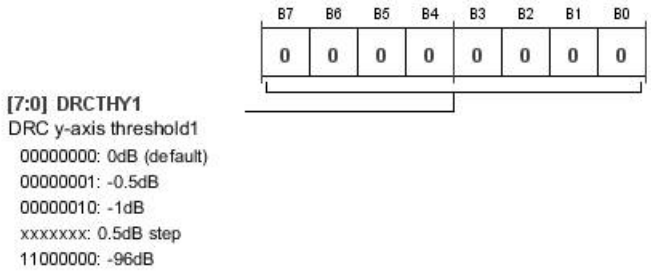


Table 189. Bit Descriptions for DRC3_CTRL7

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHY1		DRC3 Y-Axis Threshold 1.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxxx	0.5 dB step		
		11000000	−96 dB		

DRC3_CTRL8 REGISTER

Address: 0xA7, Reset: 0x00, Name: DRC3_CTRL8

DRC3 Threshold Point Y2 on Y-Axis (Output Level)

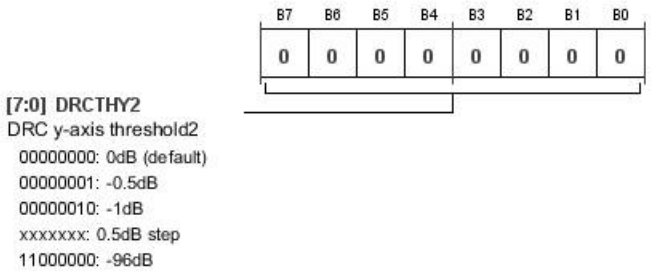


Table 190. Bit Descriptions for DRC3_CTRL8

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHY2		DRC3 Y-Axis Threshold 2.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxxx	0.5 dB step		
		11000000	−96 dB		

DRC3_CTRL9 REGISTER

Address: 0xA8, Reset: 0x00, Name: DRC3_CTRL9

DRC3 Threshold Point Y3 on Y-Axis (Output Level)

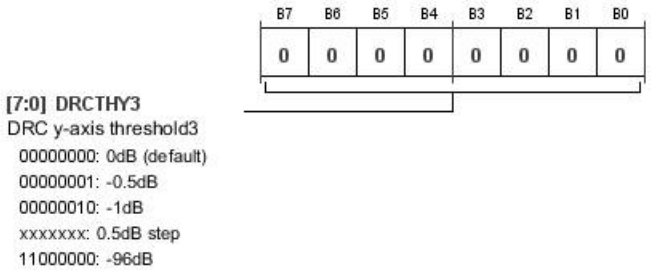


Table 191. Bit Descriptions for DRC3_CTRL9

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHY3		DRC3 Y-Axis Threshold 3.	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxxx	0.5 dB step		
		11000000	−96 dB		

DRC3_CTRL10 REGISTER

Address: 0xA9, Reset: 0xC0, Name: DRC3_CTRL10

DRC3 Threshold Point Y4 on Y-Axis (Output Level)

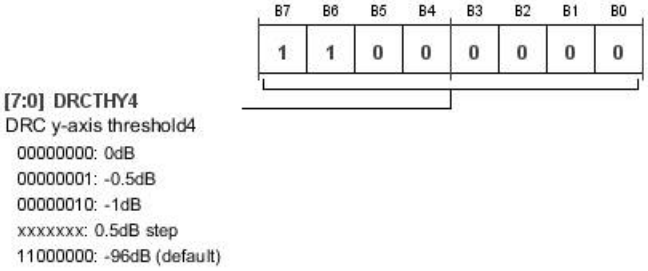


Table 192. Bit Descriptions for DRC3_CTRL10

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DRCTHY4		DRC3 Y-Axis Threshold 4.	0xC0	RW
		00000000	0 dB		
		00000001	−0.5 dB		
		00000010	−1 dB		
		xxxxxxxx	0.5 dB step		
		11000000	−96 dB (default)		

DRC3_CTRL11 REGISTER

Address: 0xAA, Reset: 0x88, Name: DRC3_CTRL11

DRC3 Gain Smoothing Attack and Decay Time Setting

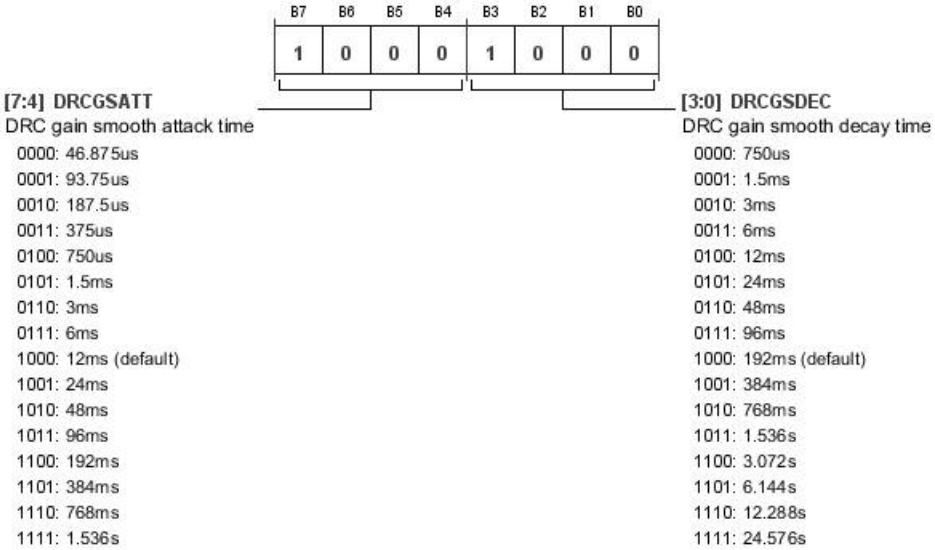


Table 193. Bit Descriptions for DRC3_CTRL11

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DRCGSATT		DRC3 Gain Smooth Attack Time.	0x8	RW
		0000	46.875 µs		
		0001	93.75 µs		
		0010	187.5 µs		
		0011	375 µs		
		0100	750 µs		
		0101	1.5 ms		
		0110	3 ms		
		0111	6 ms		
		1000	12 ms (default)		
		1001	24 ms		
		1010	48 ms		
		1011	96 ms		
		1100	192 ms		
		1101	384 ms		
		1110	768 ms		
		1111	1.536 sec		
[3:0]	DRCGSDEC		DRC3 Gain Smooth Decay Time.	0x8	RW
		0000	750 µs		
		0001	1.5 ms		
		0010	3 ms		
		0011	6 ms		
		0100	12 ms		
		0101	24 ms		
		0110	48 ms		
		0111	96 ms		
		1000	192 ms (default)		
		1001	384 ms		
		1010	768 ms		
		1011	1.536 sec		
		1100	3.072 sec		
		1101	6.144 sec		
		1110	12.288 sec		
		1111	24.576 sec		

DRC3_CTRL12 REGISTER

Address: 0xAB, Reset: 0x7A, Name: DRC3_CTRL12

DRC3 Noise Gate Hold Time and Normal Operation Hold Time Setting

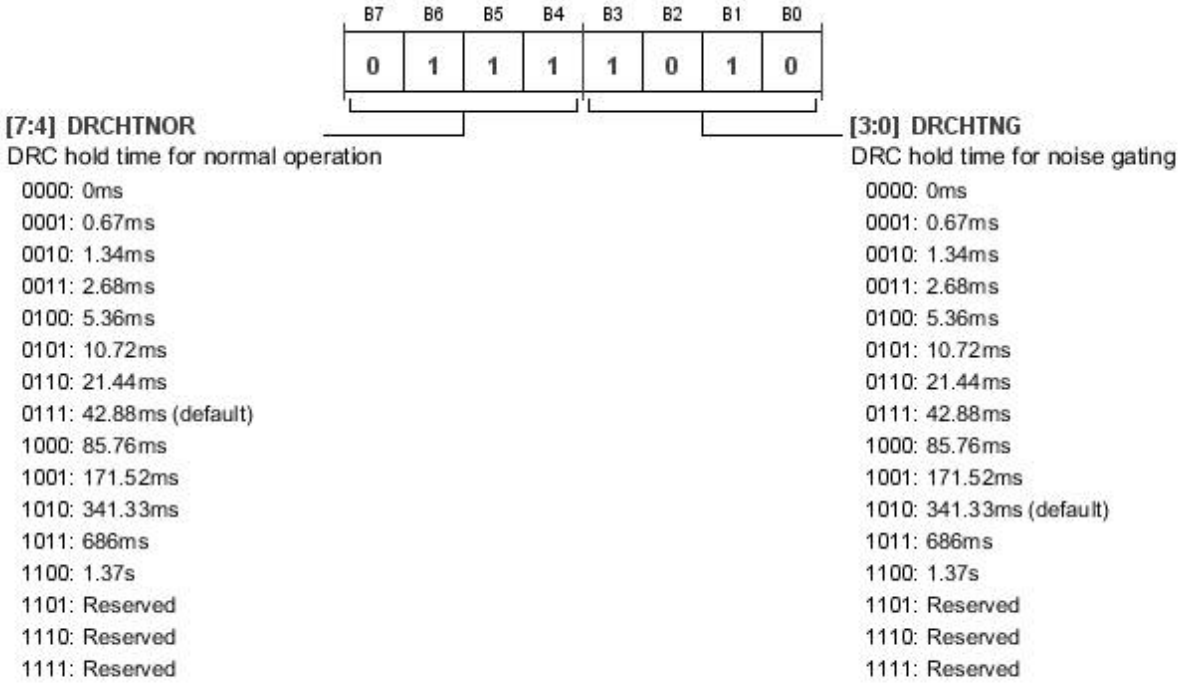


Table 194. Bit Descriptions for DRC3_CTRL12

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DRCHTNOR		DRC3 Hold Time for Normal Operation.	0x7	RW
		0000	0 ms		
		0001	0.67 ms		
		0010	1.34 ms		
		0011	2.68 ms		
		0100	5.36 ms		
		0101	10.72 ms		
		0110	21.44 ms		
		0111	42.88 ms (default)		
		1000	85.76 ms		
		1001	171.52 ms		
		1010	341.33 ms		
		1011	686 ms		
		1100	1.37 sec		
		1101	Reserved		
		1110	Reserved		
		1111	Reserved		
[3:0]	DRCHTNG		DRC3 Hold Time for Noise Gating.	0xA	RW
		0000	0 ms		
		0001	0.67 ms		
		0010	1.34 ms		
		0011	2.68 ms		
		0100	5.36 ms		
		0101	10.72 ms		

Bits	Bit Name	Settings	Description	Reset	Access
		0110	21.44 ms		
		0111	42.88 ms		
		1000	85.76 ms		
		1001	171.52 ms		
		1010	341.33 ms (default)		
		1011	686 ms		
		1100	1.37 sec		
		1101	Reserved		
		1110	Reserved		
		1111	Reserved		

DRC3_CTRL13 REGISTER

Address: 0xAC, Reset: 0xDF, Name: DRC3_CTRL13

DRC3 Gain Setting

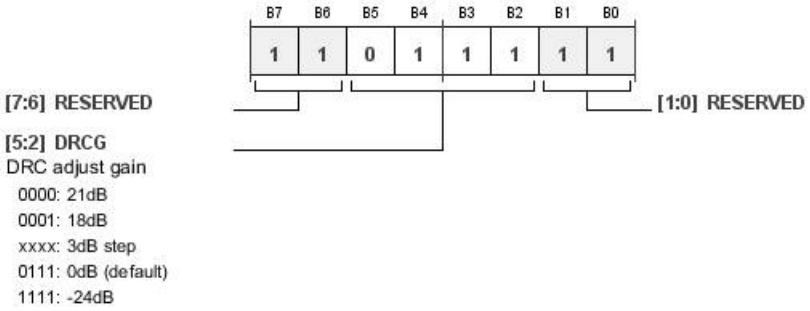


Table 195. Bit Descriptions for DRC3_CTRL13

Bits	Bit Name	Settings	Description	Reset	Access
[5:2]	DRCG		DRC3 Adjust Gain. DRC3 gain setting.	0x7	RW
		0000	21 dB		
		0001	18 dB		
		xxxx	3 dB step		
		0111	0 dB (default)		
		1111	−24 dB		

DRC3_CTRL14 REGISTER

Address: 0xAD, Reset: 0x20, Name: DRC3_CTRL14

DRC3 Enable Control

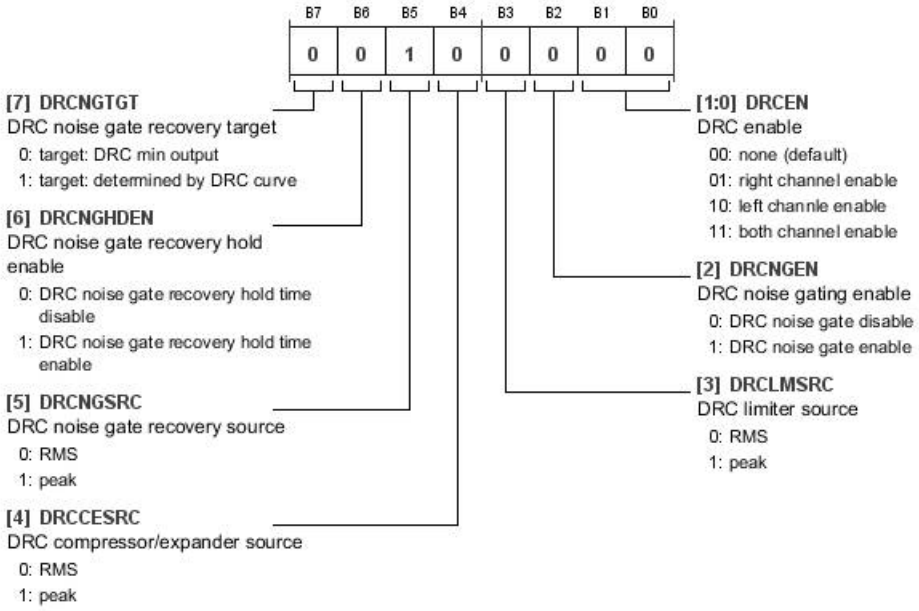


Table 196. Bit Descriptions for DRC3_CTRL14

Bits	Bit Name	Settings	Description	Reset	Access
7	DRCNGTGT		DRC3 Noise Gate Recovery Target.	0x0	RW
		0	Target: DRC minimum output		
		1	Target: determined by DRC curve		
6	DRCNGHDEN		DRC3 Noise Gate Recovery Hold Enable.	0x0	RW
		0	DRC noise gate recovery hold time disable		
		1	DRC noise gate recovery hold time enable		
5	DRCNGSRC		DRC3 Noise Gate Recovery Source.	0x1	RW
		0	RMS		
		1	Peak (default)		
4	DRCCESRC		DRC3 Compressor/Expander Source.	0x0	RW
		0	RMS		
		1	Peak		
3	DRCLMSRC		DRC3 Limiter Source.	0x0	RW
		0	RMS		
		1	Peak		
2	DRCNGEN		DRC3 Noise Gating Enable.	0x0	RW
		0	DRC noise gate disable		
		1	DRC noise gate enable		
[1:0]	DRCEN		DRC3 Enable.	0x0	RW
		00	None (default)		
		01	Right channel enable		
		10	Left channel enable		
		11	Both channels enable		

DRC3_CTRL15 REGISTER

Address: 0xAE, Reset: 0x00, Name: DRC3_CTRL15

DRC3 Peak to RMS Ratio and RMS Detector Setting Register

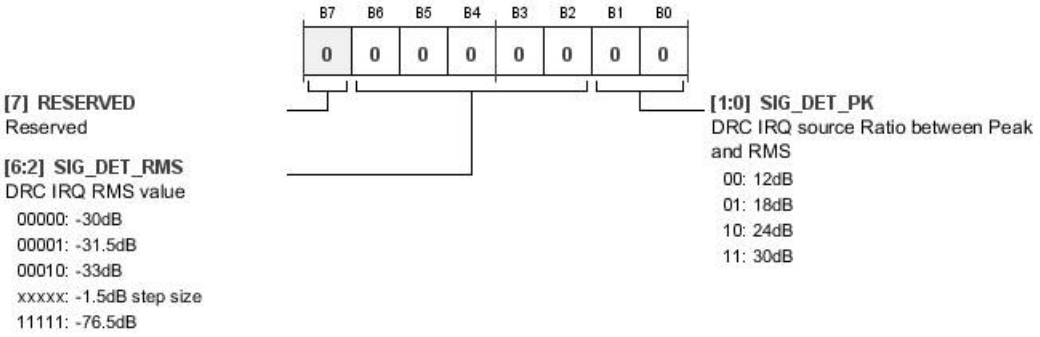


Table 197. Bit Descriptions for DRC3_CTRL15

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
[6:2]	SIG_DET_RMS		DRC3 IRQ RMS Value. DRC rms detector setting.	0x00	RW
		00000	−30 dB		
		00001	−31.5 dB		
		00010	−33 dB		
		xxxxx	−1.5 dB step size		
		11111	−76.5 dB		
[1:0]	SIG_DET_PK		DRC3 IRQ Source Ratio Between Peak and RMS. DRC peak to rms ratio setting.	0x0	RW
		00	12 dB		
		01	18 dB		
		10	24 dB		
		11	30 dB		

DRC3_CTRL16 REGISTER

Address: 0xAF, Reset: 0x00, Name: DRC3_CTRL16

DRC3 IRQ Enable/Disable and IRQ Source Selection Setting Register

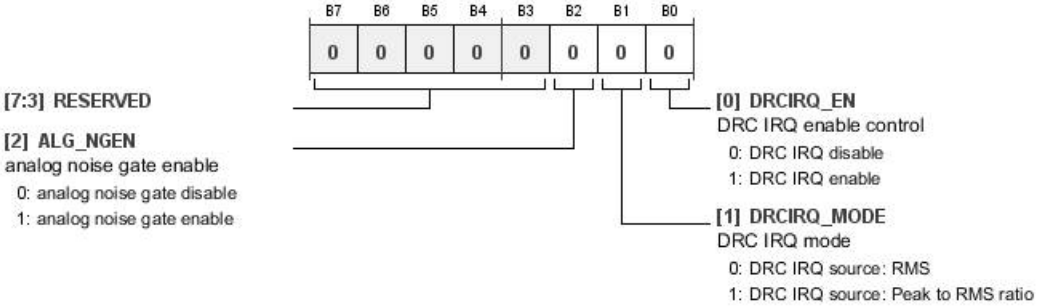


Table 198. Bit Descriptions for DRC3_CTRL16

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	RESERVED		Reserved.	0x00	RW
2	ALG_NGEN		Analog Noise Gate Enable.	0x0	RW
		0	Analog noise gate disable		
		1	Analog noise gate enable		
1	DRCIRQ_MODE		DRC IRQ Mode. DRC IRQ source selection setting.	0x0	RW
		0	DRC IRQ source: rms		
		1	DRC IRQ source: Peak to rms ratio		
0	DRCIRQ_EN		DRC IRQ Enable Control. DRC IRQ enable/disable control.	0x0	RW
		0	DRC IRQ disable		
		1	DRC IRQ enable		

MDRC_PRE_FILTER REGISTER

Address: 0xB0, Reset: 0x00, Name: MDRC_PRE_FILTER

MDRC Low-Pass and High-Pass Filter Setting

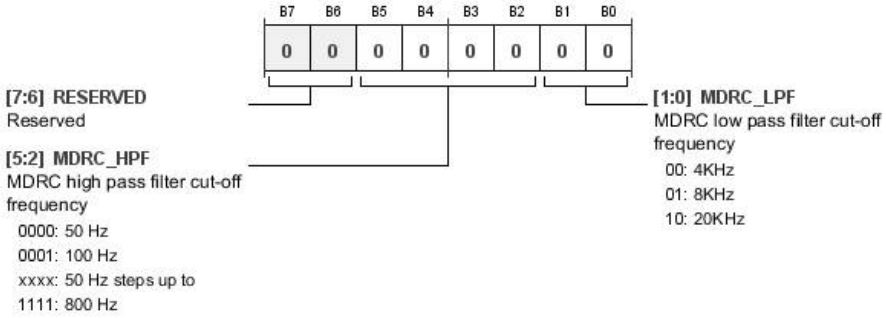


Table 199. Bit Descriptions for MDRC_PRE_FILTER

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	RW
[5:2]	MDRC_HPF		MDRC High-Pass Filter Cutoff Frequency.	0x0	RW
		0000	50 Hz		
		0001	100 Hz		
		xxxx	50 Hz step size		
		1111	800 Hz		
[1:0]	MDRC_LPF		MDRC Low-Pass Filter Cutoff Frequency.	0x0	RW
		00	4 kHz		
		01	8 kHz		
		10	20 kHz		

MDRC_SPL_CTRL (SPLITTER FREQUENCIES) REGISTER

Address: 0xB1, Reset: 0x00, Name: MDRC_SPL_CTRL

MDRC Band Splitting Crossover Frequency Setting

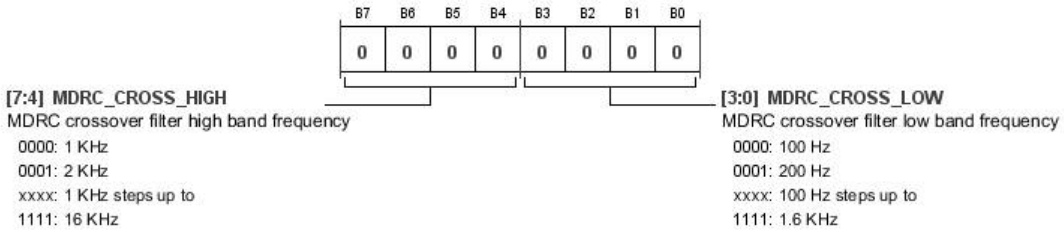


Table 200. Bit Descriptions for MDRC_SPL_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	MDRC_CROSS_HIGH		MDRC Crossover Filter High Band Frequency.	0x0	RW
		0000	1 kHz		
		0001	2 kHz		
		xxxx	1 kHz step size		
		1111	16 kHz		
[3:0]	MDRC_CROSS_LOW		MDRC Crossover Filter Low Band Frequency.	0x0	RW
		0000	100 Hz		
		0001	200 Hz		
		xxxx	100 Hz step size		
		1111	1.6 kHz		

MDRC_CTRL REGISTER

Address: 0xB2, Reset: 0x00, Name: MDRC_CTRL

MDRC Enable Setting

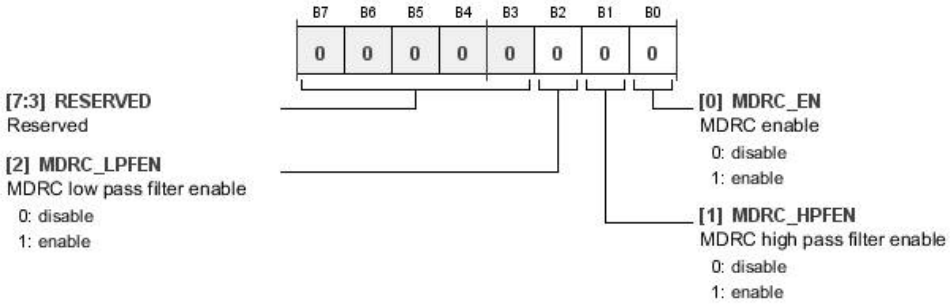


Table 201. Bit Descriptions for MDRC_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	RESERVED		Reserved	0x00	RW
2	MDRC_LPFEN		MDRC Low-Pass Filter Enable.	0x0	RW
		0	Disable		
		1	Enable		
1	MDRC_HPFEN		MDRC High-Pass Filter Enable.	0x0	RW
		0	Disable		
		1	Enable		
0	MDRC_EN		MDRC Enable.	0x0	RW
		0	Disable		
		1	Enable		

PRE_HPF1_COEFH (MSB) REGISTER

Address: 0xB3, Reset: 0xFF, Name: PRE_HPF1_COEFH

High-Pass Filter 1 Coefficient MSB

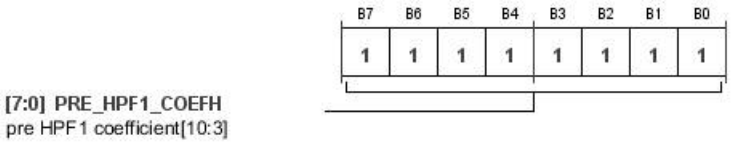


Table 202. Bit Descriptions for PRE_HPF1_COEFH

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PRE_HPF1_COEFH		Pre-HPF1 Coefficient[10:3].	0xFF	RW

PRE_HPF1_COEFL (LSB) REGISTER

Address: 0xB4, Reset: 0xFF, Name: PRE_HPF1_COEFL

High-Pass Filter 1 Coefficient LSB

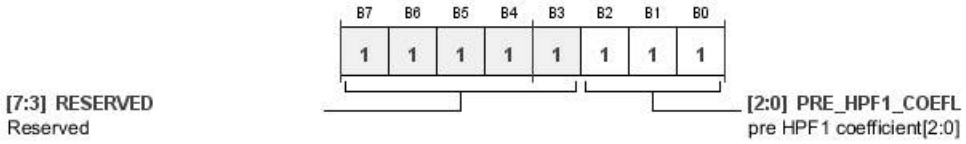


Table 203. Bit Descriptions for PRE_HPF1_COEFL

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	RESERVED		Reserved.	0x1F	RW
[2:0]	PRE_HPF1_COEFL		Pr-HPF1 Coefficient[2:0].	0x7	RW

PRE_HPF2_COEFH (MSB) REGISTER

Address: 0xB5, Reset: 0xFF, Name: PRE_HPF2_COEFH

High-Pass Filter 2 Coefficient MSB

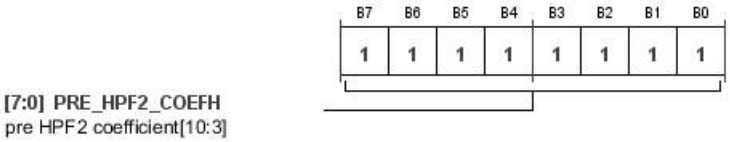


Table 204. Bit Descriptions for PRE_HPF2_COEFH

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PRE_HPF2_COEFH		Pre-HPF2 Coefficient[10:3].	0xFF	RW

PRE_HPF2_COEFL (LSB) REGISTER

Address: 0xB6, Reset: 0xFF, Name: PRE_HPF2_COEFL

High-Pass Filter 2 Coefficient LSB

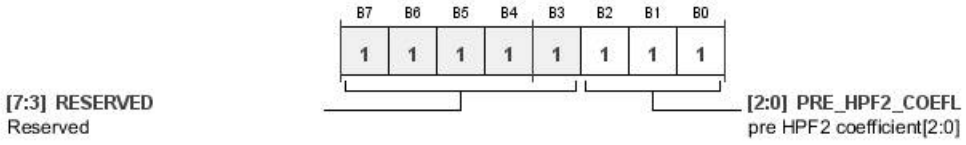


Table 205. Bit Descriptions for PRE_HPF2_COEFL

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	RESERVED		Reserved.	0x1F	RW
[2:0]	PRE_HPF2_COEFL		Pre-HPF2 Coefficient[2:0].	0x7	RW

PRE_HPF3_COEFH (MSB) REGISTER

Address: 0xB7, Reset: 0xFF, Name: PRE_HPF3_COEFH

High-Pass Filter 3 Coefficient MSB

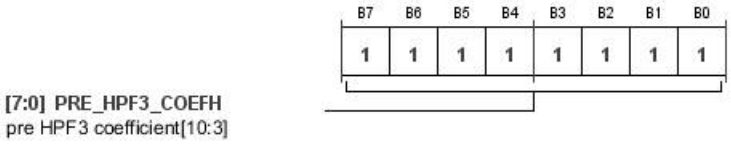


Table 206. Bit Descriptions for PRE_HPF3_COEFH

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PRE_HPF3_COEFH		Pre-HPF3 Coefficient[10:3].	0xFF	RW

PRE_HPF3_COEFL (LSB) REGISTER

Address: 0xB8, Reset: 0xFF, Name: PRE_HPF3_COEFL

High-Pass Filter 3 Coefficient LSB

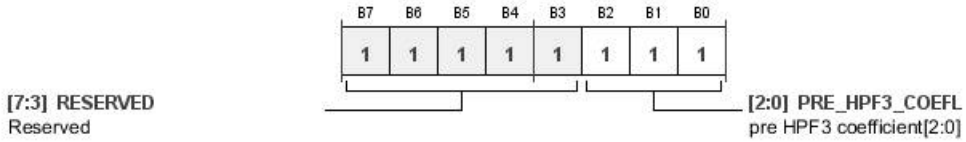


Table 207. Bit Descriptions for PRE_HPF3_COEFL

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	RESERVED		Reserved.	0x1F	RW
[2:0]	PRE_HPF3_COEFL		Pre-HPF3 Coefficient[2:0].	0x7	RW

PRE_HPF4_COEFH (MSB) REGISTER

Address: 0xB9, Reset: 0xFF, Name: PRE_HPF4_COEFH

High-Pass Filter 4 Coefficient MSB

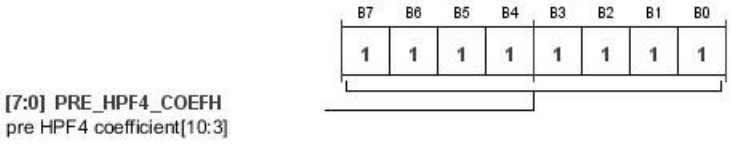


Table 208. Bit Descriptions for PRE_HPF4_COEFH

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PRE_HPF4_COEFH		Pre-HPF4 Coefficient[10:3].	0xFF	RW

PRE_HPF4_COEFL (LSB) REGISTER

Address: 0xBA, Reset: 0xFF, Name: PRE_HPF4_COEFL

High-Pass Filter 4 Coefficient LSB

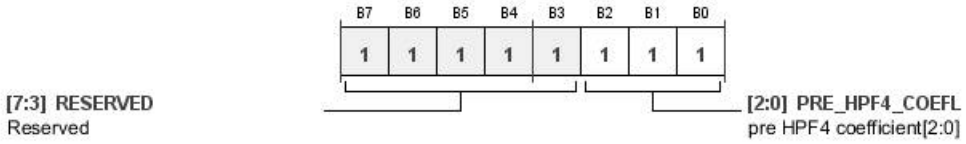


Table 209. Bit Descriptions for PRE_HPF4_COEFL

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	RESERVED		Reserved.	0x1F	RW
[2:0]	PRE_HPF4_COEFL		Pre-HPF4 Coefficient[2:0].	0x7	RW

PRE_HPF5_COEFH (MSB) REGISTER

Address: 0xBB, Reset: 0xFF, Name: PRE_HPF5_COEFH

High-Pass Filter 5 Coefficient MSB

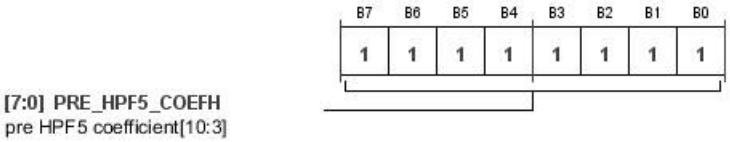


Table 210. Bit Descriptions for PRE_HPF5_COEFH

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PRE_HPF5_COEFH		Pre-HPF5 Coefficient[10:3].	0xFF	RW

PRE_HPF5_COEFL (LSB) REGISTER

Address: 0xBC, Reset: 0xFF, Name: PRE_HPF5_COEFL

High-Pass Filter 5 Coefficient LSB

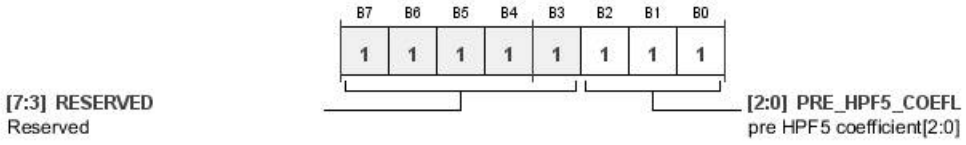


Table 211. Bit Descriptions for PRE_HPF5_COEFL

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	RESERVED		Reserved.	0x1F	RW
[2:0]	PRE_HPF5_COEFL		Pre-HPF5 Coefficient[2:0].	0x7	RW

PRE_HPF_CTRL REGISTER

Address: 0xBD, Reset: 0x1F, Name: PRE_HPF_CTRL

High-Pass Filter 1 Through High-Pass Filter 4 Enable Control

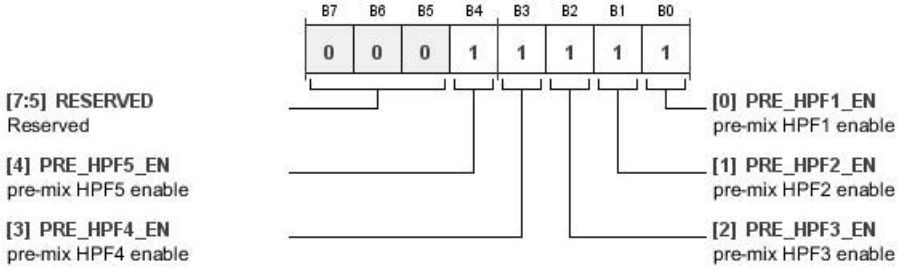


Table 212. Bit Descriptions for PRE_HPF_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
4	PRE_HPF5_EN		Pre-Mix HPF5 Enable.	0x1	RW
3	PRE_HPF4_EN		Pre-Mix HPF4 Enable.	0x1	RW
2	PRE_HPF3_EN		Pre-Mix HPF3 Enable.	0x1	RW
1	PRE_HPF2_EN		Pre-Mix HPF2 Enable.	0x1	RW
0	PRE_HPF1_EN		Pre-Mix HPF1 Enable.	0x1	RW

EQ_CTRL1 REGISTER

Address: 0xBE, Reset: 0x00, Name: EQ_CTRL1

Equalizer Control

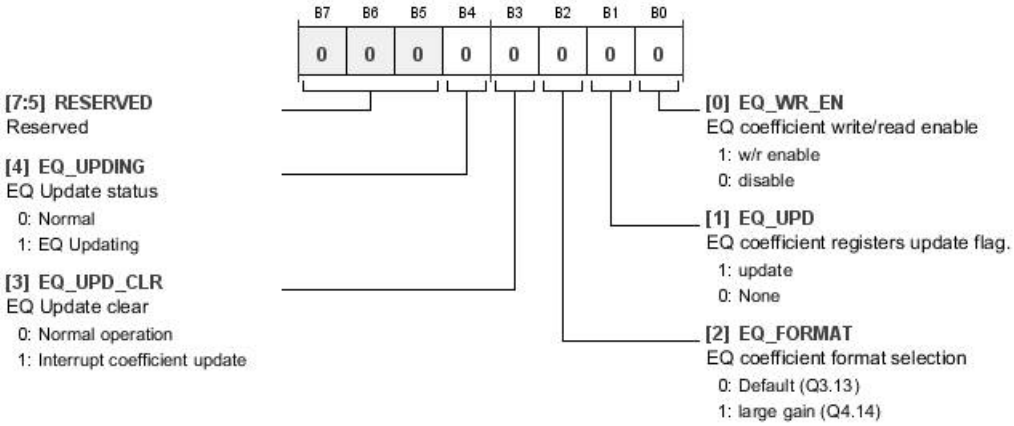


Table 213. Bit Descriptions for EQ_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
4	EQ_UPDING		EQ Update Status.	0x0	R
		0	Normal		
		1	EQ updating		
3	EQ_UPD_CLR		EQ Update Clear. Equalizer update clear.	0x0	R
		0	Normal operation		
		1	Interrupt coefficient update		
2	EQ_FORMAT		EQ Coefficient Format Selection. Equalizer coefficient format selection.	0x0	RW
		0	Default (Q3.13)		
		1	Large gain (Q4.14)		
1	EQ_UPD		EQ Coefficient Registers Update Flag. Equalizer coefficient registers update status.	0x0	R
		1	Update		
		0	None		
0	EQ_WR_EN		EQ Coefficient Write/Read Enable. Equalizer coefficient registers update status.	0x0	RW
		1	W/R enable		
		0	Disable		

EQ_CTRL2 REGISTER

Address: 0xBF, Reset: 0x00, Name: EQ_CTRL2

Equalizer Control

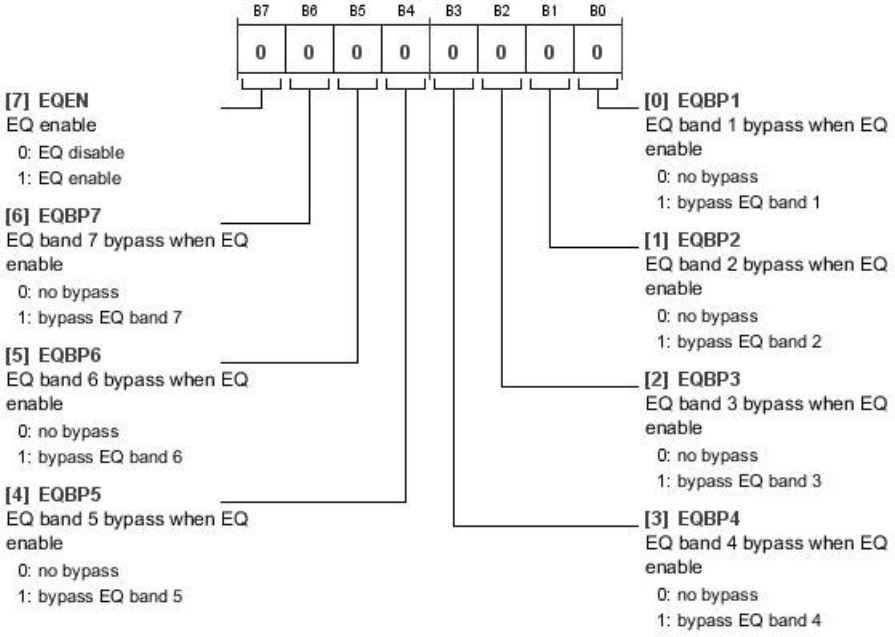


Table 214. Bit Descriptions for EQ_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
7	EQEN		EQ Enable. Equalizer enable/disable control.	0x0	RW
		0	EQ disable		
		1	EQ enable		
6	EQBP7		EQ Band 7 Bypass When EQ Enabled. Equalizer 7 bypass control.	0x0	RW
		0	No bypass		
		1	Bypass EQ Band 7		
5	EQBP6		EQ Band 6 Bypass When EQ Enabled. Equalizer 6 bypass control.	0x0	RW
		0	No bypass		
		1	Bypass EQ Band 6		
4	EQBP5		EQ Band 5 Bypass When EQ Enabled. Equalizer 5 bypass control.	0x0	RW
		0	No bypass		
		1	Bypass EQ Band 5		
3	EQBP4		EQ Band 4 Bypass When EQ Enabled. Equalizer 4 bypass control.	0x0	RW
		0	No bypass		
		1	Bypass EQ Band 4		
2	EQBP3		EQ Band 3 Bypass When EQ Enabled. Equalizer 3 bypass control.	0x0	RW
		0	No bypass		
		1	Bypass EQ Band 3		
1	EQBP2		EQ Band 2 Bypass When EQ Enabled. Equalizer 2 bypass control.	0x0	RW
		0	No bypass		
		1	Bypass EQ Band 2		
0	EQBP1		EQ Band 1 Bypass When EQ Enabled. Equalizer 1 bypass control.	0x0	RW
		0	No bypass		
		1	Bypass EQ Band 1		

E3D_CTRL1 REGISTER

Address: 0xC0, Reset: 0x00, Name: E3D_CTRL1

3D Enhancement Control Register

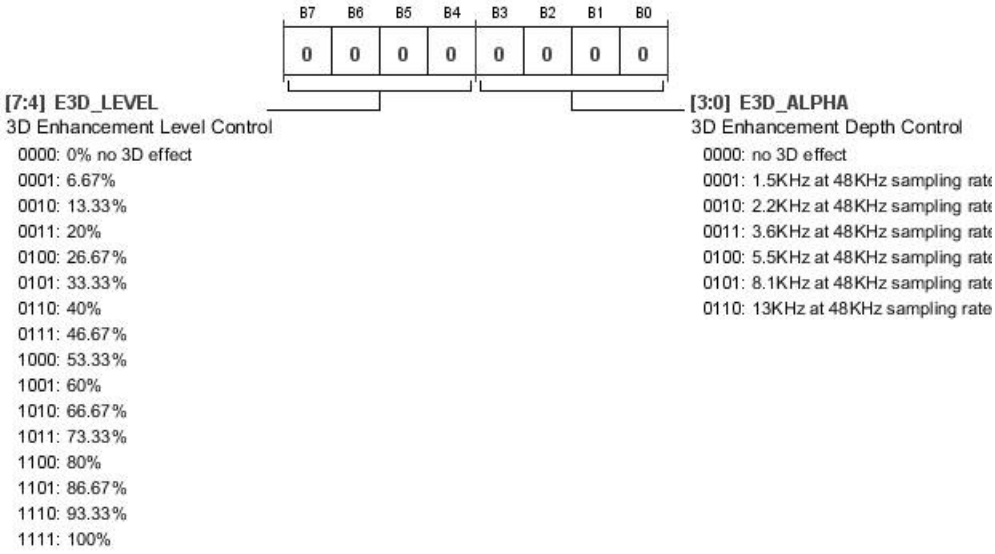


Table 215. Bit Descriptions for E3D_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	E3D_LEVEL		3D Enhancement Level Control. 3D effect level setting for 3D enhancement.	0x0	RW
		0000	0%; no 3D effect		
		0001	6.67%		
		0010	13.33%		
		0011	20%		
		0100	26.67%		
		0101	33.33%		
		0110	40%		
		0111	46.67%		
		1000	53.33%		
		1001	60%		
		1010	66.67%		
		1011	73.33%		
		1100	80%		
		1101	86.67%		
		1110	93.33%		
		1111	100%		
[3:0]	E3D_ALPHA		3D Enhancement Depth Control. Filter cutoff frequency setting for 3D enhancement.	0x0	RW
		0000	No 3D effect		
		0001	1.5 kHz at 48 kHz sampling rate		
		0010	2.2 kHz at 48 kHz sampling rate		
		0011	3.6 kHz at 48 kHz sampling rate		
		0100	5.5 kHz at 48 kHz sampling rate		
		0101	8.1 kHz at 48 kHz sampling rate		
		0110	13 kHz at 48 kHz sampling rate		

E3D_CTRL2 REGISTER

Address: 0xC1, Reset: 0x00, Name: E3D_CTRL2

3D Enhancement Control Register

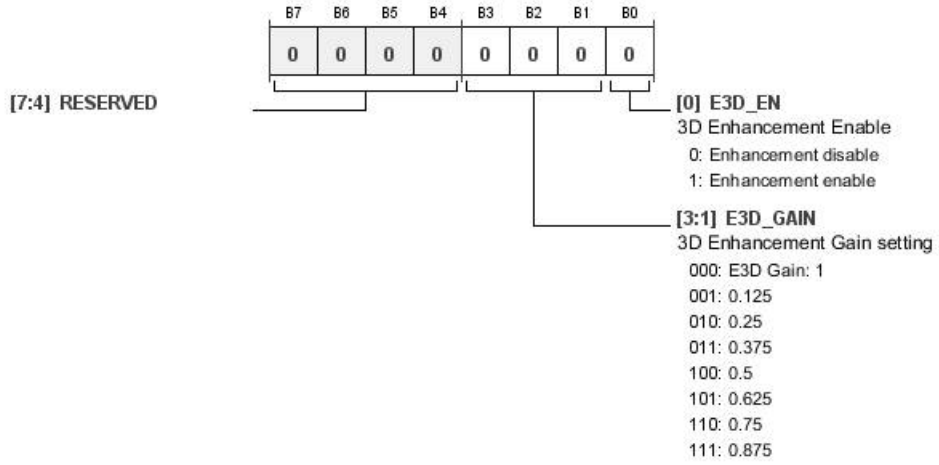


Table 216. Bit Descriptions for E3D_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved.	0x0	RW
[3:1]	E3D_GAIN		3D Enhancement Gain Setting.	0x0	RW
		000	E3D Gain: 1		
		001	0.125		
		010	0.25		
		011	0.375		
		100	0.5		
		101	0.625		
		110	0.75		
		111	0.875		
0	E3D_EN		3D Enhancement Enable. 3D enhancement enable/disable control.	0x0	RW
		0	Enhancement disable		
		1	Enhancement enable		

ALC_CTRL0 REGISTER

Address: 0xC2, Reset: 0x00, Name: ALC_CTRL0

ALC Control Register

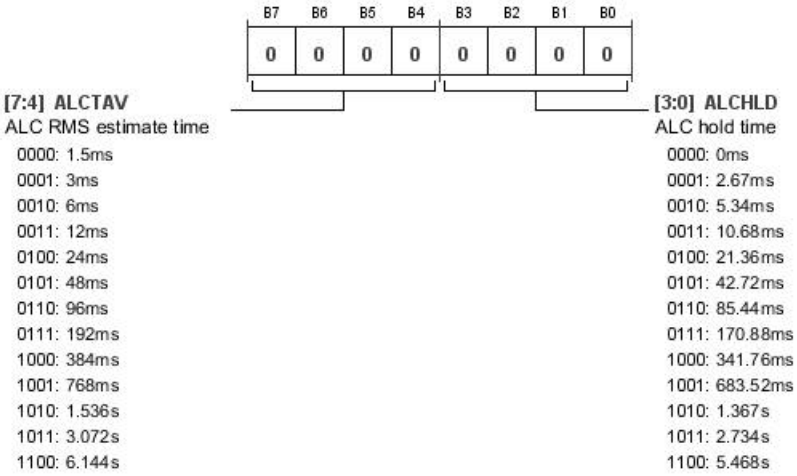


Table 217. Bit Descriptions for ALC_CTRL0

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	ALCTAV		ALC RMS Estimate Time. ALC average time setting for rms value estimation.	0x0	RW
		0000	1.5 ms		
		0001	3 ms		
		0010	6 ms		
		0011	12 ms		
		0100	24 ms		
		0101	48 ms		
		0110	96 ms		
		0111	192 ms		
		1000	384 ms		
		1001	768 ms		
		1010	1.536 sec		
		1011	3.072 sec		
		1100	6.144 sec		
[3:0]	ALCHLD		ALC Hold Time. ALC recovery hold time.	0x0	RW
		0000	0 ms		
		0001	2.67 ms		
		0010	5.34 ms		
		0011	10.68 ms		
		0100	21.36 ms		
		0101	42.72 ms		
		0110	85.44 ms		
		0111	170.88 ms		
		1000	341.76 ms		
		1001	683.52 ms		
		1010	1.367 sec		
		1011	2.734 sec		
		1100	5.468 sec		

ALC_CTRL1 REGISTER

Address: 0xC3, Reset: 0x00, Name: ALC_CTRL1

ALC Control Register

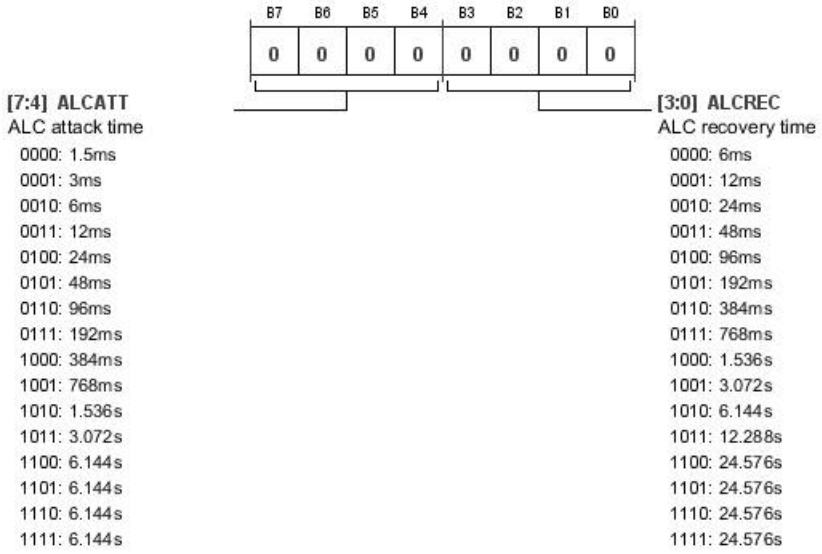


Table 218. Bit Descriptions for ALC_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	ALCATT		ALC Attack Time. ALC attack time setting.	0x0	RW
		0000	1.5 ms		
		0001	3 ms		
		0010	6 ms		
		0011	12 ms		
		0100	24 ms		
		0101	48 ms		
		0110	96 ms		
		0111	192 ms		
		1000	384 ms		
		1001	768 ms		
		1010	1.536 sec		
		1011	3.072 sec		
		1100	6.144 sec		
		1101	6.144 sec		
		1110	6.144 sec		
		1111	6.144 sec		
[3:0]	ALCREC		ALC Recovery Time. ALC recovery time setting.	0x0	RW
		0000	6 ms		
		0001	12 ms		
		0010	24 ms		
		0011	48 ms		
		0100	96 ms		
		0101	192 ms		
		0110	384 ms		
		0111	768 ms		
		1000	1.536 sec		
		1001	3.072 sec		

Bits	Bit Name	Settings	Description	Reset	Access
[3:0]	ALCREC	1010	6.144 sec		
		1011	12.288 sec		
		1100	24.576 sec		
		1101	24.576 sec		
		1110	24.576 sec		
		1111	24.576 sec		

ALC_CTRL2 REGISTER

Address: 0xC4, Reset: 0x00, Name: ALC_CTRL2

ALC Control Register

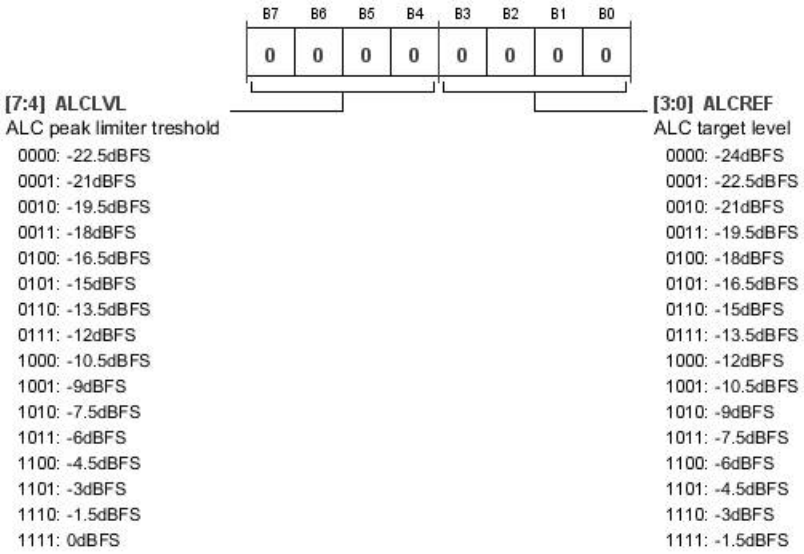


Table 219. Bit Descriptions for ALC_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	ALCLVL		ALC Peak Limiter Threshold. ALC peak limiter threshold level setting.	0x0	RW
		0000	−22.5 dBFS		
		0001	−21 dBFS		
		0010	−19.5 dBFS		
		0011	−18 dBFS		
		0100	−16.5 dBFS		
		0101	−15 dBFS		
		0110	−13.5 dBFS		
		0111	−12 dBFS		
		1000	−10.5 dBFS		
		1001	−9 dBFS		
		1010	−7.5 dBFS		
		1011	−6 dBFS		
		1100	−4.5 dBFS		
		1101	−3 dBFS		
		1110	−1.5 dBFS		
		1111	0 dBFS		

Bits	Bit Name	Settings	Description	Reset	Access
[3:0]	ALCREF		ALC Target Level. ALC reference level setting.	0x0	RW
		0000	−24 dBFS		
		0001	−22.5 dBFS		
		0010	−21 dBFS		
		0011	−19.5 dBFS		
		0100	−18 dBFS		
		0101	−16.5 dBFS		
		0110	−15 dBFS		
		0111	−13.5 dBFS		
		1000	−12 dBFS		
		1001	−10.5 dBFS		
		1010	−9 dBFS		
		1011	−7.5 dBFS		
		1100	−6 dBFS		
		1101	−4.5 dBFS		
		1110	−3 dBFS		
		1111	−1.5 dBFS		

ALC_CTRL3 REGISTER

Address: 0xC5, Reset: 0x00, Name: ALC_CTRL3

ALC Control Register

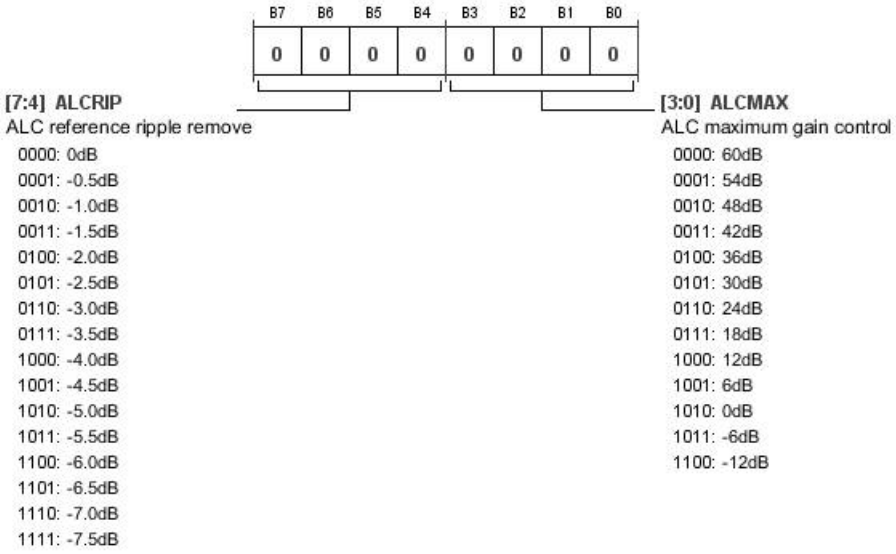


Table 220. Bit Descriptions for ALC_CTRL3

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	ALCRIP		ALC Reference Ripple Remove. ALC ripple level setting. The setting, with respect to reference level, defines the input level range in which there can be no change in ALC gain.	0x0	RW
		0000	0 dB		
		0001	−0.5 dB		
		0010	−1.0 dB		
		0011	−1.5 dB		
		0100	−2.0 dB		
		0101	−2.5 dB		
		0110	−3.0 dB		

Bits	Bit Name	Settings	Description	Reset	Access
		0111	−3.5 dB		
		1000	−4.0 dB		
		1001	−4.5 dB		
		1010	−5.0 dB		
		1011	−5.5 dB		
		1100	−6.0 dB		
		1101	−6.5 dB		
		1110	−7.0 dB		
		1111	−7.5 dB		
[3:0]	ALCMAX		ALC Maximum Gain Control. ALC maximum gain setting.	0x0	RW
		0000	60 dB		
		0001	54 dB		
		0010	48 dB		
		0011	42 dB		
		0100	36 dB		
		0101	30 dB		
		0110	24 dB		
		0111	18 dB		
		1000	12 dB		
		1001	6 dB		
		1010	0 dB		
		1011	−6 dB		
		1100	−12 dB		

ALC_CTRL4 REGISTER

Address: 0xC6, Reset: 0x00, Name: ALC_CTRL4

ALC Control Register

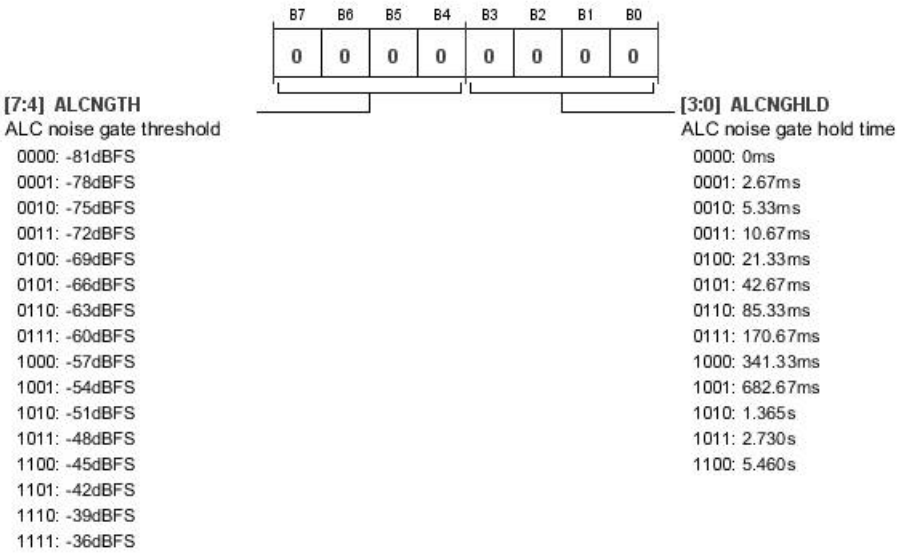


Table 221. Bit Descriptions for ALC_CTRL4

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	ALCNGTH		ALC Noise Gate Threshold. ALC noise gate threshold level setting.	0x0	RW
		0000	−81 dBFS		
		0001	−78 dBFS		
		0010	−75 dBFS		
		0011	−72 dBFS		
		0100	−69 dBFS		
		0101	−66 dBFS		
		0110	−63 dBFS		
		0111	−60 dBFS		
		1000	−57 dBFS		
		1001	−54 dBFS		
		1010	−51 dBFS		
		1011	−48 dBFS		
		1100	−45 dBFS		
		1101	−42 dBFS		
		1110	−39 dBFS		
		1111	−36 dBFS		
[3:0]	ALCNGHLD		ALC Noise Gate Hold Time. The ALC holds the gain for the set time when input level is below noise gate threshold.	0x0	RW
		0000	0 ms		
		0001	2.67 ms		
		0010	5.33 ms		
		0011	10.67 ms		
		0100	21.33 ms		
		0101	42.67 ms		
		0110	85.33 ms		
		0111	170.67 ms		
		1000	341.33 ms		
		1001	682.67 ms		
		1010	1.365 sec		
		1011	2.730 sec		
		1100	5.460 sec		

ALC_CTRL5 REGISTER

Address: 0xC7, Reset: 0x00, Name: ALC_CTRL5

ALC Control Register

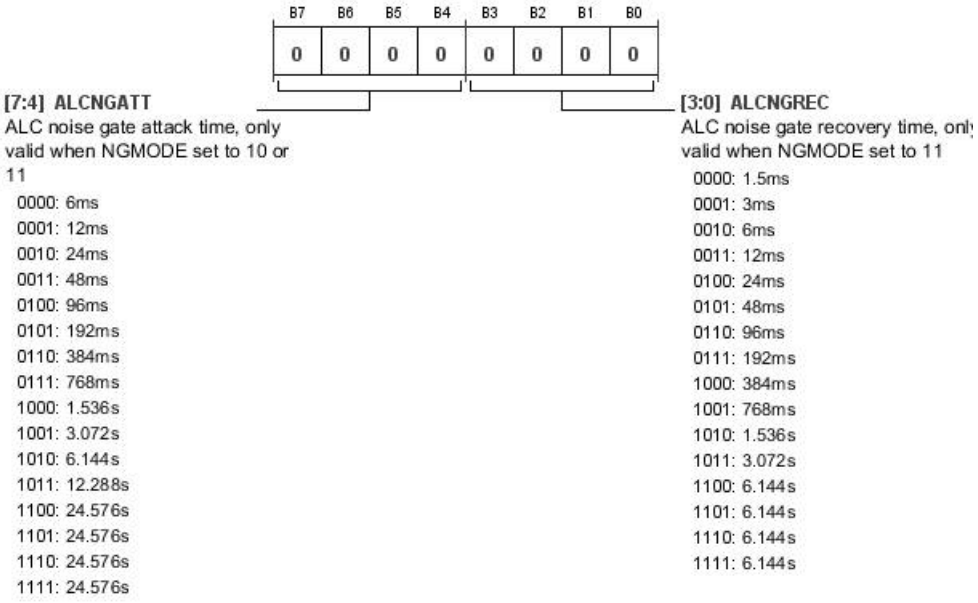


Table 222. Bit Descriptions for ALC_CTRL5

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	ALCNGATT		ALC Noise Gate Attack Time. Valid only when NGMODE set to 10 or 11. ALC noise gate attack time setting. This setting is valid only in Noise Gate Mode 2 and Noise Gate Mode 3.	0x0	RW
		0000	6 ms		
		0001	12 ms		
		0010	24 ms		
		0011	48 ms		
		0100	96 ms		
		0101	192 ms		
		0110	384 ms		
		0111	768 ms		
		1000	1.536 sec		
		1001	3.072 sec		
		1010	6.144 sec		
		1011	12.288 sec		
		1100	24.576 sec		
		1101	24.576 sec		
		1110	24.576 sec		
		1111	24.576 sec		
[3:0]	ALCNGREC		ALC Noise Gate Recovery Time. Valid only when NGMODE set to 11. ALC noise gate recovery time setting. This setting is valid only in Noise Gate Mode 3.	0x0	RW
		0000	1.5 ms		
		0001	3 ms		
		0010	6 ms		
		0011	12 ms		
		0100	24 ms		
		0101	48 ms		
		0110	96 ms		

Bits	Bit Name	Settings	Description	Reset	Access
		0111	192 ms		
		1000	384 ms		
		1001	768 ms		
		1010	1.536 sec		
		1011	3.072 sec		
		1100	6.144 sec		
		1101	6.144 sec		
		1110	6.144 sec		
		1111	6.144 sec		

ALC_CTRL6 REGISTER

Address: 0xC8, Reset: 0x00, Name: ALC_CTRL6

ALC Control Register

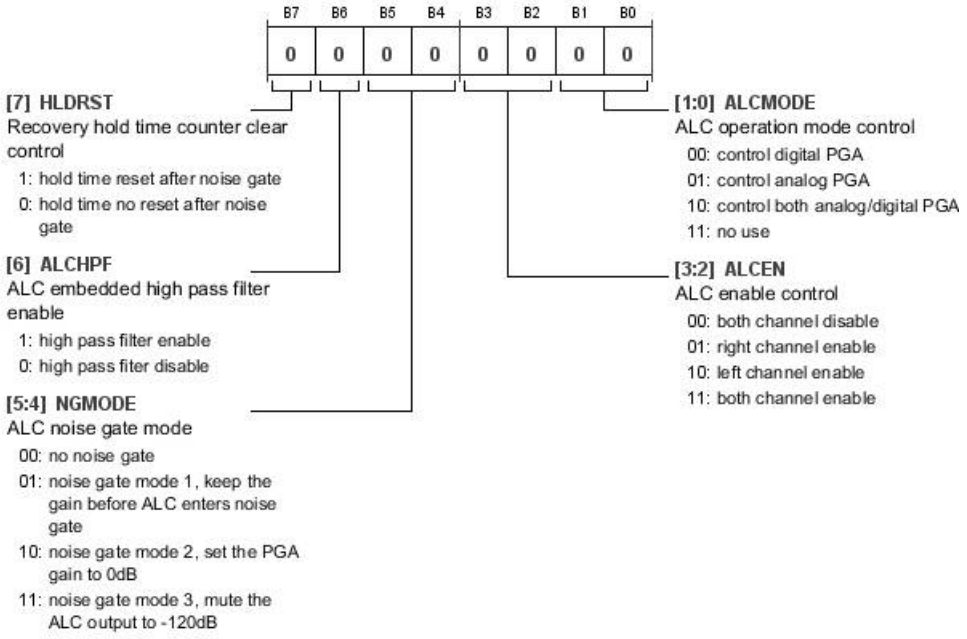


Table 223. Bit Descriptions for ALC_CTRL6

Bits	Bit Name	Settings	Description	Reset	Access
7	HLDRST		Recovery Hold Time Counter Clear Control. Noise gate reset hold time setting. The noise gate is not reset for the hold time set in Register 0xC6.	0x0	RW
		1	Hold time reset after noise gate		
		0	Hold time no reset after noise gate		
6	ALCHPF		ALC Embedded High-Pass Filter Enable. ALC high-pass filter enable/disable setting. The high-pass filter is fixed at 3.7 Hz at a 48 kHz sample rate.	0x0	RW
		1	High-pass filter enable		
		0	High-pass filter disable		
[5:4]	NGMODE		ALC Noise Gate Mode. ALC noise gate mode selection: Noise Gate Mode 1, Noise Gate Mode 2, Noise Gate Mode 3, or disable noise gate.	0x0	RW
		00	No noise gate		
		01	Noise Gate Mode 1; keeps the gain before ALC enters noise gate		
		10	Noise Gate Mode 2; sets the PGA gain to 0 dB		
		11	Noise Gate Mode 3; mutes the ALC output to −120 dB		
[3:2]	ALCEN		ALC Enable Control. ALC enable/disable control.	0x0	RW
		00	Both channels disabled		
		01	Right channel enabled		
		10	Left channel enabled		
		11	Both channels enabled		
[1:0]	ALCMODE		ALC Operation Mode Control. ALC can be applied to digital/analog PGA or both by setting this register.	0x0	RW
		00	Control digital PGA		
		01	Control analog PGA		
		10	Control both analog/digital PGA		
		11	No use		

FDSP_SEL1 REGISTER

Address: 0xDC, Reset: 0x00, Name: FDSP_SEL1

DSP Datapath Selection Control Register

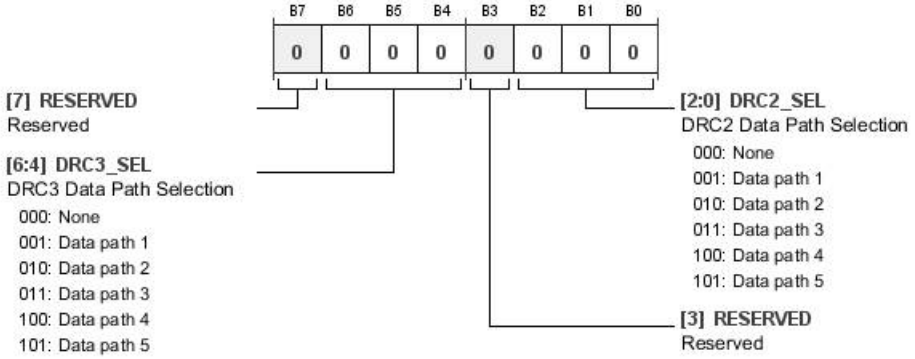


Table 224. Bit Descriptions for FDSP_SEL1

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
[6:4]	DRC3_SEL		DRC3 Datapath Selection. EQ datapath selection.	0x0	RW
		000	None		
		001	Datapath 1		
		010	Datapath 2		
		011	Datapath 3		
		100	Datapath 4		
		101	Datapath 5		
3	RESERVED		Reserved.	0x0	RW
[2:0]	DRC2_SEL		DRC2 Datapath Selection. DRC datapath selection.	0x0	RW
		000	None		
		001	Datapath 1		
		010	Datapath 2		
		011	Datapath 3		
		100	Datapath 4		
		101	Datapath 5		

FDSP_SEL2 REGISTER

Address: 0xDD, Reset: 0x00, Name: FDSP_SEL2

DSP Datapath Selection Control Register

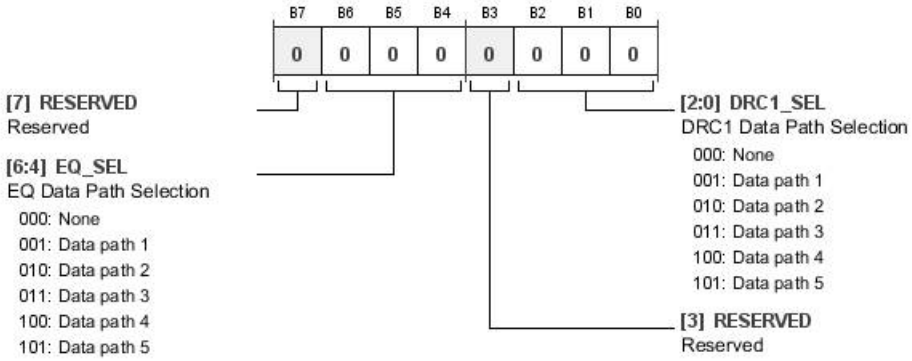


Table 225. Bit Descriptions for FDSP_SEL2

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
[6:4]	EQ_SEL		EQ Datapath Selection.	0x0	RW
		000	None		
		001	Datapath 1		
		010	Datapath 2		
		011	Datapath 3		
		100	Datapath 4		
		101	Datapath 5		
3	RESERVED		Reserved.	0x0	RW
[2:0]	DRC1_SEL		DRC1 Datapath Selection.	0x0	RW
		000	None		
		001	Datapath 1		
		010	Datapath 2		
		011	Datapath 3		
		100	Datapath 4		
		101	Datapath 5		

FDSP_SEL3 REGISTER

Address: 0xDE, Reset: 0x00, Name: FDSP_SEL3

DSP Datapath Selection Control Register

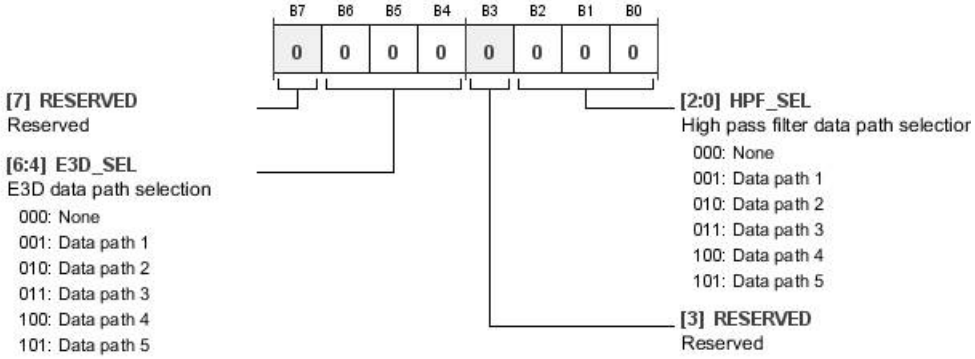


Table 226. Bit Descriptions for FDSP_SEL3

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
[6:4]	E3D_SEL		E3D Datapath Selection. 3D enhancement datapath selection.	0x0	RW
		000	None		
		001	Datapath 1		
		010	Datapath 2		
		011	Datapath 3		
		100	Datapath 4		
		101	Datapath 5		
3	RESERVED		Reserved.	0x0	RW
[2:0]	HPF_SEL		High-Pass Filter Datapath Selection.	0x0	RW
		000	None		
		001	Datapath 1		
		010	Datapath 2		
		011	Datapath 3		
		100	Datapath 4		
		101	Datapath 5		

FDSP_SEL4 REGISTER

Address: 0xDF, Reset: 0x00, Name: FDSP_SEL4

DSP Datapath Selection Control Register

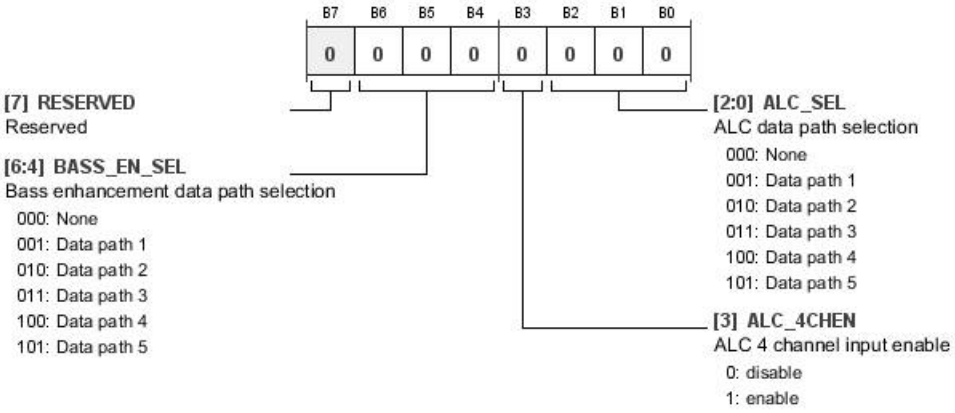


Table 227. Bit Descriptions for FDSP_SEL4

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
[6:4]	BASS_EN_SEL		Bass Enhancement Datapath Selection.	0x0	RW
		000	None		
		001	Datapath 1		
		010	Datapath 2		
		011	Datapath 3		
		100	Datapath 4		
		101	Datapath 5		
3	ALC_4CHEN		ALC 4 Channel Input Enable. ALC 4 channel input enable/disable control.	0x0	RW
		0	Disable		
		1	Enable		
[2:0]	ALC_SEL		ALC Datapath Selection.	0x0	RW
		000	None		
		001	Datapath 1		
		010	Datapath 2		
		011	Datapath 3		
		100	Datapath 4		
		101	Datapath 5		

PBALPCTRL1 REGISTER

Address: 0xE0, Reset: 0x00, Name: PBALPCTRL1

DAC1 Playback Power Control Register

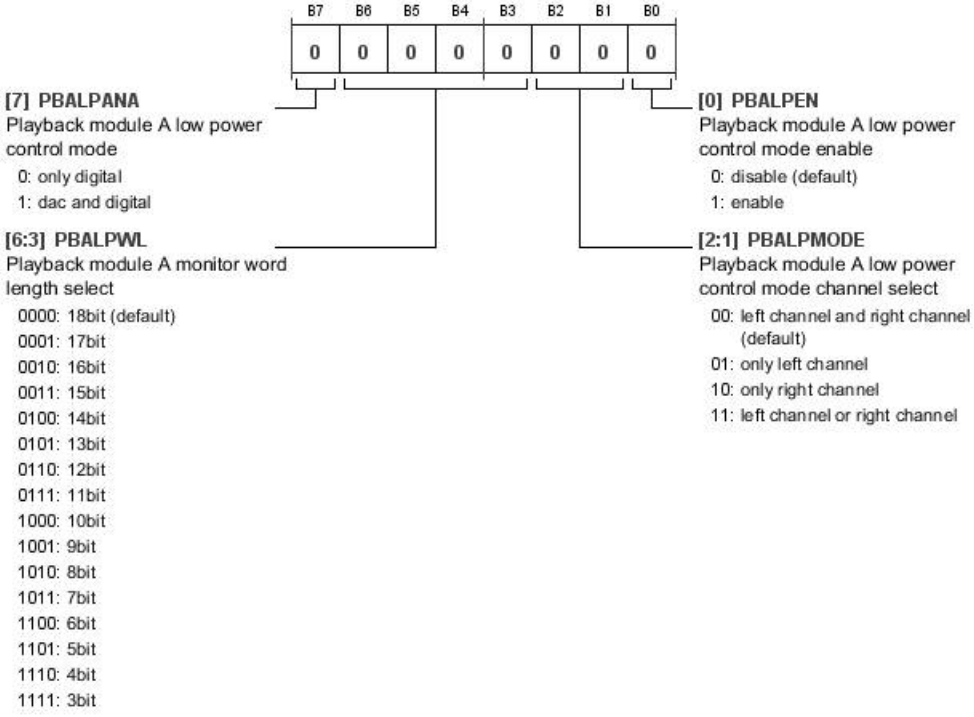


Table 228. Bit Descriptions for PBALPCTRL1

Bits	Bit Name	Settings	Description	Reset	Access
7	PBALPANA		Playback Module A Low Power Control Mode. Playback Module A low power control mode.	0x0	RW
		0	Only digital		
		1	DAC and digital		
[6:3]	PBALPWL		Playback Module A Monitor Word Length Select. Playback Module A monitor word length select.	0x0	RW
		0000	18 bit (default)		
		0001	17 bit		
		0010	16 bit		
		0011	15 bit		
		0100	14 bit		
		0101	13 bit		
		0110	12 bit		
		0111	11 bit		
		1000	10 bit		
		1001	9 bit		
		1010	8 bit		
		1011	7 bit		
		1100	6 bit		
		1101	5 bit		
		1110	4 bit		
		1111	3 bit		

Bits	Bit Name	Settings	Description	Reset	Access
[2:1]	PBALPMODE		Playback Module A Low Power Control Mode Channel Select. Playback Module A low power control mode channel select.	0x0	RW
		00	Left channel and right channel (default)		
		01	Only left channel		
		10	Only right channel		
		11	Left channel or right channel		
0	PBALPEN		Playback Module A Low Power Control Mode Enable. Playback Module A low power control mode enable.	0x0	RW
		0	Disable (default)		
		1	Enable		

PBBLPCTRL2 REGISTER

Address: 0xE1, Reset: 0x00, Name: PBBLPCTRL2

DAC2 Playback Power Control Register

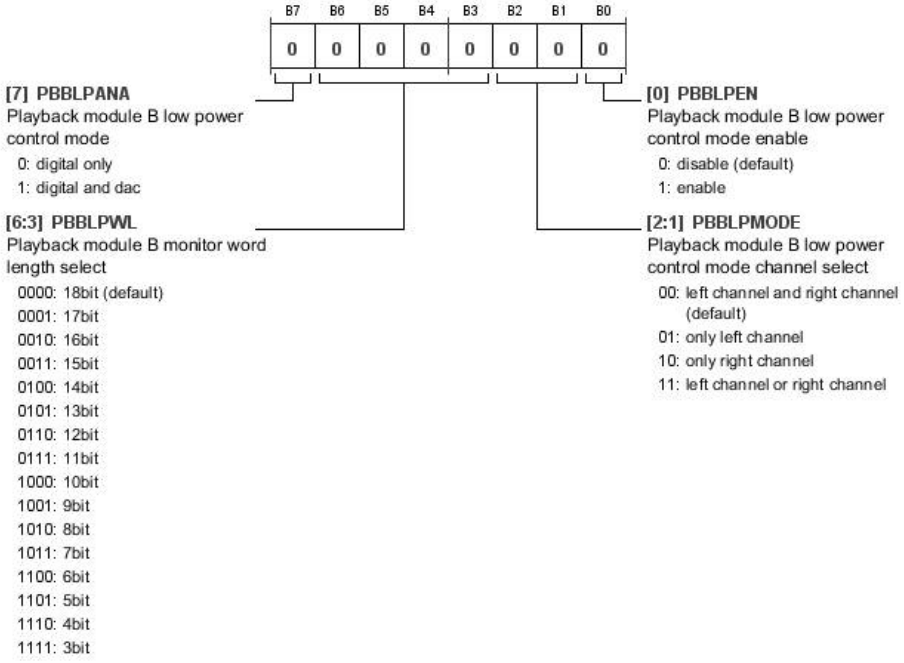


Table 229. Bit Descriptions for PBBLPCTRL2

Bits	Bit Name	Settings	Description	Reset	Access
7	PBBLPANA		Playback Module B Low Power Control Mode. Playback Module B low power control mode.	0x0	RW
		0	Digital only		
		1	Digital and DAC		
[6:3]	PBBLPWL		Playback Module B Monitor Word Length Select. Playback Module B monitor word length select.	0x0	RW
		0000	18 bit (default)		
		0001	17 bit		
		0010	16 bit		
		0011	15 bit		
		0100	14 bit		
		0101	13 bit		
		0110	12 bit		
		0111	11 bit		

Bits	Bit Name	Settings	Description	Reset	Access
		1000	10 bit		
		1001	9 bit		
		1010	8 bit		
		1011	7 bit		
		1100	6 bit		
		1101	5 bit		
		1110	4 bit		
		1111	3 bit		
[2:1]	PBBLPMODE		Playback Module B Low Power Control Mode Channel Select. Playback Module B low power control mode channel select.	0x0	RW
		00	Left channel and right channel (default)		
		01	Only left channel		
		10	Only right channel		
		11	Left channel or right channel		
0	PBBLPEN		Playback Module B Low Power Control Mode Enable. Playback Module B low power control mode enable.	0x0	RW
		0	Disable (default)		
		1	Enable		

DIGMICCTRL REGISTER

Address: 0xE2, Reset: 0x00, Name: DIGMICCTRL

Digital Microphone Control Register

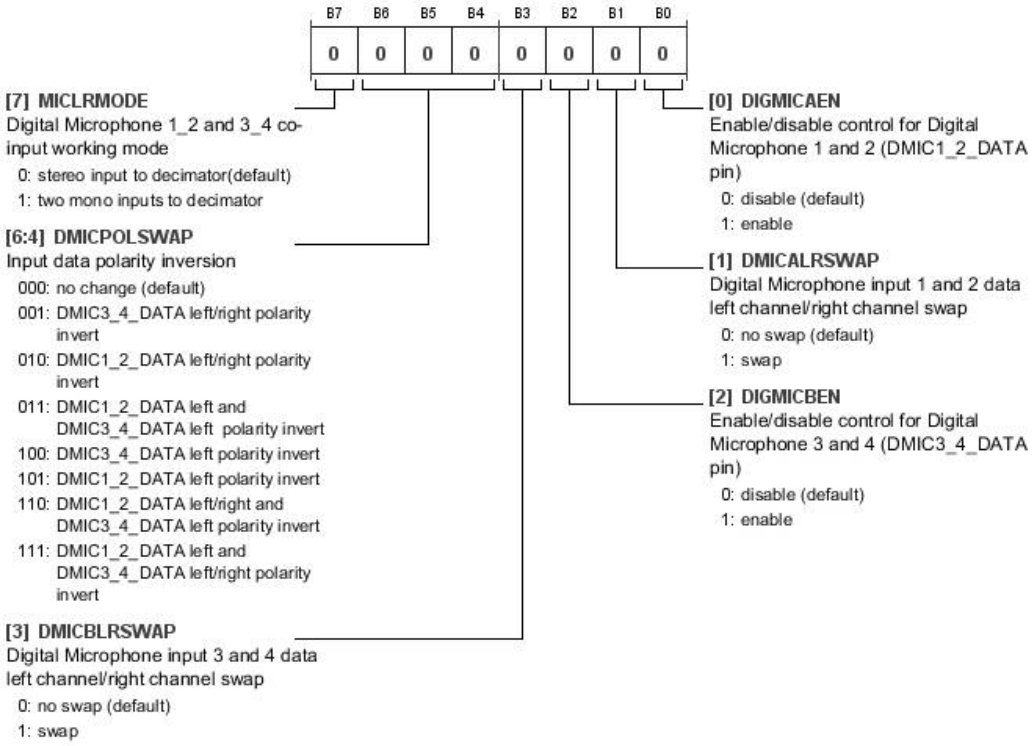


Table 230. Bit Descriptions for DIGMICCTRL

Bits	Bit Name	Settings	Description	Reset	Access
7	MICLRMODE		Digital Microphone 1_2 and Digital Microphone 3_4 Co-Input Working Mode. When enabled, uses DMIC1 from DMIC1_2_DATA pin and DMIC3 from DMIC3_4_DATA pin as two mono inputs to decimator.	0x0	RW
		0	Stereo input to decimator (default)		
		1	Two mono inputs to decimator		
[6:4]	DMICPOLSWAP		Input Data Polarity Inversion. Use to invert the input data polarity.	0x0	RW
		000	No change (default)		
		001	DMIC3_4_DATA left/right polarity invert		
		010	DMIC1_2_DATA left/right polarity invert		
		011	DMIC1_2_DATA left and DMIC3_4_DATA left polarity invert		
		100	DMIC3_4_DATA left polarity invert		
		101	DMIC1_2_DATA left polarity invert		
		110	DMIC1_2_DATA left/right and DMIC3_4_DATA left polarity invert		
		111	DMIC1_2_DATA left and DMIC3_4_DATA left/right polarity invert		
3	DMICBLRSWAP		Digital Microphone 3 and 4 Data Input Left Channel/Right Channel Swap.	0x0	RW
		0	No swap (default)		
		1	Swap		
2	DIGMICBEN		Enable/Disable Control for DMIC3_4_DATA Pin (Ball E6).	0x0	RW
		0	Disable (default)		
		1	Enable		
1	DMICALRSWAP		Digital Microphone 1 and 2 Data Input Left Channel/Right Channel Swap.	0x0	RW
		0	No swap (default)		
		1	Swap		

Bits	Bit Name	Settings	Description	Reset	Access
0	DIGMICAEN		Enable/Disable Control for DMIC1_2_DATA Pin (Ball B4). Shares the decimator with the ADC so that, when enabled, Digital Microphone 1 and 2 data is input into the decimator. The ADC output is disabled.	0x0	RW
		0	Disable (default)		
		1	Enable		

GPIOSEL1 REGISTER

Address: 0xE3, Reset: 0x00, Name: GPIOSEL1

GPIO Configuration Control Register

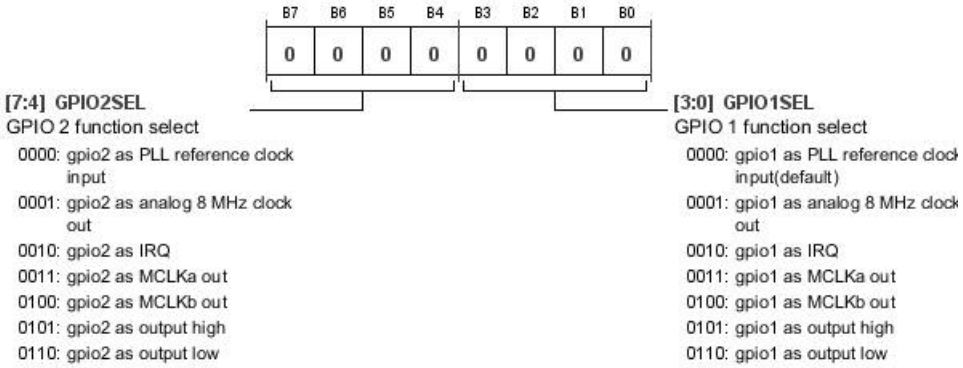


Table 231. Bit Descriptions for GPIOSEL1

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	GPIO2SEL		GPIO2 Function Select.	0x0	RW
		0000	GPIO2 as PLL reference clock input		
		0001	GPIO2 as analog 8 MHz clock output		
		0010	GPIO2 as IRQ		
		0011	GPIO2 as MCLK1 output		
		0100	GPIO2 as MCLK2 output		
		0101	GPIO2 as output high		
		0110	GPIO2 as output low		
[3:0]	GPIO1SEL		GPIO1 Function Select.	0x0	RW
		0000	GPIO1 as PLL reference clock input (default)		
		0001	GPIO1 as analog 8 MHz clock output		
		0010	GPIO1 as IRQ		
		0011	GPIO1 as MCLK1 output		
		0100	GPIO1 as MCLK2 output		
		0101	GPIO1 as output high		
		0110	GPIO1 as output low		

GPIOSEL2 REGISTER

Address: 0xE4, Reset: 0x00, Name: GPIOSEL2

GPIO Configuration Control Register

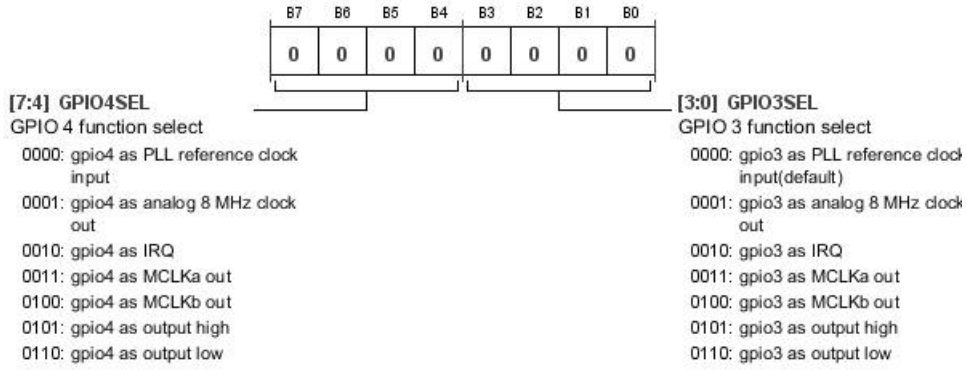


Table 232. Bit Descriptions for GPIOSEL2

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	GPIO4SEL		GPIO4 Function Select.	0x0	RW
		0000	GPIO4 as PLL reference clock input		
		0001	GPIO4 as analog 8 m clk out		
		0010	GPIO4 as IRQ		
		0011	GPIO4 as MCLK1 out		
		0100	GPIO4 as MCLK2 out		
		0101	GPIO4 as output high		
		0110	GPIO4 as output low		
[3:0]	GPIO3SEL		GPIO3 Function Select.	0x0	RW
		0000	GPIO3 as PLL reference clock input (default)		
		0001	GPIO3 as analog 8 m clk out		
		0010	GPIO3 as IRQ		
		0011	GPIO3 as MCLK1 out		
		0100	GPIO3 as MCLK2 out		
		0101	GPIO3 as output high		
		0110	GPIO3 as output low		

IRQ_MASK REGISTER

Address: 0xE5, Reset: 0x00, Name: IRQ_MASK

Interrupt Mask Control Register

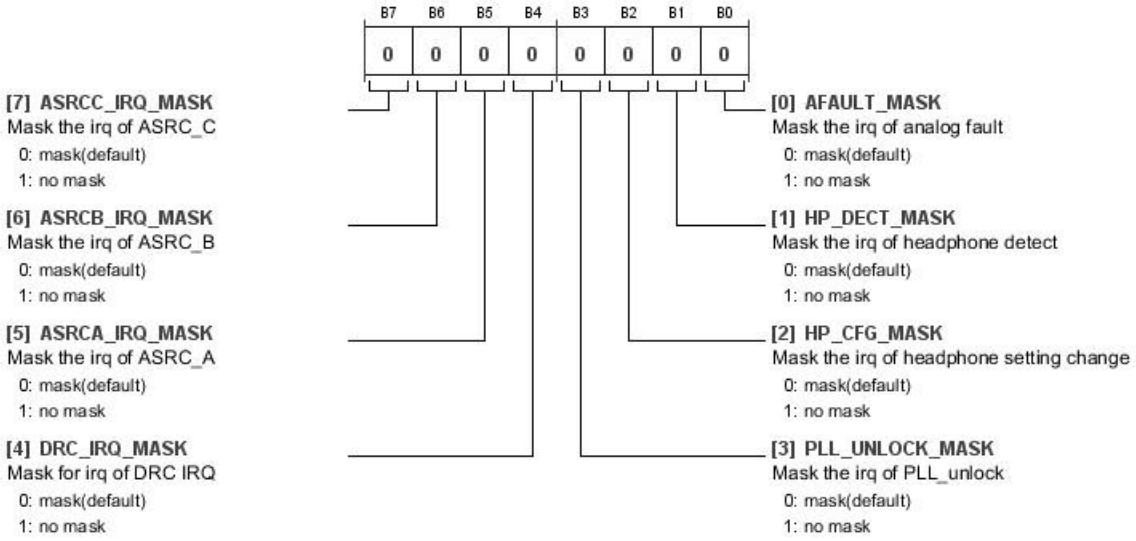


Table 233. Bit Descriptions for IRQ_MASK

Bits	Bit Name	Settings	Description	Reset	Access
7	ASRCC_IRQ_MASK		Mask the IRQ of ASRCC. Interrupt mask setting for ASRCC.	0x0	RW
		0	Mask (default)		
		1	No mask		
6	ASRCB_IRQ_MASK		Mask the IRQ of ASRCB. Interrupt mask setting for ASRCB.	0x0	RW
		0	Mask (default)		
		1	No mask		
5	ASRCA_IRQ_MASK		Mask the IRQ of ASRCA. Interrupt mask setting for ASRCA.	0x0	RW
		0	Mask (default)		
		1	No mask		
4	DRC_IRQ_MASK		Mask the IRQ of DRC IRQ. Interrupt mask setting for DRC IRQ.	0x0	RW
		0	Mask (default)		
		1	No mask		
3	PLL_UNLOCK_MASK		Mask the IRQ of PLL_UNLOCK. Interrupt mask setting for PLL unlock.	0x0	RW
		0	Mask (default)		
		1	No mask		
2	HP_CFG_MASK		Mask the IRQ of Headphone Setting Change. Interrupt mask setting for headphone setting change.	0x0	RW
		0	Mask (default)		
		1	No mask		
1	HP_DECT_MASK		Mask the IRQ of Headphone Detect. Interrupt mask setting for headphone fault.	0x0	RW
		0	Mask (default)		
		1	No mask		
0	AFAULT_MASK		Mask the IRQ of Analog Fault. Interrupt mask setting for analog fault.	0x0	RW
		0	Mask (default)		
		1	No mask		

IRQ_RAW REGISTER

Address: 0xE6, Reset: 0x02, Name: IRQ_RAW

Interrupt Status Register

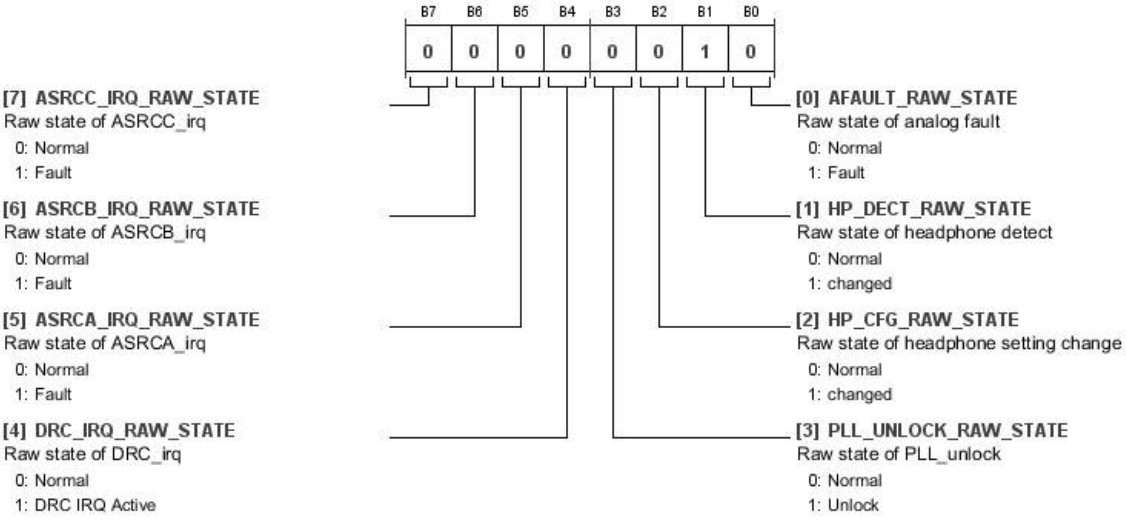


Table 234. Bit Descriptions for IRQ_RAW

Bits	Bit Name	Settings	Description	Reset	Access
7	ASRCC_IRQ_RAW_STATE		Raw State of ASRCC_IRQ. Raw status of ASRCC.	0x0	R
		0	Normal		
		1	Fault		
6	ASRCB_IRQ_RAW_STATE		Raw State of ASRCB_IRQ. Raw status of ASRCB.	0x0	R
		0	Normal		
		1	Fault		
5	ASRCA_IRQ_RAW_STATE		Raw State of ASRCA_IRQ. Raw status of ASRCA.	0x0	R
		0	Normal		
		1	Fault		
4	DRC_IRQ_RAW_STATE		Raw State of DRC_IRQ. Raw status of DRC IRQ.	0x0	R
		0	Normal		
		1	ADC clip		
3	PLL_UNLOCK_RAW_STATE		Raw State of PLL_UNLOCK. Raw status of PLL unlock.	0x0	R
		0	Normal		
		1	Unlock		
2	HP_CFG_RAW_STATE		Raw State of Headphone Setting Change. Raw status of headphone setting fault.	0x0	R
		0	Normal		
		1	Changed		
1	HP_DECT_RAW_STATE		Raw State of Headphone Detect. Raw status of headphone fault.	0x1	R
		0	Normal		
		1	Changed		
0	AFAULT_RAW_STATE		Raw State of Analog Fault. Raw status of analog fault.	0x0	R
		0	Normal		
		1	Fault		

IRQ_STATE (AFTER MASK) REGISTER

Address: 0xE7, Reset: 0x00, Name: IRQ_STATE

Interrupt Request State Register

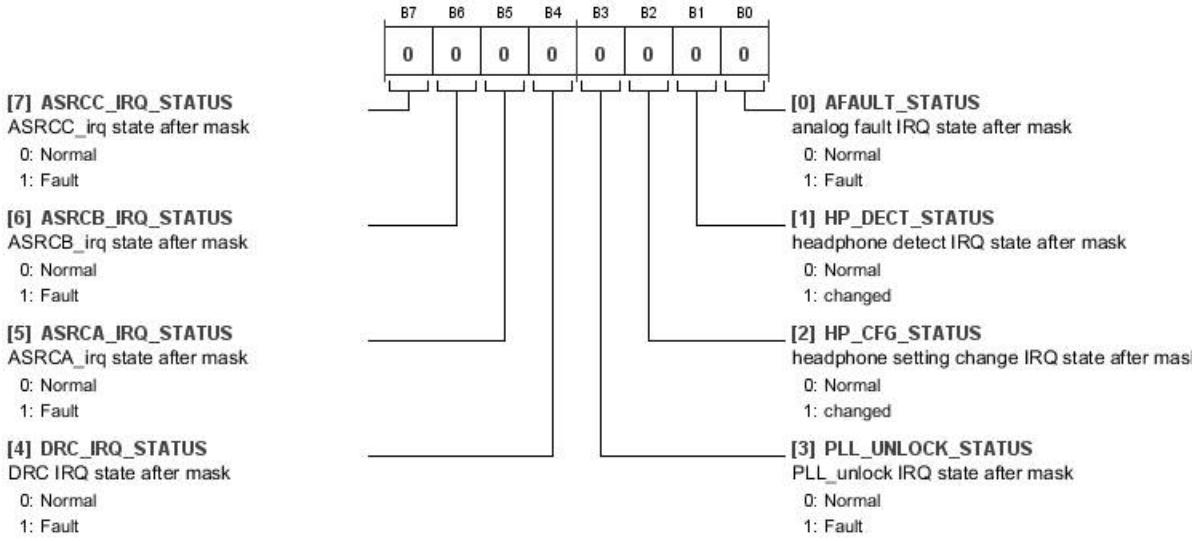


Table 235. Bit Descriptions for IRQ_STATE

Bits	Bit Name	Settings	Description	Reset	Access
7	ASRCC_IRQ_STATUS		ASRCC_IRQ State After Mask. ASRCC interrupt.	0x0	R
		0	Normal		
		1	Fault		
6	ASRCB_IRQ_STATUS		ASRCB_IRQ State After Mask. ASRCB interrupt.	0x0	R
		0	Normal		
		1	Fault		
5	ASRCA_IRQ_STATUS		ASRCA_IRQ State After Mask. ASRCA interrupt.	0x0	R
		0	Normal		
		1	Fault		
4	DRC_IRQ_STATUS		DRC IRQ State After Mask. DRC interrupt.	0x0	R
		0	Normal		
		1	Fault		
3	PLL_UNLOCK_STATUS		PLL_UNLOCK IRQ State After Mask. PLL unlock interrupt.	0x0	R
		0	Normal		
		1	Fault		
2	HP_CFG_STATUS		Headphone Setting Change IRQ State After Mask. Headphone setting change interrupt.	0x0	R
		0	Normal		
		1	Changed		
1	HP_DECT_STATUS		Headphone Detect IRQ State After Mask. Headphone fault interrupt.	0x0	R
		0	Normal		
		1	Changed		
0	AFAULT_STATUS		Analog Fault IRQ State After Mask. Analog fault interrupt.	0x0	R
		0	Normal		
		1	Fault		

IRQEN REGISTER

Address: 0xE8, Reset: 0x00, Name: IRQEN

Interrupt Request Enable/Disable Register

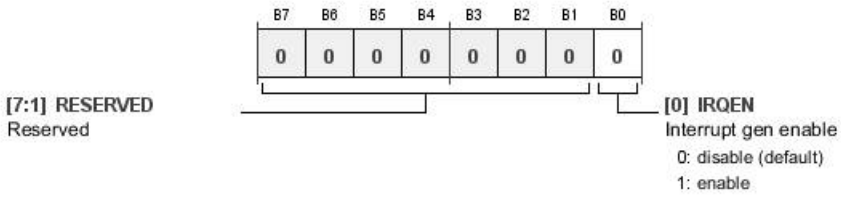


Table 236. Bit Descriptions for IRQEN

Bits	Bit Name	Settings	Description	Reset	Access
[7:1]	RESERVED		Reserved.	0x0	RW
0	IRQEN		Interrupt Gen Enable. Interrupt request enable/disable control.	0x0	RW
		0	Disable (default)		
		1	Enable		

PAD_CTRL1 REGISTER

Address: 0xE9, Reset: 0x1F, Name: PAD_CTRL1

Pin Drive Capability Control Register

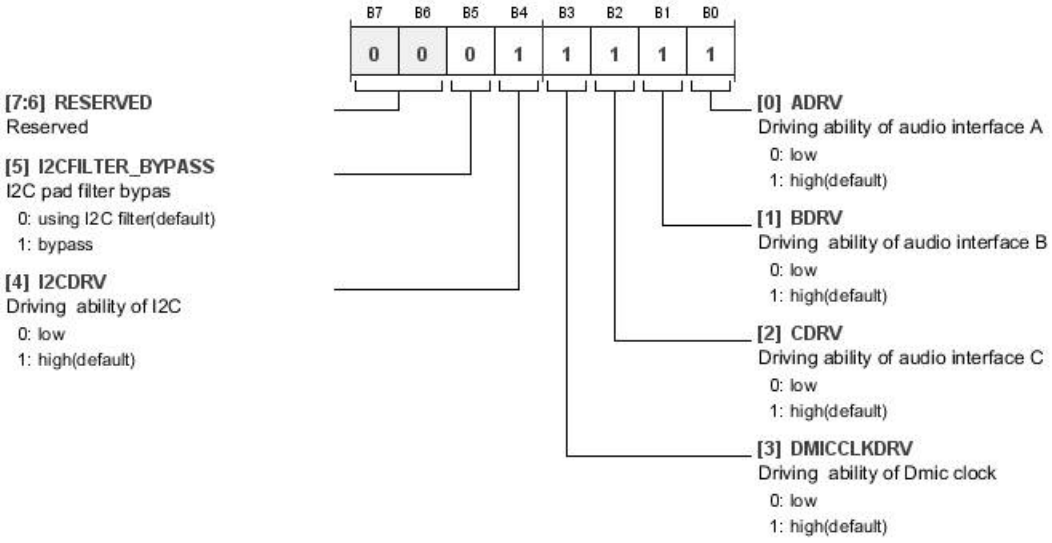


Table 237. Bit Descriptions for PAD_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	RW
5	I2CFILTER_BYPASS		I^2C Pad Filter Bypass. I^2C pad filter enable/disable control.	0x0	RW
		0	Using I^2C filter (default)		
		1	Bypass		
4	I2CDRV		Driving ability of I^2C. Driving ability setting for I^2C clock and data.	0x1	RW
		0	Low		
		1	High (default)		

Bits	Bit Name	Settings	Description	Reset	Access
3	DMICCLKDRV		Driving Ability of DMIC CLOCK. Driving ability setting for digital microphone clock.	0x1	RW
		0	Low		
		1	High (default)		
2	CDRV		Driving Ability of Audio Interface C. Driving ability setting of Audio Interface C.	0x1	RW
		0	Low		
		1	High (default)		
1	BDRV		Driving Ability of Audio Interface B. Driving ability setting of Audio Interface B.	0x1	RW
		0	Low		
		1	High (default)		
0	ADRV		Driving Ability of Audio Interface A. Driving ability setting of Audio Interface A.	0x1	RW
		0	Low		
		1	High (default)		

PAD_CTRL2 REGISTER

Address: 0xEA, Reset: 0x0F, Name: PAD_CTRL2

Pin Drive Capability Control Register

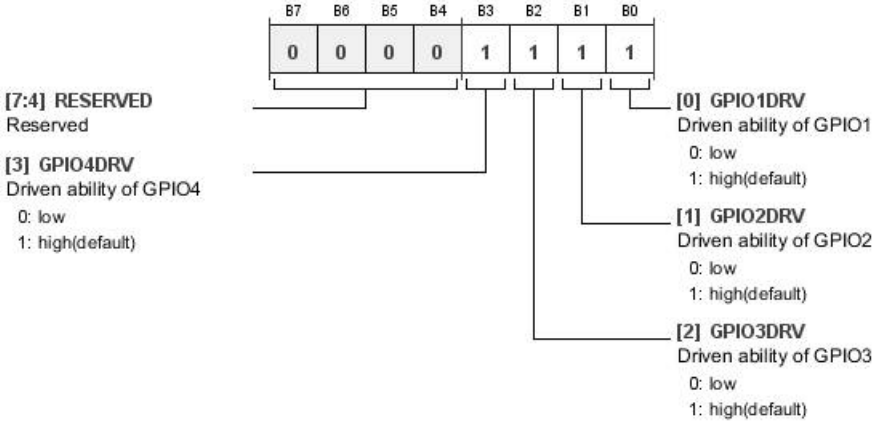


Table 238. Bit Descriptions for PAD_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved.	0x0	RW
3	GPIO4DRV		Driving Ability of GPIO4. Driving ability setting for GPIO4.	0x1	RW
		0	Low		
		1	High (default)		
2	GPIO3DRV		Driving Ability of GPIO3. Driving ability setting for GPIO3.	0x1	RW
		0	Low		
		1	High (default)		
1	GPIO2DRV		Driving Ability of GPIO2. Driving ability setting for GPIO2.	0x1	RW
		0	Low		
		1	High (default)		
0	GPIO1DRV		Driving Ability of GPIO1. Driving ability setting for GPIO1.	0x1	RW
		0	Low		
		1	High (default)		

DIGEN REGISTER

Address: 0xEB, Reset: 0x00, Name: DIGEN

Pin Drive Capability Control Register

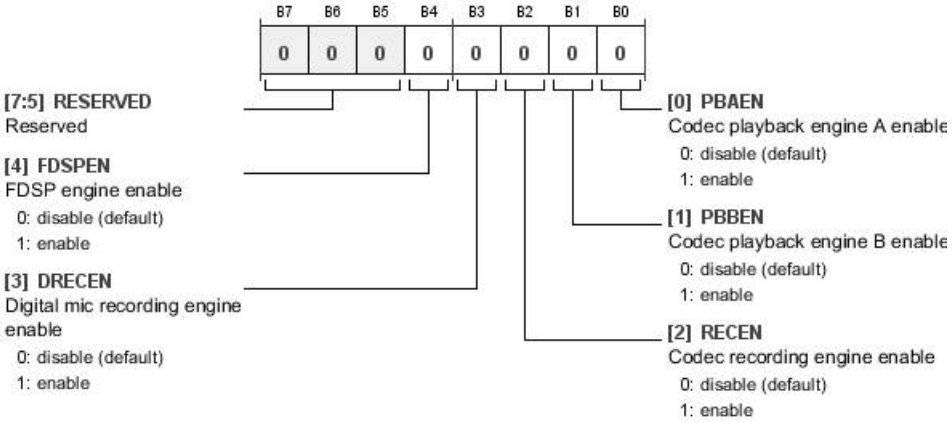


Table 239. Bit Descriptions for DIGEN

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	RW
4	FDSPEN		FDSP Engine Enable.	0x0	RW
		0	Disable (default)		
		1	Enable		
3	DRECEN		Digital Microphone Recording Engine Enable. Used to enable the Digital Microphone 3 and 4 data (DMIC3_4_DATA pin) to DSP.	0x0	RW
		0	Disable (default)		
		1	Enable		
2	RECEN		Codec Recording Engine Enable. Used to enable the codec recording engine or Digital Microphone 1 and 2 data (DMIC1_2_DATA pin) to DSP.	0x0	RW
		0	Disable (default)		
		1	Enable		
1	PBBEN		Codec Playback Engine B Enable.	0x0	RW
		0	Disable (default)		
		1	Enable		
0	PBAEN		Codec Playback Engine A Enable.	0x0	RW
		0	Disable (default)		
		1	Enable		

LPCNTCTRL (LOW POWER CONTROL COUNTER) REGISTER

Address: 0xEC, Reset: 0x00, Name: LPCNTCTRL

Low Power Control Counter

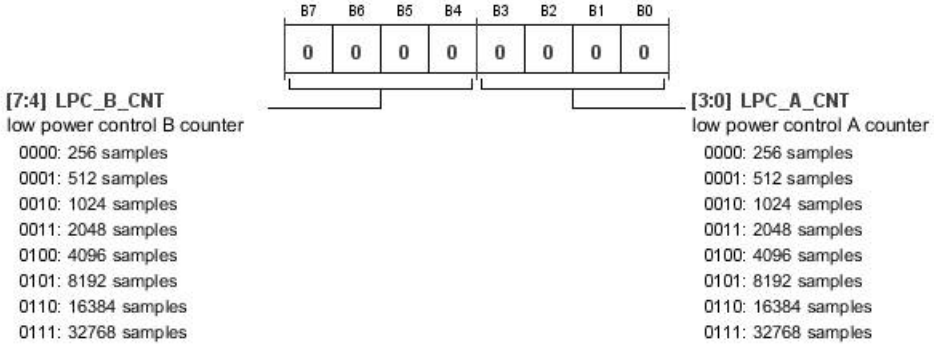


Table 240. Bit Descriptions for LPCNTCTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	LPC_B_CNT		Low Power Control B Counter.	0x0	RW
		0000	256 samples		
		0001	512 samples		
		0010	1024 samples		
		0011	2048 samples		
		0100	4096 samples		
		0101	8192 samples		
		0110	16384 samples		
		0111	32768 samples		
[3:0]	LPC_A_CNT		Low Power Control A Counter.	0x0	RW
		0000	256 samples		
		0001	512 samples		
		0010	1024 samples		
		0011	2048 samples		
		0100	4096 samples		
		0101	8192 samples		
		0110	16384 samples		
		0111	32768 samples		

CHIP_ID_HI REGISTER

Address: 0xED, Reset: 0x13, Name: CHIP_ID_HI

Chip Identification Register High Byte

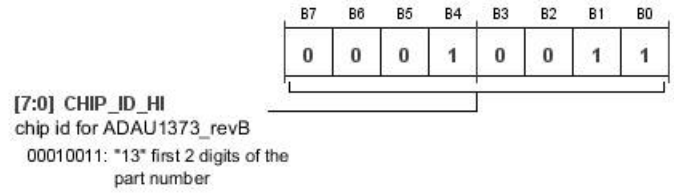


Table 241. Bit Descriptions for CHIP_ID_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CHIP_ID_HI		Chip ID for ADAU1373_REVB. Chip identification register high byte.	0x13	R
		00010011	13 (first two digits of the part number)		

CHIP_ID_MID REGISTER

Address: 0xEE, Reset: 0x73, Name: CHIP_ID_MID

Chip Identification Register Middle Byte

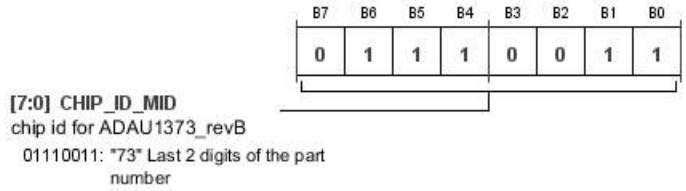


Table 242. Bit Descriptions for CHIP_ID_MID

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CHIP_ID_MID	01110011	Chip ID for ADAU1373_REVB. Chip Identification register middle byte. 73 (last two digits of the part number)	0x73	R

CHIP_ID_LOW REGISTER

Address: 0xEF, Reset: 0x0B, Name: CHIP_ID_LO

Chip Identification Register Low Byte

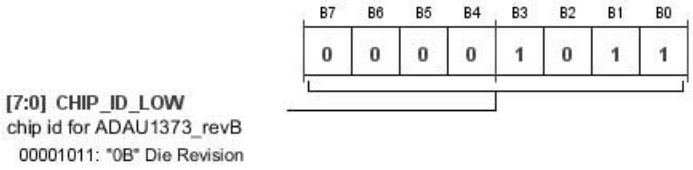


Table 243. Bit Descriptions for CHIP_ID_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CHIP_ID_LOW	00001011	Chip ID for ADAU1373_REVB. Chip identification register lower byte. 0B (die revision)	0x0B	R

SOFT_RESET REGISTER

Address: 0xFF, Reset: 0x00, Name: SOFT_RESET

Software Reset Register

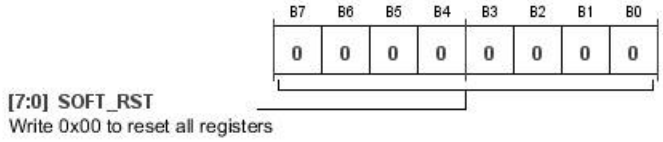


Table 244. Bit Descriptions for SOFT_RESET

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SOFT_RST		Software Reset Register. Write 0x00 to reset all registers.	0x00	RW

REGISTER MAP—EQ COEFFICIENTS

Table 245 shows the register map for seven-band EQ coefficients. Register 0x80 through Register 0xBD should be used for programming the EQ coefficients. Register addresses are in hexadecimal format.

Table 245. EQ Register Summary

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x80	EQ1_COEF0_HI	[7:0]	EQ1_COEF0_HI								0x00	RW
0x81	EQ1_COEF0_LO	[7:0]	EQ1_COEF0_LO								0x00	RW
0x82	EQ1_COEF1_HI	[7:0]	EQ1_COEF1_HI								0x00	RW
0x83	EQ1_COEF1_LO	[7:0]	EQ1_COEF1_LO								0x00	RW
0x84	EQ1_COEF2_HI	[7:0]	EQ1_COEF2_HI								0x00	RW
0x85	EQ1_COEF2_LO	[7:0]	EQ1_COEF2_LO								0x00	RW
0x86	EQ1_COEF3_HI	[7:0]	EQ1_COEF3_HI								0x00	RW
0x87	EQ1_COEF3_LO	[7:0]	EQ1_COEF3_LO								0x00	RW
0x88	EQ1_COEF4_HI	[7:0]	EQ1_COEF4_HI								0x00	RW
0x89	EQ1_COEF4_LO	[7:0]	EQ1_COEF4_LO								0x00	RW
0x8A	EQ2_COEF0_HI	[7:0]	EQ2_COEF0_HI								0x00	RW
0x8B	EQ2_COEF0_LO	[7:0]	EQ2_COEF0_LO								0x00	RW
0x8C	EQ2_COEF1_HI	[7:0]	EQ2_COEF1_HI								0x00	RW
0x8D	EQ2_COEF1_LO	[7:0]	EQ2_COEF1_LO								0x00	RW
0x8E	EQ2_COEF2_HI	[7:0]	EQ2_COEF2_HI								0x00	RW
0x8F	EQ2_COEF2_LO	[7:0]	EQ2_COEF2_LO								0x00	RW
0x90	EQ2_COEF3_HI	[7:0]	EQ2_COEF3_HI								0x00	RW
0x91	EQ2_COEF3_LO	[7:0]	EQ2_COEF3_LO								0x00	RW
0x92	EQ2_COEF4_HI	[7:0]	EQ2_COEF4_HI								0x00	RW
0x93	EQ2_COEF4_LO	[7:0]	EQ2_COEF4_LO								0x00	RW
0x94	EQ3_COEF0_HI	[7:0]	EQ3_COEF0_HI								0x00	RW
0x95	EQ3_COEF0_LO	[7:0]	EQ3_COEF0_LO								0x00	RW
0x96	EQ3_COEF1_HI	[7:0]	EQ3_COEF1_HI								0x00	RW
0x97	EQ3_COEF1_LO	[7:0]	EQ3_COEF1_LO								0x00	RW
0x98	EQ3_COEF2_HI	[7:0]	EQ3_COEF2_HI								0x00	RW
0x99	EQ3_COEF2_LO	[7:0]	EQ3_COEF2_LO								0x00	MMRW
0x9A	EQ3_COEF3_HI	[7:0]	EQ3_COEF3_HI								0x00	MMRW
0x9B	EQ3_COEF3_LO	[7:0]	EQ3_COEF3_LO								0x00	MMRW
0x9C	EQ3_COEF4_HI	[7:0]	EQ3_COEF4_HI								0x00	MMRW
0x9D	EQ3_COEF4_LO	[7:0]	EQ3_COEF4_LO								0x00	MMRW
0x9E	EQ4_COEF0_HI	[7:0]	EQ4_COEF0_HI								0x00	MMRW
0x9F	EQ4_COEF0_LO	[7:0]	EQ4_COEF0_LO								0x00	MMRW
0xA0	EQ4_COEF1_HI	[7:0]	EQ4_COEF1_HI								0x00	MMRW
0xA1	EQ4_COEF1_LO	[7:0]	EQ4_COEF1_LO								0x00	MMRW
0xA2	EQ4_COEF2_HI	[7:0]	EQ4_COEF2_HI								0x00	MMRW
0xA3	EQ4_COEF2_LO	[7:0]	EQ4_COEF2_LO								0x00	MMRW
0xA4	EQ4_COEF3_HI	[7:0]	EQ4_COEF3_HI								0x00	MMRW
0xA5	EQ4_COEF3_LO	[7:0]	EQ4_COEF3_LO								0x00	MMRW
0xA6	EQ4_COEF4_HI	[7:0]	EQ4_COEF4_HI								0x00	MMRW
0xA7	EQ4_COEF4_LO	[7:0]	EQ4_COEF4_LO								0x00	MMRW
0xA8	EQ5_COEF0_HI	[7:0]	EQ5_COEF0_HI								0x00	MMRW
0xA9	EQ5_COEF0_LO	[7:0]	EQ5_COEF0_LO								0x00	MMRW
0xAA	EQ5_COEF1_HI	[7:0]	EQ5_COEF1_HI								0x00	MMRW
0xAB	EQ5_COEF1_LO	[7:0]	EQ5_COEF1_LO								0x00	MMRW
0xAC	EQ5_COEF2_HI	[7:0]	EQ5_COEF2_HI								0x00	MMRW
0xAD	EQ5_COEF2_LO	[7:0]	EQ5_COEF2_LO								0x00	MMRW
0xAE	EQ5_COEF3_HI	[7:0]	EQ5_COEF3_HI								0x00	MMRW
0xAF	EQ5_COEF3_LO	[7:0]	EQ5_COEF3_LO								0x00	MMRW
0xB0	EQ5_COEF4_HI	[7:0]	EQ5_COEF4_HI								0x00	MMRW
0xB1	EQ5_COEF4_LO	[7:0]	EQ5_COEF4_LO								0x00	MMRW
0xB2	EQ6_COEF0_HI	[7:0]	EQ6_COEF0_HI								0x00	MMRW
0xB3	EQ6_COEF0_LO	[7:0]	EQ6_COEF0_LO								0x00	MMRW
0xB4	EQ6_COEF1_HI	[7:0]	EQ6_COEF1_HI								0x00	MMRW
0xB5	EQ6_COEF1_LO	[7:0]	EQ6_COEF1_LO								0x00	MMRW
0xB6	EQ6_COEF2_HI	[7:0]	EQ6_COEF2_HI								0x00	MMRW
0xB7	EQ6_COEF2_LO	[7:0]	EQ6_COEF2_LO								0x00	MMRW

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0xB8	EQ7_COEF0_HI	[7:0]	EQ7_COEF0_HI								0x00	MMRW
0xB9	EQ7_COEF0_LO	[7:0]	EQ7_COEF0_LO								0x00	MMRW
0xBA	EQ7_COEF1_HI	[7:0]	EQ7_COEF1_HI								0x00	MMRW
0xBB	EQ7_COEF1_LO	[7:0]	EQ7_COEF1_LO								0x00	MMRW
0xBC	EQ7_COEF2_HI	[7:0]	EQ7_COEF2_HI								0x00	MMRW
0xBD	EQ7_COEF2_LO	[7:0]	EQ7_COEF2_LO								0x00	MMRW

EQ1_COEF0_HI REGISTER

Address: 0x80, Reset: 0x00, Name: EQ1_COEF0_HI

Equalizer 1 Coefficient 0 Upper Byte

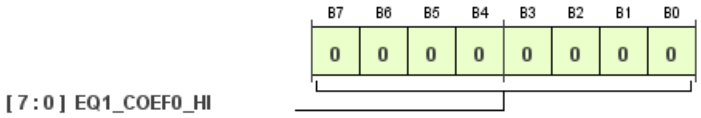


Table 246. Bit Descriptions for EQ1_COEF0_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ1_COEF0_HI		EQ1 Coefficient. Equalizer 1 Coefficient 0 Upper Byte.	0x00	RW

EQ1_COEF0_LO REGISTER

Address: 0x81, Reset: 0x00, Name: EQ1_COEF0_LO

Equalizer 1 Coefficient 0 Lower Byte

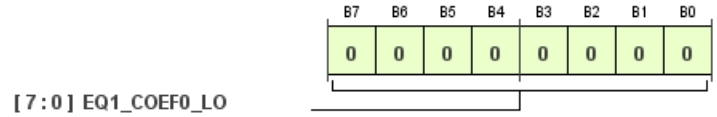


Table 247. Bit Descriptions for EQ1_COEF0_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ1_COEF0_LO		EQ1 Coefficient. Equalizer 1 Coefficient 0 Lower Byte.	0x00	RW

EQ1_COEF1_HI REGISTER

Address: 0x82, Reset: 0x00, Name: EQ1_COEF1_HI

Equalizer 1 Coefficient 1 Upper Byte

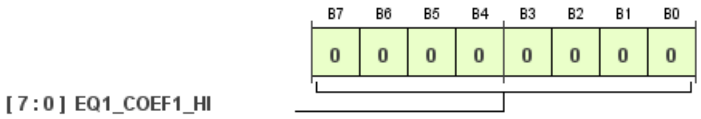


Table 248. Bit Descriptions for EQ1_COEF1_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ1_COEF1_HI		EQ1 Coefficient. Equalizer 1 Coefficient 1 Upper Byte.	0x00	RW

EQ1_COEF1_LO REGISTER

Address: 0x83, Reset: 0x00, Name: EQ1_COEF1_LO

Equalizer 1 Coefficient 1 Lower Byte

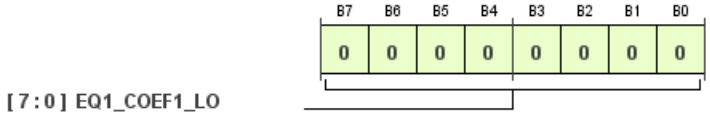


Table 249. Bit Descriptions for EQ1_COEF1_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ1_COEF1_LO		EQ1 Coefficient. Equalizer 1 Coefficient 1 Lower Byte.	0x00	RW

EQ1_COEF2_HI REGISTER

Address: 0x84, Reset: 0x00, Name: EQ1_COEF2_HI

Equalizer 1 Coefficient 2 Upper Byte

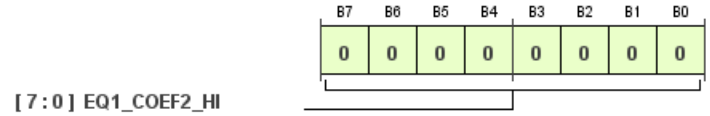


Table 250. Bit Descriptions for EQ1_COEF2_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ1_COEF2_HI		EQ1 Coefficient. Equalizer 1 Coefficient 2 Upper Byte.	0x00	RW

EQ1_COEF2_LO REGISTER

Address: 0x85, Reset: 0x00, Name: EQ1_COEF2_LO

Equalizer 1 Coefficient 2 Lower Byte

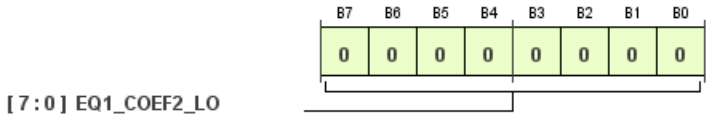


Table 251. Bit Descriptions for EQ1_COEF2_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ1_COEF2_LO		EQ1 Coefficient. Equalizer 1 Coefficient 2 Lower Byte.	0x00	RW

EQ1_COEF3_HI REGISTER

Address: 0x86, Reset: 0x00, Name: EQ1_COEF3_HI

Equalizer 1 Coefficient 3 Upper Byte

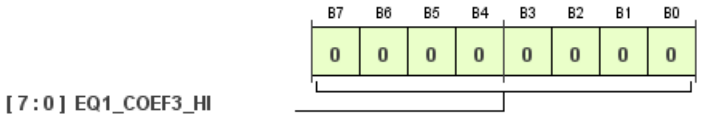


Table 252. Bit Descriptions for EQ1_COEF3_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ1_COEF3_HI		EQ1 Coefficient. Equalizer 1 Coefficient 3 Upper Byte.	0x00	RW

EQ1_COEF3_LO REGISTER

Address: 0x87, Reset: 0x00, Name: EQ1_COEF3_LO

Equalizer 1 Coefficient 3 Lower Byte

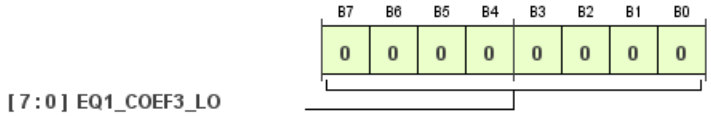


Table 253. Bit Descriptions for EQ1_COEF3_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ1_COEF3_LO		EQ1 Coefficient. Equalizer 1 Coefficient 3 Lower Byte.	0x00	RW

EQ1_COEF4_HI REGISTER

Address: 0x88, Reset: 0x00, Name: EQ1_COEF4_HI

Equalizer 1 Coefficient 4 Upper Byte

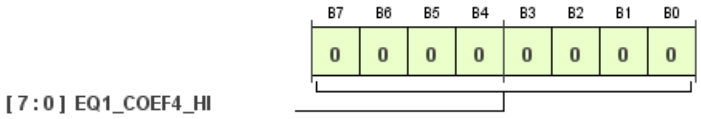


Table 254. Bit Descriptions for EQ1_COEF4_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ1_COEF4_HI		EQ1 Coefficient. Equalizer 1 Coefficient 4 Upper Byte.	0x00	RW

EQ1_COEF4_LO REGISTER

Address: 0x89, Reset: 0x00, Name: EQ1_COEF4_LO

Equalizer 1 Coefficient 4 Lower Byte

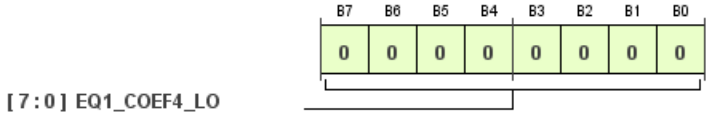


Table 255. Bit Descriptions for EQ1_COEF4_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ1_COEF4_LO		EQ1 Coefficient. Equalizer 1 Coefficient 4 Lower Byte.	0x00	RW

EQ2_COEF0_HI REGISTER

Address: 0x8A, Reset: 0x00, Name: EQ2_COEF0_HI

Equalizer 2 Coefficient 0 Upper Byte

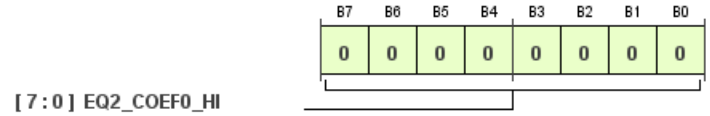


Table 256. Bit Descriptions for EQ2_COEF0_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ2_COEF0_HI		EQ2 Coefficient. Equalizer 2 Coefficient 0 Upper Byte.	0x00	RW

EQ2_COEF0_LO REGISTER

Address: 0x8B, Reset: 0x00, Name: EQ2_COEF0_LO

Equalizer 2 Coefficient 0 Lower Byte

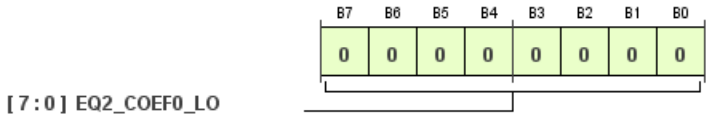


Table 257. Bit Descriptions for EQ2_COEF0_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ2_COEF0_LO		EQ2 Coefficient. Equalizer 2 Coefficient 0 Lower Byte.	0x00	RW

EQ2_COEF1_HI REGISTER

Address: 0x8C, Reset: 0x00, Name: EQ2_COEF1_HI

Equalizer 2 Coefficient 1 Upper Byte

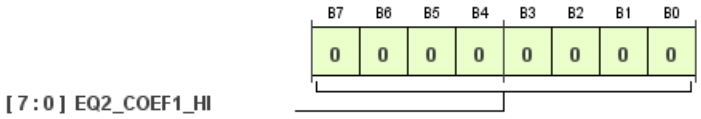


Table 258. Bit Descriptions for EQ2_COEF1_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ2_COEF1_HI		EQ2 Coefficient. Equalizer 2 Coefficient 1 Upper Byte.	0x00	RW

EQ2_COEF1_LO REGISTER

Address: 0x8D, Reset: 0x00, Name: EQ2_COEF1_LO

Equalizer 2 Coefficient 1 Lower Byte

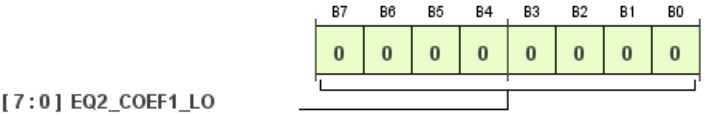


Table 259. Bit Descriptions for EQ2_COEF1_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ2_COEF1_LO		EQ2 Coefficient. Equalizer 2 Coefficient 1 Lower Byte.	0x00	RW

EQ2_COEF2_HI REGISTER

Address: 0x8E, Reset: 0x00, Name: EQ2_COEF2_HI

Equalizer 2 Coefficient 2 Upper Byte

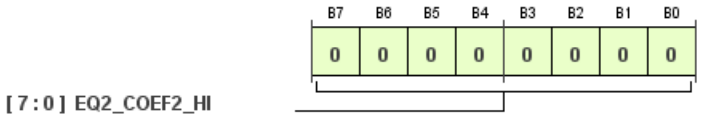


Table 260. Bit Descriptions for EQ2_COEF2_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ2_COEF2_HI		EQ2 Coefficient. Equalizer 2 Coefficient 2 Upper Byte.	0x00	RW

EQ2_COEF2_LO REGISTER

Address: 0x8F, Reset: 0x00, Name: EQ2_COEF2_LO

Equalizer 2 Coefficient 2 Lower Byte

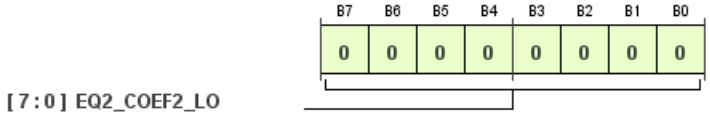


Table 261. Bit Descriptions for EQ2_COEF2_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ2_COEF2_LO		EQ2 Coefficient. Equalizer 2 Coefficient 2 Lower Byte.	0x00	RW

EQ2_COEF3_HI REGISTER

Address: 0x90, Reset: 0x00, Name: EQ2_COEF3_HI

Equalizer 2 Coefficient 3 Upper Byte

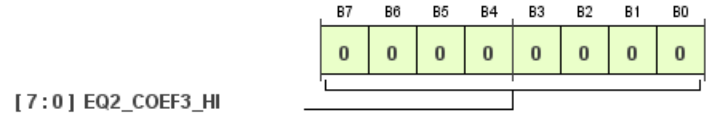


Table 262. Bit Descriptions for EQ2_COEF3_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ2_COEF3_HI		EQ2 Coefficient. Equalizer 2 Coefficient 3 Upper Byte.	0x00	RW

EQ2_COEF3_LO REGISTER

Address: 0x91, Reset: 0x00, Name: EQ2_COEF3_LO

Equalizer 2 Coefficient 3 Lower Byte

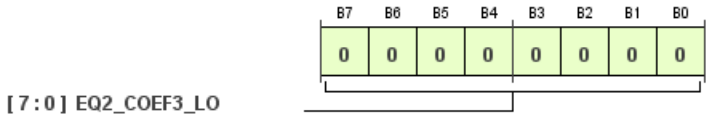


Table 263. Bit Descriptions for EQ2_COEF3_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ2_COEF3_LO		EQ2 Coefficient. Equalizer 2 Coefficient 3 Lower Byte.	0x00	RW

EQ2_COEF4_HI REGISTER

Address: 0x92, Reset: 0x00, Name: EQ2_COEF4_HI

Equalizer 2 Coefficient 4 Upper Byte

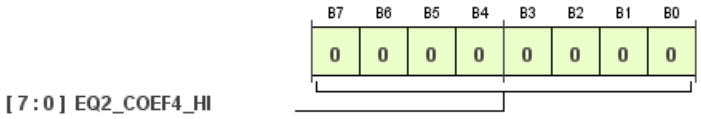


Table 264. Bit Descriptions for EQ2_COEF4_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ2_COEF4_HI		EQ2 Coefficient. Equalizer 2 Coefficient 4 Upper Byte.	0x00	RW

EQ2_COEF4_LO REGISTER

Address: 0x93, Reset: 0x00, Name: EQ2_COEF4_LO

Equalizer 2 Coefficient 4 Lower Byte

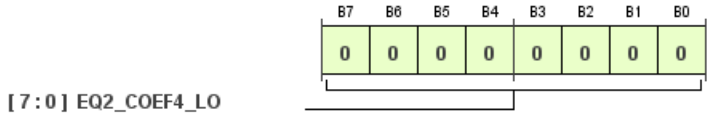


Table 265. Bit Descriptions for EQ2_COEF4_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ2_COEF4_LO		EQ2 Coefficient. Equalizer 2 Coefficient 4 Lower Byte.	0x00	RW

EQ3_COEF0_HI REGISTER

Address: 0x94, Reset: 0x00, Name: EQ3_COEF0_HI

Equalizer 3 Coefficient 0 Upper Byte

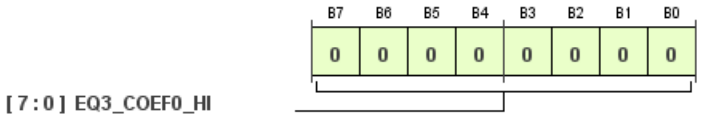


Table 266. Bit Descriptions for EQ3_COEF0_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ3_COEF0_HI		EQ3 Coefficient. Equalizer 3 Coefficient 0 Upper Byte.	0x00	RW

EQ3_COEF0_LO REGISTER

Address: 0x95, Reset: 0x00, Name: EQ3_COEF0_LO

Equalizer 3 Coefficient 0 Lower Byte

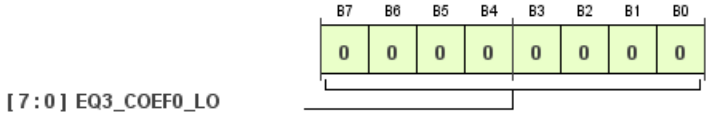


Table 267. Bit Descriptions for EQ3_COEF0_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ3_COEF0_LO		EQ3 Coefficient. Equalizer 3 Coefficient 0 Lower Byte.	0x00	RW

EQ3_COEF1_HI REGISTER

Address: 0x96, Reset: 0x00, Name: EQ3_COEF1_HI

Equalizer 3 Coefficient 1 Upper Byte

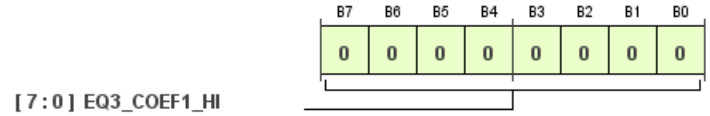


Table 268. Bit Descriptions for EQ3_COEF1_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ3_COEF1_HI		EQ3 Coefficient. Equalizer 3 Coefficient 1 Upper Byte.	0x00	RW

EQ3_COEF1_LO REGISTER

Address: 0x97, Reset: 0x00, Name: EQ3_COEF1_LO

Equalizer 3 Coefficient 1 Lower Byte

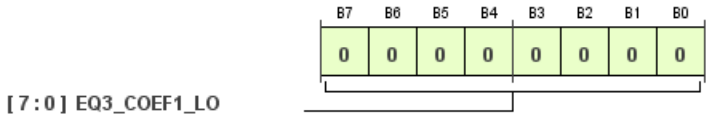


Table 269. Bit Descriptions for EQ3_COEF1_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ3_COEF1_LO		EQ3 Coefficient. Equalizer 3 Coefficient 1 Lower Byte.	0x00	RW

EQ3_COEF2_HI REGISTER

Address: 0x98, Reset: 0x00, Name: EQ3_COEF2_HI

Equalizer 3 Coefficient 2 Upper Byte

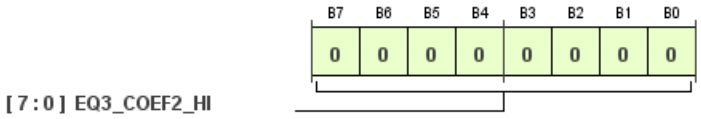


Table 270. Bit Descriptions for EQ3_COEF2_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ3_COEF2_HI		EQ3 Coefficient. Equalizer 3 Coefficient 2 Upper Byte.	0x00	RW

EQ3_COEF2_LO REGISTER

Address: 0x99, Reset: 0x00, Name: EQ3_COEF2_LO

Equalizer 3 Coefficient 2 Lower Byte

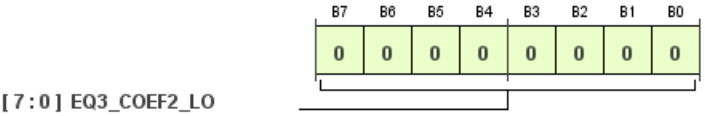


Table 271. Bit Descriptions for EQ3_COEF2_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ3_COEF2_LO		EQ3 Coefficient. Equalizer 3 Coefficient 2 Lower Byte.	0x00	RW

EQ3_COEF3_HI REGISTER

Address: 0x9A, Reset: 0x00, Name: EQ3_COEF3_HI

Equalizer 3 Coefficient 3 Upper Byte

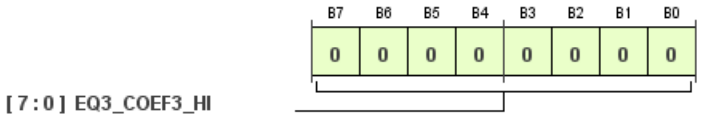


Table 272. Bit Descriptions for EQ3_COEF3_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ3_COEF3_HI		EQ3 Coefficient. Equalizer 3 Coefficient 3 Upper Byte.	0x00	RW

EQ3_COEF3_LO REGISTER

Address: 0x9B, Reset: 0x00, Name: EQ3_COEF3_LO

Equalizer 3 Coefficient 3 Lower Byte

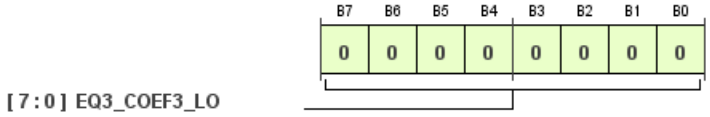


Table 273. Bit Descriptions for EQ3_COEF3_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ3_COEF3_LO		EQ3 Coefficient. Equalizer 3 Coefficient 3 Lower Byte.	0x00	RW

EQ3_COEF4_HI REGISTER

Address: 0x9C, Reset: 0x00, Name: EQ3_COEF4_HI

Equalizer 3 Coefficient 4 Upper Byte

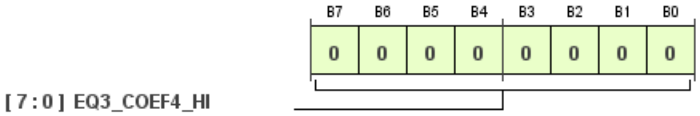


Table 274. Bit Descriptions for EQ3_COEF4_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ3_COEF4_HI		EQ3 Coefficient. Equalizer 3 Coefficient 4 Upper Byte.	0x00	RW

EQ3_COEF4_LO REGISTER

Address: 0x9D, Reset: 0x00, Name: EQ3_COEF4_LO

Equalizer 3 Coefficient 4 Lower Byte

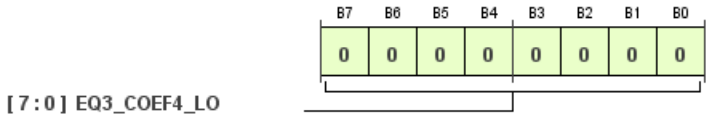


Table 275. Bit Descriptions for EQ3_COEF4_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ3_COEF4_LO		EQ3 Coefficient. Equalizer 3 Coefficient 4 Lower Byte.	0x00	RW

EQ4_COEF0_HI REGISTER

Address: 0x9E, Reset: 0x00, Name: EQ4_COEF0_HI

Equalizer 4 Coefficient 0 Upper Byte

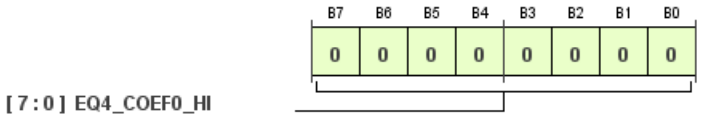


Table 276. Bit Descriptions for EQ4_COEF0_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ4_COEF0_HI		EQ4 Coefficient. Equalizer 4 Coefficient 0 Upper Byte.	0x00	RW

EQ4_COEF0_LO REGISTER

Address: 0x9F, Reset: 0x00, Name: EQ4_COEF0_LO

Equalizer 4 Coefficient 0 Lower Byte

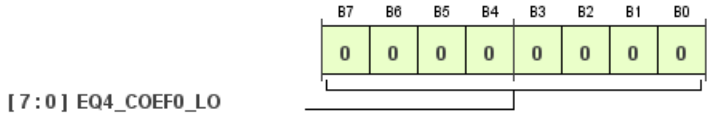


Table 277. Bit Descriptions for EQ4_COEF0_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ4_COEF0_LO		EQ4 Coefficient. Equalizer 4 Coefficient 0 Lower Byte.	0x00	RW

EQ4_COEF1_HI REGISTER

Address: 0xA0, Reset: 0x00, Name: EQ4_COEF1_HI

Equalizer 4 Coefficient 1 Upper Byte

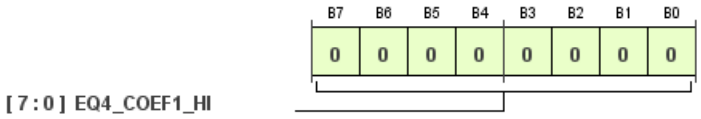


Table 278. Bit Descriptions for EQ4_COEF1_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ4_COEF1_HI		EQ4 Coefficient. Equalizer 4 Coefficient 1 Upper Byte.	0x00	RW

EQ4_COEF1_LO REGISTER

Address: 0xA1, Reset: 0x00, Name: EQ4_COEF1_LO

Equalizer 4 Coefficient 1 Lower Byte

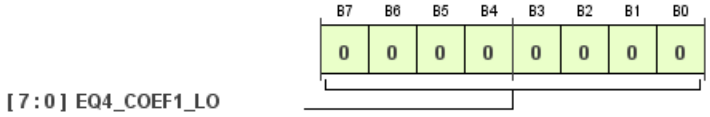


Table 279. Bit Descriptions for EQ4_COEF1_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ4_COEF1_LO		EQ4 Coefficient. Equalizer 4 Coefficient 1 Lower Byte.	0x00	RW

EQ4_COEF2_HI REGISTER

Address: 0xA2, Reset: 0x00, Name: EQ4_COEF2_HI

Equalizer 4 Coefficient 2 Upper Byte

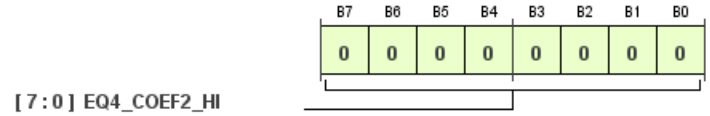


Table 280. Bit Descriptions for EQ4_COEF2_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ4_COEF2_HI		EQ4 Coefficient. Equalizer 4 Coefficient 2 Upper Byte.	0x00	RW

EQ4_COEF2_LO REGISTER

Address: 0xA3, Reset: 0x00, Name: EQ4_COEF2_LO

Equalizer 4 Coefficient 2 Lower Byte

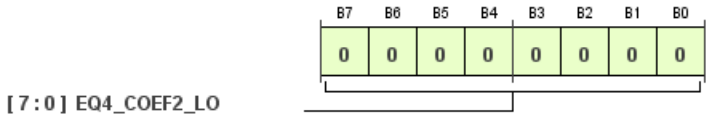


Table 281. Bit Descriptions for EQ4_COEF2_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ4_COEF2_LO		EQ4 Coefficient. Equalizer 4 Coefficient 2 Lower Byte.	0x00	RW

EQ4_COEF3_HI REGISTER

Address: 0xA4, Reset: 0x00, Name: EQ4_COEF3_HI

Equalizer 4 Coefficient 3 Upper Byte

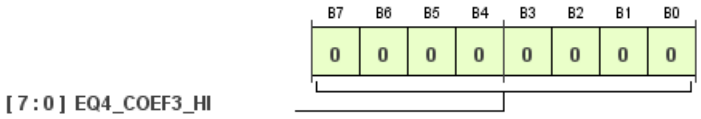


Table 282. Bit Descriptions for EQ4_COEF3_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ4_COEF3_HI		EQ4 Coefficient. Equalizer 4 Coefficient 3 Upper Byte.	0x00	RW

EQ4_COEF3_LO REGISTER

Address: 0xA5, Reset: 0x00, Name: EQ4_COEF3_LO

Equalizer 4 Coefficient 3 Lower Byte

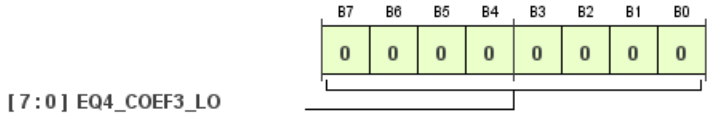


Table 283. Bit Descriptions for EQ4_COEF3_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ4_COEF3_LO		EQ4 Coefficient. Equalizer 4 Coefficient 3 Lower Byte.	0x00	RW

EQ4_COEF4_HI REGISTER

Address: 0xA6, Reset: 0x00, Name: EQ4_COEF4_HI

Equalizer 4 Coefficient 4 Upper Byte

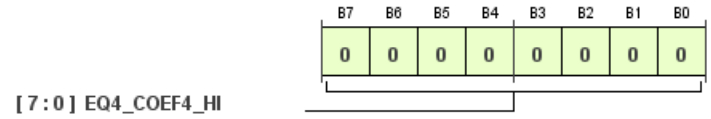


Table 284. Bit Descriptions for EQ4_COEF4_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ4_COEF4_HI		EQ4 Coefficient. Equalizer 4 Coefficient 4 Upper Byte.	0x00	RW

EQ4_COEF4_LO REGISTER

Address: 0xA7, Reset: 0x00, Name: EQ4_COEF4_LO

Equalizer 4 Coefficient 4 Lower Byte

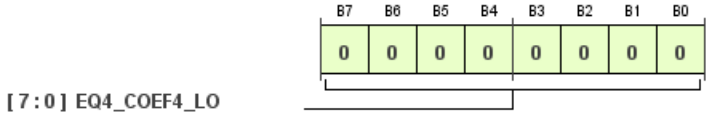


Table 285. Bit Descriptions for EQ4_COEF4_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ4_COEF4_LO		EQ4 Coefficient. Equalizer 4 Coefficient 4 Lower Byte.	0x00	RW

EQ5_COEF0_HI REGISTER

Address: 0xA8, Reset: 0x00, Name: EQ5_COEF0_HI

Equalizer 5 Coefficient 0 Upper Byte

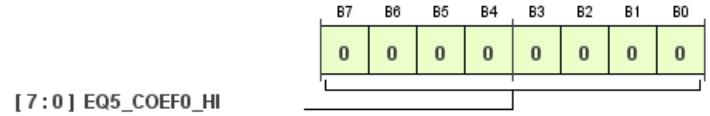


Table 286. Bit Descriptions for EQ5_COEF0_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ5_COEF0_HI		EQ5 Coefficient. Equalizer 5 Coefficient 0 Upper Byte.	0x00	RW

EQ5_COEF0_LO REGISTER

Address: 0xA9, Reset: 0x00, Name: EQ5_COEF0_LO

Equalizer 5 Coefficient 0 Lower Byte

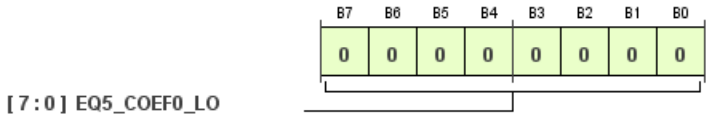


Table 287. Bit Descriptions for EQ5_COEF0_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ5_COEF0_LO		EQ5 Coefficient. Equalizer 5 Coefficient 0 Lower Byte.	0x00	RW

EQ5_COEF1_HI REGISTER

Address: 0xAA, Reset: 0x00, Name: EQ5_COEF1_HI

Equalizer 5 Coefficient 1 Upper Byte

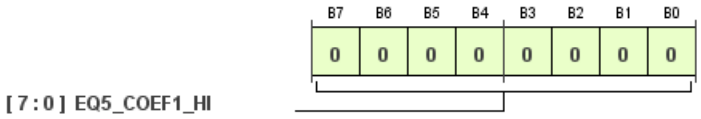


Table 288. Bit Descriptions for EQ5_COEF1_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ5_COEF1_HI		EQ5 Coefficient. Equalizer 5 Coefficient 1 Upper Byte.	0x00	RW

EQ5_COEF1_LO REGISTER

Address: 0xAB, Reset: 0x00, Name: EQ5_COEF1_LO

Equalizer 5 Coefficient 1 Lower Byte

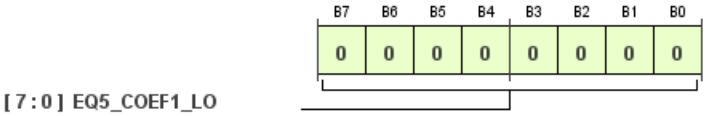


Table 289. Bit Descriptions for EQ5_COEF1_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ5_COEF1_LO		EQ5 Coefficient. Equalizer 5 Coefficient 1 Lower Byte.	0x00	RW

EQ5_COEF2_HI REGISTER

Address: 0xAC, Reset: 0x00, Name: EQ5_COEF2_HI

Equalizer 5 Coefficient 2 Upper Byte

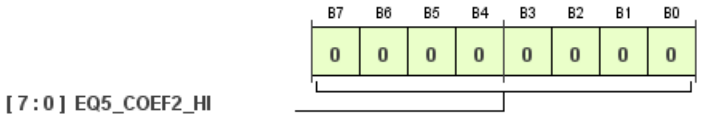


Table 290. Bit Descriptions for EQ5_COEF2_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ5_COEF2_HI		EQ5 Coefficient. Equalizer 5 Coefficient 2 Upper Byte.	0x00	RW

EQ5_COEF2_LO REGISTER

Address: 0xAD, Reset: 0x00, Name: EQ5_COEF2_LO

Equalizer 5 Coefficient 2 Lower Byte

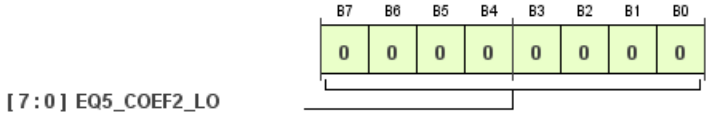


Table 291. Bit Descriptions for EQ5_COEF2_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ5_COEF2_LO		EQ5 Coefficient. Equalizer 5 Coefficient 2 Lower Byte.	0x00	RW

EQ5_COEF3_HI REGISTER

Address: 0xAE, Reset: 0x00, Name: EQ5_COEF3_HI

Equalizer 5 Coefficient 3 Upper Byte

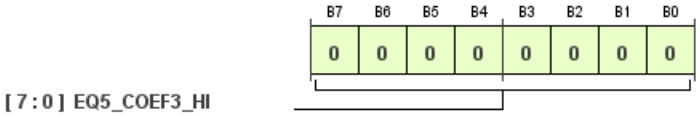


Table 292. Bit Descriptions for EQ5_COEF3_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ5_COEF3_HI		EQ5 Coefficient. Equalizer 5 Coefficient 3 Upper Byte.	0x00	RW

EQ5_COEF3_LO REGISTER

Address: 0xAF, Reset: 0x00, Name: EQ5_COEF3_LO

Equalizer 5 Coefficient 3 Lower Byte

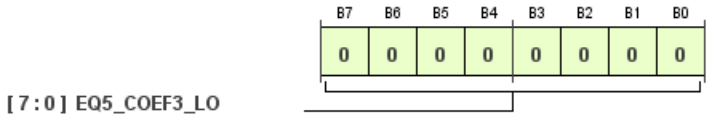


Table 293. Bit Descriptions for EQ5_COEF3_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ5_COEF3_LO		EQ5 Coefficient. Equalizer 5 Coefficient 3 Lower Byte.	0x00	RW

EQ5_COEF4_HI REGISTER

Address: 0xB0, Reset: 0x00, Name: EQ5_COEF4_HI

Equalizer 5 Coefficient 4 Upper Byte

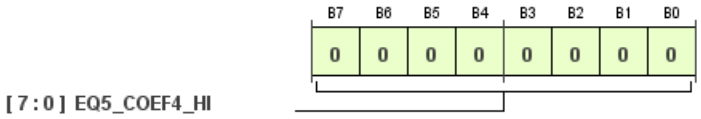


Table 294. Bit Descriptions for EQ5_COEF4_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ5_COEF4_HI		EQ5 Coefficient. Equalizer 5 Coefficient 4 Upper Byte.	0x00	RW

EQ5_COEF4_LO REGISTER

Address: 0xB1, Reset: 0x00, Name: EQ5_COEF4_LO

Equalizer 5 Coefficient 4 Lower Byte

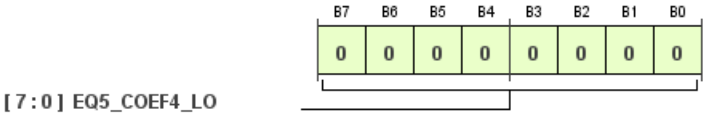


Table 295. Bit Descriptions for EQ5_COEF4_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ5_COEF4_LO		EQ5 Coefficient. Equalizer 5 Coefficient 4 Lower Byte.	0x00	RW

EQ6_COEF0_HI REGISTER

Address: 0xB2, Reset: 0x00, Name: EQ6_COEF0_HI

Equalizer 6 Coefficient 0 Upper Byte

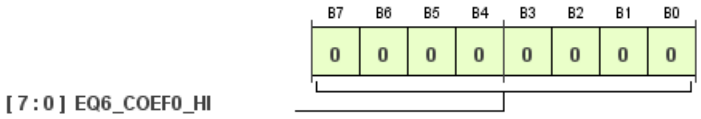


Table 296. Bit Descriptions for EQ6_COEF0_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ6_COEF0_HI		EQ6 Coefficient. Equalizer 6 Coefficient 0 Upper Byte.	0x00	RW

EQ6_COEF0_LO REGISTER

Address: 0xB3, Reset: 0x00, Name: EQ6_COEF0_LO

Equalizer 6 Coefficient 0 Lower Byte

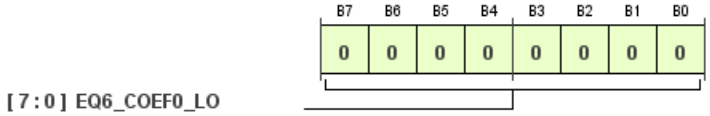


Table 297. Bit Descriptions for EQ6_COEF0_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ6_COEF0_LO		EQ6 Coefficient. Equalizer 6 Coefficient 0 Lower Byte.	0x00	RW

EQ6_COEF1_HI REGISTER

Address: 0xB4, Reset: 0x00, Name: EQ6_COEF1_HI

Equalizer 6 Coefficient 1 Upper Byte

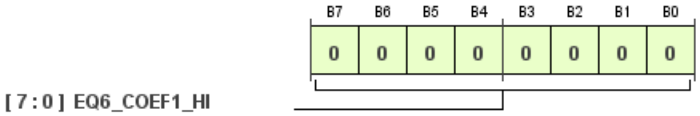


Table 298. Bit Descriptions for EQ6_COEF1_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ6_COEF1_HI		EQ6 Coefficient. Equalizer 6 Coefficient 1 Upper Byte.	0x00	RW

EQ6_COEF1_LO REGISTER

Address: 0xB5, Reset: 0x00, Name: EQ6_COEF1_LO

Equalizer 6 Coefficient 1 Lower Byte

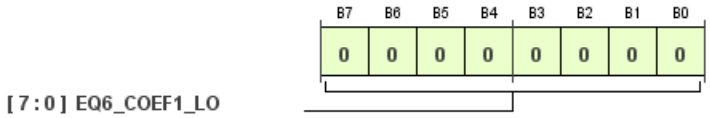


Table 299. Bit Descriptions for EQ6_COEF1_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ6_COEF1_LO		EQ6 Coefficient. Equalizer 6 Coefficient 1 Lower Byte.	0x00	RW

EQ6_COEF2_HI REGISTER

Address: 0xB6, Reset: 0x00, Name: EQ6_COEF2_HI

Equalizer 6 Coefficient 2 Upper Byte

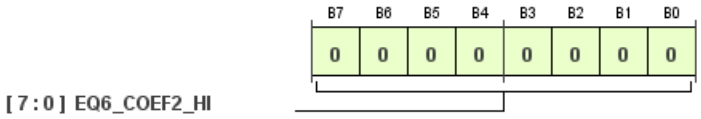


Table 300. Bit Descriptions for EQ6_COEF2_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ6_COEF2_HI		EQ6 Coefficient. Equalizer 6 Coefficient 2 Upper Byte.	0x00	RW

EQ6_COEF2_LO REGISTER

Address: 0xB7, Reset: 0x00, Name: EQ6_COEF2_LO

Equalizer 6 Coefficient 2 Lower Byte

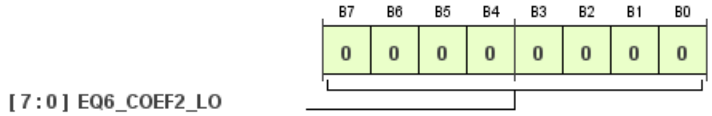


Table 301. Bit Descriptions for EQ6_COEF2_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ6_COEF2_LO		EQ6 Coefficient. Equalizer 6 Coefficient 2 Lower Byte.	0x00	RW

EQ7_COEF0_HI REGISTER

Address: 0xB8, Reset: 0x00, Name: EQ7_COEF0_HI

Equalizer 7 Coefficient 0 Upper Byte

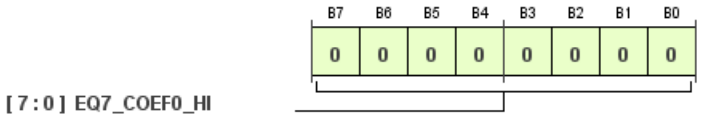


Table 302. Bit Descriptions for EQ7_COEF0_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ7_COEF0_HI		EQ7 Coefficient. Equalizer 7 Coefficient 0 Upper Byte.	0x00	RW

EQ7_COEF0_LO REGISTER

Address: 0xB9, Reset: 0x00, Name: EQ7_COEF0_LO

Equalizer 7 Coefficient 0 Lower Byte

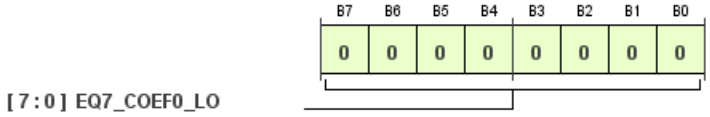


Table 303. Bit Descriptions for EQ7_COEF0_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ7_COEF0_LO		EQ7 Coefficient. Equalizer 7 Coefficient 0 Lower Byte.	0x00	RW

EQ7_COEF1_HI REGISTER

Address: 0xBA, Reset: 0x00, Name: EQ7_COEF1_HI

Equalizer 7 Coefficient 1 Upper Byte

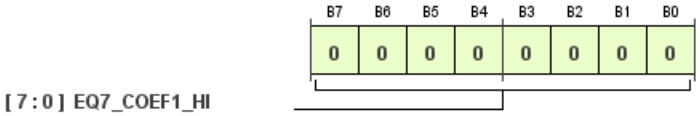


Table 304. Bit Descriptions for EQ7_COEF1_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ7_COEF1_HI		EQ7 Coefficient. Equalizer 7 Coefficient 1 Upper Byte.	0x00	RW

EQ7_COEF1_LO REGISTER

Address: 0xBB, Reset: 0x00, Name: EQ7_COEF1_LO

Equalizer 7 Coefficient 1 Lower Byte

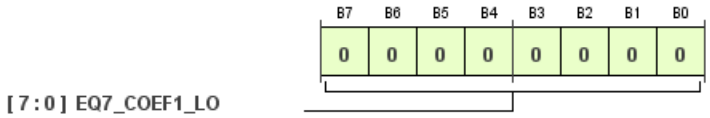


Table 305. Bit Descriptions for EQ7_COEF1_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ7_COEF1_LO		EQ7 Coefficient. Equalizer 7 Coefficient 1 Lower Byte.	0x00	RW

EQ7_COEF2_HI REGISTER

Address: 0xBC, Reset: 0x00, Name: EQ7_COEF2_HI

Equalizer 7 Coefficient 2 Upper Byte

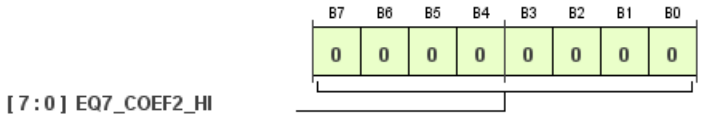


Table 306. Bit Descriptions for EQ7_COEF2_HI

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ7_COEF2_HI		EQ7 Coefficient. Equalizer 7 Coefficient 2 Upper Byte.	0x00	RW

EQ7_COEF2_LO REGISTER

Address: 0xBD, Reset: 0x00, Name: EQ7_COEF2_LO

Equalizer 7 Coefficient 2 Lower Byte

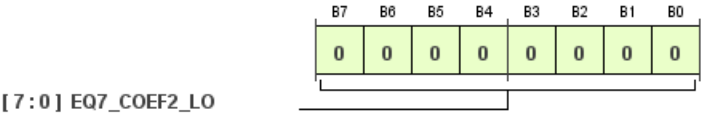
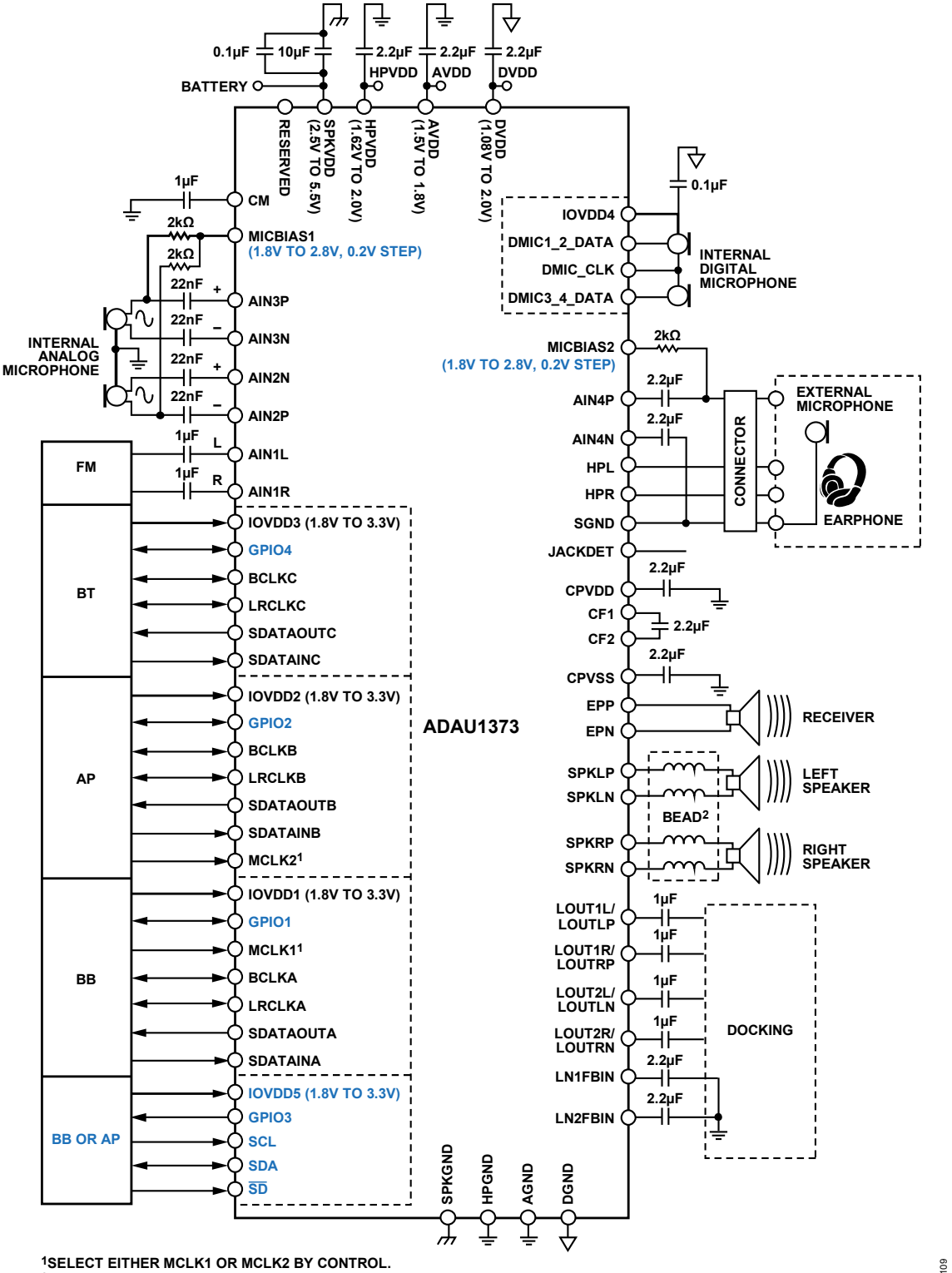


Table 307. Bit Descriptions for EQ7_COEF2_LO

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	EQ7_COEF2_LO		EQ7 Coefficient. Equalizer 7 Coefficient 2 Lower Byte.	0x00	RW

APPLICATIONS CIRCUIT



[1]SELECT EITHER MCLK1 OR MCLK2 BY CONTROL.
[2]REQUIRED FOR EMI SENSITIVE APPLICATIONS WHERE THE OUTPUT SPEAKER TRACE PLUS THE CABLE LENGTH EXCEED 4 INCHES.

Figure 123. Typical Stereo Class-D Applications Circuit

OUTLINE DIMENSIONS

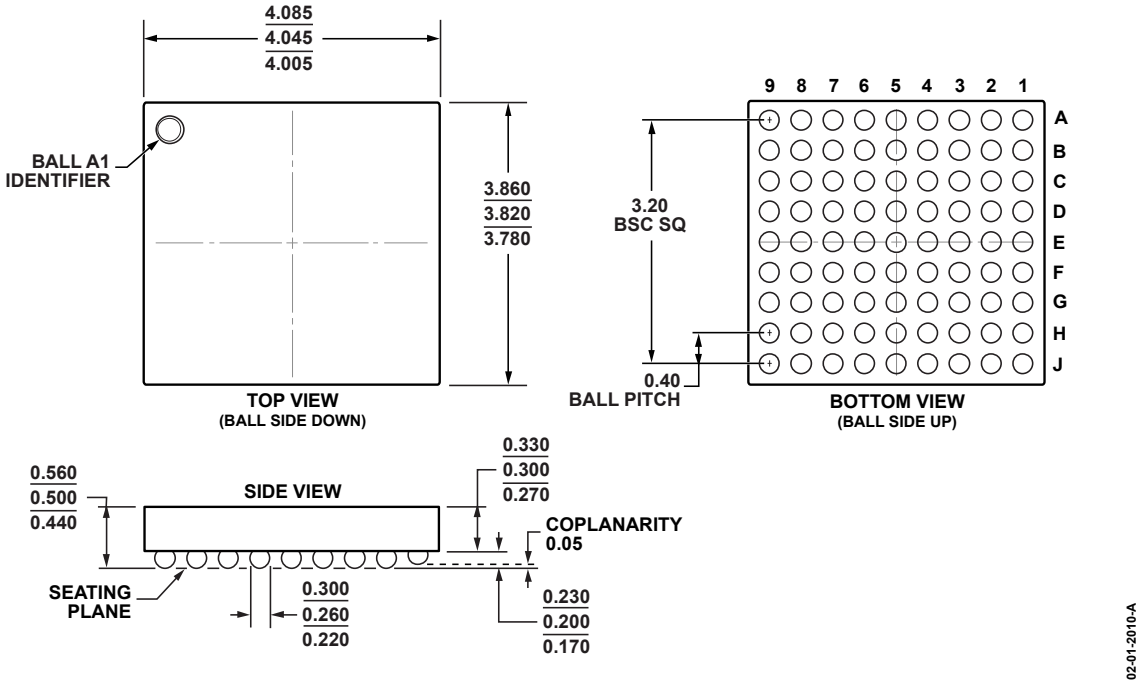


Figure 124. 81-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-81-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADAU1373BCBZ-R7	−40°C to +85°C	81-Ball WLCSP	CB-81-1
ADAU1373BCBZ-RL	−40°C to +85°C	81-Ball WLCSP	CB-81-1
EVAL-ADAU1373Z		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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