4-Channel, Software-Selectable, True Bipolar Input, 12-Bit Plus Sign ADC

Data Sheet **AD7324**

FEATURES

- 12-bit plus sign SAR ADC
- True bipolar input ranges
- Software-selectable input ranges
  - ±10 V, ±5 V, ±2.5 V, 0 V to +10 V
- 1 MSPS throughput rate
- 4 analog input channels with channel sequencer
- Single-ended, true differential, and pseudo differential analog input capability
- High analog input impedance
- Low power: 21 mW
- Full power signal bandwidth: 22 MHz
- Internal 2.5 V reference
- High speed serial interface
- Power-down modes
- 16-lead TSSOP package
- *i*CMOS™ process technology

FUNCTIONAL BLOCK DIAGRAM

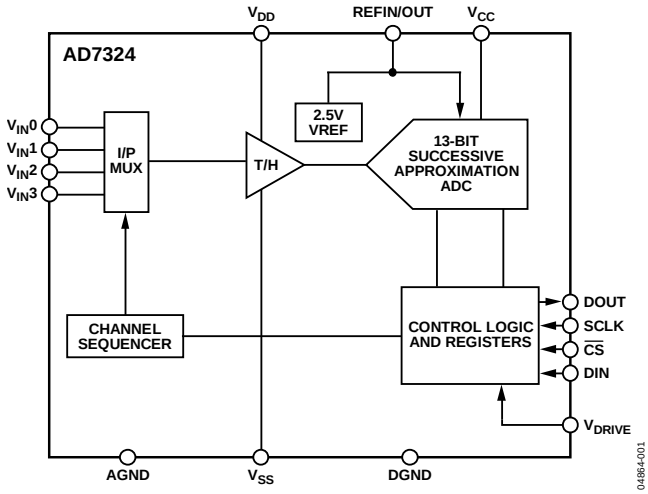

Figure 1.

GENERAL DESCRIPTION

The AD7324[1] is a 4-channel, 12-bit plus sign, successive approximation ADC designed on the *i*CMOS (industrial CMOS) process. *i*CMOS is a process combining high voltage silicon with submicron CMOS and complementary bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage parts could achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can accept bipolar input signals while providing increased performance, dramatically reduced power consumption, and reduced package size.

The AD7324 can accept true bipolar analog input signals. The AD7324 has four software-selectable input ranges: ±10 V, ±5 V, ±2.5 V, and 0 V to +10 V. Each analog input channel can be independently programmed to one of the four input ranges. The analog input channels on the AD7324 can be programmed to be single-ended, true differential, or pseudo differential.

The ADC contains a 2.5 V internal reference. The AD7324 also allows for external reference operation. If a 3 V reference is applied to the REFIN/OUT pin, the AD7324 can accept a true bipolar ±12 V analog input. Minimum ±12 V V_{DD} and V_{SS} supplies are required for the ±12 V input range. The ADC has a high speed serial interface that can operate at throughput rates up to 1 MSPS.

[1]Protected by U.S. Patent No. 6,731,232.

PRODUCT HIGHLIGHTS

1. The AD7324 can accept true bipolar analog input signals, ±10 V, ±5 V, ±2.5 V, and 0 V to +10 V unipolar signals.
2. The four analog inputs can be configured as four single-ended inputs, two true differential input pairs, two pseudo differential inputs, or three pseudo differential inputs.
3. 1 MSPS serial interface. SPI®-/QSPI™-/DSP-/MICROWIRE™-compatible interface.
4. Low power, 31 mW maximum, at 1 MSPS throughput rate.
5. Channel sequencer.

Table 1. Similar Products Selection Table

Device Number	Throughput Rate	Number of bits	Number of Channels
AD7329	1000 kSPS	12-bit plus sign	8
AD7328	1000 kSPS	12-bit plus sign	8
AD7327	500 kSPS	12-bit plus sign	8
AD7323	500 kSPS	12-bit plus sign	4
AD7322	1000 kSPS	12-bit plus sign	2
AD7321	500 kSPS	12-bit plus sign	2

Rev. B Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

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Added Power Supply Configuration Section, Figure 54, and Table 16 ... 33

12/05—Revision 0: Initial Version

SPECIFICATIONS

Unless otherwise noted, V_{DD} = 12 V to 16.5 V, V_{SS} = −12 V to −16.5 V, V_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.7 V to 5.25 V, V_{REF} = 2.5 V to 3.0 V internal/external, f_{SCLK} = 20 MHz, f_S = 1 MSPS, T_A = T_{MAX} to T_{MIN}; For V_{CC} < 4.75 V, all specifications are typical.

Table 2.

	B Version				
Parameter[1]	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
DYNAMIC PERFORMANCE					F_{IN} = 50 kHz sine wave
Signal-to-Noise Ratio (SNR)[2]	76			dB	Differential mode
	72.5			dB	Single-ended/pseudo differential mode
Signal-to-Noise + Distortion (SINAD)[2]	75			dB	Differential mode; ±2.5 V and ±5 V ranges
		76		dB	Differential mode; 0 V to 10 V and ±10 V ranges
	72			dB	Single-ended/pseudo differential mode; ±2.5 V and ±5 V ranges
		72.5		dB	Single-ended/pseudo differential mode; 0 V to +10 V and ±10 V ranges
Total Harmonic Distortion (THD)[2]			−80	dB	Differential mode; ±2.5 V and ±5 V ranges
		−82		dB	Differential mode; 0 V to +10 V and ±10 V ranges
			−77	dB	Single-ended/pseudo differential mode; ±2.5 V and ±5 V ranges
		−80		dB	Single-ended/pseudo differential mode; 0 V to +10 V and ±10 V ranges
Peak Harmonic or Spurious Noise (SFDR)[2]			−80	dB	Differential mode; ±2.5 V and ±5 V ranges
		−82		dB	Differential mode; 0 V to +10 V and ±10 V ranges
			−78	dB	Single-ended/pseudo differential mode; ±2.5 V and ±5 V ranges
		−79		dB	Single-ended/pseudo differential mode; 0 V to +10 V and ±10 V ranges
Intermodulation Distortion (IMD)[2]					fa = 50 kHz, fb = 30 kHz
Second-Order Terms		−88		dB	
Third-Order Terms		−90		dB	
Aperture Delay[3]		7		ns	
Aperture Jitter[3]		50		ps	
Common-Mode Rejection Ratio (CMRR)[2]		−79		dB	Up to 100 kHz ripple frequency; see Figure 17
Channel-to-Channel Isolation[2]		−72		dB	F_{IN} on unselected channels up to 100 kHz; see Figure 14
Full Power Bandwidth		22		MHz	At 3 dB
		5		MHz	At 0.1 dB
DC ACCURACY[4]					All dc accuracy specifications are typical for 0 V to 10 V mode. Single-ended/pseudo differential mode 1 LSB = FSR/4096, unless otherwise noted. Differential mode 1 LSB = FSR/8192, unless otherwise noted.
Resolution	13			Bits	
No Missing Codes	12-bit plus sign (13 bits)			Bits	Differential mode
	11-bit plus sign (12 bits)			Bits	Single-ended/pseudo differential mode
Integral Nonlinearity[2]			±1.1	LSB	Differential mode
			±1	LSB	Single-ended/pseudo differential mode
		−0.7/+1.2		LSB	Single-ended/pseudo differential mode (LSB = FSR/8192)

Parameter[1]	Min	B Version Typ	Max	Unit	Test Conditions/Comments
Differential Nonlinearity[2]			−0.9/+1.5	LSB	Differential mode; guaranteed no missing codes to 13 bits
			±0.9	LSB	Single-ended mode; guaranteed no missing codes to 12 bits
		−0.7/+1		LSB	Single-ended/pseudo differential mode (LSB = FSR/8192)
Offset Error[2, 5]			−4/+9	LSB	Single-ended/pseudo differential mode
			−7/+10	LSB	Differential mode
Offset Error Match[2, 5]			±0.6	LSB	Single-ended/pseudo differential mode
			±0.5	LSB	Differential mode
Gain Error[2, 5]			±8	LSB	Single-ended/pseudo differential mode
			±14	LSB	Differential mode
Gain Error Match[2, 5]			±0.5	LSB	Single-ended/pseudo differential mode
			±0.5	LSB	Differential mode
Positive Full-Scale Error[2, 6]			±4	LSB	Single-ended/pseudo differential mode
			±7	LSB	Differential mode
Positive Full-Scale Error Match[2, 6]			±0.5	LSB	Single-ended/pseudo differential mode
			±0.5	LSB	Differential mode
Bipolar Zero Error[2, 6]			±8.5	LSB	Single-ended/pseudo differential mode
			±7.5	LSB	Differential mode
Bipolar Zero Error Match[2, 6]			±0.5	LSB	Single-ended/pseudo differential mode
			±0.5	LSB	Differential mode
Negative Full-Scale Error[2, 6]			±4	LSB	Single-ended/pseudo differential mode
			±6	LSB	Differential mode
Negative Full-Scale Error Match[2, 6]			±0.5	LSB	Single-ended/pseudo differential mode
			±0.5	LSB	Differential mode
ANALOG INPUT					
Input Voltage Ranges					Reference = 2.5 V; see Table 6
(Programmed via Range Register)		±10		V	V_{DD} = 10 V min, V_{SS} = −10 V min, V_{CC} = +2.7 V to +5.25 V
		±5		V	V_{DD} = +5 V min, V_{SS} = −5 V min, V_{CC} = +2.7 V to +5.25 V
		±2.5		V	V_{DD} = +5 V min, V_{SS} = −5 V min, V_{CC} = +2.7 V to +5.25 V
		0 to 10		V	V_{DD} = +10 V min, V_{SS} = AGND min, V_{CC} = +2.7 V to +5.25 V
Pseudo Differential V_{IN}(−) Input Range					V_{DD} = +16.5 V, V_{SS} = −16.5 V, V_{CC} = +5 V; see Figure 40 and Figure 41
		±3.5		V	Reference = 2.5 V; range = ±10 V
		±6		V	Reference = 2.5 V; range = ±5 V
		±5		V	Reference = 2.5 V; range = ±2.5 V
		+3/−5		V	Reference = 2.5 V; range = 0 V to +10 V
DC Leakage Current			±80	nA	V_{IN} = V_{DD} or V_{SS}
		3		nA	Per channel, V_{IN} = V_{DD} or V_{SS}
Input Capacitance[3]		13.5		pF	When in track, ±10 V range
		16.5		pF	When in track, ±5 V and 0 V to +10 V ranges
		21.5		pF	When in track, ±2.5 V range
		3		pF	When in hold, all ranges
REFERENCE INPUT/OUTPUT					
Input Voltage Range	2.5		3	V	
Input DC Leakage Current			±1	µA	
Input Capacitance		10		pF	
Reference Output Voltage		2.5		V	
Reference Output Voltage Error at 25°C			±5	mV	

Parameter[1]	B Version Min	Typ	Max	Unit	Test Conditions/Comments
Reference Output Voltage			±10	mV	
T_{MIN} to T_{MAX}					
Reference Temperature Coefficient			25	ppm/°C	
		3		ppm/°C	
Reference Output Impedance		7		Ω	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4			V	
Input Low Voltage, V_{INL}			0.8	V	V_{CC} = 4.75 V to 5.25 V
			0.4	V	V_{CC} = 2.7 V to 3.6 V
Input Current, I_{IN}			±1	μA	V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[3]		10		pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	V_{DRIVE} − 0.2 V			V	I_{SOURCE} = 200 μA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 μA
Floating-State Leakage Current			±1	μA	
Floating-State Output Capacitance[3]		5		pF	
Output Coding	Straight natural binary				Coding bit set to 1 in control register
	Twos complement				Coding bit set to 0 in control register
CONVERSION RATE					
Conversion Time			800	ns	16 SCLK cycles with SCLK = 20 MHz
Track-and-Hold Acquisition Time[2, 3]			305	ns	Full-scale step input; see the Terminology section
Throughput Rate			1	MSPS	See the Serial Interface section; V_{CC} = 4.75 V to 5.25 V
			770	kSPS	V_{CC} < 4.75 V
POWER REQUIREMENTS					Digital inputs = 0 V or V_{DRIVE}
V_{DD}	12		16.5	V	See Table 6
V_{SS}	−12		−16.5	V	See Table 6
V_{CC}	2.7		5.25	V	See Table 6; typical specifications for V_{CC} < 4.75 V
V_{DRIVE}	2.7		5.25	V	
Normal Mode (Static)		0.9		mA	V_{DD}/V_{SS} = ±16.5 V, V_{CC}/V_{DRIVE} = 5.25 V
Normal Mode (Operational)					f_{SAMPLE} = 1 MSPS
I_{DD}			360	μA	V_{DD} = 16.5 V
I_{SS}			410	μA	V_{SS} = −16.5 V
I_{CC} and I_{DRIVE}			3.4	mA	V_{CC}/V_{DRIVE} = 5.25 V
Autostandby Mode (Dynamic)					f_{SAMPLE} = 250 kSPS
I_{DD}			200	μA	V_{DD} = 16.5 V
I_{SS}			210	μA	V_{SS} = −16.5 V
I_{CC} and I_{DRIVE}			1.3	mA	V_{CC}/V_{DRIVE} = 5.25 V
Autoshutdown Mode (Static)					SCLK on or off
I_{DD}			1	μA	V_{DD} = 16.5 V
I_{SS}			1	μA	V_{SS} = −16.5 V
I_{CC} and I_{DRIVE}			1	μA	V_{CC}/V_{DRIVE} = 5.25 V
Full Shutdown Mode					SCLK on or off
I_{DD}			1	μA	V_{DD} = 16.5 V
I_{SS}			1	μA	V_{SS} = −16.5 V
I_{CC} and I_{DRIVE}			1	μA	V_{CC}/V_{DRIVE} = 5.25 V

Parameter[1]	B Version Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION					
Normal Mode (Operational)			31	mW	V_{DD} = +16.5 V, V_{SS} = −16.5 V, V_{CC} = +5.25 V
		21		mW	V_{DD} = +12 V, V_{SS} = −12 V, V_{CC} = +5 V
Full Shutdown Mode			38.25	µW	V_{DD} = +16.5 V, V_{SS} = −16.5 V, V_{CC} = +5.25 V

[1] Temperature range is −40°C to +85°C.
[2] See the Terminology section.
[3] Sample tested during initial release to ensure compliance.
[4] For dc accuracy specifications, the LSB size for differential mode is FSR/8192. For single-ended mode/pseudo differential mode, the LSB size is FSR/4096, unless otherwise noted.
[5] Unipolar 0 V to 10 V range with straight binary output coding.
[6] Bipolar range with twos complement output coding.

TIMING SPECIFICATIONS

V_{DD} = 12 V to 16.5 V, V_{SS} = −12 V to −16.5 V, V_{CC} = 2.7 V to 5.25 V, V_{DRIVE} = 2.7 V to 5.25, V_{REF} = 2.5 V to 3.0 V internal/external, T_A = T_{MAX} to T_{MIN}. Timing specifications apply with a 32 pF load, unless otherwise noted.[1]

Table 3.

	Limit at T_{MIN}, T_{MAX}			Description
Parameter	**V_{CC} < 4.75 V**	**V_{CC} = 4.75 V to 5.25 V**	**Unit**	**$V_{DRIVE} \le V_{CC}$**
f_{SCLK}	50	50	kHz min	
	14	20	MHz max	
$t_{CONVERT}$	16 × t_{SCLK}	16 × t_{SCLK}	ns max	$t_{SCLK} = 1/f_{SCLK}$
t_{QUIET}	75	60	ns min	Minimum time between end of serial read and next falling edge of $\overline{CS}$
t_1	12	5	ns min	Minimum $\overline{CS}$ pulse width
t_2[2]	25	20	ns min	$\overline{CS}$ to SCLK setup time; bipolar input ranges (±10 V, ±5 V, ±2.5 V)
	45	35	ns min	Unipolar input range (0 V to 10 V)
t_3	26	14	ns max	Delay from $\overline{CS}$ until DOUT three-state disabled
t_4	57	43	ns max	Data access time after SCLK falling edge
t_5	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK low pulse width
t_6	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK high pulse width
t_7	13	8	ns min	SCLK to data valid hold time
t_8	40	22	ns max	SCLK falling edge to DOUT high impedance
	10	9	ns min	SCLK falling edge to DOUT high impedance
t_9	4	4	ns min	DIN setup time prior to SCLK falling edge
t_{10}	2	2	ns min	DIN hold time after SCLK falling edge
$t_{POWER-UP}$	750	750	ns max	Power up from autostandby
	500	500	µs max	Power up from full shutdown/autoshutdown mode, internal reference
	25	25	µs typ	Power up from full shutdown/autoshutdown mode, external reference

[1] Sample tested during initial release to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DRIVE}) and timed from a voltage level of 1.6 V.
[2] When using V_{CC} = 4.75 V to 5.25 V and the 0 V to 10 V unipolar range, running at 1 MSPS throughput rate with t_2 at 20 ns, the mark space ratio needs to be limited to 50:50.

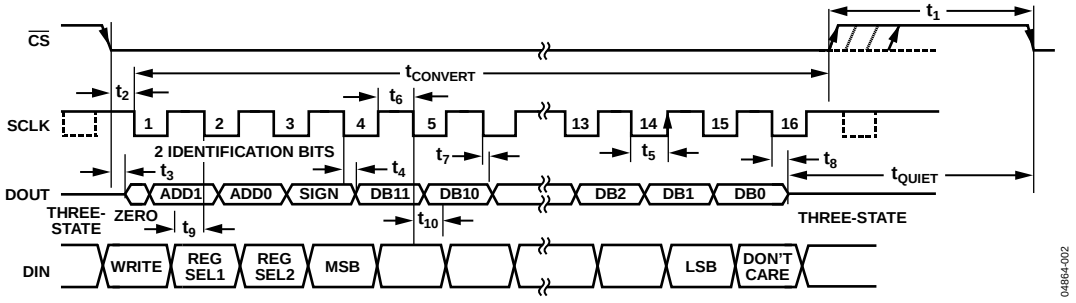

Figure 2. Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to AGND, DGND	−0.3 V to +16.5 V
V_{SS} to AGND, DGND	+0.3 V to −16.5 V
V_{DD} to V_{CC}	V_{CC} − 0.3 V to 16.5 V
V_{CC} to AGND, DGND	−0.3 V to +7 V
V_{DRIVE} to AGND, DGND	−0.3 V to +7 V
AGND to DGND	−0.3 V to +0.3 V
Analog Input Voltage to AGND[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to +7 V
Digital Output Voltage to GND	−0.3 V to V_{DRIVE} + 0.3 V
REFIN to AGND	−0.3 V to V_{CC} + 0.3 V
Input Current to Any Pin Except Supplies[2]	±10 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSSOP Package	
θ_{JA} Thermal Impedance	150.4°C/W
θ_{JC} Thermal Impedance	27.6°C/W
Pb-Free Temperature, Soldering Reflow	260(0)°C
ESD	2.5 kV

[1] If the analog inputs are being driven from alternative V_{DD} and V_{SS} supply circuitry, Schottky diodes should be placed in series with the AD7324 V_{DD} and V_{SS} supplies. See Power Supply Configuration section.
[2] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

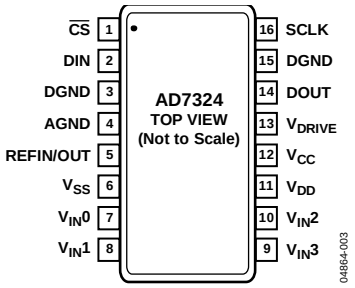

Figure 3. TSSOP Pin Configuration

Table 5. Pin Function Description

Pin No.	Mnemonic	Description
1	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7324 and frames the serial data transfer.
2	DIN	Data In. Data should be written to the on-chip registers is provided on this input and is clocked into the register on the falling edge of SCLK (see the Reference section).
3, 15	DGND	Digital Ground. Ground reference point for all digital circuitry on the AD7324. The DGND and AGND voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
4	AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7324. All analog input signals and any external reference signal should be referred to this AGND voltage. The AGND and DGND voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
5	REFIN/OUT	Reference Input/Reference Output. The on-chip reference is available on this pin for external use to the AD7324. The nominal internal reference voltage is 2.5 V, which appears at the pin. A 680 nF capacitor should be placed on the reference pin. Alternatively, the internal reference can be disabled, and an external reference applied to this input. On power-up, the external reference mode is the default condition (see the Reference section).
6	V_{SS}	Negative Power Supply Voltage. This is the negative supply voltage for the analog input section.
7, 8, 10, 9	$V_{IN}0$ to $V_{IN}3$	Analog Input 0 to Analog Input 3. The analog inputs are multiplexed into the on-chip track-and-hold. The analog input channel for conversion is selected by programming the channel address Bit ADD1 and Bit ADD0 in the control register. The inputs can be configured as four single-ended inputs, two true differential input pairs, two pseudo differential inputs, or three pseudo differential inputs. The configuration of the analog inputs is selected by programming the mode bits, Bit Mode 1 and Bit Mode 0, in the control register. The input range on each input channel is controlled by programming the range register. Input ranges of ±10 V, ±5 V, ±2.5 V, and 0 V to +10 V can be selected on each analog input channel when a +2.5 V reference voltage is used (see the Reference section).
11	V_{DD}	Positive Power Supply Voltage. This is the positive supply voltage for the analog input section.
12	V_{CC}	Analog Supply Voltage, 2.7 V to 5.25 V. This is the supply voltage for the ADC core on the AD7324. This supply should be decoupled to AGND. Specifications apply from V_{CC} = 4.75 V to 5.25 V.
13	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface operates. This pin should be decoupled to DGND. The voltage at this pin may be different to that at V_{CC}, but it should not exceed V_{CC} by more than 0.3 V.
14	DOUT	Serial Data Output. The conversion output data is supplied to this pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input, and 16 SCLKs are required to access the data. The data stream consists of a leading ZERO bit, two channel identification bits, the sign bit, and 12 bits of conversion data. The data is provided MSB first (see the Serial Interface section).
16	SCLK	Serial Clock, Logic Input. A serial clock input provides the SCLK used for accessing the data from the AD7324. This clock is also used as the clock source for the conversion process.

TYPICAL PERFORMANCE CHARACTERISTICS

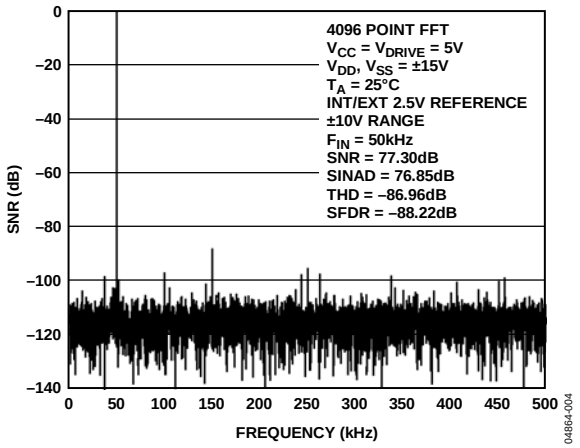

Figure 4. FFT True Differential Mode

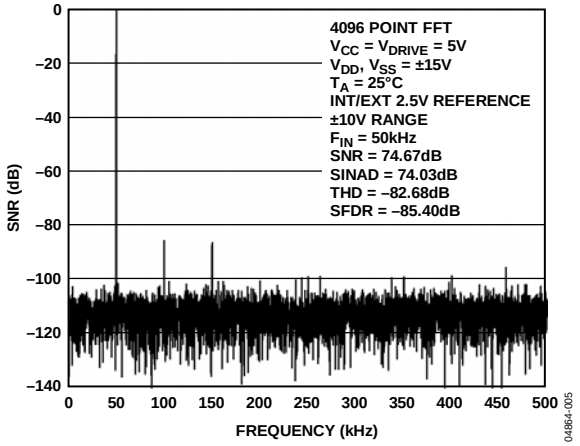

Figure 5. FFT Single-Ended Mode

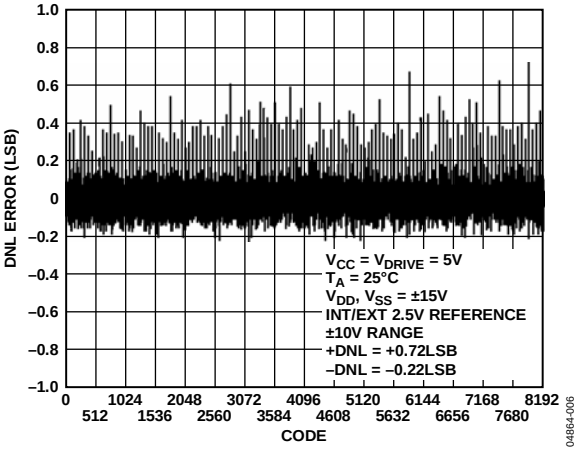

Figure 6. Typical DNL True Differential Mode

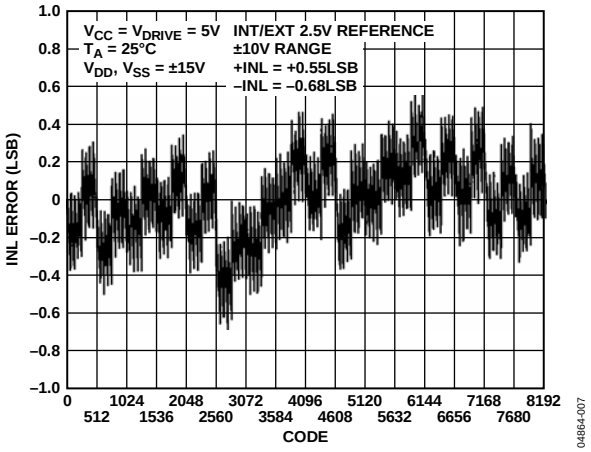

Figure 7. Typical INL True Differential Mode

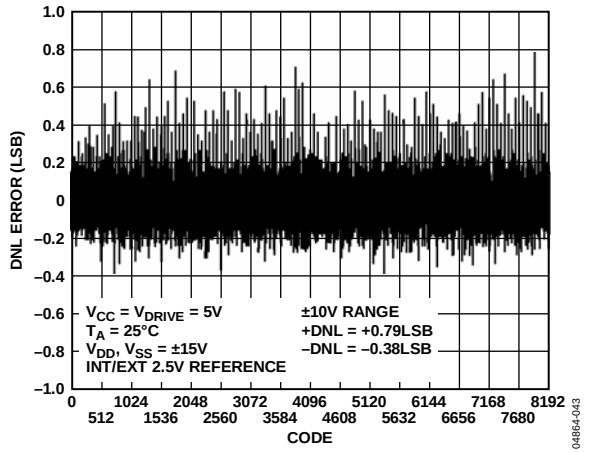

Figure 8. Typical DNL Single-Ended Mode

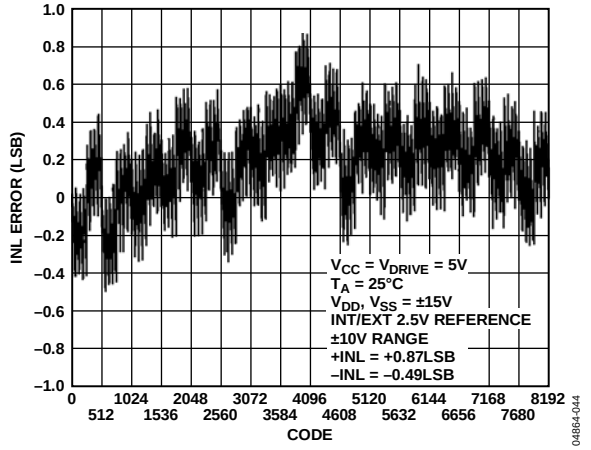

Figure 9. Typical INL Single-Ended Mode

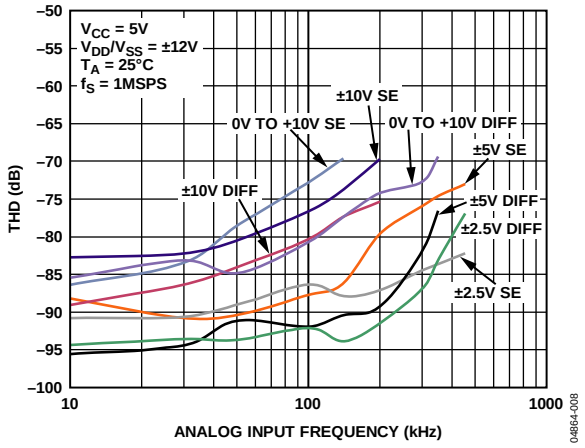

Figure 10. THD vs. Analog Input Frequency for Single-Ended (SE) and True Differential Mode (Diff) at 5 V V_{CC}

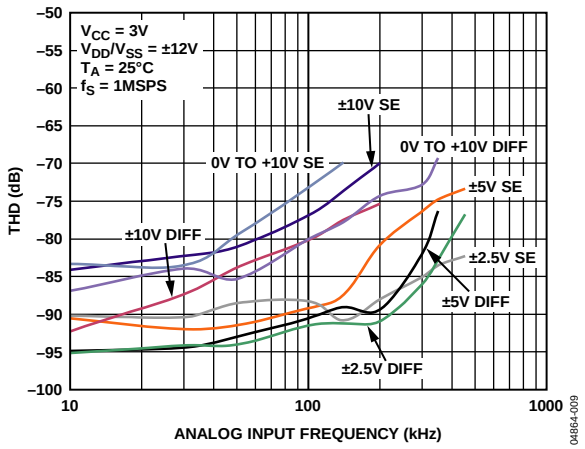

Figure 11. THD vs. Analog Input Frequency for Single-Ended (SE) and True Differential Mode (Diff) at 3 V V_{CC}

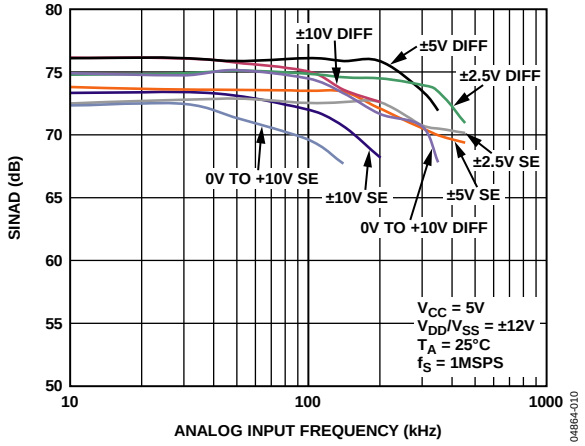

Figure 12. SINAD vs. Analog Input Frequency for Single-Ended (SE) and Differential Mode (Diff) at 5 V V_{CC}

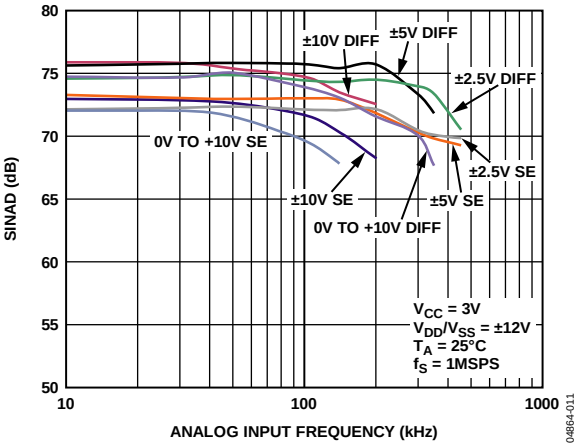

Figure 13. SINAD vs. Analog Input Frequency for Single-Ended (SE) and Differential Mode (Diff) at 3 V V_{CC}

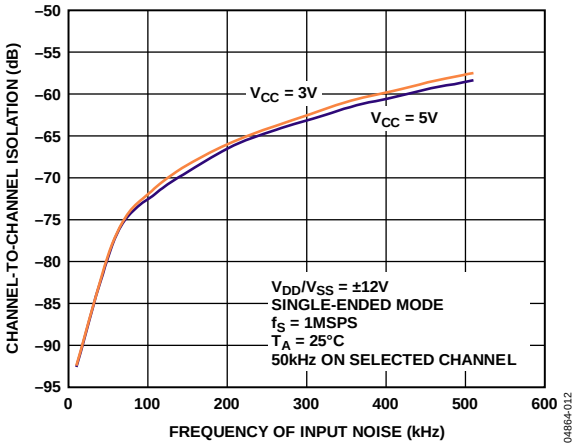

Figure 14. Channel-to-Channel Isolation

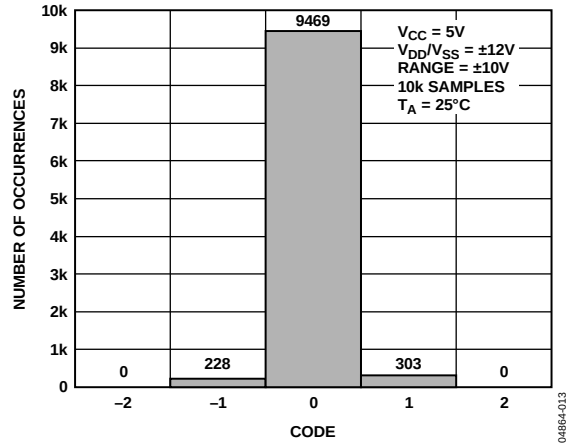

Figure 15. Histogram of Codes, True Differential Mode

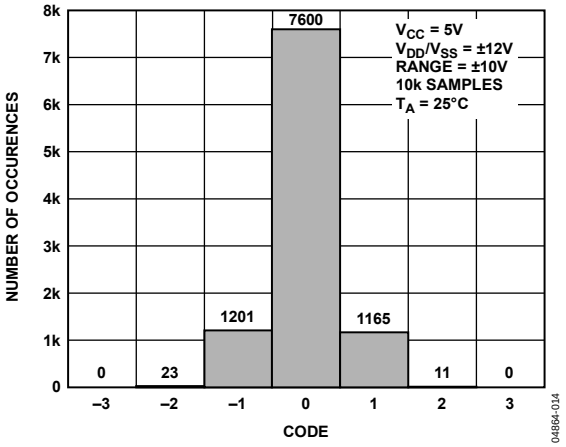

Figure 16. Histogram of Codes, Single-Ended Mode

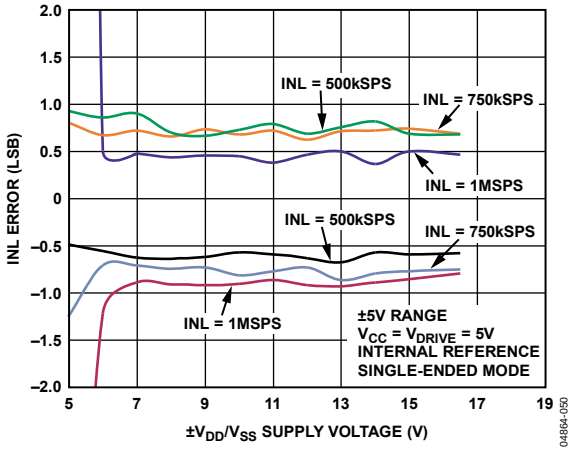

Figure 19. INL Error vs. Supply Voltage at 500 kSPS, 750 kSPS, and 1 MSPS

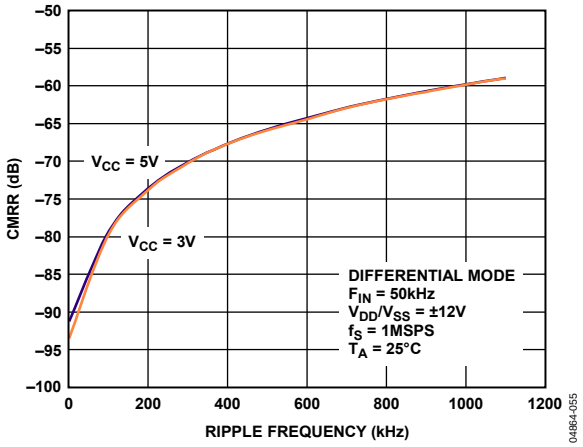

Figure 17. CMRR vs. Common-Mode Ripple Frequency

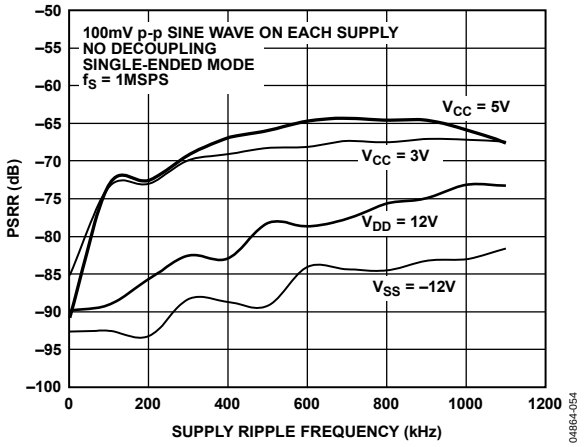

Figure 20. PSRR vs. Supply Ripple Frequency Without Supply Decoupling

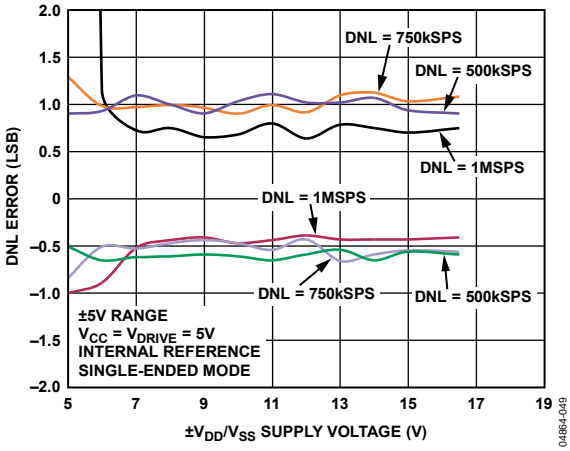

Figure 18. DNL Error vs. Supply Voltage at 500 kSPS, 750 kSPS, and 1 MSPS

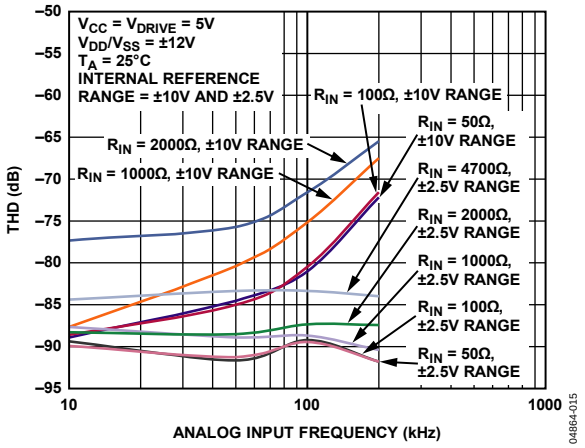

Figure 21. THD vs. Analog Input Frequency for Various Source Impedances, True Differential Mode

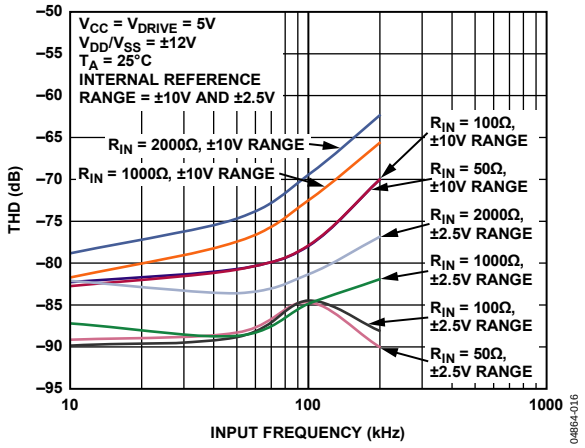

Figure 22. THD vs. Analog Input Frequency for Various Source Impedances, Single-Ended Mode

TERMINOLOGY

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale (a point 1 LSB below the first code transition) and full scale (a point 1 LSB above the last code transition).

Offset Code Error
This applies to straight binary output coding. It is the deviation of the first code transition (00 ... 000) to (00 ... 001) from the ideal, that is, AGND + 1 LSB.

Offset Error Match
This is the difference in offset error between any two input channels.

Gain Error
This applies to straight binary output coding. It is the deviation of the last code transition (111 ... 110) to (111 ... 111) from the ideal (that is, $4 \times V_{REF} - 1$ LSB, $2 \times V_{REF} - 1$ LSB, $V_{REF} - 1$ LSB) after adjusting for the offset error.

Gain Error Match
This is the difference in gain error between any two input channels.

Bipolar Zero Code Error
This applies when using twos complement output coding and a bipolar analog input. It is the deviation of the midscale transition (all 1s to all 0s) from the ideal input voltage, that is, AGND − 1 LSB.

Bipolar Zero Code Error Match
This refers to the difference in bipolar zero code error between any two input channels.

Positive Full-Scale Error
This applies when using twos complement output coding and any of the bipolar analog input ranges. It is the deviation of the last code transition (011 … 110) to (011 … 111) from the ideal ($4 \times V_{REF} - 1$ LSB, $2 \times V_{REF} - 1$ LSB, $V_{REF} - 1$ LSB) after adjusting for the bipolar zero code error.

Positive Full-Scale Error Match
This is the difference in positive full-scale error between any two input channels.

Negative Full-Scale Error
This applies when using twos complement output coding and any of the bipolar analog input ranges. This is the deviation of the first code transition (10 … 000) to (10 … 001) from the ideal (that is, $-4 \times V_{REF} + 1$ LSB, $-2 \times V_{REF} + 1$ LSB, $-V_{REF} + 1$ LSB) after adjusting for the bipolar zero code error.

Negative Full-Scale Error Match

This is the difference in negative full-scale error between any two input channels.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns into track mode after the 14th SCLK rising edge. Track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1/2 LSB, after the end of a conversion. For the ±2.5 V range, the specified acquisition time is the time required for the track-and-hold amplifier to settle to within ±1 LSB.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process. The more levels, the smaller the quantization noise. Theoretically, the signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\ to\ (Noise + Distortion) = (6.02\ N + 1.76)\ \text{dB}$$

For a 13-bit converter, this is 80.02 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7324, it is defined as

$$THD\ (\text{dB}) = 20 \log \frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where V_1 is the rms amplitude of the fundamental, and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, the largest harmonic could be a noise peak.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between any two channels. It is measured by applying a full-scale, 100 kHz sine wave signal to all unselected input channels and determining the degree to which the signal attenuates in the selected channel with a 50 kHz signal. Figure 14 shows the worst-case across all eight channels for the AD7324. The analog input range is programmed to be the same on all channels.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), whereas the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7324 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, whereas the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels.

PSR (Power Supply Rejection)
Variations in power supply affect the full-scale transition but not the linearity of the converter. Power supply rejection is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value (see the Typical Performance Characteristics section).

CMRR (Common-Mode Rejection Ratio)
CMRR is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV sine wave applied to the common-mode voltage of the $V_{IN}+$ and $V_{IN}-$ frequency, f_S, as

$$CMRR\ (\text{dB}) = 10 \log (Pf/Pf_S)$$

where Pf is the power at frequency f in the ADC output, and Pf_S is the power at frequency f_S in the ADC output (see Figure 17).

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7324 is a fast, 4-channel, 12-bit plus sign, bipolar input, serial ADC. The AD7324 can accept bipolar input ranges that include ±10 V, ±5 V, and ±2.5 V; it can also accept a 0 V to +10 V unipolar input range. A different analog input range can be programmed on each analog input channel via the on-chip registers. The AD7324 has a high speed serial interface that can operate at throughput rates up to 1 MSPS.

The AD7324 requires V_{DD} and V_{SS} dual supplies for the high voltage analog input structures. These supplies must be equal to or greater than the analog input range. See Table 6 for the requirements of these supplies for each analog input range. The AD7324 requires a low voltage 2.7 V to 5.25 V V_{CC} supply to power the ADC core.

Table 6. Reference and Supply Requirements for Each Analog Input Range

Selected Analog Input Range (V)	Reference Voltage (V)	Full-Scale Input Range (V)	AV_{CC} (V)	Minimum V_{DD}/V_{SS} (V)[1]
±10	2.5	±10	3/5	±10
	3.0	±12	3/5	±12
±5	2.5	±5	3/5	±5
	3.0	±6	3/5	±6
±2.5	2.5	±2.5	3/5	±5
	3.0	±3	3/5	±5
0 to +10	2.5	0 to +10	3/5	+10/AGND
	3.0	0 to +12	3/5	+12/AGND

[1] Guaranteed performance for V_{DD} = 12 V to 16.5 V and V_{SS} = −12 V to −16.5 V.

The performance specifications are guaranteed for V_{DD} = 12 V to 16.5 V and V_{SS} = −12 V to −16.5 V. With V_{DD} and V_{SS} supplies outside this range, the AD7324 is functional but performance is not guaranteed. To meet the specified performance specifications when the AD7324 is configured with the minimum V_{DD} and V_{SS} supplies for a chosen analog input range, the throughput rate should be decreased from the maximum throughput range (see the Typical Performance Characteristics section). Figure 18 and Figure 19 show the change in INL and DNL as the V_{DD} and V_{SS} voltages are varied. When operating at the maximum throughput rate, as the V_{DD} and V_{SS} supply voltages are reduced, the INL and DNL error increases. However, as the throughput rate is reduced with the minimum V_{DD} and V_{SS} supplies, the INL and DNL error is reduced.

Figure 31 shows the change in THD as the V_{DD} and V_{SS} supplies are reduced. At the maximum throughput rate, the THD degrades significantly as V_{DD} and V_{SS} are reduced. It is, therefore, necessary to reduce the throughput rate when using minimum V_{DD} and V_{SS} supplies so that there is less degradation of THD and the specified performance can be maintained. The degradation is due to an increase in the on resistance of the input multiplexer when the V_{DD} and V_{SS} supplies are reduced.

The analog inputs can be configured as four single-ended inputs, two true differential input pairs, two pseudo differential inputs, or three pseudo differential inputs. Selection can be made by programming the mode bits, Mode 0 and Mode 1, in the control register.

The serial clock input accesses data from the part and provides the clock source for the successive approximation ADC. The AD7324 has an on-chip 2.5 V reference. However, the AD7324 can also work with an external reference. On power-up, the external reference operation is the default option. If the internal reference is the preferred option, the user must write to the reference bit in the control register to select the internal reference operation.

The AD7324 also features power-down options to allow power saving between conversions. The power-down modes are selected by programming the on-chip control register as described in the Modes of Operation section.

CONVERTER OPERATION

The AD7324 is a successive approximation ADC built around two capacitive DACs. Figure 23 and Figure 24 show simplified schematics of the ADC in single-ended mode during the acquisition and conversion phases, respectively. Figure 25 and Figure 26 show simplified schematics of the ADC in differential mode during acquisition and conversion phases, respectively. The ADC is composed of control logic, a SAR, and capacitive DACs. In Figure 23 (the acquisition phase), SW2 is closed and SW1 is in Position A, the comparator is held in a balanced condition, and the sampling capacitor array acquires the signal on the input.

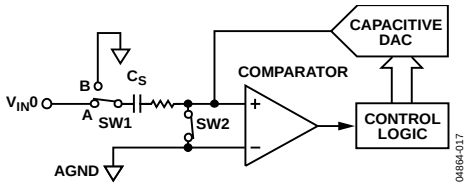

Figure 23. ADC Acquisition Phase (Single-Ended)

When the ADC starts a conversion (Figure 24), SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced. The control logic and the charge redistribution DAC are used to add and subtract fixed amounts of charge from the capacitive DAC to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code.

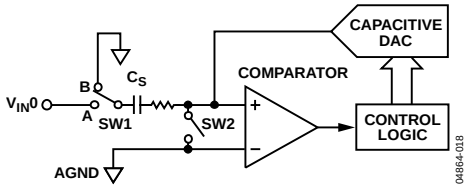

Figure 24. ADC Conversion Phase (Single-Ended)

Figure 25 shows the differential configuration during the acquisition phase. For the conversion phase, SW3 opens and SW1 and SW2 move to Position B (Figure 26). The output impedances of the source driving the $V_{IN}+$ and $V_{IN}-$ pins must be matched; otherwise, the two inputs have different settling times, resulting in errors.

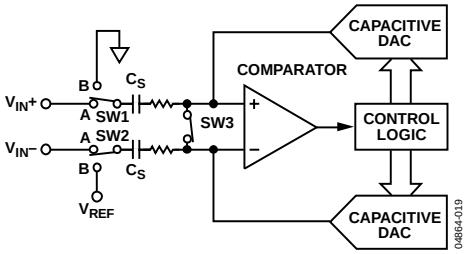

Figure 25. ADC Differential Configuration During Acquisition Phase

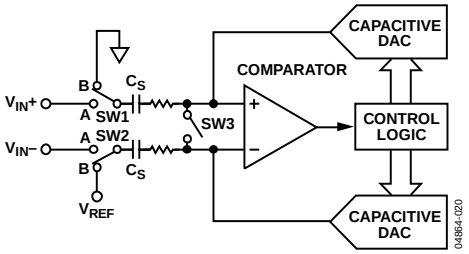

Figure 26. ADC Differential Configuration During Conversion Phase

Output Coding

The AD7324 default output coding is set to twos complement. The output coding is controlled by the coding bit in the control register. To change the output coding to straight binary coding, the coding bit in the control register must be set. When operating in sequence mode, the output coding for each channel in the sequence is the value written to the coding bit during the last write to the control register.

Transfer Functions

The designed code transitions occur at successive integer LSB values (that is, 1 LSB, 2 LSB, and so on). The LSB size is dependent on the analog input range selected.

Table 7. LSB Sizes for Each Analog Input Range

Input Range	Full-Scale Range/8192 Codes	LSB Size
±10 V	20 V	2.441 mV
±5 V	10 V	1.22 mV
±2.5 V	5 V	0.61 mV
0 V to +10 V	10 V	1.22 mV

The ideal transfer characteristic for the AD7324 when twos complement coding is selected is shown in Figure 27. The ideal transfer characteristic for the AD7324 when straight binary coding is selected is shown in Figure 28.

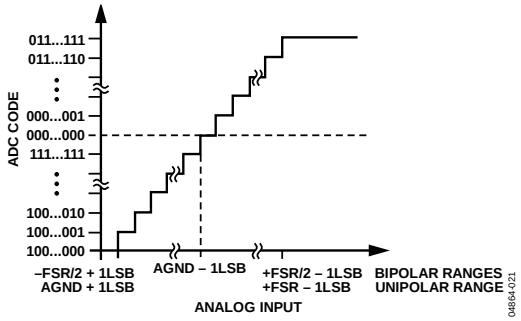

Figure 27. Twos Complement Transfer Characteristic (Bipolar Ranges)

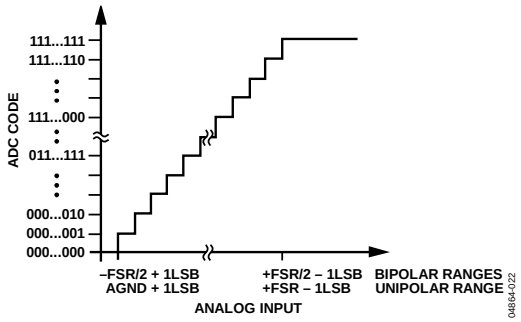

Figure 28. Straight Binary Transfer Characteristic (Bipolar Ranges)

ANALOG INPUT STRUCTURE

The analog inputs of the AD7324 can be configured as single-ended, true differential, or pseudo differential via the control register mode bits (see Table 10). The AD7324 can accept true bipolar input signals. On power-up, the analog inputs operate as four single-ended analog input channels. If true differential or pseudo differential is required, a write to the control register is necessary after power-up to change this configuration.

Figure 29 shows the equivalent analog input circuit of the AD7324 in single-ended mode. Figure 30 shows the equivalent analog input structure in differential mode. The two diodes provide ESD protection for the analog inputs.

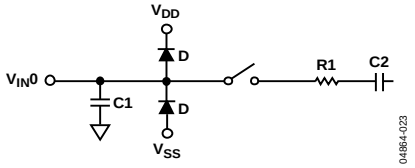

Figure 29. Equivalent Analog Input Circuit (Single-Ended)

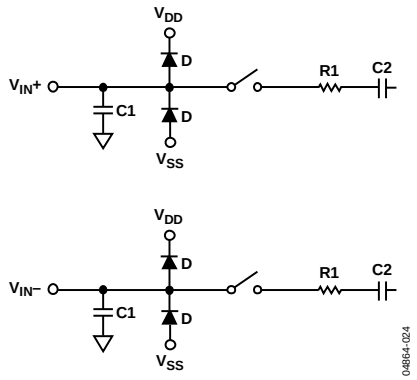

Figure 30. Equivalent Analog Input Circuit (Differential)

Care should be taken to ensure that the analog input does not exceed the V_{DD} and V_{SS} supply rails by more than 300 mV. Exceeding this value causes the diodes to become forward biased and to start conducting into either the V_{DD} supply rail or V_{SS} supply rail. These diodes can conduct up to 10 mA without causing irreversible damage to the part.

In Figure 29 and Figure 30, Capacitor C1 is typically 4 pF and can primarily be attributed to pin capacitance. Resistor R1 is a lumped component made up of the on resistance of the input multiplexer and the track-and-hold switch. Capacitor C2 is the sampling capacitor; its capacitance varies depending on the analog input range selected (see the Specifications section).

Track-and-Hold Section

The track-and-hold on the analog input of the AD7324 allows the ADC to accurately convert an input sine wave of full-scale amplitude to 13-bit accuracy. The input bandwidth of the track-and-hold is greater than the Nyquist rate of the ADC. The AD7324 can handle frequencies up to 22 MHz.

The track-and-hold enters its tracking mode on the 14th SCLK rising edge after the $\overline{CS}$ falling edge. The time required to acquire an input signal depends on how quickly the sampling capacitor is charged. With 0 source impedance, 305 ns are sufficient to acquire the signal to the 13-bit level. The acquisition time required is calculated using the following formula:

$$t_{ACQ} = 10 \times ((R_{SOURCE} + R) \times C)$$

where C is the sampling capacitance and R is the resistance seen by the track-and-hold amplifier looking back on the input. For the AD7324, the value of R includes the on resistance of the input multiplexer and is typically 300 Ω. R_{SOURCE} should include any extra source impedance on the analog input.

The AD7324 enters track mode on the 14th SCLK rising edge. When running the AD7324 at a throughput rate of 1 MSPS with a 20 MHz SCLK signal, the ADC has approximately

$$1.5 \text{ SCLK} + t8 + t_{QUIET}$$

to acquire the analog input signal. The ADC goes back into hold mode on the $\overline{CS}$ falling edge.

As the V_{DD}/V_{SS} supply voltage is reduced, the on resistance of the input multiplexer increases. Therefore, based on the equation for t_{ACQ}, it is necessary to increase the amount of acquisition time provided to the AD7324 and, therefore, decrease the overall throughput rate. Figure 31 shows that if the throughput rate is reduced when operating with minimum V_{DD} and V_{SS} supplies, the specified THD performance is maintained.

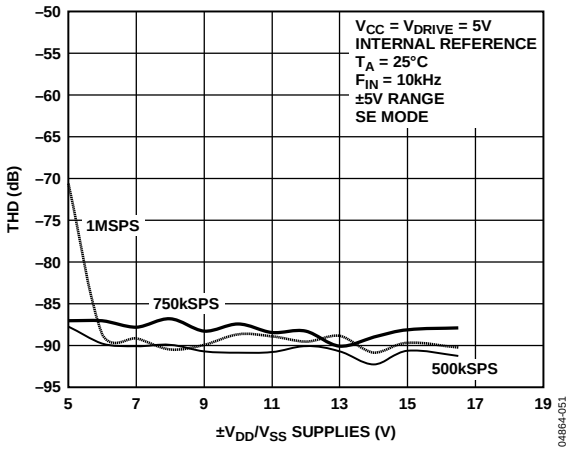

Figure 31. THD vs. ±V_{DD}/V_{SS} Supply Voltage at 500 kSPS, 750 kSPS, and 1 MSPS

Unlike other bipolar ADCs, the AD7324 does not have a resistive analog input structure. On the AD7324, the bipolar analog signal is sampled directly onto the sampling capacitor. This gives the AD7324 high analog input impedance. An approximation for the analog input impedance can be calculated from the following formula:

$$Z = 1/(f_S \times C_S)$$

where f_S is the sampling frequency, and C_S is the sampling capacitor value.

C_S depends on the analog input range chosen (see the Specifications section). When operating at 1 MSPS, the analog input impedance is typically 75 kΩ for the ±10 V range. As the sampling frequency is reduced, the analog input impedance further increases. As the analog input impedance increases the current required to drive the analog input, therefore, decreases.

TYPICAL CONNECTION DIAGRAM

Figure 32 shows a typical connection diagram for the AD7324. In this configuration, the AGND pin is connected to the analog ground plane of the system, and the DGND pin is connected to the digital ground plane of the system. The analog inputs on the AD7324 can be configured to operate in single-ended, true differential, or pseudo differential mode. The AD7324 can operate with either an internal or external reference. In Figure 32, the AD7324 is configured to operate with the internal 2.5 V reference. A 680 nF decoupling capacitor is required when operating with the internal reference.

The V_{CC} pin can be connected to either a 3 V supply voltage or a 5 V supply voltage. The V_{DD} and V_{SS} are the dual supplies for the high voltage analog input structures. The voltage on these pins must be equal to or greater than the highest analog input range selected on the analog input channels (see Table 6). The V_{DRIVE} pin is connected to the supply voltage of the microprocessor. The voltage applied to the V_{DRIVE} input controls the voltage of the serial interface. V_{DRIVE} can be set to 3 V or 5 V.

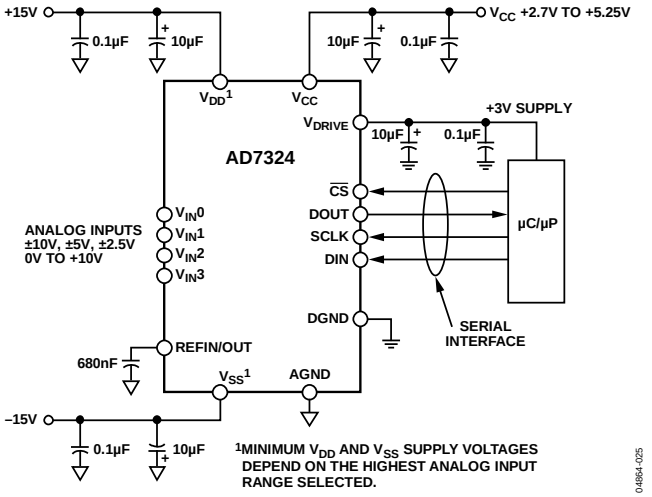

Figure 32. Typical Connection Diagram

ANALOG INPUT

Single-Ended Inputs

The AD7324 has a total of four analog inputs when operating in single-ended mode. Each analog input can be independently programmed to one of the four analog input ranges. In applications where the signal source is high impedance, it is recommended to buffer the signal before applying it to the ADC analog inputs. Figure 33 shows the configuration of the AD7324 in single-ended mode.

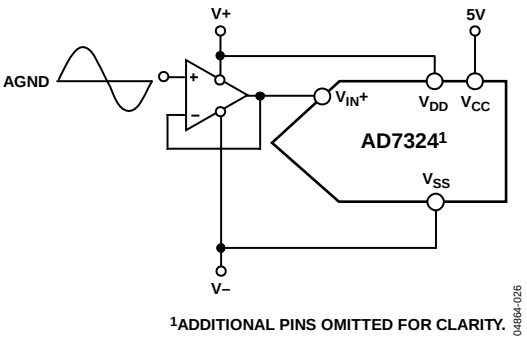

Figure 33. Single-Ended Mode Typical Connection Diagram

True Differential Mode

The AD7324 can have a total of two true differential analog input pairs. Differential signals have some benefits over single-ended signals, including better noise immunity based on the common-mode rejection of the device and improvements in distortion performance. Figure 34 defines the configuration of the true differential analog inputs of the AD7324.

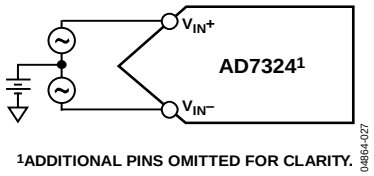

Figure 34. True Differential Inputs

The amplitude of the differential signal is the difference between the signals applied to the $V_{IN}+$ and $V_{IN}-$ pins in each differential pair ($V_{IN}+ - V_{IN}-$). $V_{IN}+$ and $V_{IN}-$ should be simultaneously driven by two signals of equal amplitude, dependent on the input range selected, that are 180° out of phase. Assuming the ±4 × V_{REF} mode, the amplitude of the differential signal is −20 V to +20 V p-p (2 × 4 × V_{REF}), regardless of the common mode.

The common mode is the average of the two signals

$$(V_{IN}+ + V_{IN}-)/2$$

and is, therefore, the voltage on which the two input signals are centered.

This voltage is set up externally, and its range varies with reference voltage. As the reference voltage increases, the common-mode range decreases. When driving the differential inputs with an amplifier, the actual common mode range is determined by the output swing of the amplifier. If the differential inputs are not driven from an amplifier, the common-mode range is determined by the supply voltage on the V_{DD} supply pin and the V_{SS} supply pin.

When a conversion takes place, the common mode is rejected, resulting in a noise-free signal of amplitude −2 × (4 × V_{REF}) to +2 × (4 × V_{REF}) corresponding to digital Code −4096 to Code +4095.

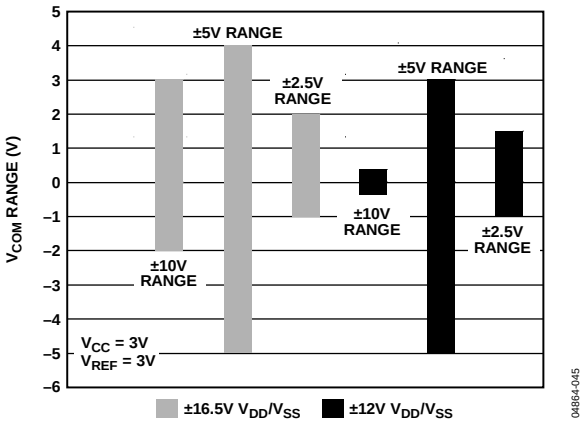

Figure 35. Common-Mode Range for V_{CC} = 3 V and REFIN/OUT = 3 V

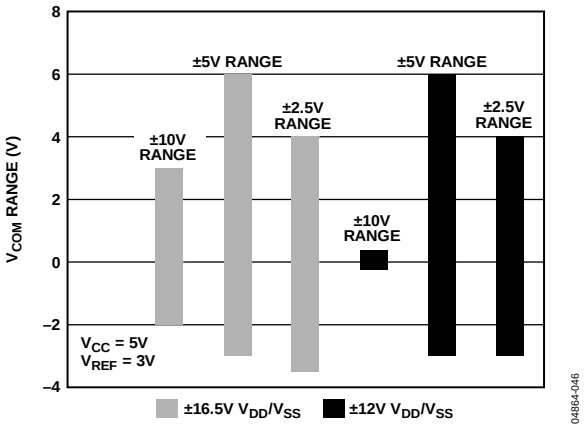

Figure 36. Common-Mode Range for V_{CC} = 5 V and REFIN/OUT = 3 V

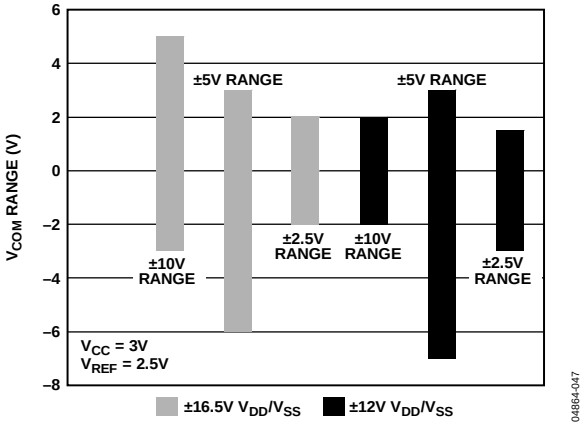

Figure 37. Common-Mode Range for V_{CC} = 3 V and REFIN/OUT = 2.5 V

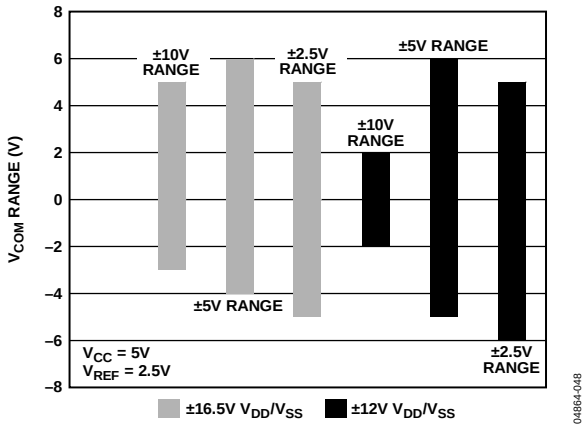

Figure 38. Common-Mode Range for V_{CC} = 5 V and REFIN/OUT = 2.5 V

Pseudo Differential Inputs

The AD7324 can have two pseudo differential pairs or three pseudo differential inputs referenced to a common $V_{IN}-$ pin. The $V_{IN}+$ inputs are coupled to the signal source and must have an amplitude within the selected range for that channel as programmed in the range register. A dc input is applied to the $V_{IN}-$ pin. The voltage applied to this input provides an offset for the $V_{IN}+$ input from ground or a pseudo ground. Pseudo differential inputs separate the analog input signal ground from the ADC ground, allowing cancellation of dc common-mode voltages. Figure 39 shows the AD7324 configured in pseudo differential mode.

When a conversion takes place, the pseudo ground corresponds to Code −4096, and the maximum amplitude corresponds to Code +4095.

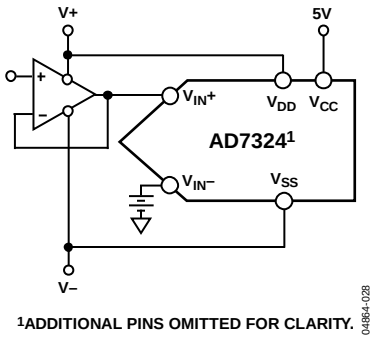

Figure 39. Pseudo Differential Inputs

Figure 40 and Figure 41 show the typical voltage range on the $V_{IN}-$ pin for the different analog input ranges when configured in the pseudo differential mode.

For example, when the AD7324 is configured to operate in pseudo differential mode and the ±5 V range is selected with ±16.5 V V_{DD}/V_{SS} supplies and 5 V V_{CC}, the voltage on the $V_{IN}-$ pin can vary from −6.5 V to +6.5 V.

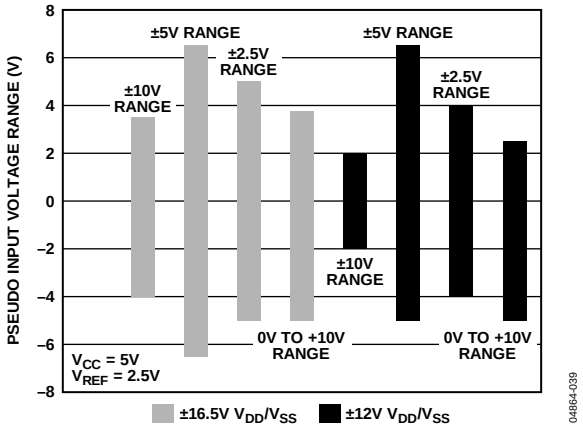

Figure 40. Pseudo Input Range with V_{CC} = 5 V

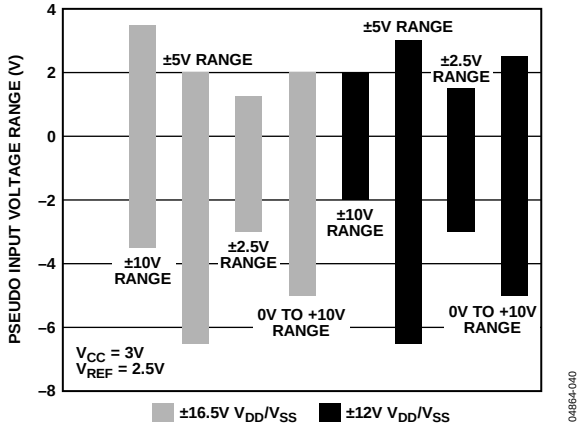

Figure 41. Pseudo Input Range with V_{CC} = 3 V

DRIVER AMPLIFIER CHOICE

In applications where the harmonic distortion and signal-to-noise ratio are critical specifications, the analog input of the AD7324 should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC and can necessitate the use of an input buffer amplifier.

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of THD that can be tolerated in the application. The THD increases as the source impedance increases and performance degrades. Figure 21 and Figure 22 show graphs of the THD vs. the analog input frequency for various source impedances. Depending on the input range and analog input configuration selected, the AD7324 can handle source impedances of up to 4.7 kΩ before the THD starts to degrade.

Due to the programmable nature of the analog inputs on the AD7324, the choice of op amp used to drive the inputs is a function of the particular application and depends on the input configuration and the analog input voltage ranges selected.

The driver amplifier must be able to settle for a full-scale step to a 13-bit level, 0.0122%, in less than the specified acquisition time of the AD7324. An op amp such as the AD8021 meets this requirement when operating in single-ended mode. The AD8021 needs an external compensating NPO type of capacitor. The AD8022 can also be used in high frequency applications where a dual version is required. For lower frequency applications, op amps such as the AD797, AD845, and AD8610 can be used with the AD7324 in single-ended mode configuration.

Differential operation requires that V_{IN}+ and V_{IN}– be simultaneously driven with two signals of equal amplitude that are 180° out of phase. The common mode must be set up externally to the AD7324. The common-mode range is determined by the REFIN/OUT voltage, the V_{CC} supply voltage, and the particular amplifier used to drive the analog inputs. Differential mode with either an ac input or a dc input provides the best THD performance over a wide frequency range. Because not all applications have a signal preconditioned for differential operation, there is often a need to perform the single-ended-to-differential conversion.

This single-ended-to-differential conversion can be performed using an op amp pair. Typical connection diagrams for an op amp pair are shown in Figure 42 and Figure 43. In Figure 42, the common-mode signal is applied to the noninverting input of the second amplifier.

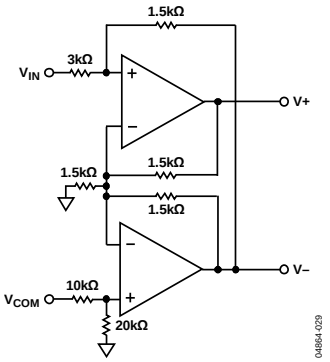

Figure 42. Single-Ended-to-Differential Configuration with the AD845

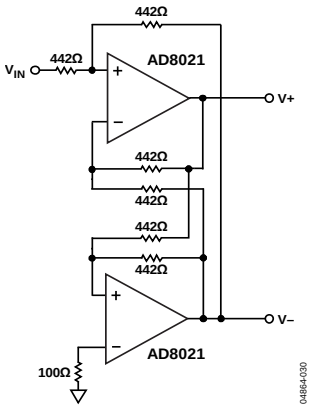

Figure 43. Single-Ended-to-Differential Configuration with the AD8021

REGISTERS

The AD7324 has three programmable registers, the control register, the sequence register, and the range register. These registers are write-only registers.

ADDRESSING REGISTERS

A serial transfer on the AD7324 consists of 16 SCLK cycles. The three MSBs on the DIN line during the 16 SCLK transfer are decoded to determine which register is addressed. The three MSBs consist of the write bit, the Register Select 1 bit, and the Register Select 2 bit. The register select bits are used to determine which of the three on-board registers is selected. The write bit determines if the data on the DIN line following the register select bits loads into the addressed register. If the write bit is 1, the bits load into the register addressed by the register select bits. If the write bit is 0, the data on the DIN line does not load into any register.

Combinations of the write bit, the Register Select 1 bit, and the Register Select 2 bit other than those specified in Table 8 access registers for Analog Devices internal use only. Do not access these registers, as doing so may lead to unspecified operation of the device.

Table 8. Decoding Register Select Bits and Write Bit

Write	Register Select 1	Register Select 2	Comment
0	0	0	Data on the DIN line during this serial transfer is ignored.
1	0	0	This combination selects the control register. The subsequent 12 bits are loaded into the control register.
1	0	1	This combination selects the range register. The subsequent 8 bits are loaded into the range register.
1	1	1	This combination selects the sequence register. The subsequent 4 bits are loaded into the sequence register.

CONTROL REGISTER

The control register is used to select the analog input channel, analog input configuration, reference, coding, and power mode. The control register is a write-only, 12-bit register. Data loaded on the DIN line corresponds to the AD7324 configuration for the next conversion. If the sequence register is being used, data should be loaded into the control register after the range register and the sequence register have been initialized. The bit functions of the control register are shown in Table 9 (the power-up status of all bits is 0).

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	1	3	2	1	0
Write	Register Select 1	Register Select 2	ZERO	ADD1	ADD0	Mode 1	Mode 0	PM1	PM0	Coding	Ref	Seq1	Seq2	ZERO	0

Table 9. Control Register Details

Bit	Mnemonic	Description
12, 1	ZERO	A 0 must be written to this bit to ensure correct operation of the device.
11, 10	ADD1, ADD0	These two channel address bits are used to select the analog input channel for the next conversion if the sequencer is not being used. If the sequencer is being used, the two channel address bits are used to select the final channel in a consecutive sequence.
9, 8	Mode 1, Mode 0	These two mode bits are used to select the configuration of the four analog input pins, $V_{IN}0$ to $V_{IN}3$. These pins are used in conjunction with the channel address bits. On the AD7324, the analog inputs can be configured as four single-ended inputs, two true differential input pairs, two pseudo differential inputs, or three pseudo differential inputs (see Table 10).
7, 6	PM1, PM0	The power management bits are used to select different power mode options on the AD7324 (see Table 11).
5	Coding	This bit is used to select the type of output coding the AD7324 uses for the next conversion result. If coding = 0, the output coding is twos complement. If coding = 1, the output coding is straight binary. When operating in sequence mode, the output coding for each channel is the value written to the coding bit during the last write to the control register.
4	Ref	The reference bit is used to enable or disable the internal reference. If Ref = 0, the external reference is enabled and used for the next conversion, and the internal reference is disabled. If Ref = 1, the internal reference is used for the next conversion. When operating in sequence mode, the reference used for each channel is the value written to the Ref bit during the last write to the control register.
3, 2	Seq1, Seq2	The Sequence 1 and Sequence 2 bits are used to control the operation of the sequencer (see Table 12).

The four analog input channels can be configured as three pseudo differential analog inputs, two pseudo differential inputs, two true differential input pairs, or four single-ended analog inputs.

Table 10. Analog Input Configuration Selection

		Mode 1 = 1, Mode 0 = 1		Mode 1 = 1, Mode 0 = 0		Mode 1 = 0, Mode 0 =1		Mode 1 = 0, Mode 0 = 0	
Channel Address Bits		3 Pseudo Differential Inputs		2 Fully Differential Inputs		2 Pseudo Differential Inputs		4 Single-Ended Inputs	
ADD1	ADD0	$V_{IN}+$	$V_{IN}-$	$V_{IN}+$	$V_{IN}-$	$V_{IN}+$	$V_{IN}-$	$V_{IN}+$	$V_{IN}-$
0	0	$V_{IN}0$	$V_{IN}3$	$V_{IN}0$	$V_{IN}1$	$V_{IN}0$	$V_{IN}1$	$V_{IN}0$	AGND
0	1	$V_{IN}1$	$V_{IN}3$	$V_{IN}0$	$V_{IN}1$	$V_{IN}0$	$V_{IN}1$	$V_{IN}1$	AGND
1	0	$V_{IN}2$	$V_{IN}3$	$V_{IN}2$	$V_{IN}3$	$V_{IN}2$	$V_{IN}3$	$V_{IN}2$	AGND
1	1	Not a valid selection		$V_{IN}2$	$V_{IN}3$	$V_{IN}2$	$V_{IN}3$	$V_{IN}3$	AGND

Table 11. Power Mode Selection

PM1	PM0	Description
1	1	Full Shutdown Mode. In this mode, all internal circuitry on the AD7324 is powered down. Information in the control register is retained when the AD7324 is in full shutdown mode.
1	0	Autoshutdown Mode. The AD7324 enters autoshutdown on the 15th SCLK rising edge when the control register is updated. All internal circuitry is powered down in autoshutdown.
0	1	Autostandby Mode. In this mode, all internal circuitry is powered down excluding the internal reference. The AD7324 enters autostandby mode on the 15th SCLK rising edge after the control register is updated.
0	0	Normal Mode. All internal circuitry is powered up at all times.

Table 12. Sequencer Selection

Seq1	Seq2	Sequence Type
0	0	The channel sequencer is not used. The analog channel, selected by programming the ADD1 bit and ADD0 bit in the control register, selects the next channel for conversion.
0	1	Uses sequence of channels that were previously programmed in the sequence register for conversion. The AD7324 starts converting on the lowest channel in the sequence. The channels are converted in ascending order. If uninterrupted, the AD7324 keeps converting the sequence. The range for each channel defaults to the range previously written into the range register.
1	0	Used in conjunction with the channel address bits in the control register. This allows continuous conversions on a consecutive sequence of channels, from Channel 0 up to and including a final channel selected by the channel address bits in the control register. The range for each channel defaults to the range previously written into the range register.
1	1	The channel sequencer is not used. The analog channel, selected by programming the ADD1 bit and ADD0 bit in the control register, selects the next channel for conversion.

SEQUENCE REGISTER

The sequence register on the AD7324 is a 4-bit, write-only register. Each of the four analog input channels has one corresponding bit in the sequence register. To select a channel for inclusion in the sequence, set the corresponding channel bit to 1 in the sequence register.

MSB															LSB
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Write	Register Select 1	Register Select 2	$V_{IN}0$	$V_{IN}1$	$V_{IN}2$	$V_{IN}3$	0	0	0	0	0	0	0	0	0

RANGE REGISTER

The range register is used to select one analog input range per analog input channel. It is an 8-bit, write-only register with two dedicated range bits for each of the analog input channels from Channel 0 to Channel 3. There are four analog input ranges, ±10 V, ±5 V, ±2.5 V, and 0 V to +10 V. A write to the range register is selected by setting the write bit to 1 and the register select bits to 0 and 1. After the initial write to the range register occurs, each time an analog input is selected, the AD7324 automatically configures the analog input to the appropriate range, as indicated by the range register. The ±10 V input range is selected by default on each analog input channel (see Table 13).

MSB **LSB**

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Write	Register Select 1	Register Select 2	$V_{IN}0A$	$V_{IN}0B$	$V_{IN}1A$	$V_{IN}1B$	$V_{IN}2A$	$V_{IN}2B$	$V_{IN}3A$	$V_{IN}3B$	0	0	0	0	0

Table 13. Range Selection

$V_{IN}xA$	$V_{IN}xB$	Description
0	0	This combination selects the ±10 V input range on $V_{IN}x$.
0	1	This combination selects the ±5 V input range on $V_{IN}x$.
1	0	This combination selects the ±2.5 V input range on $V_{IN}x$.
1	1	This combination selects the 0 V to +10 V input range on $V_{IN}x$.

SEQUENCER OPERATION

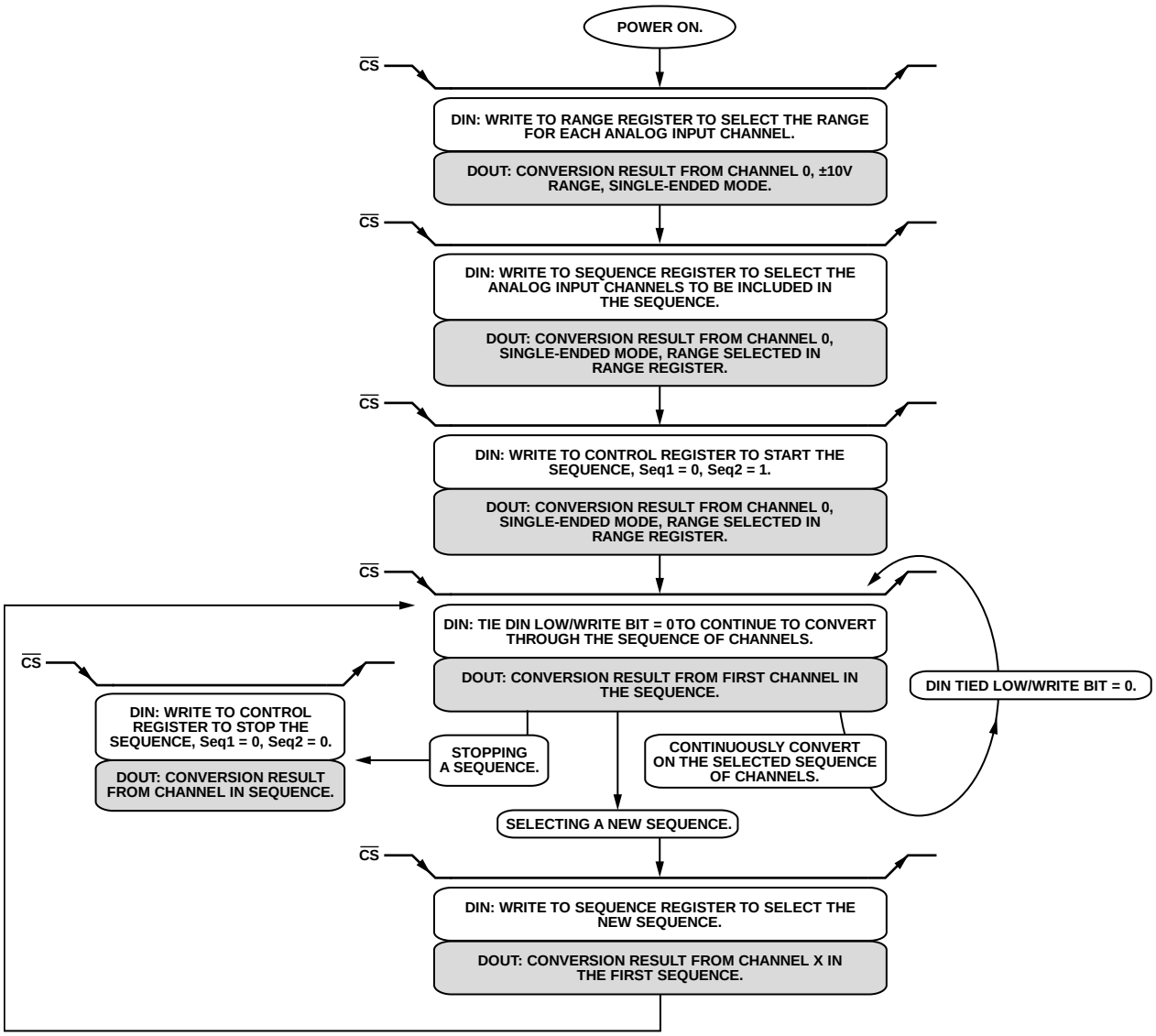

Figure 44. Programmable Sequence Flowchart

The AD7324 can be configured to automatically cycle through a number of selected channels using the on-chip sequence register with the Seq1 bit and the Seq2 bit in the control register. Figure 44 shows how to program the AD7324 register to operate in sequence mode.

After power-up, all of the three on-chip registers contain default values. Each analog input has a default input range of ±10 V. If different analog input ranges are required, a write to the range register is required. This is shown in the first serial transfer of Figure 44.

This initial serial transfer is only necessary if input ranges other than the default ranges are required. After the analog input ranges are configured, a write to the sequence register is necessary to select the channels to be included in the sequence. Once the channels for the sequence have been selected, the sequence can be initiated by writing to the control register and setting Seq1 to 0 and Seq2 to 1. The AD7324 continues to convert the selected sequence without interruption provided that the sequence register remains unchanged, and Seq1 = 0 and Seq2 = 1 in the control register.

If a change to the range register is required during a sequence, it is necessary to first stop the sequence by writing to the control register and setting Seq1 to 0 and Seq2 to 0. Next, the write to the range register should be completed to change the required range. The previously selected sequence should then be initiated again by writing to the control register and setting Seq1 to 0 and Seq2 to 1. The ADC converts on the first channel in the sequence.

The AD7324 can be configured to convert a sequence of consecutive channels (see Figure 45). This sequence begins by converting on Channel 0 and ends with a final channel as selected by Bit ADD1 to Bit ADD0 in the control register. In this configuration, there is no need for a write to the sequence register. To operate the AD7324 in this mode, set Seq1 to 1 and Seq2 to 0 in the control register, and then select the final channel in the sequence by programming Bit ADD1 to Bit ADD0 in the control register.

Once the control register is configured to operate the AD7324 in this mode, the DIN line can be held low, or the write bit can be set to 0. To return to traditional multichannel operation, a write to the control register to set Seq1 to 0 and Seq2 to 0 is necessary.

When the Seq1 and Seq2 are both set to 0, or when both are set to 1, the AD7324 is configured to operate in traditional multichannel mode, where a write to Channel Address Bit ADD1 to Bit ADD0 in the control register selects the next channel for conversion.

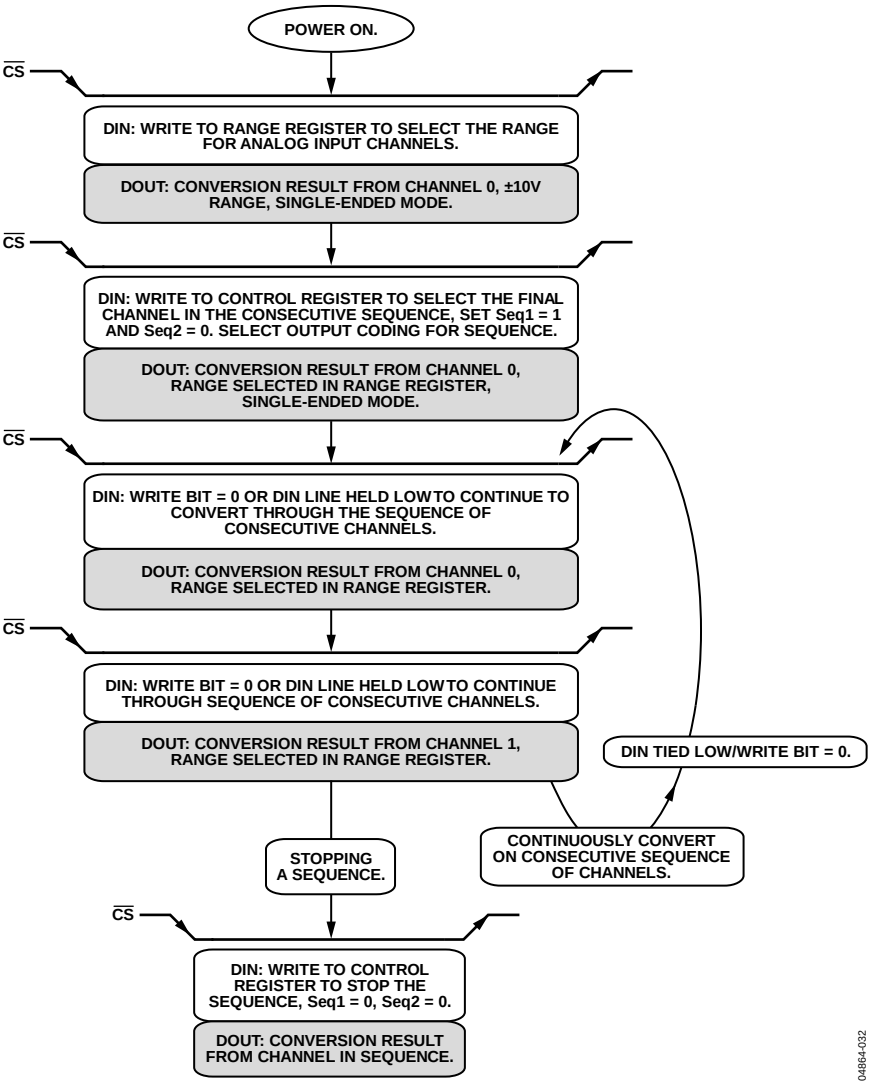

Figure 45. Flowchart for Consecutive Sequence of Channels

REFERENCE

The AD7324 can operate with either the internal 2.5 V on-chip reference or an externally applied reference. The internal reference is selected by setting the Ref bit in the control register to 1. On power-up, the Ref bit is 0, selecting the external reference for the AD7324 conversion. Suitable reference sources for the AD7324 include AD780, AD1582, ADR431, REF193, and ADR391.

The internal reference circuitry consists of a 2.5 V band gap reference and a reference buffer. When operating the AD7324 in internal reference mode, the 2.5 V internal reference is available at the REFIN/OUT pin, which should be decoupled to AGND using a 680 nF capacitor. It is recommended that the internal reference be buffered before applying it elsewhere in the system. The internal reference is capable of sourcing up to 90 μA.

On power-up, if the internal reference operation is required for the ADC conversion, a write to the control register is necessary to set the Ref bit to 1. During the control register write, the conversion result from the first initial conversion is invalid. The reference buffer requires 500 μs to power up and charge the 680 nF decoupling capacitor during the power-up time.

The AD7324 is specified for a 2.5 V to 3 V reference range. When a 3 V reference is selected, the ranges are ±12 V, ±6 V, ±3 V, and 0 V to +12 V. For these ranges, the V_{DD} and V_{SS} supply must be equal to or greater than the maximum analog input range selected, see Table 6.

V_{DRIVE}

The AD7324 has a V_{DRIVE} feature to control the voltage at which the serial interface operates. V_{DRIVE} allows the ADC to easily interface to both 3 V and 5 V processors. For example, if the AD7324 is operated with a V_{CC} of 5 V, the V_{DRIVE} pin can be powered from a 3 V supply. This allows the AD7324 to accept large bipolar input signals with low voltage digital processing.

MODES OF OPERATION

The AD7324 has several modes of operation that are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for different application requirements. The mode of operation of the AD7324 is controlled by the power management bits, Bit PM1 and Bit PM0, in the control register as shown in Table 11. The default mode is normal mode, where all internal circuitry is fully powered up.

NORMAL MODE

(PM1 = PM0 = 0)

This mode is intended for the fastest throughput rate performance, with the AD7324 being fully powered up at all times. Figure 46 shows the general operation of the AD7324 in normal mode.

The conversion is initiated on the falling edge of $\overline{CS}$, and the track-and-hold enters hold mode as described in the Serial Interface section. Data on the DIN line during the 16 SCLK transfer is loaded into one of the on-chip registers if the write bit is set. The register is selected by programming the register select bits (see Figure 46).

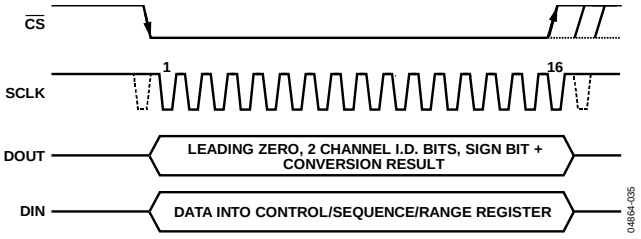

Figure 46. Normal Mode

The AD7324 remains fully powered up at the end of the conversion if both PM1 and PM0 contain 0 in the control register.

To complete the conversion and access the conversion result 16 serial clock cycles are required. At the end of the conversion, $\overline{CS}$ can idle either high or low until the next conversion.

Once the data transfer is complete, another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed.

FULL SHUTDOWN MODE

(PM1 = PM0 = 1)

In this mode, all internal circuitry on the AD7324 is powered down. The part retains information in the registers during full shutdown. The AD7324 remains in full shutdown mode until the power management bits, Bit PM1 and Bit PM0, in the control register are changed.

A write to the control register with PM1 = 1 and PM0 = 1 places the part into full shutdown mode. The AD7324 enters full shutdown mode on the 15th SCLK rising edge once the control register is updated.

If a write to the control register occurs while the part is in full shutdown mode with the power management bits, Bit PM1 and Bit PM0, set to 0 (normal mode), the part begins to power up on the 15th SCLK rising edge once the control register is updated. Figure 47 shows how the AD7324 is configured to exit full shutdown mode. To ensure the AD7324 is fully powered up, $t_{POWER-UP}$ for full shutdown mode should elapse before the next $\overline{CS}$ falling edge

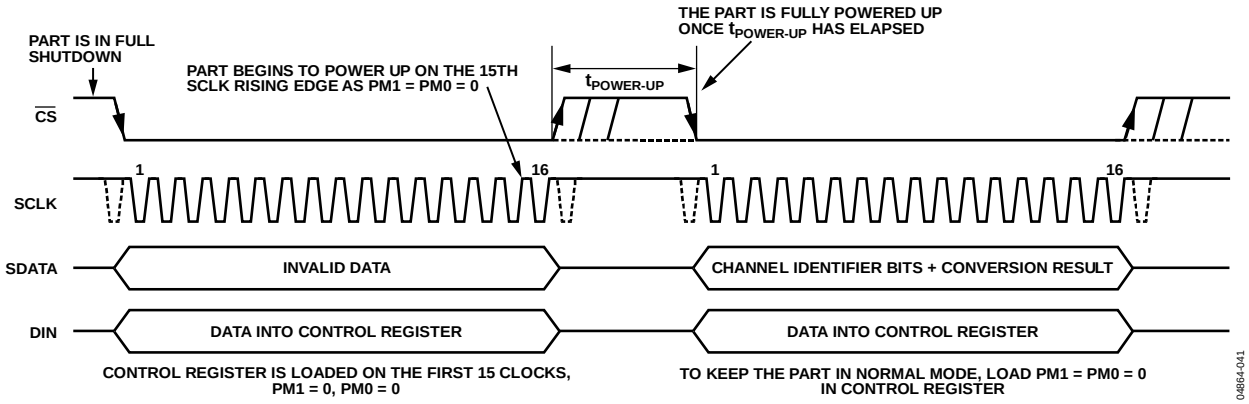

Figure 47. Exiting Full Shutdown Mode

AUTOSHUTDOWN MODE

(PM1 = 1, PM0 = 0)

Once the autoshutdown mode is selected, the AD7324 automatically enters shutdown on the 15th SCLK rising edge. In autoshutdown mode, all internal circuitry is powered down. The AD7324 retains information in the registers during autoshutdown. The track-and-hold is in hold mode during autoshutdown. On the rising $\overline{CS}$ edge, the track-and-hold, which was in hold during shutdown, returns to track as the AD7324 begins to power up. The power-up from autoshutdown is 500 µs.

When the control register is programmed to transition to autoshutdown mode, it does so on the 15th SCLK rising edge. Figure 48 shows the part entering autoshutdown mode. Once in autoshutdown mode, the $\overline{CS}$ signal must remain low to keep the part in autoshutdown mode. The AD7324 automatically begins to power up on the $\overline{CS}$ rising edge. The $t_{POWER-UP}$ for autoshutdown is required before a valid conversion, initiated by bringing the $\overline{CS}$ signal low, can take place. Once this valid conversion is complete, the AD7324 powers down again on the 15th SCLK rising edge. The $\overline{CS}$ signal must remain low again to keep the part in autoshutdown mode.

AUTOSTANDBY MODE

(PM1 = 0, PM0 =1)

In autostandby mode, portions of the AD7324 are powered down, but the on-chip reference remains powered up. The reference bit in the control register should be 1 to ensure that the on-chip reference is enabled. This mode is similar to autoshutdown, but allows the AD7324 to power up much faster. This allows faster throughput rates to be achieved.

As is the case with the autoshutdown mode, the AD7324 enters standby on the 15th SCLK rising edge once the control register is updated (see Figure 48). The part retains information in the registers during standby. Once in autostandby mode, the $\overline{CS}$ signal must remain low to keep the part in autostandby mode. The AD7324 remains in standby until it receives a $\overline{CS}$ rising edge. The ADC begins to power up on the $\overline{CS}$ rising edge. On the $\overline{CS}$ rising edge, the track-and-hold, which was in hold mode while the part was in standby, returns to track. The power-up time from standby is 700 ns.

The user should ensure that 700 ns have elapsed before bringing $\overline{CS}$ low to attempt a valid conversion. Once this valid conversion is complete, the AD7324 again returns to standby on the 15th SCLK rising edge. The $\overline{CS}$ signal must remain low to keep the part in standby mode.

Figure 48 shows the part entering autoshutdown mode. The sequence of events is the same when entering autostandby mode. In Figure 48, the power management bits are configured for autoshutdown. For autostandby mode, the power management bits, PM1 and PM0, should be set to 0 and 1, respectively.

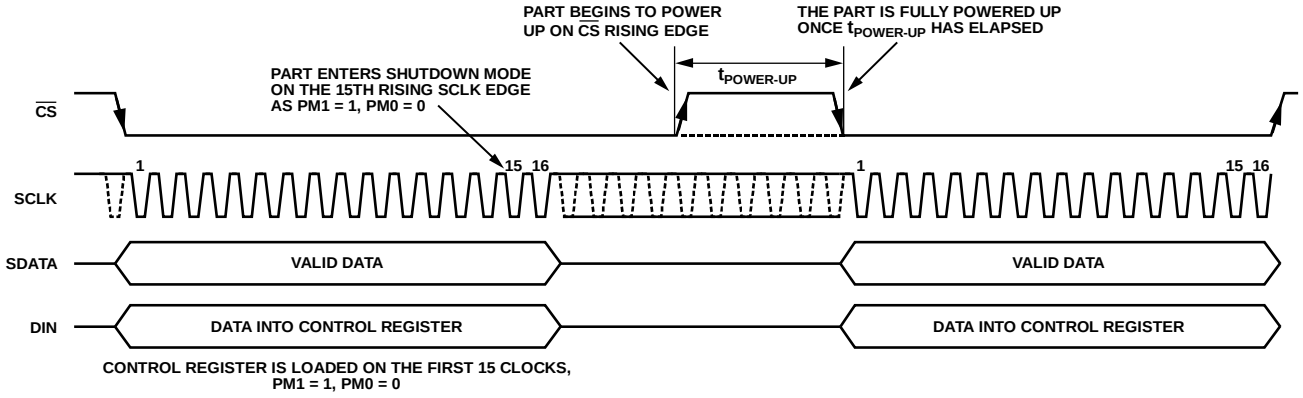

Figure 48. Entering Autoshutdown/Autostandby Mode

POWER VS. THROUGHPUT RATE

The power consumption of the AD7324 varies with throughput rate. The static power consumed by the AD7324 is very low, and a significant power savings can be achieved as the throughput rate is reduced. Figure 49 and Figure 50 shows the power vs. throughput rate for the AD7324 at a V_{CC} of 3 V and 5 V, respectively. Both plots clearly show that the average power consumed by the AD7324 is greatly reduced as the sample frequency is reduced. This is true whether a fixed SCLK value is used or if it is scaled with the sampling frequency. Figure 49 and Figure 50 show the power consumption when operating in normal mode for a fixed 20 MHz SCLK and a variable SCLK that scales with the sampling frequency.

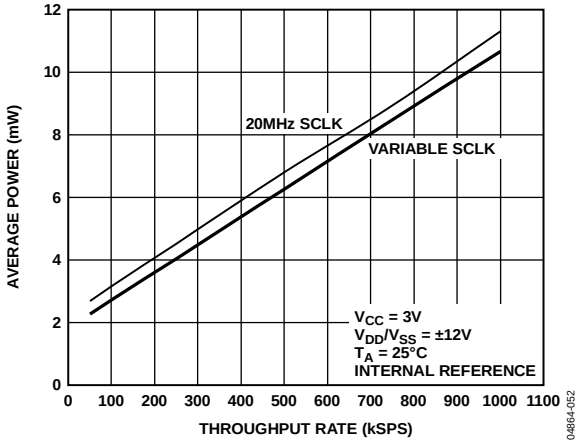

Figure 49. Power vs. Throughput Rate with 3 V V_{CC}

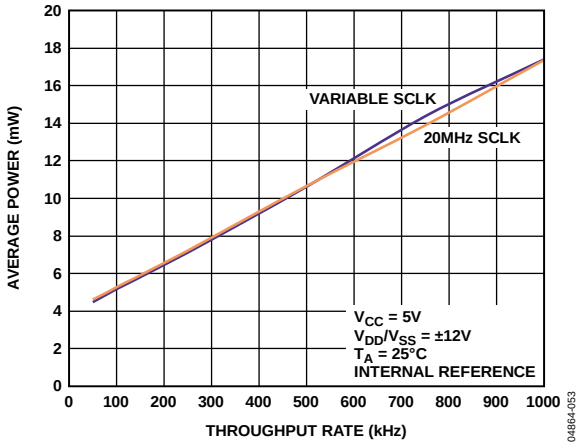

Figure 50. Power vs. Throughput Rate with 5 V V_{CC}

SERIAL INTERFACE

Figure 51 shows the timing diagram for the serial interface of the AD7324. The serial clock applied to the SCLK pin provides the conversion clock and controls the transfer of information to and from the AD7324 during a conversion.

The $\overline{CS}$ signal initiates the data transfer and the conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode and takes the bus out of three-state. Then the analog input signal is sampled. Once the conversion is initiated, it requires 16 SCLK cycles to complete.

The track-and-hold goes back into track mode on the 14th SCLK rising edge. On the 16th SCLK falling edge, the DOUT line returns to three-state. If the rising edge of $\overline{CS}$ occurs before 16 SCLK cycles have elapsed, the conversion is terminated, and the DOUT line returns to three-state. Depending on where the $\overline{CS}$ signal is brought high, the addressed register may be updated.

Data is clocked into the AD7324 on the SCLK falling edge. The 3 MSBs on the DIN line are decoded to select which register is being addressed. The control register is a 12-bit register. If the control register is addressed by the 3 MSBs, the data on the DIN line is loaded into the control on the 15th SCLK rising edge. If the sequence register or the range register is addressed, the data on the DIN line is loaded into the addressed register on the 11th SCLK falling edge.

Conversion data is clocked out of the AD7324 on each SCLK falling edge. Data on the DOUT line consists of a leading ZERO bit, two channel identifier bits, a sign bit, and a 12-bit conversion result. The channel identifier bits are used to indicate which channel corresponds to the conversion result. The leading ZERO bit is clocked out on the $\overline{CS}$ falling edge, and the first channel identifier bit is clocked out on the first SCLK falling edge.

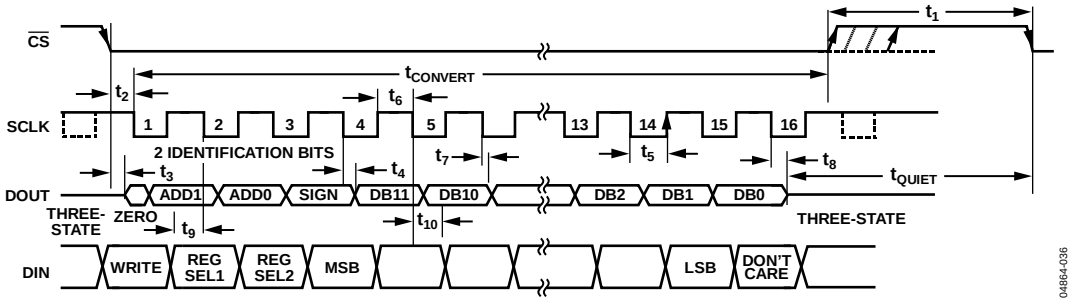

Figure 51. Serial Interface Timing Diagram (Control Register Write)

MICROPROCESSOR INTERFACING

The serial interface on the AD7324 allows the part to be directly connected to a range of different microprocessors. This section explains how to interface the AD7324 with some common microcontroller and DSP serial interface protocols.

AD7324 TO ADSP-21xx

The ADSP-21xx family of DSPs interface directly to the AD7324 without requiring glue logic. The V_{DRIVE} pin of the AD7324 takes the same supply voltage as that of the ADSP-21xx. This allows the ADC to operate at a higher supply voltage than its serial interface. The SPORT0 on the ADSP-21xx should be configured as shown in Table 14.

Table 14. SPORT0 Control Register Setup

Setting	Description
TFSW = RFSW = 1	Alternative framing
INVRFS = INVTFS = 1	Active low frame signal
DTYPE = 00	Right justify data
SLEN = 1111	16-bit data word
ISCLK = 1	Internal serial clock
TFSR = RFSR = 1	Frame every word
IRFS = 0	
ITFS = 1	

The connection diagram is shown in Figure 52. The ADSP-21xx has TFS0 and RFS0 tied together. TFS0 is set as an output, and RFS0 is set as an input. The DSP operates in alternative framing mode, and the SPORT0 control register is set up as described in Table 14. The frame synchronization signal generated on the TFS is tied to $\overline{CS}$ and, as with all signal processing applications, requires equidistant sampling. However, as in this example, the timer interrupt is used to control the sampling rate of the ADC, and under certain conditions, equidistant sampling cannot be achieved.

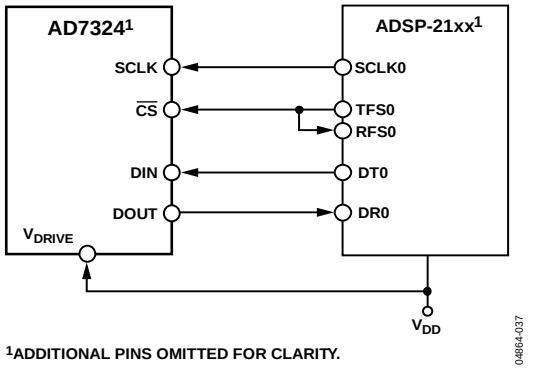

Figure 52. Interfacing the AD7324 to the ADSP-21xx

The timer registers are loaded with a value that provides an interrupt at the required sampling interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS and, therefore, the reading of data.

The frequency of the serial clock is set in the SCLKDIV register. When the instruction to transmit with TFS is given (AX0 = TX0), the state of the serial clock is checked. The DSP waits until the SCLK has gone high, low, and high again before starting the transmission. If the timer and SCLK are chosen, so that the instruction to transmit occurs on or near the rising edge of SCLK, data can be transmitted immediately or at the next clock edge.

For example, the ADSP-2111 has a master clock frequency of 16 MHz. If the SCLKDIV register is loaded with the value 3, an SCLK of 2 MHz is obtained, and eight master clock periods elapse for every one SCLK period. If the timer registers are loaded with the value 803, 100.5 SCLKs occur between interrupts and, subsequently, between transmit instructions. This situation leads to nonequidistant sampling because the transmit instruction occurs on an SCLK edge. If the number of SCLKs between interrupts is an integer of N, equidistant sampling is implemented by the DSP.

AD7324 TO ADSP-BF53x

The ADSP-BF53x family of DSPs interface directly to the AD7324 without requiring glue logic, as shown in Figure 53. The SPORT0 Receive Configuration 1 register should be set up as outlined in Table 15.

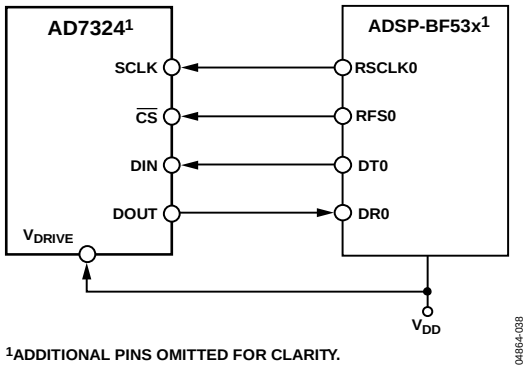

Figure 53. Interfacing the AD7324 to the ADSP-BF53x

Table 15. SPORT0 Receive Configuration 1 Register

Setting	Description
RCKFE = 1	Sample data with falling edge of RSCLK
LRFS = 1	Active low frame signal
RFSR = 1	Frame every word
IRFS = 1	Internal RFS used
RLSBIT = 0	Receive MSB first
RDTYPE = 00	Zero fill
IRCLK = 1	Internal receive clock
RSPEN = 1	Receive enable
SLEN = 1111	16-bit data-word
TFSR = RFSR = 1	

APPLICATION HINTS

LAYOUT AND GROUNDING

The printed circuit board that houses the AD7324 should be designed so that the analog and digital sections are confined to certain areas of the board. This design facilitates the use of ground planes that can easily be separated.

To provide optimum shielding for ground planes, a minimum etch technique is generally best. All AGND pins on the AD7324 should be connected to the AGND plane. Digital and analog ground pins should be joined in only one place. If the AD7324 is in a system where multiple devices require an AGND and DGND connection, the connection should still be made at only one point. A star point should be established as close as possible to the ground pins on the AD7324.

Good connections should be made to the power and ground planes. This can be done with a single via or multiple vias for each supply and ground pin.

Avoid running digital lines under the AD7324 device because this couples noise onto the die. However, the analog ground plane should be allowed to run under the AD7324 to avoid noise coupling. The power supply lines to the AD7324 device should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

To avoid radiating noise to other sections of the board, components, such as clocks, with fast switching signals should be shielded with digital ground and never run near the analog inputs. Avoid crossover of digital and analog signals. To reduce the effects of feedthrough within the board, traces should be run at right angles to each other. A microstrip technique is the best method, but its use may not be possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, and signals are placed on the other side.

Good decoupling is also important. All analog supplies should be decoupled with 10 µF tantalum capacitors in parallel with 0.1 µF capacitors to AGND. To achieve the best results from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. The 0.1 µF capacitors should have a low effective series resistance (ESR) and low effective series inductance (ESI), such as is typical of common ceramic and surface mount types of capacitors. These low ESR, low ESI capacitors provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

POWER SUPPLY CONFIGURATION

It is recommended that Schottky diodes be placed in series with the AD7324 V_{DD} and V_{SS} supply signals. Figure 54 shows this Schottky diode configuration. BAT43 Schottky diodes are used.

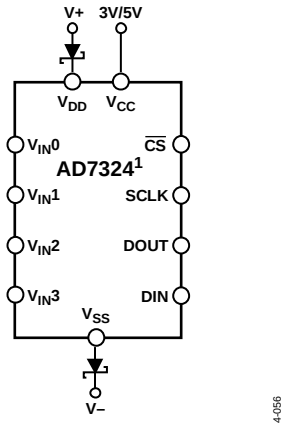

Figure 54. Schottky Diode Connection

In an application where non-symmetrical V_{DD} and V_{SS} supplies are being used, adhere to the following guidelines. Table 16 outlines the V_{SS} supply range that can be used for particular V_{DD} voltages when non-symmetrical supplies are required. When operating the AD7324 with low V_{DD} and V_{SS} voltages, it is recommended that these supplies be symmetrical.

Table 16. Non-Symmetrical V_{DD} and V_{SS} Requirements

V_{DD}	Typical V_{SS} Range
5 V	−5 V to −5.5 V
6 V	−5 V to −8.5 V
7 V	−5 V to −11.5 V
8 V	−5 V to −15 V
9 V	−5 V to −16.5 V
10 V to 16.5 V	−5 V to −16.5 V

For the 0 to 4 × V_{REF} range, V_{SS} can be tied to AGND as per minimum supply recommendations outlined in Table 6.

OUTLINE DIMENSIONS

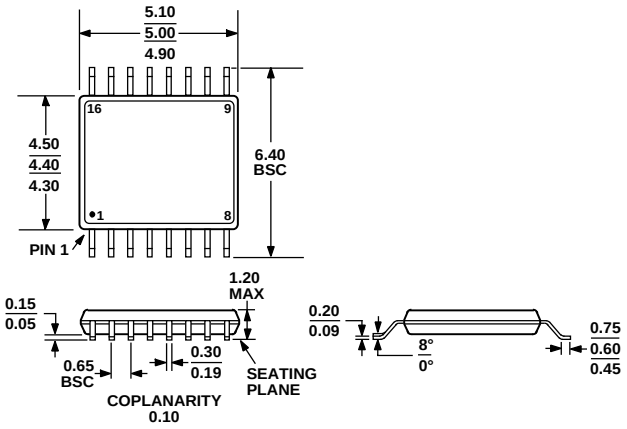

Figure 55. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions show in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7324BRUZ	−40°C to +85°C	16-Lead TSSOP	RU-16
AD7324BRUZ-REEL	−40°C to +85°C	16-Lead TSSOP	RU-16
AD7324BRUZ-REEL7	−40°C to +85°C	16-Lead TSSOP	RU-16

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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