MP2183

3A, Synchronous Step-Down Converter with SS & PG

DESCRIPTION

The MP2183 is a monolithic, step-down, switch-mode converter with built-in internal power MOSFETs. It achieves 3A continuous output current from a 2.5V to 5.5V input voltage with excellent load and line regulation. The output voltage can be regulated to as low as 0.6V.

The constant-on-time control scheme provides fast transient response and eases loop stabilization. Fault protections include cycle-by-cycle current limiting and thermal shutdown.

The MP2183 is available in an ultra-small SOT583 package and requires a minimal number of readily available, standard external components.

The MP2183 is ideal for a wide range of applications including high-performance DSPs, wireless power, portable and mobile devices, and other low-power systems.

FEATURES

- Low I_Q: 21μA
- 1.2MHz Switching Frequency
- EN for Power Sequencing
- 1% FB Accuracy
- Wide 2.5V to 5.5V Operating Input Range
- Output Adjustable from 0.6V
- Up to 3A Output Current
- 65mΩ and 35mΩ Internal Power MOSFET Switches
- 100% Duty On
- Output Discharge
- V_O OVP
- External Soft-Start Control
- Short-Circuit Protection with Hiccup Mode
- Power Good
- Available in a SOT583 Package

APPLICATIONS

- Wireless/Networking Cards
- Portable Instruments
- Battery-Powered Devices
- Low-Voltage I/O System Power
- Multi-Function Printer

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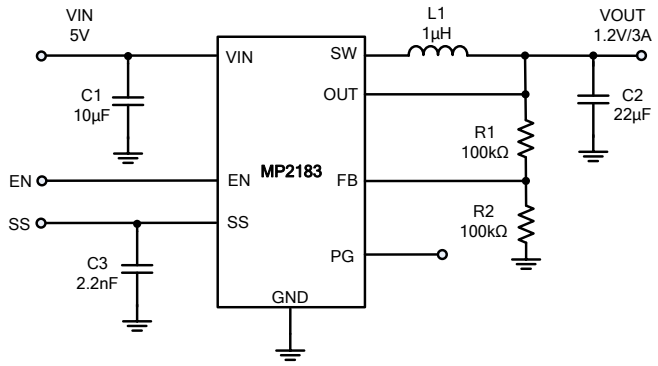
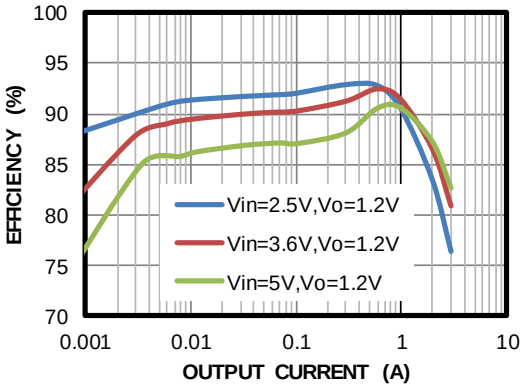
TYPICAL APPLICATION



Efficiency vs. Output Current

L = 1μH (DCR = 27mΩ)



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2183GTL	SOT583	*See Below*

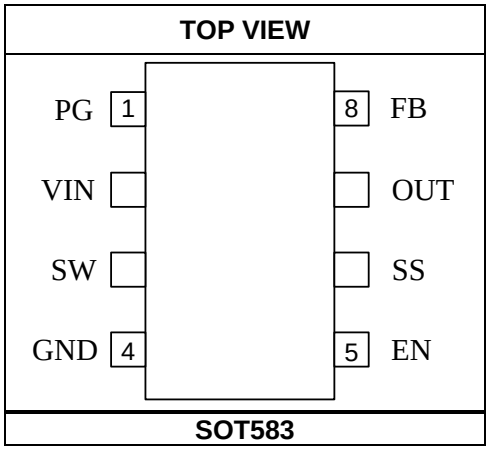
* For Tape & Reel, add suffix –Z (e.g. MP2183GTL–Z).

TOP MARKING

BEZY
LLL

BEZ: Product code of MP2183GTL
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	PG	**Power good indicator.** The output of this pin is an open drain.
2	VIN	**Supply voltage.** The MP2183 operates from a +2.5V to +5.5V unregulated input. A decoupling capacitor is needed to prevent large voltage spikes from appearing at the input.
3	SW	**Output switching node.** SW is the drain of the internal high-side P-Channel MOSFET. Connect the inductor to SW to complete the converter.
4	GND	**Ground.**
5	EN	**On/off control.**
6	SS	**Soft start.** Connect a capacitor across SS and GND to set the soft-start time to avoid start-up inrush current.
7	OUT	**Output voltage power rail and input sense pin for output voltage.** Connect load to this pin. An output capacitor is needed to decrease the output voltage ripple.
8	FB	**Feedback pin.** An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage.

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 6.5V
V_{SW}.....
-0.3V (-5V for <10ns) to 6.5V (8V for <10ns)
All other pins .....-0.3V to 6.5 V
Junction temperature .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = +25°C) (2) (4)
……. 2.3W
Storage temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....2.5V to 5.5V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance	θ_{JA}	θ_{JC}
SOT583		
EV2183-TL-00A (4)	58	13 °C/W
JESD51-7 (5)	120	55 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EV2183-TL-00A, 2-layer PCB.
5) Measured on JESD51-7, 4-layer PCB.
note 5) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values are calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +125°C [6], typical value is tested at T_J = 25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} range			2.5		5.5	V
Under-voltage lockout threshold rising				2.3	2.45	V
Under-voltage lockout threshold hysteresis				200		mV
Supply current (shutdown)		V_{EN} = 0V, T_J = 25°C		0	1	μA
Supply current (quiescent)		V_{EN} = 2V, V_{FB} = 0.63V, V_{IN} = 3.6V, T_J = 25°C		21	26	μA
Feedback voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to +125°C	591	600	609	
Feedback current	I_{FB}	V_{FB} = 0.63V		50	100	nA
PFET switch on resistance	R_{DSON_P}	V_{IN} = 5V		65		mΩ
NFET switch on resistance	R_{DSON_N}	V_{IN} = 5V		35		mΩ
Switch leakage		V_{EN} = 0V, V_{IN} = 6V V_{SW} = 0V or 6V, T_J = 25°C		0	1	μA
Switching frequency	f_{SW}	V_{IN} = 5V, V_{OUT} = 1.2V, operating under CCM		1200		kHz
Minimum on time [7]	t_{MIN-ON}	V_{IN} = 3.6V		70		ns
		V_{IN} = 2.5V		80		ns
Minimum off time [7]	$t_{MIN-OFF}$	V_{IN} = 3.6V		80		ns
		V_{IN} = 2.5V		90		ns
PFET peak current limit			4	5	6	A
NFET valley current limit				3		A
ZCD				50		mA
Soft-start current	I_{SS_ON}		1.5	3	4.5	μA
Maximum duty cycle			100			%
Power good rising threshold UV		FB rising edge	87	90	93	%
Power good falling threshold UV		FB falling edge	82	85	88	%
Power good delay	PG_D	PG rising/falling edge		80		μs
Power good sink current capability	V_{PG-L}	Sink 1mA			0.4	V
Power good logic high voltage	V_{PG-H}	V_{IN} = 5V, V_{FB} = 0.6V	4.9			V
Self-bias PG		When VIN & EN are not available, PG pull-up voltage = 3.6V, pull-up resistor = 300kΩ			0.7	V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +125°C [6], typical value is tested at T_J = 25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power good leakage current/logic high		5V logic high			100	nA
EN turn-on delay		EN on to SW active		100		µs
EN turn-off delay		EN off to stop switching		30		µs
EN input logic low voltage					0.4	V
EN input logic high voltage			1.2			V
EN pull-down resistor				2		MΩ
Output discharge resistor	R_{DIS}	V_{EN} = 0V, V_{OUT} = 1.2V		150		Ω
EN input current		V_{EN} = 2V		1		µA
		V_{EN} = 0V		0		µA
Output over-voltage threshold	V_{OVP}		110%	115%	120%	V_{FB}
V_O OVP hysteresis	V_{OVP_HYS}			10%		V_{FB}
OVP delay				6		µs
Low-side current limit		Current flow from SW to GND		1.5		A
Absolute VIN OVP		After V_O OVP enable		6.1		V
Absolute VIN OVP hysteresis				160		mV
Thermal shutdown [7]				160		°C
Thermal hysteresis [7]				30		°C

Notes:

6) Not tested in production. Guaranteed by over-temperature correlation.
7) Guaranteed by engineer sample characterization.

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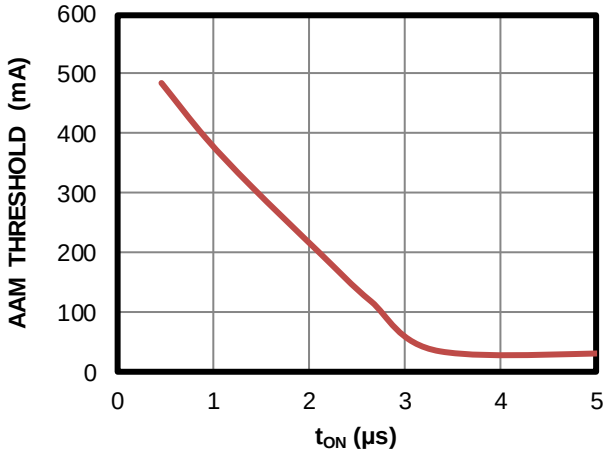
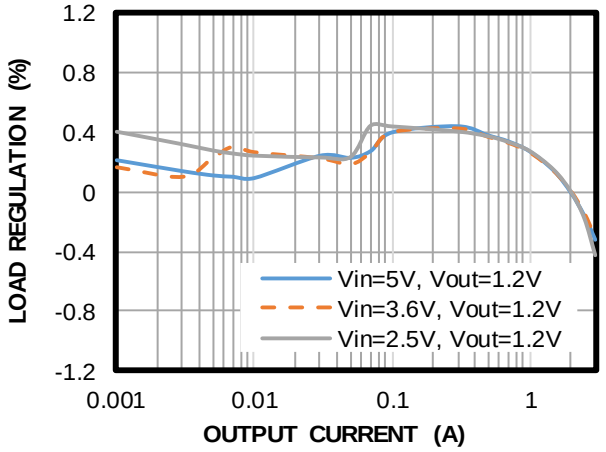
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1μH, C_{OUT} = 44μF, T_A = 25°C, unless otherwise noted.

AAM Threshold vs. t_{ON}

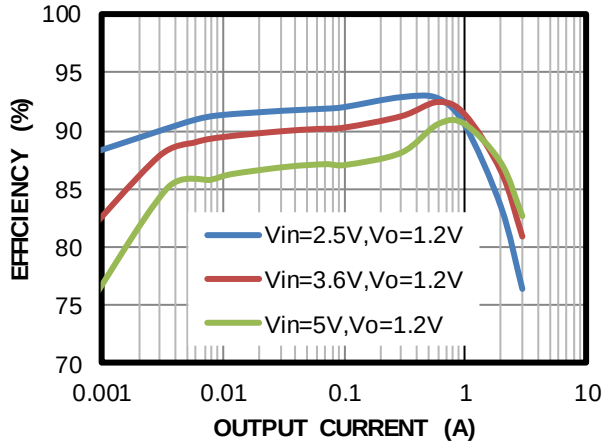


Load Regulation vs. Output Current

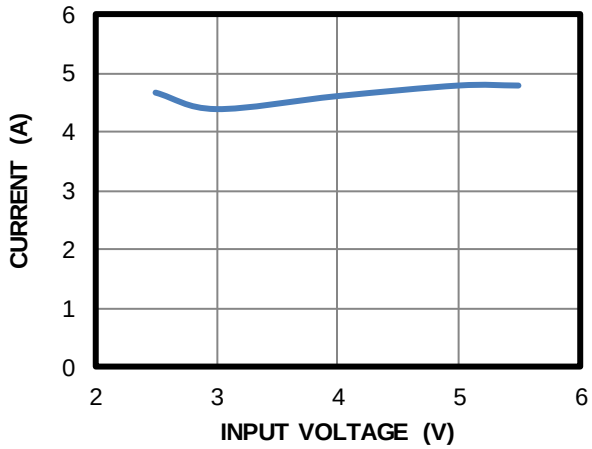


Efficiency vs. Output Current

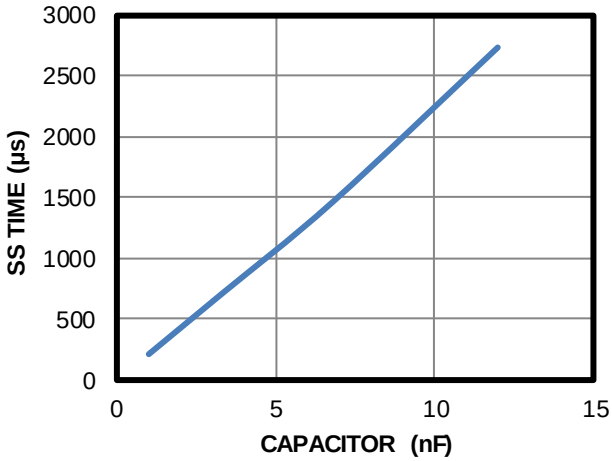
L = 1μH (DCR = 27mΩ)



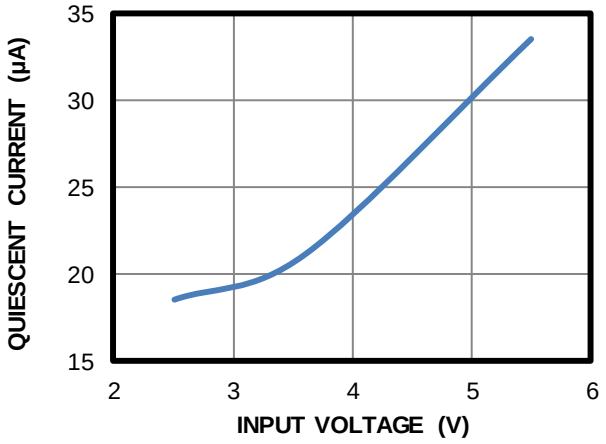
I_{PEAK} vs. V_{IN}



SS Time vs. SS Capacitor



Quiescent Current vs. V_{IN}



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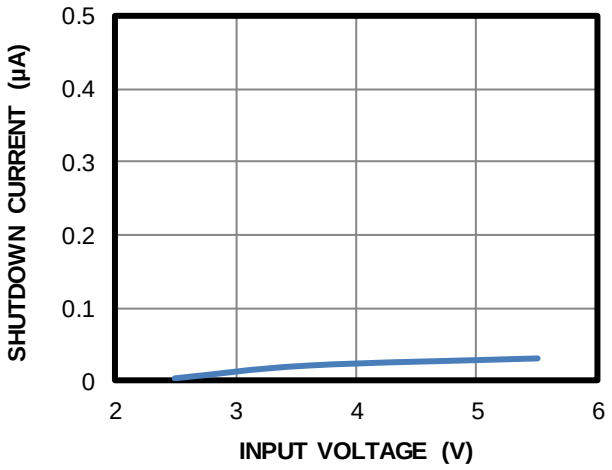
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

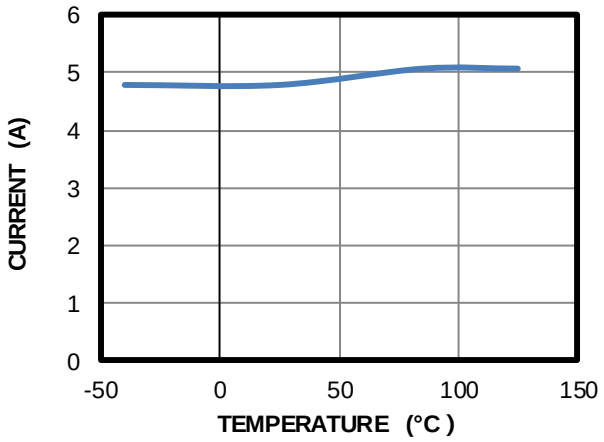
V_{IN} = 5V, V_{OUT} = 1.2V, L = 1μH, C_{OUT} = 44μF, T_A = 25°C, unless otherwise noted.

Shutdown Current vs. Input Voltage



Peak Current Limit vs. Temperature

V_{IN} = 5V



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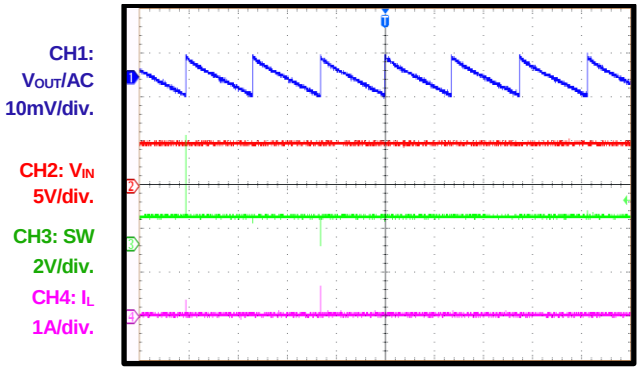
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1μH, C_{OUT} = 44μF, T_A = 25°C, unless otherwise noted.

Steady State

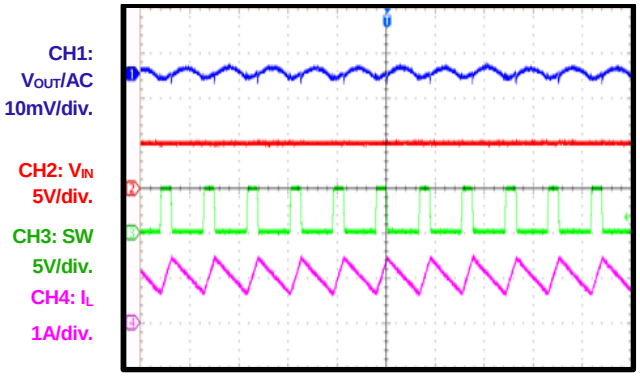
I_{OUT} = 0A



4ms/div.

V_{OUT} Ripple

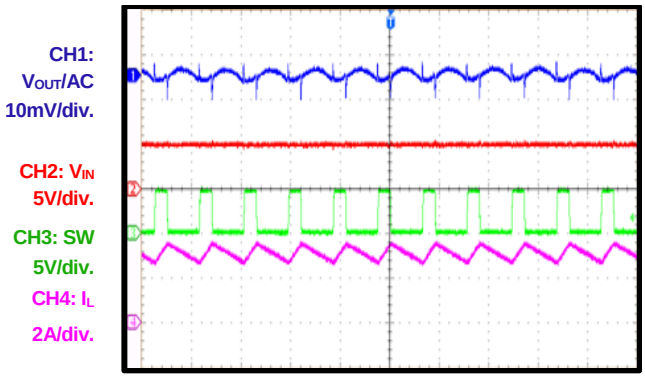
with 1A load



1μs/div.

V_{OUT} Ripple

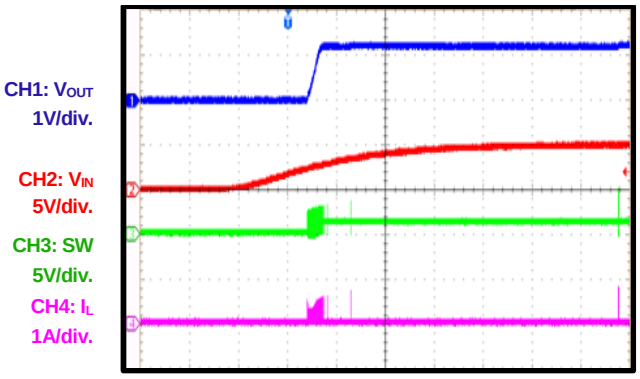
with 3A load



1μs/div.

V_{IN} Power On

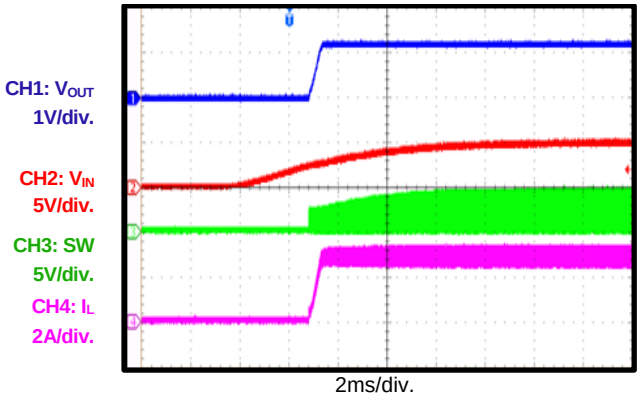
without load



2ms/div.

V_{IN} Power On

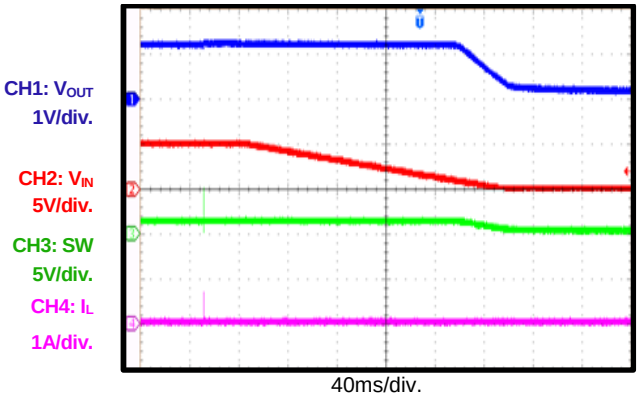
with 3A load



2ms/div.

V_{IN} Power Off

without load



40ms/div.

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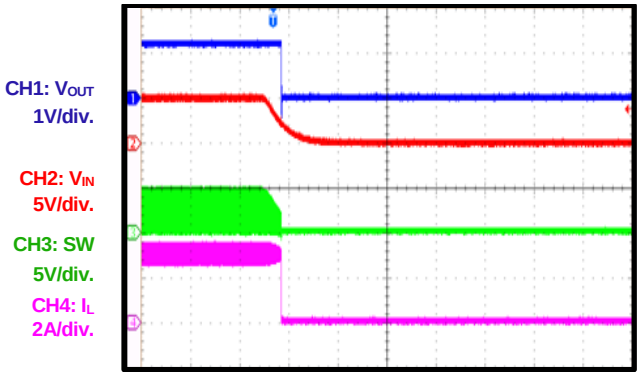
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

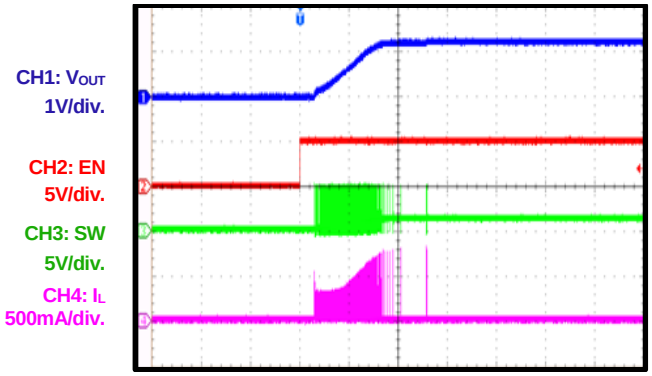
V_{IN} = 5V, V_{OUT} = 1.2V, L = 1μH, C_{OUT} = 44μF, T_A = 25°C, unless otherwise noted.

V_{IN} Power Off
with 3A load



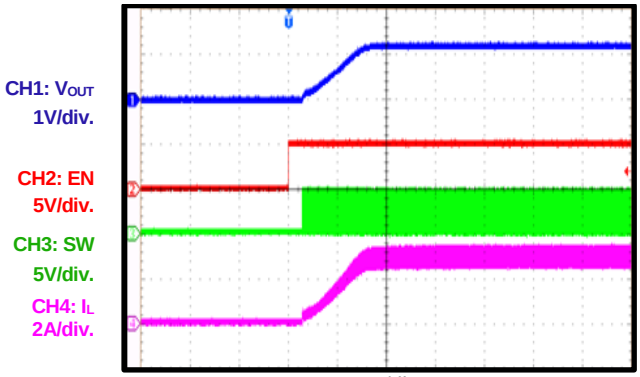
10ms/div.

EN On
without load



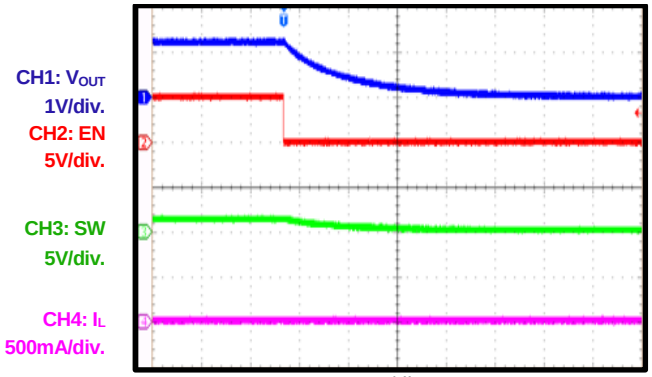
400μs/div.

EN On
with 3A load



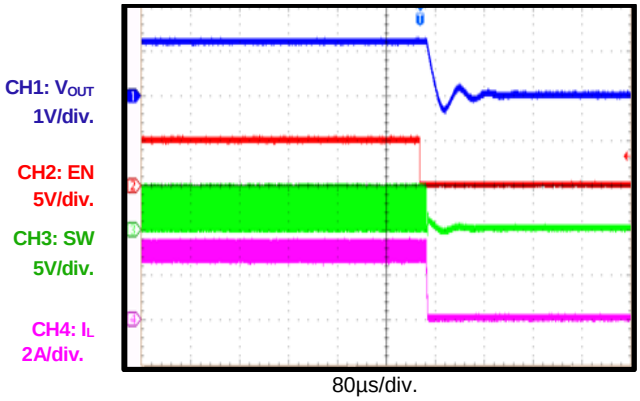
400μs/div.

EN Off
without load



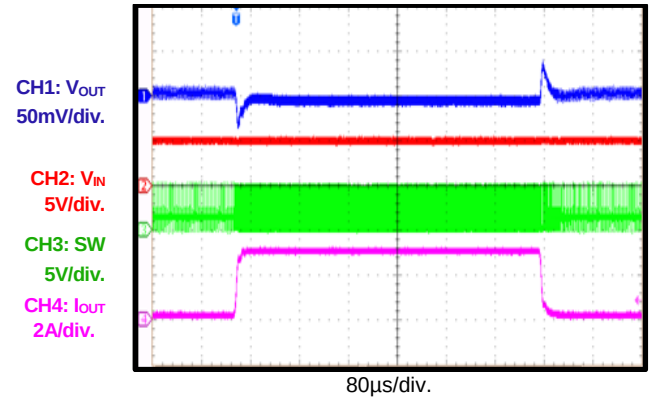
4ms/div.

EN Off
with 3A load



80μs/div.

Load Transient Response
I_{OUT} = 0.1A to 3A



80μs/div.

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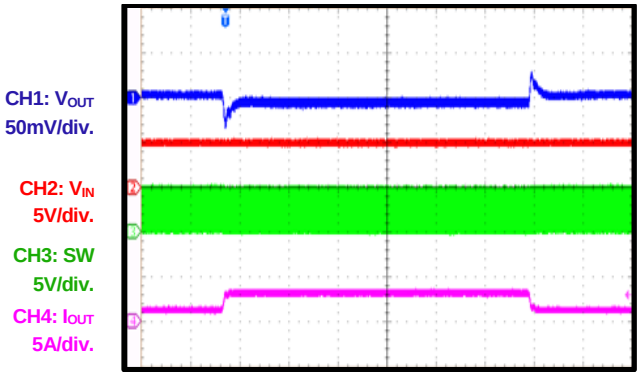
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 44µF, T_A = 25°C, unless otherwise noted.

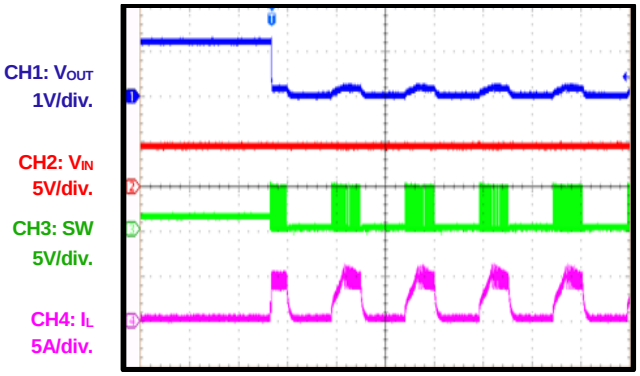
Load Transient Response

I_{OUT} = 1A to 3A



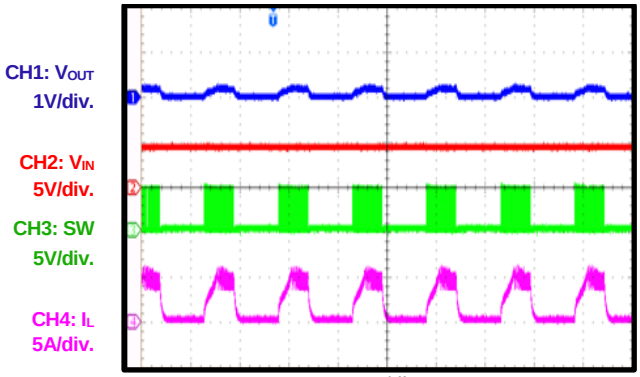
80µs/div.

Short-Circuit Entry



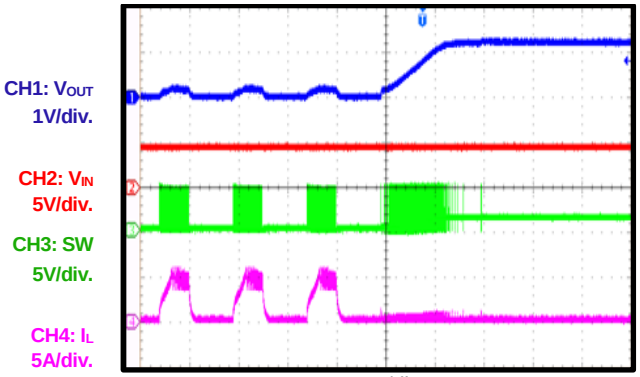
400µs/div.

Short Circuit



400µs/div.

Short-Circuit Recovery



400µs/div.

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FUNCTIONAL BLOCK DIAGRAM

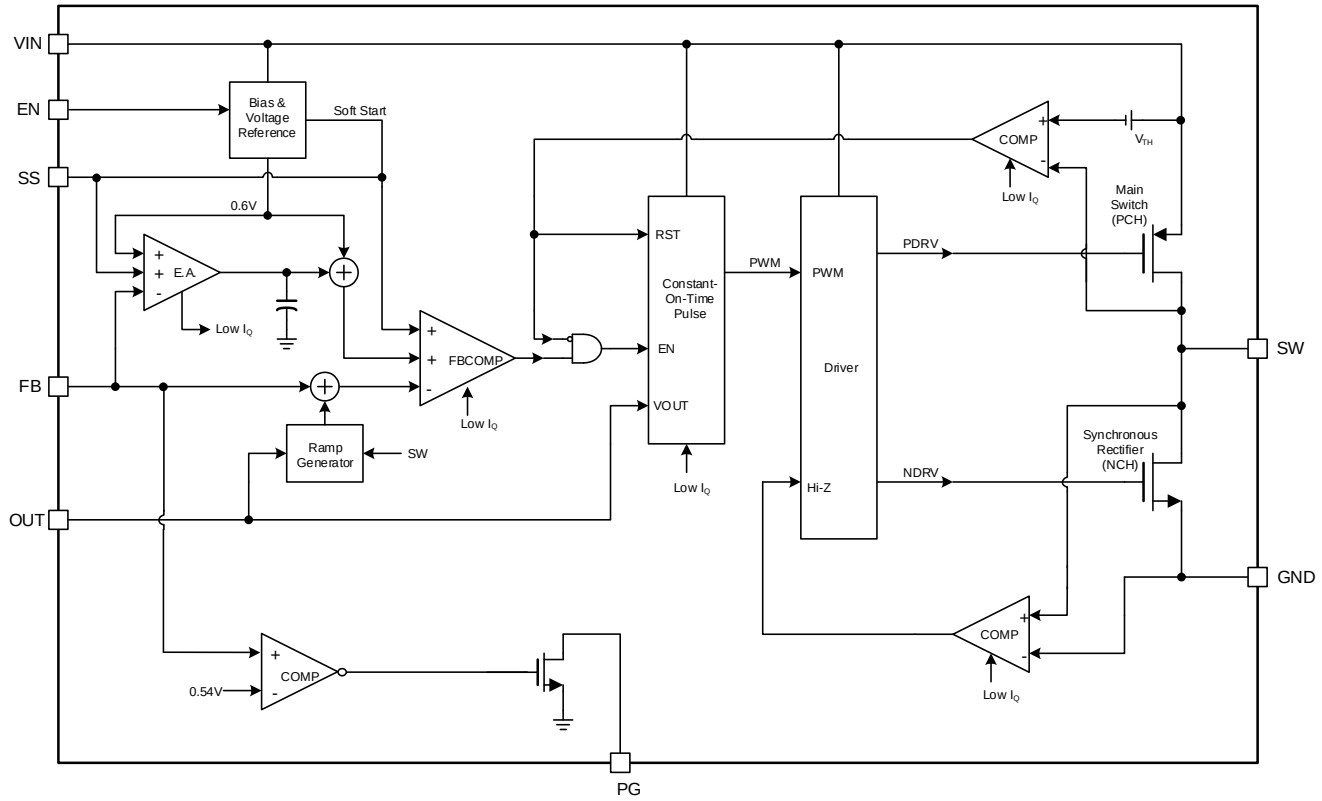

Figure 1: Functional Block Diagram

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OPERATION

The MP2183 uses constant-on-time control with input-voltage feed forward to stabilize the switching frequency over the full input range. It achieves 3A continuous output current from a 2.5V to 5.5V input voltage with excellent load and line regulation. The output voltage can be regulated to as low as 0.6V.

Constant-On-Time Control

Constant-on-time control offers a simpler control loop and a faster transient response than fixed frequency PWM control. By using input-voltage feed forward, the MP2183 maintains a nearly constant switching frequency across the input and output voltage ranges. The switching pulse on time can be estimated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 0.83\mu s \qquad (1)$$

To prevent inductor current runaway during load transient, the MP2183 has a fixed minimum off time of 90ns.

Sleep Mode Operation

The MP2183 features sleep mode to get high efficiency in extreme light-load conditions. In sleep mode, most of the circuit blocks' input currents are decreased, including the error amplifier and PWM comparator.

When the load gets lighter, the MP2183 slows down the frequency. If the off time is longer than 3.5µs, the MP2183 enters sleep mode. When a high-side pulse occurs, the MP2183 exits sleep mode.

AAM Operation at Light-Load Operation

The MP2183 has AAM (advanced asynchronous modulation) power-save mode and a ZCD (zero-current cross-detection) circuit for light load.

The MP2183 has AAM power-save mode for light load. Figure 2 shows the simplified AAM control theory. The AAM current (I_{AAM}) is set internally. The SW on pulse time is decided by the on-timer generator and AAM comparator.

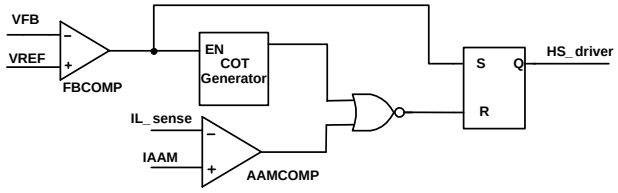

Figure 2: Simplified AAM Control Logic

In light-load conditions, the SW on pulse time is longer than the AAM comparator pulse. Figure 3 shows the operation mode if the AAM comparator pulse is longer than the on-timer generator.

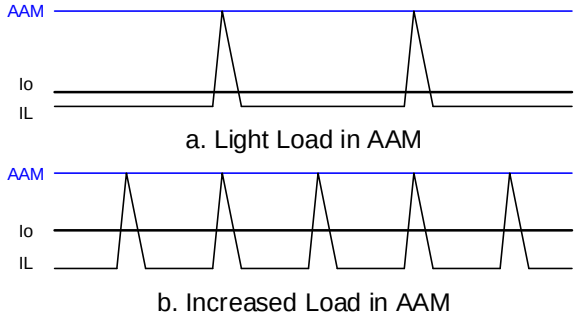

Figure 3: AAM Comparator Control t_{ON}

Figure 4 shows the operation mode if the AAM comparator pulse is shorter than the on-timer generator. Using very small inductance may cause this to occur.

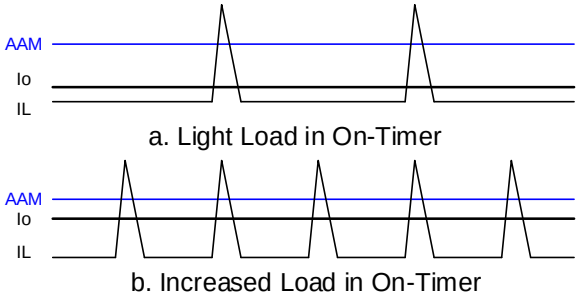

Figure 4: On-Timer Control t_{ON}

Except when using the upper on-timer method, the AAM circuit has another 150ns AAM blank time in sleep mode. This means if the on-timer is less than 150ns, the high-side MOSFET may turn off after the on-timer generator pulse without AAM control. The on-time pulse in sleep mode is about 40% larger than during DCM or CCM mode. In this condition, I_L may not reach the AAM threshold (see Figure 5).

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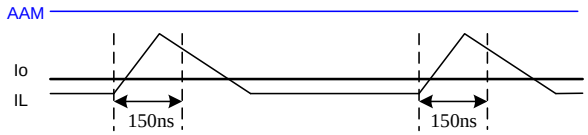

Figure 5: AAM Blank Time in Sleep Mode

Figure 6 shows how the AAM threshold decreases as t_{ON} increases gradually. For the CCM state, I_O must reach or exceed half of the AAM threshold.

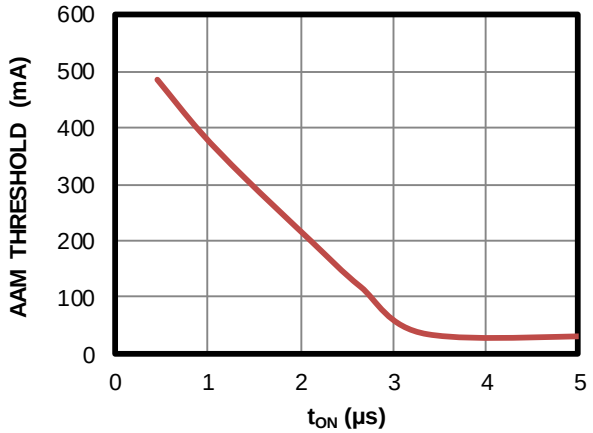

Figure 6: AAM Threshold Decreases as t_{ON} Increases

The MP2183 has a zero-current cross-detection (ZCD) circuit to judge if the inductor current starts to reverse. When the inductor current reaches the ZCD threshold, the low-side switch turns off.

Together, AAM mode and the ZCD circuit make the MP2183 always work on DCM mode at light load, even if V_O is close to V_{IN}.

Enable

When the input voltage is greater than the under-voltage lockout (UVLO) threshold (typically 2V), the MP2183 can be enabled by pulling EN above 1.2V. Leave EN floating or pull down to ground to disable the MP2183. There is an internal 2MΩ resistor from EN to ground.

When the device is disabled, the part goes into output discharge mode automatically and its internal discharge MOSFET provides a resistive discharge path for the output capacitor.

Soft Start

The MP2183 has an external soft start pin that ramps up the output voltage at a controlled slew rate to avoid overshoot at start-up. The soft start pin charge current is typically 3µA. The soft-start time is decided by its SS capacitor.

Current Limit

The MP2183 typically has a 5A high-side switch current limit. When the high-side switch hits its current limit, the MP2183 remains in hiccup mode until the current drops. This prevents the inductor current from continuing to rise and damaging components.

Short Circuit and Recovery

The MP2183 also enters short-circuit protection mode when it hits the current limit, and tries to recover with hiccup mode. The MP2183 disables the output power stage, discharges the soft-start capacitor, then automatically retries soft-start. If the short-circuit condition remains after soft start ends, the MP2183 repeats this cycle until the short circuit disappears and the output rises back to regulation level.

Over-Voltage Protection (V_O OVP)

The MP2183 monitors a resistor-divided feedback voltage to detect over-voltage. When the feedback voltage exceeds 115% of the target voltage, the controller enters dynamic regulation. During this period, the LS stays on until the LS current goes to -1.5A. This discharges the output and tries to keep it within the normal range. If OV still exists, the LS turns on again after an 800ns delay. The part exits this regulation period when the feedback voltage falls below 105% of the reference voltage. If dynamic regulation cannot limit V_{OUT} increasing, once the input detects the 6.1V input OVP, the MP2183 stops switching until the input voltage drops below 6V. The MP2183 then resumes operation.

Power Good Indicator

The MP2183 has an open-drain output and requires an external pull-up resistor (about 100kΩ to 500kΩ) for the power good indicator. When V_{FB} exceeds 90% of the regulation voltage, V_{PG} is pulled up to V_{OUT}/V_{IN} by the external resistor. If V_{FB} exceeds this window, the internal MOSFET pulls PG to ground. The MOSFET has a maximum $R_{DS(ON)}$ of less than 400Ω. When VIN and EN are not available, and if PG has an external power supply pulled up, the PG self-bias voltage is smaller than 0.7V.

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APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider sets the output voltage (see Figure 9). Select the feedback resistor (R1) that reduces the VOUT leakage current (typically 100kΩ to 200kΩ). There is no strict requirement on the feedback resistor. Select R1 to be greater than 10kΩ. R2 can then be calculated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6} - 1} \quad (2)$$

Figure 7 shows the feedback circuit.

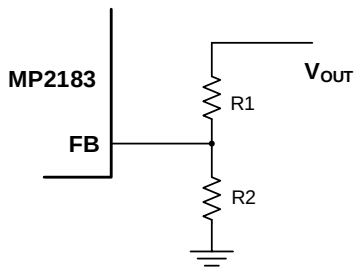

Figure 7: Feedback Network

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Values for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	200 (1%)	300 (1%)
1.2	200 (1%)	200 (1%)
1.8	200 (1%)	100 (1%)
2.5	200 (1%)	63.2 (1%)
3.3	200 (1%)	44.2 (1%)

Selecting the Inductor

Most applications work best with a 0.47µH to 1.5µH inductor. Select an inductor with a DC resistance less than 25mΩ to optimize efficiency.

A high-frequency, switch-mode power supply with a magnetic device creates strong electronic magnetic inference in a system. Any un-shielded power inductor should be avoided, as they provide poor magnetic shielding. Shielded inductors, such as metal alloy or multiplayer chip powers, are the best candidates for application and can decrease the influence effectively. Table 2 lists suggested inductors.

Table 2: Suggested Inductor List

Manufacturer P/N	Inductance (µH)	Manufacturer
PIFE25201B-1R0MS	1.0	CYNTEC CO. LTD.
1239AS-H-1R0M	1.0	Tokyo
74438322010	1.0	Wurth

For most designs, estimate the inductance value with Equation (3):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (3)$$

Where ΔI_L is the inductor ripple current.

Choose an inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10µF capacitor is sufficient. Higher output voltages may require a 22µF capacitor to increase system stability.

The input capacitor requires an adequate ripple current rating because it absorbs the input switching current. Estimate the RMS current in the input capacitor with Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case scenario occurs at $V_{IN} = 2V_{OUT}$, estimated with Equation (6):

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$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic 0.1μF capacitor as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Selecting the Output Capacitor

The output capacitor (C2) stabilizes the DC output voltage. Ceramic capacitors are recommended, and low-ESR capacitors are preferred to limit the output voltage ripple. Estimate the output voltage ripple with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (8)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

The characteristics of the output capacitor also affect the stability of the regulation system.

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PCB Layout Guidelines

Efficient layout is important for proper function of the MP2183. Poor layout design can result in poor line or load regulation and stability issues. For best results, refer to Figure 8 and follow the guidelines below:

1. Place the high-current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.
2. Place the input capacitor as close as possible to the IN and GND pins.
3. Place the output capacitor GND as close as possible to the chip GND pins.
4. Place the external feedback resistors next to the FB pin.
5. Keep the switching node (SW) short and away from the feedback network.
6. Keep the V_{OUT} sense line need as short as possible and away from power inductor, especially from surrounding the inductor.

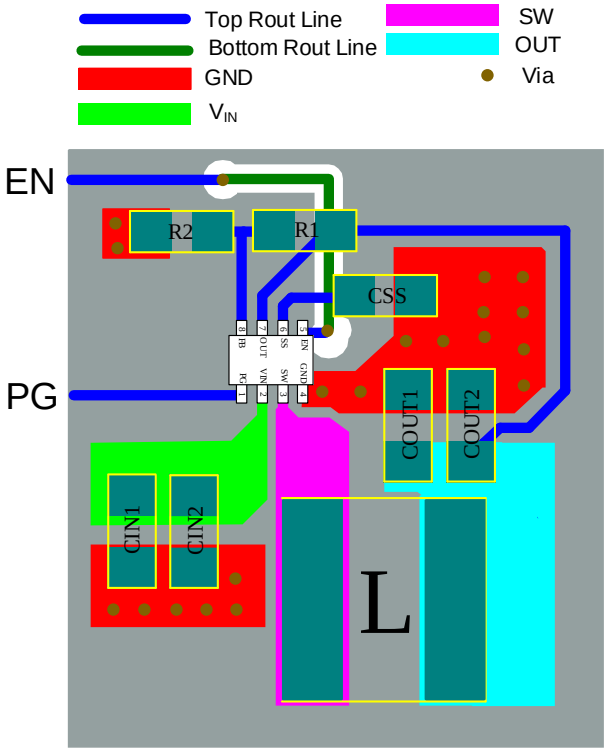

Figure 8: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

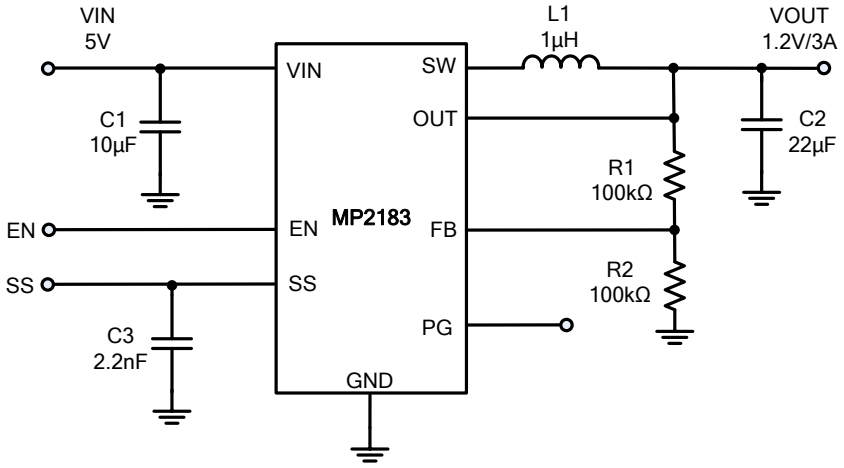

Figure 9: Typical Application Circuit

Note: V_{IN} < 3.3V may need a greater input capacitor.

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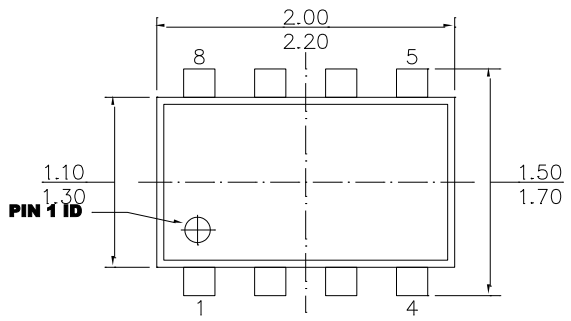
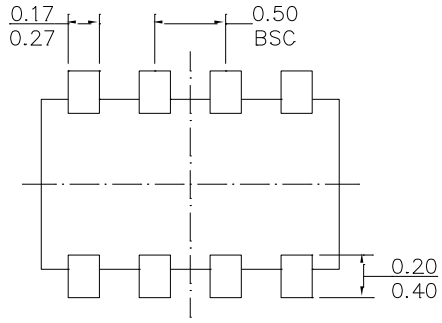
PACKAGE INFORMATION

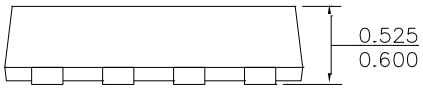
SOT583



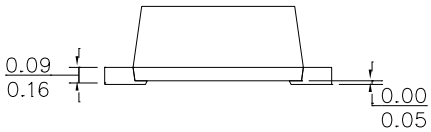
TOP VIEW



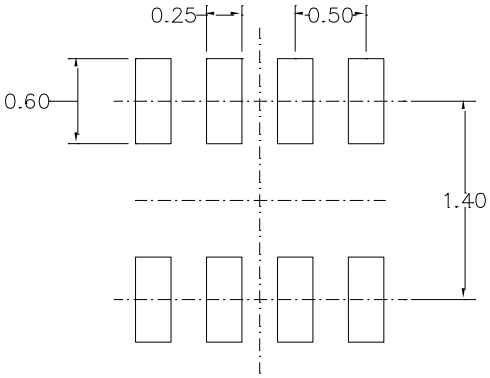
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

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2) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
3) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
4) DRAWING IS NOT TO SCALE.

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