8-Bit, High Bandwidth Multiplying DAC with Serial Interface

Data Sheet **AD5425**

FEATURES

- 2.5 V to 5.5 V supply operation
- 50 MHz serial interface
- 2.47 MSPS update rate
- INL of ±0.25 LSB
- 10 MHz multiplying bandwidth
- ±10 V reference input
- Low glitch energy: <2 nV-s
- Extended temperature range: −40°C to +125°C
- 10-lead MSOP package
- Guaranteed monotonic
- 4-quadrant multiplication
- Power-on reset with brownout detection
- $\overline{\text{LDAC}}$ function
- 0.4 µA typical power consumption

APPLICATIONS

- Portable battery-powered applications
- Waveform generators
- Analog processing
- Instrumentation applications
- Programmable amplifiers and attenuators
- Digitally controlled calibration
- Programmable filters and oscillators
- Composite video
- Ultrasound
- Gain, offset, and voltage trimming

GENERAL DESCRIPTION

The AD5425[1] is a CMOS, 8-bit, current output digital-to-analog converter (DAC) that operates from a 2.5 V to 5.5 V power supply, making it suitable for battery-powered applications and many other applications.

This DAC utilizes a double buffered, 3-wire serial interface that is compatible with SPI®, QSPI™, MICROWIRE™, and most DSP interface standards. An $\overline{\text{LDAC}}$ pin is also provided, which allows simultaneous updates in a multiDAC configuration. On power-up, the internal shift register and latches are filled with 0s and the DAC outputs are 0 V.

As a result of manufacturing on a CMOS submicron process, this DAC offers excellent 4-quadrant multiplication characteristics with large signal multiplying bandwidths of 10 MHz.

The applied external reference input voltage (V_{REF}) determines the full-scale output current. An integrated feedback resistor, R_{FB}, provides temperature tracking and full-scale voltage output when combined with an external I to V precision amplifier.

The AD5425 is available in a small, 10-lead MSOP package.

FUNCTIONAL BLOCK DIAGRAM

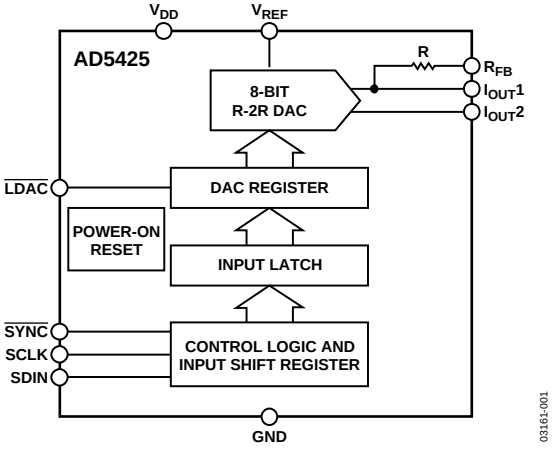


Figure 1.

[1] U.S. Patent No. 5,969,657.

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REVISION HISTORY

1/16—Rev. C to Rev. D

Deleted Positive Output Voltage Section ... 16
Changes to Adding Gain Section ... 16
Changes to ADSP-21xx to AD5425 Interface Section and Figure 39 ... 19
Changes to ADSP-BF504 to ADSP-BF592 Device Family to AD5425 Interface Section, MC68HC11 Interface to AD5425 Interface Section, and Figure 40 and Figure 41 Captions ... 20
Changes to PIC16C6x/PIC16C7x to AD5425 Section ... 21

9/12—Rev. B to Rev. C

Change to Features ... 1

6/12—Rev. A to Rev. B

Deleted ADSP-2103 and changed ADSP-2191 to ADSP-2191M Throughout ... 19
Deleted Evaluation Board Section and Operating the Evaluation Board Section, deleted Figure 46 to Figure 49, and deleted Table 11 ... 23
Changes to Ordering Guide ... 23

3/05—Rev. 0 to Rev. A

Updated Format ... Universal
Changes to Specifications Section ... 3
Added Figure 18, Figure 20, Figure 21 ... 10
Change to Table 7 ... 18

2/04—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.5 V to 5.5 V, V_{REF} = 10 V, $I_{OUT}2$ = 0 V. Temperature range for Y version: −40°C to +125°C. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. DC performance measured with OP177, ac performance with AD8038, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution			8	Bits	
Relative Accuracy			±0.25	LSB	
Differential Nonlinearity			±0.5	LSB	Guaranteed monotonic
Gain Error			±10	mV	
Gain Error Temperature Coefficient		±5		ppm FSR/°C	
Output Leakage Current			±10	nA	Data = 0x0000, T_A = 25°C, $I_{OUT}1$
			±20	nA	Data = 0x0000, T = −40°C to +125°C, I_{OUT} 1
REFERENCE INPUT[1]					
Reference Input Range		±10		V	
V_{REF} Input Resistance	8	10	12	kΩ	Input resistance TC = −50 ppm/°C
R_{FB} Resistance	8	10	12	kΩ	Input resistance TC = −50 ppm/°C
Input Capacitance					
Code Zero Scale		3	6	pF	
Code Full Scale		5	8	pF	
DIGITAL INPUT/OUTPUT[1]					
Input High Voltage, V_{IH}	1.7			V	
Input Low Voltage, V_{IL}			0.6	V	
Output High Voltage, V_{OH}	V_{DD} − 1			V	V_{DD} = 4.5 V to 5 V, I_{SOURCE} = 200 µA
	V_{DD} − 0.5			V	V_{DD} = 2.5 V to 3.6 V, I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}			0.4	V	V_{DD} = 4.5 V to 5 V, I_{SINK} = 200 µA
			0.4	V	V_{DD} = 2.5 V to 3.6 V, I_{SINK} = 200 µA
Input Leakage Current, I_{IL}			1	µA	
Input Capacitance		4	10	pF	
DYNAMIC PERFORMANCE[1]					
Reference Multiplying Bandwidth		10		MHz	V_{REF} = ±3.5 V, DAC loaded all 1s
Output Voltage Settling Time					V_{REF} = ±3.5 V, R_{LOAD} = 100 Ω, DAC latch alternately loaded with 0s and 1s
Measured to ±1 mV		90	160	ns	
Measured to ±4 mV		55	110	ns	
Measured to ±16 mV		50	100	ns	
Digital Delay		40	75	ns	Interface delay time
10% to 90% Settling Time		15	30	ns	Rise and fall time, V_{REF} = 10 V, R_{LOAD} = 100 Ω
Digital-to-Analog Glitch Impulse		2		nV-s	1 LSB change around major carry V_{REF} = 0 V
Multiplying Feedthrough Error					DAC latch loaded with all 0s. V_{REF} = ±3.5 V
		70		dB	1 MHz
		48		dB	10 MHz
Output Capacitance					
$I_{OUT}1$		12	17	pF	All 0s loaded
		25	30	pF	All 1s loaded
$I_{OUT}2$		22	25	pF	All 0s loaded
		10	12	pF	All 1s loaded
Digital Feedthrough		0.1		nV-s	Feedthrough to DAC output with $\overline{SYNC}$ high and alternate loading of all 0s and all 1s
Analog THD		81		dB	V_{REF} = 3.5 V p-p; all 1s loaded, f = 1 kHz
Digital THD					Clock = 1 MHz, V_{REF} = 3.5 V, C_{COMP} = 1.8 pF
50 kHz f_{OUT}		70		dB	
20 kHz f_{OUT}		73		dB	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Output Noise Spectral Density		25		nV√Hz	At 1 kHz
SFDR Performance (Wide Band)					Clock = 2 MHz , V_{REF} = 3.5 V
50 kHz f_{OUT}		67		dB	
20 kHz f_{OUT}		68		dB	
SFDR Performance (Narrow Band)					Clock = 2 MHz, V_{REF} = 3.5 V
50 kHz f_{OUT}		73		dB	
20 kHz f_{OUT}		75		dB	
Intermodulation Distortion		79		dB	f_1 = 20 kHz, f_2 = 25 kHz, clock = 2 MHz, V_{REF} = 3.5 V
POWER REQUIREMENTS					
Power Supply Range	2.5		5.5	V	
I_{DD}			0.6	µA	T_A = 25°C, logic inputs = 0 V or V_{DD}
		0.4	5	µA	Logic inputs = 0 V or V_{DD}, T = −40°C to +125°C
Power Supply Sensitivity			0.001	%/%	ΔV_{DD} = ±5%

[1] Guaranteed by design and characterization, not subject to production test.

TIMING CHARACTERISTICS

All input signals are specified with tr = tf = 1 ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. V_{DD} =2.5 V to 5.5 V, V_{REF} = 10 V, I_{OUT}2 = 0 V, temperature range for Y version: −40°C to +125°C ; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	V_{DD} = 2.5 V to 5.5 V	Unit	Test Conditions/Comments
f_{SCLK}	50	MHz max	Maximum clock frequency
t_1	20	ns min	SCLK cycle time
t_2	8	ns min	SCLK high time
t_3	8	ns min	SCLK low time
t_4[2]	13	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	5	ns min	Data setup time
t_6	3	ns min	Data hold time
t_7	5	ns min	$\overline{SYNC}$ rising edge to SCLK falling edge
t_8	30	ns min	Minimum $\overline{SYNC}$ high time
t_9	0	ns min	SCLK falling edge to $\overline{LDAC}$ falling edge
t_{10}	12	ns min	$\overline{LDAC}$ pulse width
t_{11}	10	ns min	SCLK falling edge to $\overline{LDAC}$ rising edge

[1] Guaranteed by design and characterization, not subject to production test.
[2] Falling or rising edge as determined by control bits of serial word.

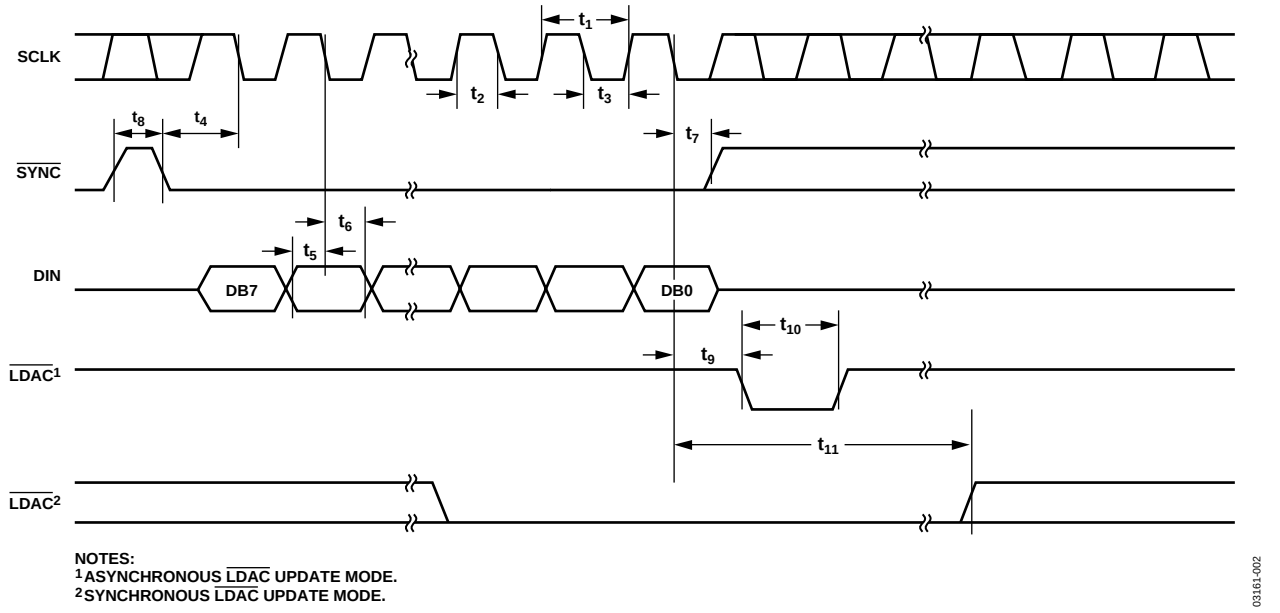


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{REF}, R_{FB} to GND	−12 V to +12 V
$I_{OUT}1$, $I_{OUT}2$ to GND	−0.3 V to V_{DD} + 0.3 V
Logic Input and Output[1]	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Extended Industrial (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
10-lead MSOP θ_{JA} Thermal Impedance	206°C/W
Lead Temperature, Soldering (10 secs)	300°C
IR Reflow, Peak Temperature (<20 secs)	235°C

[1] Overvoltages at SCLK, $\overline{SYNC}$, DIN, and $\overline{LDAC}$ are clamped by internal diodes. Current must be limited to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

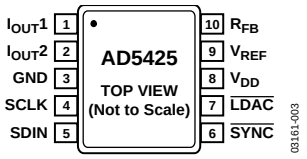


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	$I_{OUT}1$	DAC Current Output.
2	$I_{OUT}2$	DAC Analog Ground. This pin must normally be tied to the analog ground of the system.
3	GND	Digital Ground Pin.
4	SCLK	Serial Clock Input. Data is clocked into the input shift register on each falling edge of the serial clock input. This device can accommodate clock rates of up to 50 MHz.
5	SDIN	Serial Data Input. Data is clocked into the 8-bit input register on each falling edge of the serial clock input.
6	$\overline{SYNC}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it powers on the SCLK and DIN buffers and the input shift register is enabled. Data is transferred on each falling edge of the following 8 clocks.
7	$\overline{LDAC}$	Load DAC Input. Updates the DAC output. The DAC is updated when this signal goes low or alternatively; if this line is held permanently low, an automatic update mode is selected whereby the DAC is updated after 8 SCLK falling edges with $\overline{SYNC}$ low.
8	V_{DD}	Positive Power Supply Input. This device can be operated from a supply of 2.5 V to 5.5 V.
9	V_{REF}	DAC Reference Voltage Input Terminal.
10	R_{FB}	DAC Feedback Resistor Pin. Establishes voltage output for the DAC by connecting to external amplifier output.

TYPICAL PERFORMANCE CHARACTERISTICS

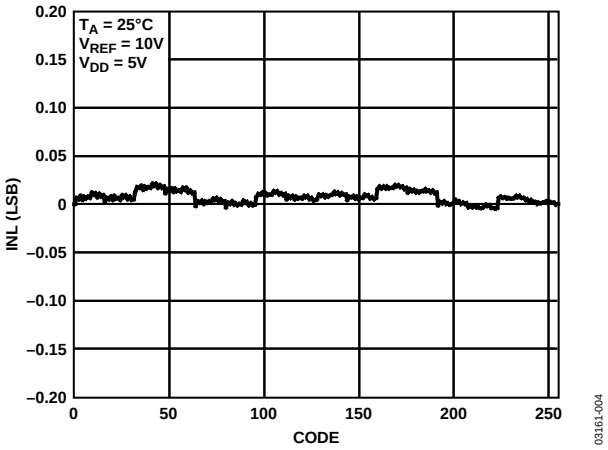


Figure 4. Integral Nonlinearity (INL) vs. Code (8-Bit DAC)

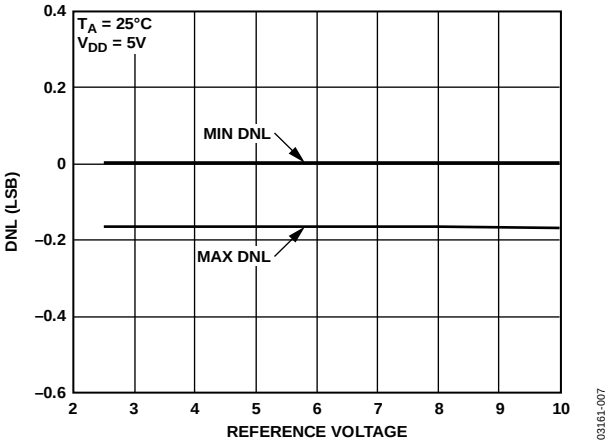


Figure 7. DNL vs. Reference Voltage

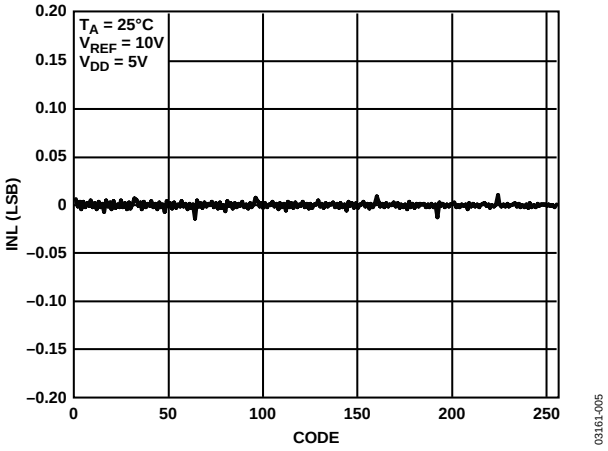


Figure 5. Differential Nonlinearity (DNL) vs. Code (8-Bit DAC)

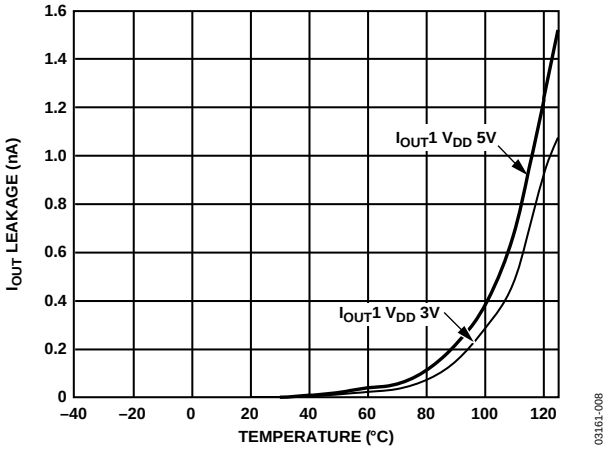


Figure 8. $I_{OUT}1$ Leakage Current vs. Temperature

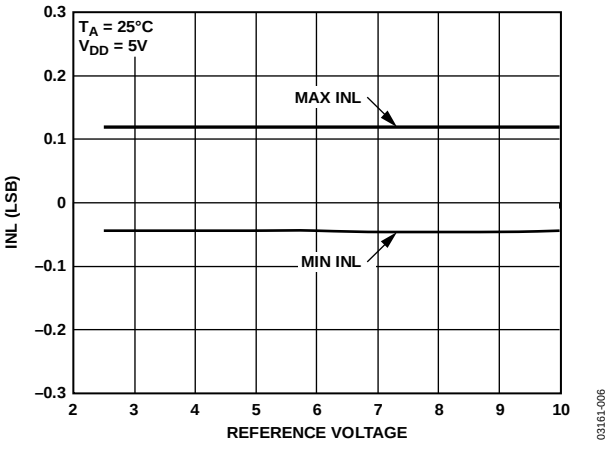


Figure 6. INL vs. Reference Voltage

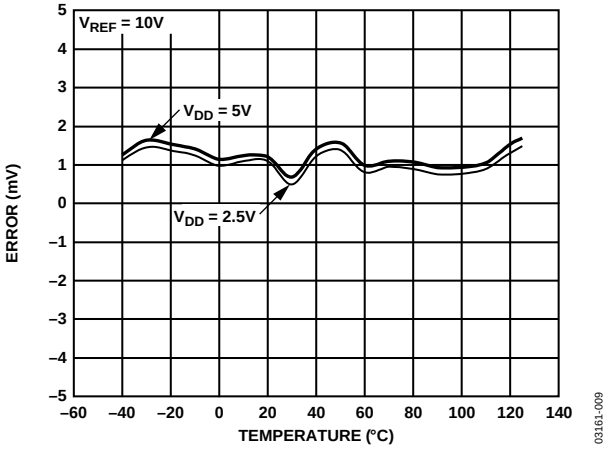


Figure 9. Gain Error vs. Temperature

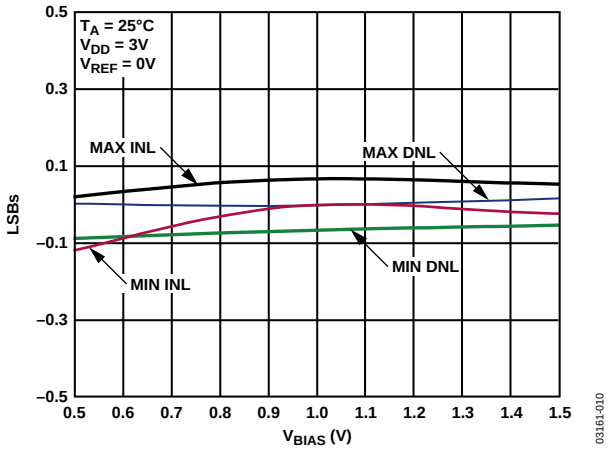


Figure 10. Linearity vs. V_{BIAS} Voltage Applied to $I_{OUT}2$

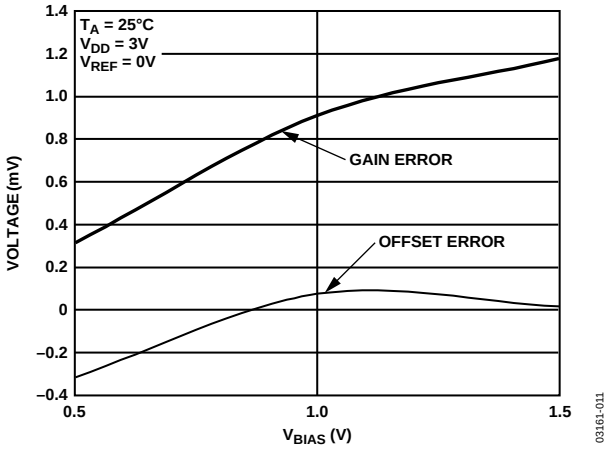


Figure 11. Gain and Offset Errors vs. V_{BIAS} Voltage Applied to $I_{OUT}2$

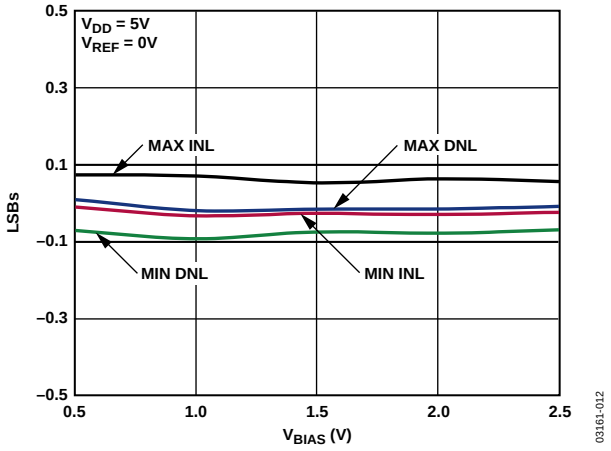


Figure 12. Linearity vs. V_{BIAS} Voltage Applied to $I_{OUT}2$

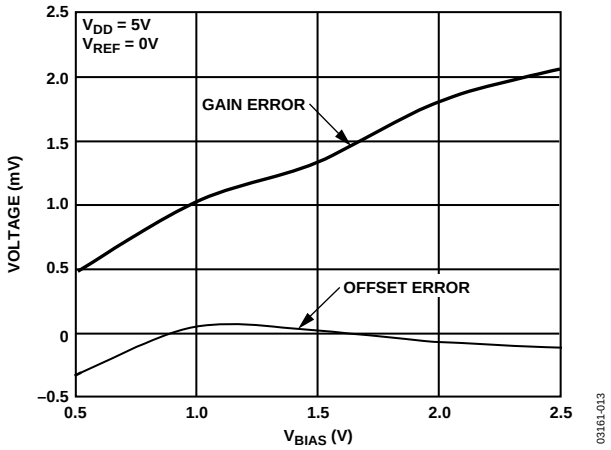


Figure 13. Gain and Offset Errors vs. Voltage Applied to $I_{OUT}2$

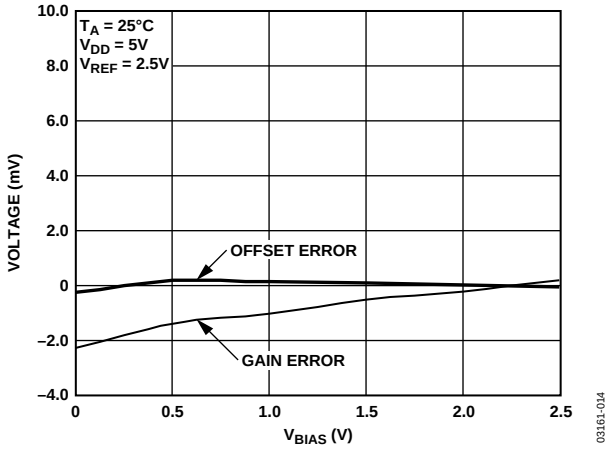


Figure 14. Gain and Offset Errors vs. V_{BIAS} Voltage Applied to $I_{OUT}2$

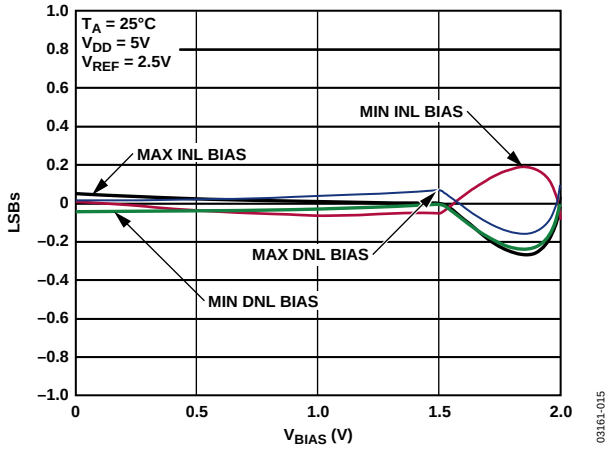


Figure 15. Linearity vs. V_{BIAS} Voltage Applied to $I_{OUT}2$

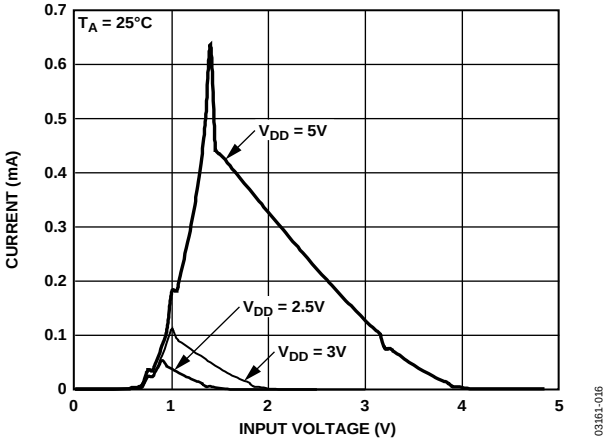


Figure 16. Supply Current vs. Input Voltage

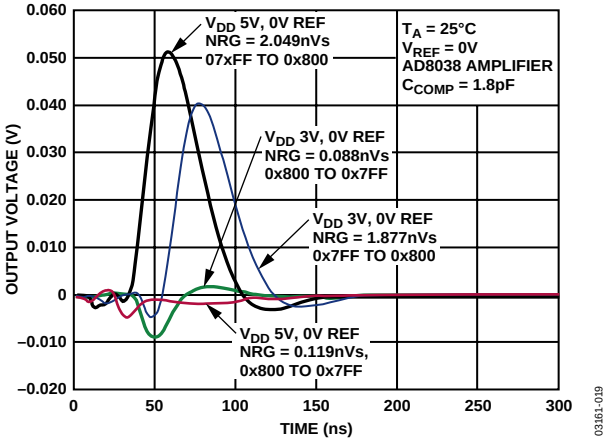


Figure 19. Midscale Transition, V_{REF} = 3.5 V

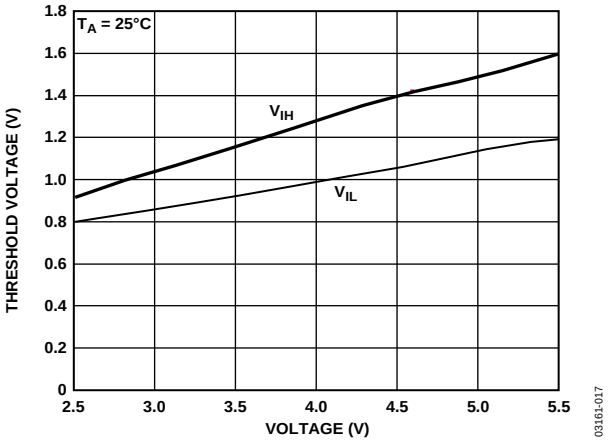


Figure 17. Threshold Voltages vs. Supply Voltage

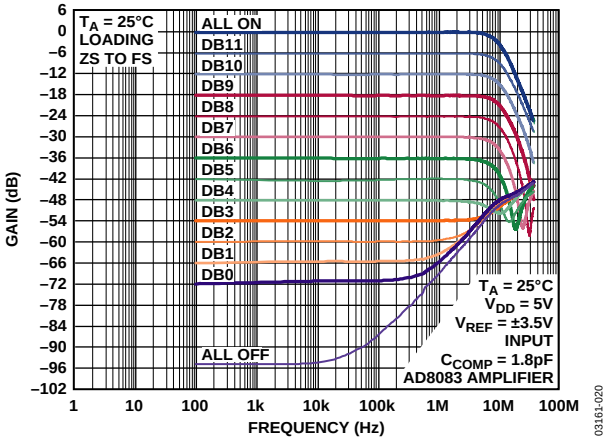


Figure 20. Reference Multiplying Bandwidth vs. Frequency and Code

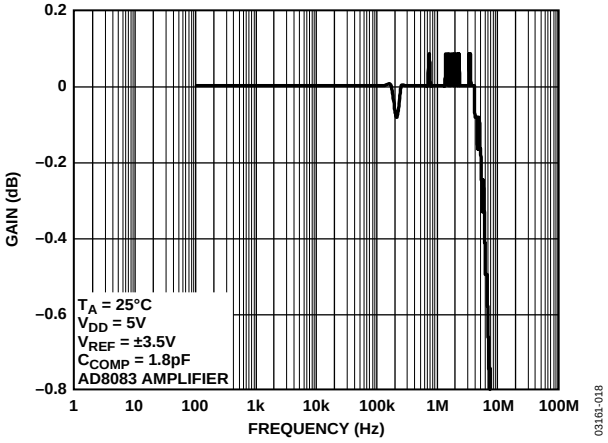


Figure 18. Reference Multiplying Bandwidth—All 1s Loaded

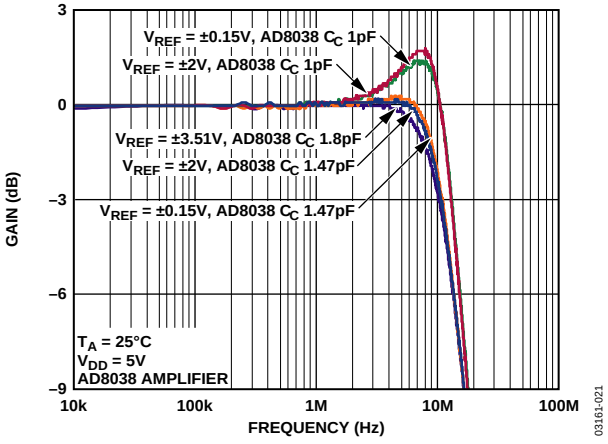


Figure 21. Reference Multiplying Bandwidth vs. Frequency and Compensation Capacitor

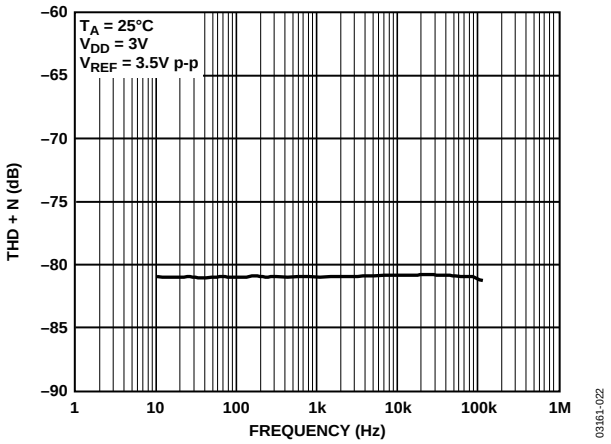


Figure 22. THD and Noise vs. Frequency

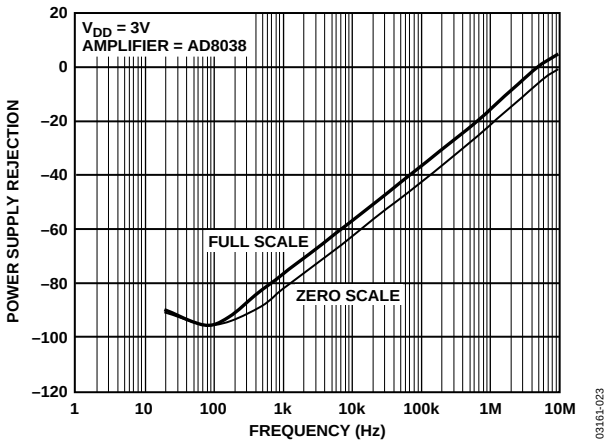


Figure 23. Power Supply Rejection vs. Frequency

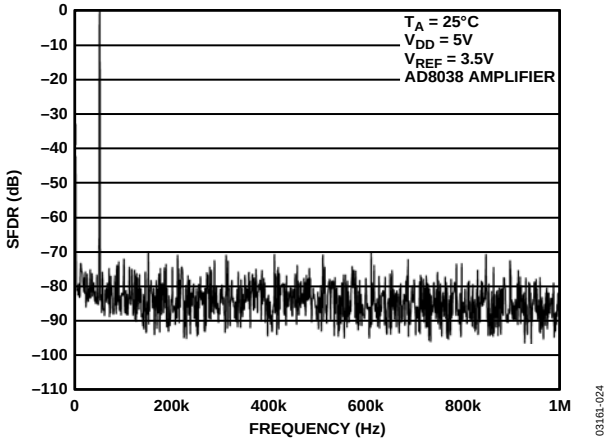


Figure 24. Wideband SFDR, Clock = 2 MHz, f_{OUT} = 50 kHz

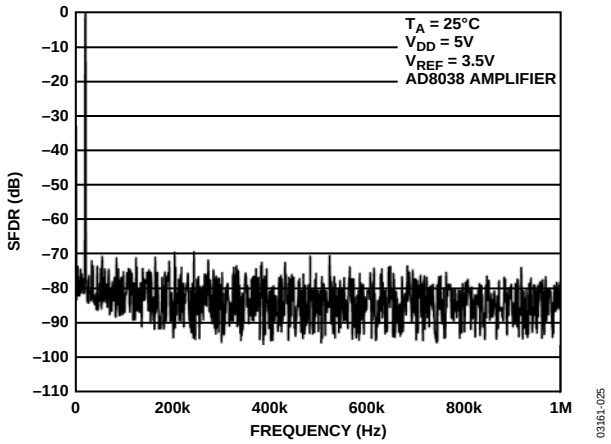


Figure 25. Wideband SFDR, Clock = 2 MHz, f_{OUT} = 20 kHz

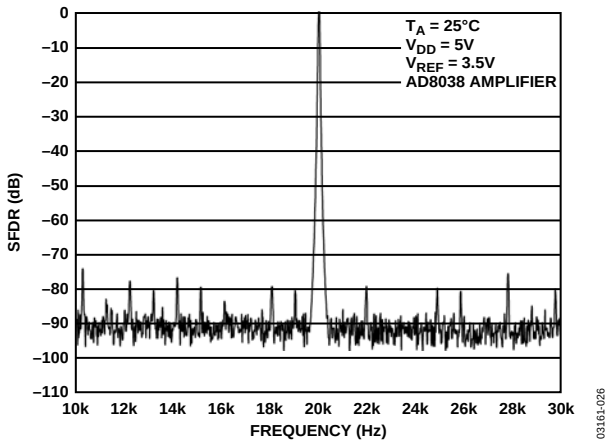


Figure 26. Narrow-Band SFDR, Clock = 2 MHz, f_{OUT} = 20 kHz

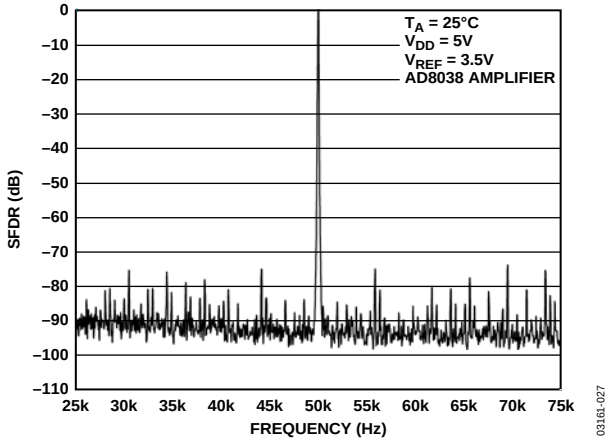


Figure 27. Narrow-Band SFDR, Clock = 2 MHz, f_{OUT} = 50 kHz

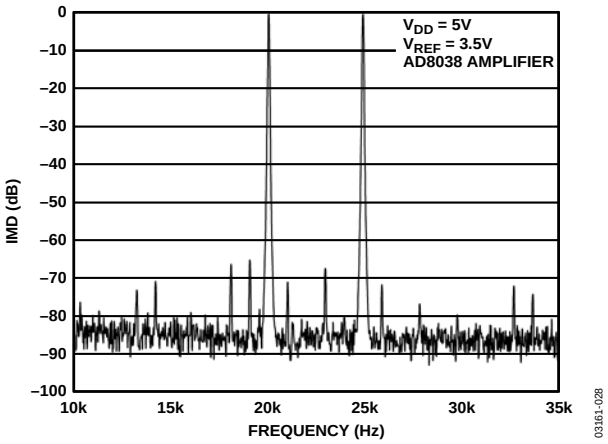


Figure 28. Narrow-Band IMD (±50%) Clock = 2 MHz, $f_{OUT}1$ = 20 kHz, $f_{OUT}2$ = 25 kHz

TERMINOLOGY

Relative Accuracy
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is normally expressed in LSBs or as a percentage of full-scale reading.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of −1 LSB maximum over the operating temperature range ensures monotonicity.

Gain Error
Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For these DACs, ideal maximum output is V_{REF} − 1 LSB. Gain error of the DACs is adjustable to 0 with external resistance.

Output Leakage Current
Output leakage current is current that flows in the DAC ladder switches when the switches are turned off. The $I_{OUT}1$ terminal can be measured by loading all 0s to the DAC and measuring the $I_{OUT}1$ current. Minimum current flows in the $I_{OUT}2$ line when the DAC is loaded with all 1s.

Output Capacitance
Capacitance from $I_{OUT}1$ or $I_{OUT}2$ to AGND.

Output Current Settling Time
This is the amount of time it takes for the output to settle to a specified level for a full-scale input change. For these devices, it is specified with a 100 Ω resistor to ground.

The settling time specification includes the digital delay from $\overline{SYNC}$ rising edge to the full-scale output charge.

Digital-to-Analog Glitch Impulse
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-s or nV-s depending upon whether the glitch is measured as a current or voltage signal.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the device digital inputs can be capacitively coupled to display as noise on the I_{OUT} pins and subsequently into the following circuitry. This noise is digital feedthrough.

Multiplying Feedthrough Error
This is the error due to capacitive feedthrough from the DAC reference input to the DAC $I_{OUT}1$ terminal, when all 0s are loaded to the DAC.

Total Harmonic Distortion (THD)
The DAC is driven by an ac reference. The ratio of the rms sum of the harmonics of the DAC output to the fundamental value is the THD. Usually only the lower order harmonics are included, such as second to fifth.

$$THD = 20\log\frac{\sqrt{\left(V_2^2 + V_3^2 + V_4^2 + V_5^2\right)}}{V_1}$$

Digital Intermodulation Distortion (IMD)
Second-order IMD measurements are the relative magnitude of the fa and fb tones generated digitally by the DAC and the second-order products at 2fa − fb and 2fb − fa.

Spurious-Free Dynamic Range (SFDR)
SFDR is the usable dynamic range of a DAC before spurious noise interferes or distorts the fundamental signal. It is the measure of the difference in amplitude between the fundamental and the largest harmonically or nonharmonically related spur from dc to full Nyquist bandwidth (half the DAC sampling rate, or $f_S/2$). Narrow-band SFDR is a measure of SFDR over an arbitrary window size, in this case 50% of the fundamental. Digital SFDR is a measure of the usable dynamic range of the DAC when the signal is a digitally generated sine wave.

THEORY OF OPERATION

The AD5425 is an 8-bit current output DAC consisting of a standard inverting R-2R ladder configuration. A simplified diagram is shown in Figure 29. The feedback resistor, R_{FB}, has a value of R. The value of R is typically 10 kΩ (minimum 8 kΩ and maximum 12 kΩ). If $I_{OUT}1$ and $I_{OUT}2$ are kept at the same potential, a constant current flows in each ladder leg, regardless of digital input code. Therefore, the input resistance presented at V_{REF} is always constant and nominally of value R. The DAC output, I_{OUT}, is code dependent, producing various resistances and capacitances. When choosing the external amplifier, take into account the variation in impedance generated by the DAC on the amplifiers inverting input node.

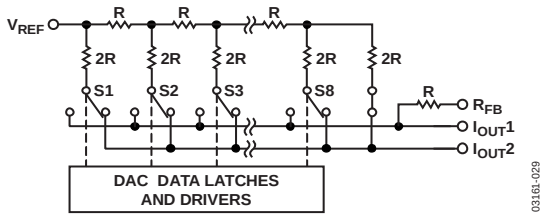


Figure 29. Simplified Ladder

Access is provided to the V_{REF}, R_{FB}, $I_{OUT}1$, and $I_{OUT}2$ terminals of the DAC, making the device extremely versatile and allowing it to be configured in several different operating modes, for example, to provide a unipolar output, bipolar output, or in single-supply modes of operation in unipolar mode or 4-quadrant multiplication in bipolar mode. Note that a matching switch is used in series with the internal R_{FB} feedback resistor. If users attempt to measure R_{FB}, power must be applied to V_{DD} to achieve continuity.

CIRCUIT OPERATION

Unipolar Mode

Using a single operational amplifier, this device can easily be configured to provide 2-quadrant multiplying operation or a unipolar output voltage swing, as shown in Figure 30.

When an output amplifier is connected in unipolar mode, the output voltage is given by

$$V_{OUT} = -V_{REF} \times \frac{D}{2^n}$$

where D is the fractional representation of the digital word loaded to the DAC, in this case 0 to 255, and n is the number of bits.

Note that the output voltage polarity is opposite to the V_{REF} polarity for dc reference voltages.

This DAC is designed to operate with either negative or positive reference voltages. The VDD power pin is used by only the internal digital logic to drive the on and off states of the DAC switches.

This DAC is also designed to accommodate ac reference input signals in the range of −10 V to +10 V.

With a fixed 10 V reference, the circuit shown in Figure 30 gives a unipolar 0 V to −10 V output voltage swing. When V_{IN} is an ac signal, the circuit performs 2-quadrant multiplication.

Table 5 shows the relationship between digital code and the expected output voltage for unipolar operation.

Table 5. Unipolar Code Table

Digital Input	Analog Output (V)
1111 1111	$-V_{REF}$ (255/256)
1000 0000	$-V_{REF}$ (128/256) = $-V_{REF}/2$
0000 0001	$-V_{REF}$ (1/256)
0000 0000	$-V_{REF}$ (0/256) = 0

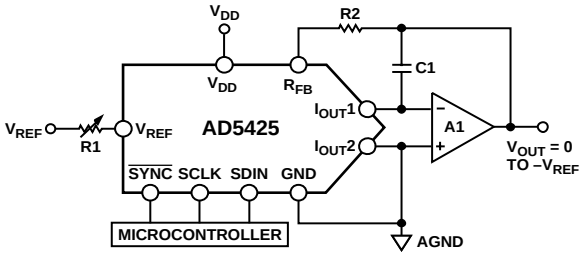


Figure 30. Unipolar Operation

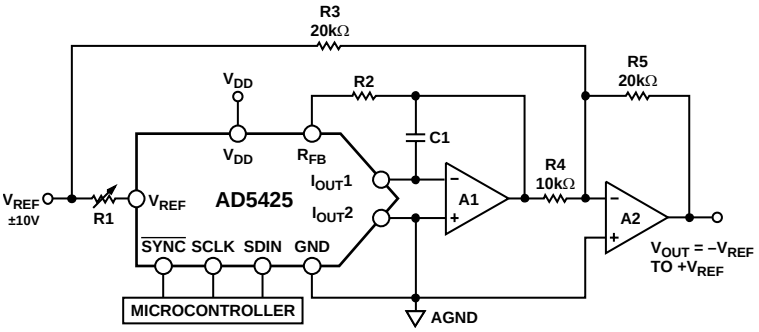


Figure 31. Bipolar Operation (4-Quadrant Multiplication)

Bipolar Operation

In some applications, it may be necessary to generate full 4-quadrant multiplying operation or a bipolar output swing. This can be easily accomplished by using another external amplifier and some external resistors, as shown in Figure 31. In this circuit, the second amplifier, A2, provides a gain of 2. Biasing the external amplifier with an offset from the reference voltage, results in full 4-quadrant multiplying operation. The transfer function of this circuit shows that both negative and positive output voltages are created as the input data, D, is incremented from code zero ($V_{OUT} = -V_{REF}$), to midscale ($V_{OUT} = 0$ V), to full scale ($V_{OUT} = +V_{REF}$).

$$V_{OUT} = \left(V_{REF} \times \quad D/2^{n-1}\right) - V_{REF}$$

Where D is the fractional representation of the digital word loaded to the DAC and n is the resolution of the DAC.

When V_{IN} is an ac signal, the circuit performs 4-quadrant multiplication.

Table 6 shows the relationship between digital code and the expected output voltage for bipolar operation.

Table 6. Bipolar Code Table

Digital Input	Analog Output (V)
1111 1111	$+V_{REF}$ (127/128)
1000 0000	0
0000 0001	$-V_{REF}$ (127/128)
0000 0000	$-V_{REF}$ (128/128)

Stability

In the I to V configuration, the I_{OUT} of the DAC and the inverting node of the operational amplifier must be connected as closely as possible and proper printed circuit board (PCB) layout techniques must be employed. Since every code change corresponds to a step function, gain peaking can occur if the operational amplifier has limited gain bandwidth product (GBP) and there is excessive parasitic capacitance at the inverting node. This parasitic capacitance introduces a pole into the open-loop response, which can cause ringing or instability in closed-loop applications.

An optional compensation capacitor, C1, can be added in parallel with R_{FB} for stability, as shown in Figure 30 and Figure 31. Too small a value of C1 can produce ringing at the output, while too large a value can adversely affect the settling time. C1 must be found empirically, but 1 pF to 2 pF is generally adequate for compensation.

SINGLE-SUPPLY APPLICATIONS

Current Mode Operation

In the current mode circuit of Figure 32, $I_{OUT}2$ and hence $I_{OUT}1$ is biased positive by an amount applied to V_{BIAS}. In this configuration, the output voltage is given by

$$V_{OUT} = [D \times (R_{FB}/R_{DAC}) \times (V_{BIAS} - V_{IN})] + V_{BIAS}$$

As D varies from 0 to 255, the output voltage varies from

$$V_{OUT} = V_{BIAS} \text{ to } V_{OUT} = 2V_{BIAS} - V_{IN}$$

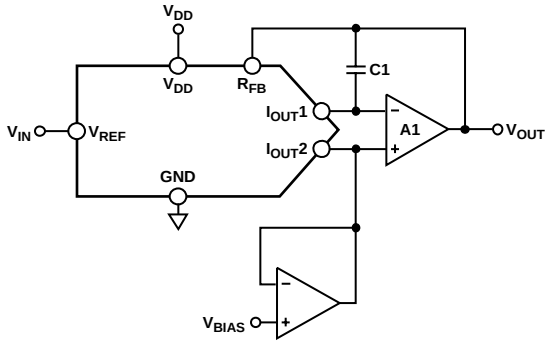


Figure 32. Single-Supply Current Mode Operation

V_{BIAS} must be a low impedance source capable of sinking and sourcing all possible variations in current at the $I_{OUT}2$ terminal without any problems.

It is important to note that V_{IN} is limited to low voltages because the switches in the DAC ladder no longer have the same source-drain drive voltage. As a result, the on resistance differs and this degrades the linearity of the DAC.

Voltage Switching Mode of Operation

Figure 33 shows this DAC operating in the voltage switching mode. The reference voltage V_{IN} is applied to the $I_{OUT}1$ pin, $I_{OUT}2$ is connected to AGND, and the output voltage is available at the V_{REF} terminal. In this configuration, a positive reference voltage results in a positive output voltage, making single-supply operation possible. The output from the DAC is voltage at a constant impedance (the DAC ladder resistance), thus an operational amplifier is necessary to buffer the output voltage. The reference input no longer sees constant input impedance, but one that varies with code. So, the voltage input must be driven from a low impedance source.

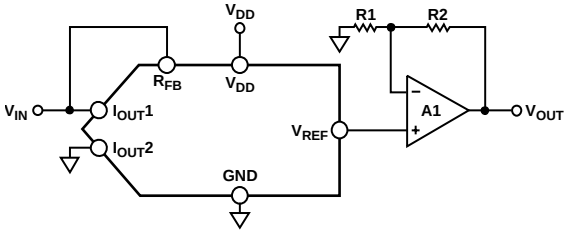


Figure 33. Single-Supply Voltage Switching Mode Operation

It is important to note that V_{IN} is limited to low voltage because the switches in the DAC ladder no longer have the same source drain drive voltage. As a result, the on resistance differs, which degrades the linearity of the DAC.

V_{IN} must also not go negative by more than 0.3 V, otherwise an internal diode turns on, exceeding the maximum ratings of the device. In this type of application, the full range of the DAC multiplying capability is lost.

ADDING GAIN

In applications where the output voltage is required to be greater than V_{IN}, gain can be added with an additional external amplifier or it can be achieved in a single stage. It is important to take into consideration the effect of temperature coefficients of the thin film resistors of the DAC. Simply placing a resistor in series with the R_{FB} resistor causes mismatches in the temperature coefficients and results in larger gain temperature coefficient errors. Instead, the circuit of Figure 34 is a recommended method of increasing the gain of the circuit. R1, R2, and R3 must all have similar temperature coefficients but do not need to match the temperature coefficients of the DAC. This approach is recommended in circuits where gains of greater than 1 are required. Note that $R_{FB} \gg R2//R3$ and a gain error percentage of $100 \times (R2//R3)/R_{FB}$ must be taken into consideration.

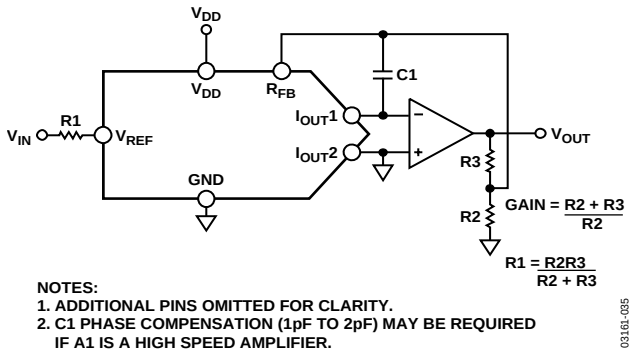


Figure 34. Increasing the Gain of Current Output DAC

DACs USED AS A DIVIDER OR PROGRAMMABLE GAIN ELEMENT

Current steering DACs are very flexible and lend themselves to many different applications. If this type of DAC is connected as the feedback element of an operational amplifier and R_{FB} is used as the input resistor as shown in Figure 35, then the output voltage is inversely proportional to the digital input fraction, D.

For $D = 1 - 2^{-n}$, the output voltage is

$$V_{OUT} = -V_{IN}/D = -V_{IN}/(1 - 2^{-n})$$

As D is reduced, the output voltage increases. For small values of D, it is important to ensure that the amplifier does not saturate and that the required accuracy is met. For example, an 8-bit DAC driven with the Binary Code 0x10 (00010000), that is, 16 decimal, in the circuit of Figure 35, causes the output voltage to be $16 \times V_{IN}$.

However, if the DAC has a linearity specification of ±0.5 LSB, then D can in fact have a weight anywhere in the range 15.5/256 to 16.5/256. Therefore, the possible output voltage is in the range of 15.5 V_{IN} to 16.5 V_{IN}—an error of 3%, even though the DAC itself has a maximum error of 0.2%.

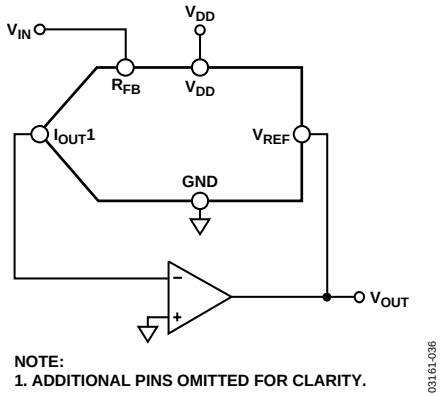


Figure 35. Current Steering DAC Used as a Divider or Programmable Gain Element

DAC leakage current is also a potential error source in divider circuits. The leakage current must be counterbalanced by an opposite current supplied from the operational amplifier through the DAC. Since only a fraction, D, of the current into the V_{REF} terminal is routed to the $I_{OUT}1$ terminal, the output voltage has to change as follows:

$$\textit{Output Error Voltage Due to DAC Leakage} = (\textit{Leakage} \times R)/D$$

where R is the DAC resistance at the V_{REF} terminal. For a DAC leakage current of 10 nA, R = 10 kΩ. With a gain (that is, 1/D) of 16, the error voltage is 1.6 mV.

REFERENCE SELECTION

When selecting a reference for use with the AD5425 current output DAC, pay attention to the reference output voltage temperature coefficient specification. This parameter not only affects the full-scale error, but can also affect the linearity (INL and DNL) performance. The reference temperature coefficient must be consistent with the system accuracy specifications. For example, an 8-bit system required to hold the overall specification to within 1 LSB over the temperature range 0°C to 50°C dictates that the maximum system drift with temperature must be less than 78 ppm/°C. A 12-bit system with the same temperature range to overall specification within 2 LSB requires a maximum drift of 10 ppm/°C. By choosing a precision reference with a low output temperature coefficient, this error source can be minimized. Table 7 suggests some of the references available from Analog Devices, Inc., that are suitable for use with this range of current output DACs.

AMPLIFIER SELECTION

The primary requirement for the current steering mode is an amplifier with low input bias currents and low input offset voltage. The input offset voltage of an operational amplifier is multiplied by the variable gain (due to the code dependent output resistance of the DAC) of the circuit.

A change in this noise gain between two adjacent digital fractions produces a step change in the output voltage due to the amplifier input offset voltage. This output voltage change is superimposed on the desired change in output between the two codes and gives rise to a differential linearity error, which if large enough, could cause the DAC to be nonmonotonic.

The input bias current of an operational amplifier also generates an offset at the voltage output as a result of the bias current flowing in the feedback resistor, R_{FB}. Most operational amplifiers have input bias currents low enough to prevent any significant errors.

Common-mode rejection of the operational amplifier is important in voltage switching circuits, since it produces a code dependent error at the voltage output of the circuit. Most operational amplifiers have adequate common-mode rejection for use at an 8-bit resolution.

Provided the DAC switches are driven from true wideband low impedance sources (V_{IN} and AGND), they settle quickly. Consequently, the slew rate and settling time of a voltage switching DAC circuit is determined largely by the output operational amplifier. To obtain minimum settling time in this configuration, it is important to minimize capacitance at the V_{REF} node (voltage output node in this application) of the DAC. This is done by using low inputs capacitance buffer amplifiers and careful board design.

Most single-supply circuits include ground as part of the analog signal range, which requires an amplifier that can handle rail-to-rail signals. There is a large range of single-supply amplifiers available from Analog Devices.

Table 7. Suitable Analog Devices Precision References

Part No.	Output Voltage (V)	Initial Tolerance (%)	Temp Drift (ppm/°C)	I_{SS} (mA)	Output Noise (μV p-p)	Package
ADR01	10	0.05	3	1	20	SOIC-8
ADR01	10	0.05	9	1	20	TSOT-23, SC70
ADR02	5	0.06	3	1	10	SOIC-8
ADR02	5	0.06	9	1	10	TSOT-23, SC70
ADR03	2.5	0.10	3	1	6	SOIC-8
ADR03	2.5	0.10	9	1	6	TSOT-23, SC70
ADR06	3	0.10	3	1	10	SOIC-8
ADR06	3	0.10	9	1	10	TSOT-23, SC70
ADR431	2.5	0.04	3	0.8	3.5	SOIC-8
ADR435	5	0.04	3	0.8	8	SOIC-8
ADR391	2.5	0.16	9	0.12	5	TSOT-23
ADR395	5	0.10	9	0.12	8	TSOT-23

Table 8. Suitable Precision Analog Devices Operational Amplifiers

Part No.	Supply Voltage (V)	V_{OS} (Max) (µV)	I_B (Max) (nA)	0.1 Hz to 10 Hz Noise (µV p-p)	Supply Current (µA)	Package
OP97	±2 to ±20	25	0.1	0.5	600	SOIC-8
OP1177	±2.5 to ±15	60	2	0.4	500	MSOP, SOIC-8
AD8551	2.7 to 5	5	0.05	1	975	MSOP, SOIC-8
AD8603	1.8 to 6	50	0.001	2.3	50	TSOT
AD8628	2.7 to 6	5	0.1	0.5	850	TSOT, SOIC-8

Table 9. Suitable High Speed Analog Devices Operational Amplifiers

Part No.	Supply Voltage (V)	BW at ACL (MHz)	Slew Rate (V/µs)	V_{OS} (Max) (µV)	I_B (Max) (nA)	Package
AD8065	5 to 24	145	180	1500	6000	SOIC-8, SOT-23,MSOP
AD8021	±2.5 to ±12	490	120	1000	10500	SOIC-8, MSOP
AD8038	3 to 12	350	425	3000	750	SOIC-8, SC70-5
AD9631	±3 to ±6	320	1300	10000	7000	SOIC-8

SERIAL INTERFACE

The AD5425 has a simple 3-wire interface that is compatible with SPI, QSPI, MICROWIRE, and DSP interface standards. Data is written to the device in 8-bit words. This 8-bit word consists of 8 data bits, as shown in Figure 36.

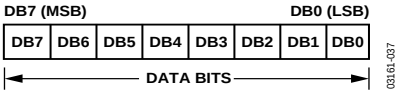


Figure 36. 8-Bit Input Shift Register Contents

$\overline{SYNC}$ is an edge triggered input that acts as a frame synchronization signal and chip enable. Data can be transferred into the device only while $\overline{SYNC}$ is low. To start the serial data transfer, $\overline{SYNC}$ must be taken low, observing the minimum $\overline{SYNC}$ falling to SCLK falling edge setup time, t_4.

After loading eight data bits to the shift register, the $\overline{SYNC}$ line is brought high. The contents of the DAC register and the output are updated by bringing $\overline{LDAC}$ low any time after the 8-bit data transfer is complete, as seen in the timing diagram of Figure 2. $\overline{LDAC}$ can be tied permanently low if required. For another serial transfer to take place, the interface must be enabled by another falling edge of $\overline{SYNC}$.

Low Power Serial Interface

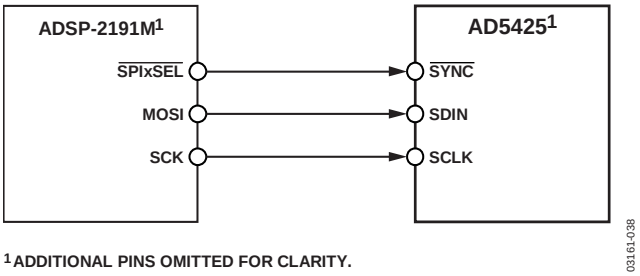
To minimize the power consumption of the device, the interface fully powers up only when the device is being written to, that is, on the falling edge of $\overline{SYNC}$. The SCLK and SDIN input buffers are powered down on the rising edge of $\overline{SYNC}$.

MICROPROCESSOR INTERFACING

Microprocessor interfacing to this DAC is via a serial bus that uses standard protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire interface consisting of a clock signal, a data signal, and a synchronization signal. An $\overline{LDAC}$ pin is also included. The AD5425 requires an 8-bit word with the default being data valid on the falling edge of SCLK, but this is changeable via the control bits in the data-word.

ADSP-21xx to AD5425 Interface

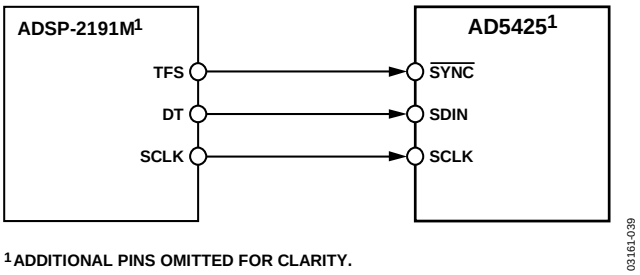
The ADSP-21xx family of DSPs is easily interfaced to this family of DACs without extra glue logic. Figure 37 shows an example of an SPI interface between the DAC and the ADSP-2191M. SCK of the DSP drives the serial clock line, SCLK. SYNC is driven from one of the port lines, in this case $\overline{SPIxSEL}$.



1 ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 37. ADSP-2191M SPI to AD5425 Interface

A serial interface between the DAC and DSP SPORT is shown in Figure 38. In this interface example, SPORT0 is transfers data to the DAC shift register. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. In a write sequence, data is clocked out on each rising edge of the DSP serial clock and clocked into the DAC input shift register on the falling edge of the SCLK. The update of the DAC output takes place on the rising edge of the $\overline{SYNC}$ signal.



1 ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 38. ADSP-2191M SPORT to AD5425 Interface

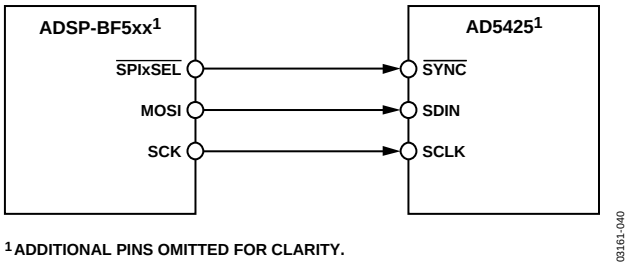
Communication between two devices at a given clock speed is possible when the following specifications from one device to the other are compatible: frame sync delay and frame sync setup and hold, data delay and data setup and hold, and SCLK width. The DAC interface expects a t_4 (SYNC falling edge to SCLK falling edge setup time) of 13 ns minimum. Consult the ADSP-21xx user manual for information on clock and frame sync frequencies for the SPORT register.

Table 10. SPORT Control Register Setup

Name	Setting	Description
TFSW	1	Alternate framing
INVTFS	1	Active low frame signal
DTYPE	00	Right justify data
ISCLK	1	Internal serial clock
TFSR	1	Frame every word
ITFS	1	Internal framing signal
SLEN	0111	8-bit data-word

ADSP-BF504 to ADSP-BF592 Device Family to AD5425 Interface

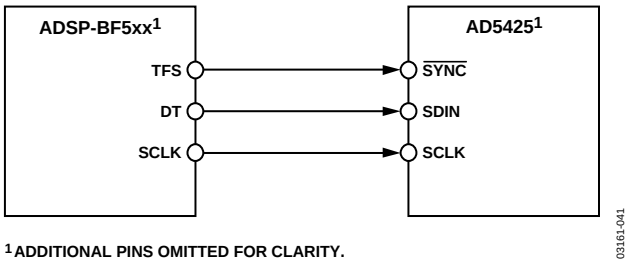
The ADSP-BF504 to ADSP-BF592 device family of processors has an SPI-compatible port that enables the processor to communicate with SPI-compatible devices. A serial interface between the ADSP-BF504 to ADSP-BF592 device family and the AD5425 DAC is shown in Figure 39. In this configuration, data is transferred through the MOSI (master output/slave input) pin. $\overline{\text{SYNC}}$ is driven by the SPI chip select pin, which is a reconfigured programmable flag pin.



[1] ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 39. ADSP-BF504 to ADSP-BF592 Device Family to AD5425 Interface (ADSP-BFxx Denotes the ADSP-BF504 to ADSP-BF592)

The ADSP-BF504 to ADSP-BF592 processors incorporate channel synchronous serial ports (SPORT). A serial interface between the DAC and the DSP SPORT is shown in Figure 40. When the SPORT is enabled, initiate transmission by writing a word to the Tx register. The data is clocked out on each rising edge of the DSP serial clock and clocked into the DAC input shift register on the falling edge of the SCLK. The DAC output is updated by using the transmit frame synchronization (TFS) line to provide a $\overline{\text{SYNC}}$ signal.



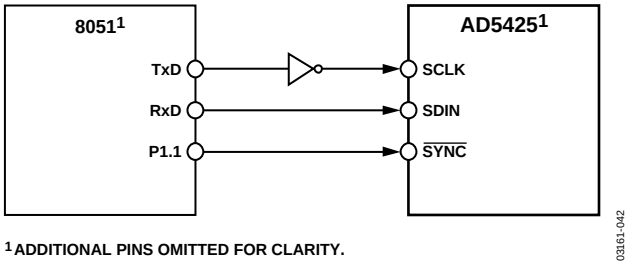
[1] ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 40. ADSP-BF504 to ADSP-BF592 Device Family to AD5425 Interface (ADSP-BFxx Denotes the ADSP-BF504 to ADSP-BF592)

80C51/80L51 to AD5425 Interface

A serial interface between the DAC and the 8051 is shown in Figure 41. TxD of the 8051 drives SCLK of the DAC serial interface, while RxD drives the serial data line, D_{IN}. P3.3 is a bit-programmable pin on the serial port that drives $\overline{\text{SYNC}}$. When data is transmitted to the switch, P3.3 is taken low. The 80C51/80L51 transmits data in 8-bit bytes, which fits the AD5425 since it only requires an 8-bit word.

Data on RxD is clocked out of the microcontroller on the rising edge of TxD and is valid on the falling edge. As a result, no glue logic is required between the DAC and microcontroller interface. P3.3 is taken high at the completion of this cycle. The 8051 provides the LSB of the SBUF register as the first bit in the data stream. The DAC input register requires that the MSB is the first bit received. The transmit routine must take this into account.

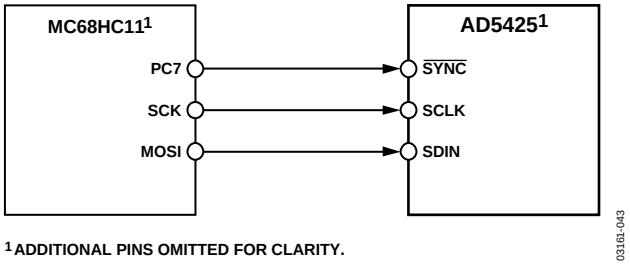


[1] ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 41. 80C51/80L51 to AD5425 Interface

MC68HC11 Interface to AD5425 Interface

Figure 42 shows an example of a serial interface between the DAC and the MC68HC11 microcontroller. The serial peripheral interface (SPI) on the MC68HC11 is configured for master mode (MSTR = 1), clock polarity bit (CPOL) = 0, and the clock phase bit (CPHA) = 1. The SPI is configured by writing to the SPI control register (SPCR). SCK of the MC68HC11 drives the SCLK of the DAC interface, the MOSI output drives the serial data line, D_{IN}, of the AD5425. The $\overline{\text{SYNC}}$ signal is derived from a port line, PC7. When data is being transmitted to the AD5425, the $\overline{\text{SYNC}}$ line is taken low (PC7). Data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the MC68HC11 is transmitted in 8-bit bytes with only 8 falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. PC7 is taken high at the end of the write.

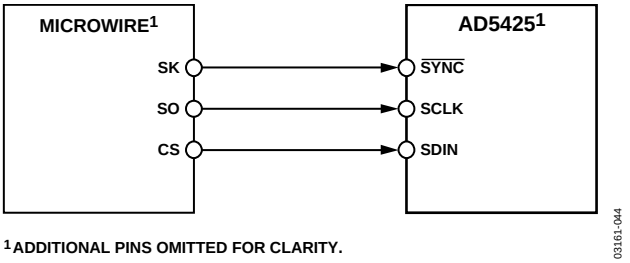


[1] ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 42. 68HC11/68L11 to AD5425 Interface

MICROWIRE to AD5425 Interface

Figure 43 shows an interface between the DAC and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock, SK, and is clocked into the DAC input shift register on the rising edge of SK, which corresponds to the falling edge of the DAC SCLK.

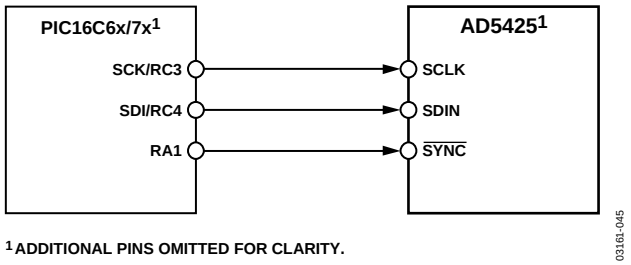


1 ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 43. MICROWIRE to AD5425 Interface

PIC16C6x/PIC16C7x to AD5425

The PIC16C6x/PIC16C7x (Microchip) synchronous serial port (SSP) is configured as an SPI master with the clock polarity bit (CKP) = 0. This is done by writing to the synchronous serial port control register (SSPCON). In this example, RA1 input/output port provides a $\overline{\text{SYNC}}$ signal and enable the DAC serial port. This microcontroller transfers eight bits of data during each serial transfer operation. Figure 44 shows the connection diagram.



1 ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 44. PIC16C6x/PIC16C7x to AD5425 Interface

PCB LAYOUT AND POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The PDB on which the AD5425 is mounted must be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the DAC is in a system where multiple devices require an AGND to DGND connection, the connection must be made at one point only. The star ground point must be established as close as possible to the device.

These DACs must have an ample supply bypassing of 10 μF in parallel with 0.1 μF on the supply and located as close to the package as possible—ideally up against the device. The 0.1 μF capacitor must have low effective series resistance (ESR) and effective series inductance (ESI), such as found in the common ceramic types that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching. Low ESR, 1 μF to 10 μF tantalum or electrolytic capacitors must also be applied at the supplies to minimize transient disturbance and to filter out low frequency ripple.

Fast switching signals such as clocks must be shielded with digital ground to avoid radiating noise to other parts of the board and must never be run near the reference inputs.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board must run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane while signal traces are placed on the solder side.

It is good practice to employ compact, minimum lead length PCB layout design. Leads to the input must be as short as possible to minimize infrared drops and stray inductance.

The PCB metal traces between V_{REF} and R_{FB} must also be matched to minimize gain error. To maximize high frequency performance, the I to V amplifier must be located as close to the device as possible.

OUTLINE DIMENSIONS

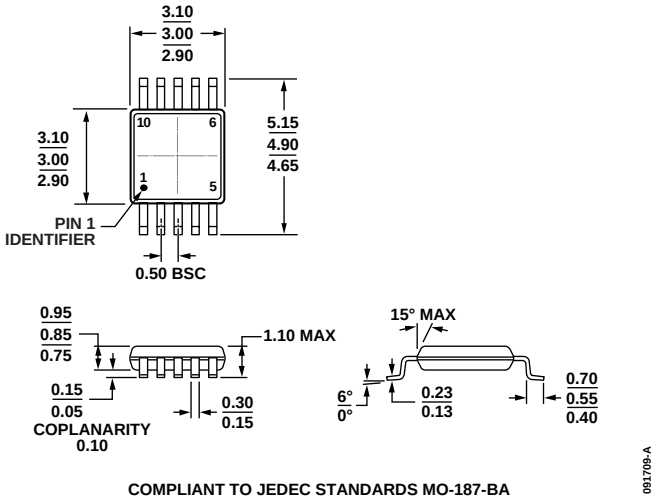


Figure 45. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Resolution (Bits)	INL (LSBs)	Temperature Range	Package Description	Branding	Package Option
AD5425YRMZ	8	±0.25	−40°C to +125°C	10-Lead MSOP	D9U	RM-10
AD5425YRMZ-REEL	8	±0.25	−40°C to +125°C	10-Lead MSOP	D9U	RM-10
AD5425YRMZ-REEL7	8	±0.25	−40°C to +125°C	10-Lead MSOP	D9U	RM-10

[1] Z = RoHS Compliant Part.

NOTES

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