L6788A

3-phase controller with embedded drivers for the next GPU generation

Features

- 1, 2 or 3 selectable phase operation
- Phases self detection
- High current internal drivers
- Versatile solution: serial and parallel VID for output voltage setting
- Serial BUS interface for power manager and monitoring
- Automatic startup phase procedure
- Advanced IC and VRM thermal management to assure robust design and safe operation
- 5 V LDO regulator output to increases design flexibility.
- Adjustable and precise output voltage
- Full differential current sense across inductor
- Differential remote voltage sensing
- LSLess startup to manage pre-biased output
- Programmable overcurrent protection
- Adjustable switching frequency
- Enable signal
- VPQFN40 6x6 mm package with exposed pad

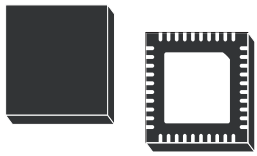
Applications

- Graphic card GPU supply
- High current DC-DC converters

Description

The device implements a one-to-three phases step-down controller with three integrated high current drivers in a compact 6x6 mm body package with exposed pad.

Output voltage can be selected trough serial and parallel VID up to 1.3500 V and managing D-VID with ±2% output voltage accuracy.



VPQFN40 - 6 x 6 mm

The device manages serial BUS communication to program power management functionalities as well as monitoring.

The device features automatic startup phase procedure and phases self detection for safe operation.

The controller embeds 5 V LDO regulator increasing design flexibility.

Advanced IC and VRM thermal management to assure robust design and safe operation.

The controller assures fast protection against load overcurrent and under / overvoltage.

L6788A is available in VPQFN 6 x 6 mm package.

Table 1. Device summary

Order code	Package	Packing
L6788A	VPQFN40	Tray
L6788ATR	VPQFN40	Tape and reel

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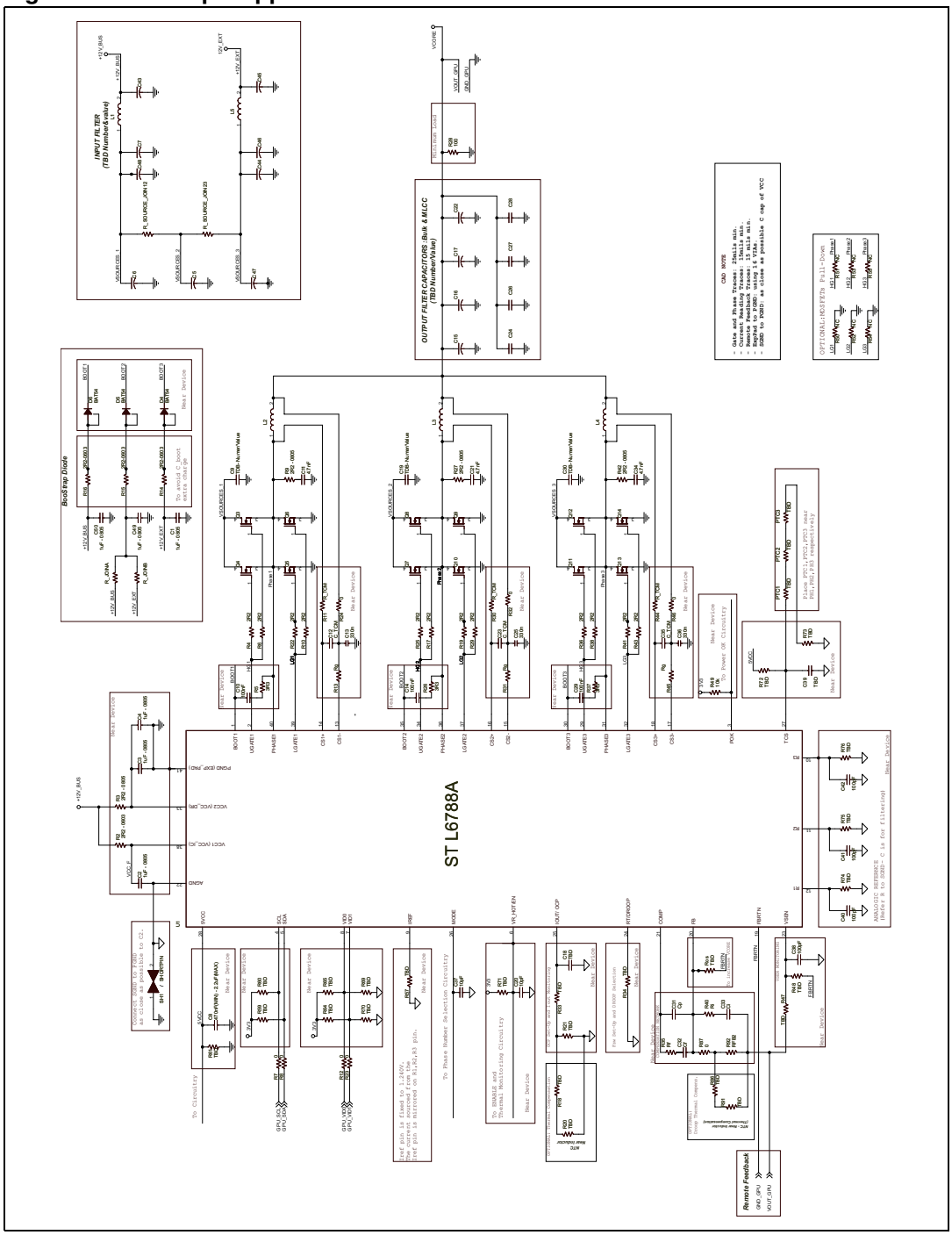
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1 Application circuit and block diagram

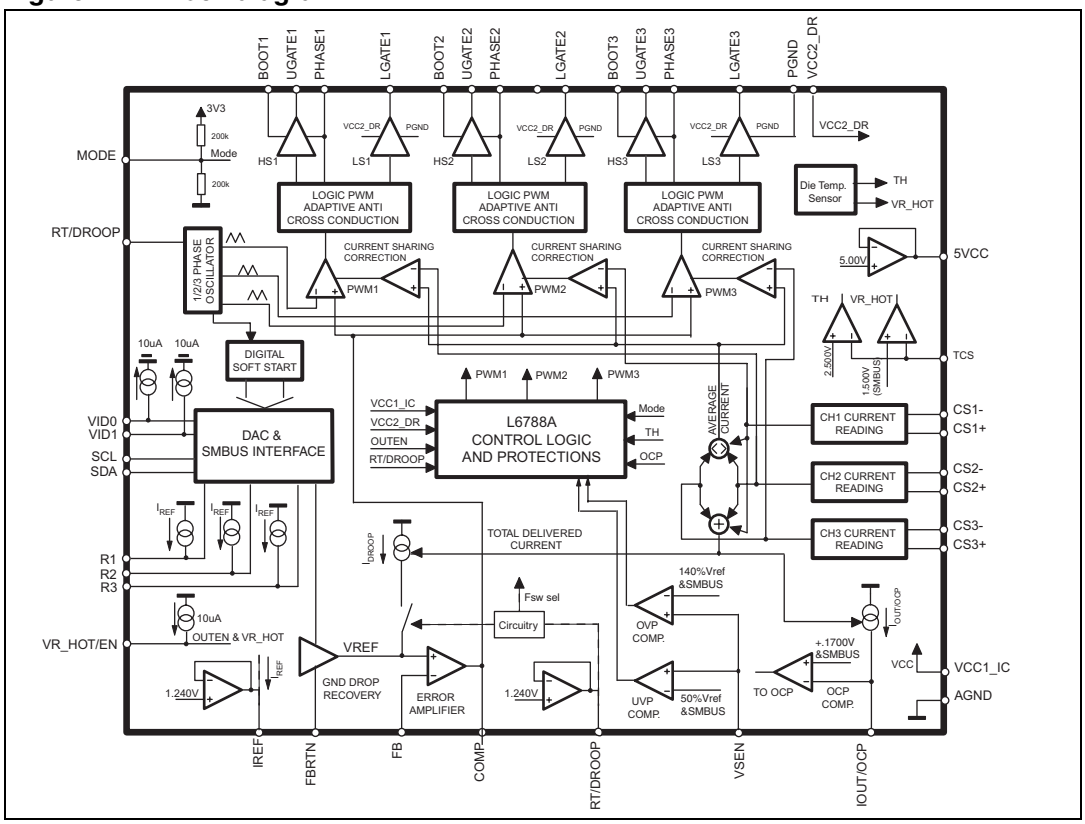
1.1 Principle application circuit

Figure 1. Principle application circuit (a)



1.2 Block diagram

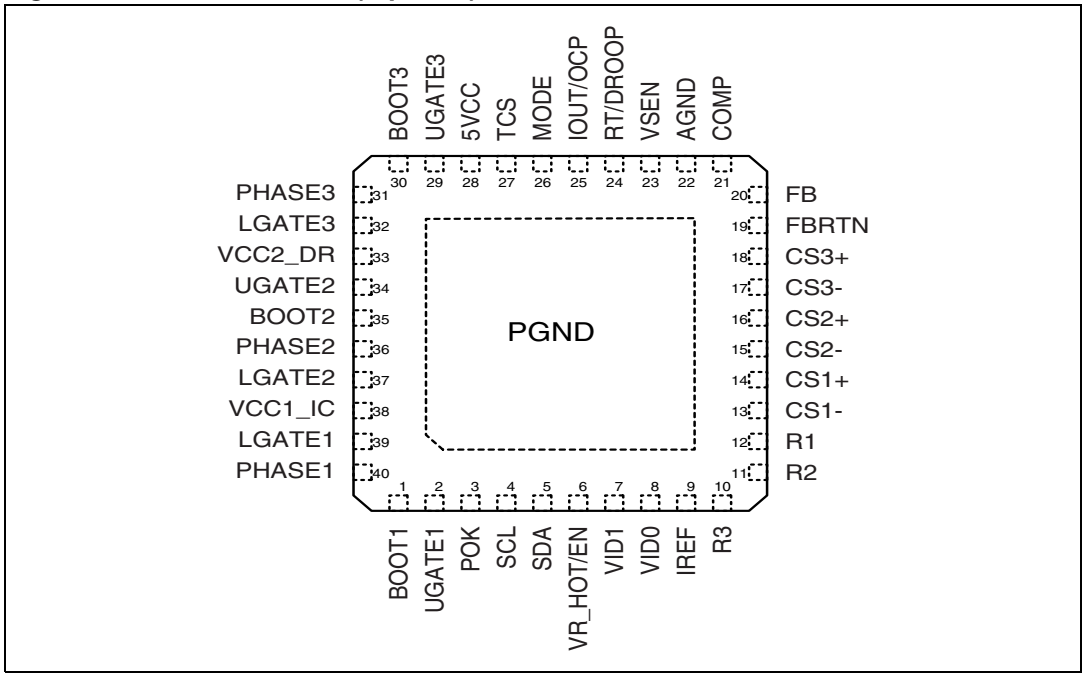
Figure 2. Block diagram



a. Refer to the application note for the reference schematic

2 Pins description and connection diagram

Figure 3. Pin connection (top view)



2.1 Pin description

Table 2. Pin description

Pin n°	Name	Description
1	BOOT1	Channel 1 HS driver supply. Connect through a capacitor (100 nF typ.) to PHASE1 Needed external bootstrap diode. The device implements Vin detections through this pin. See “vin detection” section for details. A small resistor in series to the boot diode helps in reducing Boot capacitor overcharge (see reference schematic).
2	UGATE1	Channel 1 HS driver output. It must be connected to the HS1 MOSFET gate. A small series resistors helps in reducing device-dissipated power.
3	POK	Power OK Open drain output sets free after soft start has finished and pulled low when triggering any latched protection (OVP, UVP, OCP average). Pull up to a voltage lower than 3.3 V (typ), if not used it can be left floating.
4	SCL	Serial BUS clock input.
5	SDA	Serial BUS data input.

Table 2. Pin description (continued)

Pin n°	Name	Description
6	VR_HOT/ EN	Voltage regulator HOT / enable pin. Internally pulled up by 10 µA (typ) to 3.3 V. Multifunction pin to enable/disable the system (input-signal) and to provide the information about the warning temperature (output-signal). Forced low, the device stops operations with all MOSFETs OFF: all the latched protections are disabled. Removing the short on VR_HOT/EN pin, the device starts-up implementing soft-start and the voltage at the pin is clamped by the device at 1.5 V (typ). When a warning temperature is detected the device leaves the pin floating. Thermal monitoring enabled if Vcc > UVLOVCC (See “thermal monitoring” section for details). VR_HOT/EN pin is set free when: • Either TCS pin voltage overcomes the warning threshold voltage (see TCS pin for details). • Or Tj_IC Die temperature overcomes the die warning temperature (T_HOT) Where T_HOT=T_Shutdown-T_Delta Use a pull-up resistor in the range of 10 kΩ–30 kΩ when VR_HOT/EN pin is directly pulled up to 3.3 V. (see VR_HOT/EN pin voltage Electrical Characteristic table). Cycle this pin to recover latch from protections.
7	VID1	Voltage identification pins. Internally pulled low by 10 µA. They allow programming output voltage from the 4-level “power play table” in PVID mode.
8	VID0	
9	IREF	Current reference pin. Internally fixed at 1.240 V, connecting a RIREF = 12.4 kΩ (+/-0.1%) resistor vs. AGND allows setting 100 µA current that is mirrored into R1, R2, R3 pins in order to program the three power play table levels voltage. See “power play table level” section for details.
10	R3	Default “power play table” voltage setting pins. The device sources from each Rx pin the same constant current sourced from the IREF pin (Internally mirrored). As a consequence the Voltage between Rx pin and AGND is given by the following relationship: VRx= IREF * Rx=100 µA*Rx, where IREF is the current programmed on IREF pin (100 µA). As soon as the ENABLE is released the device reads the Rx pin voltage and it stores these value. As a consequence if the power play table is re-written by serial BUS the analog values can not be recovered (voltage fixed by Rx resistor). See “power play table level” section for details.
11	R2	
12	R1	
13	CS1-	Channel 1 current sense negative input. Connect through a Rg resistor to the output-side of the channel 1 inductor.
14	CS1+	Channel 1 current sense positive input. Connect through an R-C filter to the phase-side of the channel 1 inductor.
15	CS2-	Channel 2 current sense negative input. Connect through a Rg resistor to the output-side of the channel 2 inductor. Still connect to V_{OUT} through Rg resistor when using 1-phase operation.

Table 2. Pin description (continued)

Pin n°	Name	Description
16	CS2+	Channel 2 current sense positive input. Connect through an R-C filter to the phase-side of the channel 2 inductor. Short to V_{OUT} when using 1-Phase operation.
17	CS3-	Channel 3 current sense negative input. Connect through a Rg resistor to the output-side of the channel 3 inductor. Still connect to V_{OUT} through Rg resistor when using 1 or 2-phase operation.
18	CS3+	Channel 3 current sense positive input. Connect through an R-C filter to the phase-side of the channel 3 inductor. Short to V_{OUT} when using 1 or 2-phase operation.
19	FBRTN	Feedback return. This pin is the ground return for remote sensing the output voltage. Connect directly to the point where the output voltage is to be regulated.
20	FB	Error amplifier inverting input pin. Connect with a resistor RFB vs. VSEN and with an RF - CF//CP vs. COMP pin. See reference schematic for more details. A current proportional to the load current can be sourced (in according to RT/DROOP pin status) from this pin in order to implement the droop effect. See “droop function” section for details.
21	COMP	Error amplifier output. Connect with an RF - CF//CP vs. FB pin.
22	AGND	Signal ground pin. All the internal references are referred to this pin. Connect it to the PCB signal ground (AGND).
23	VSEN	Output voltage monitor, manages OVP/UVP protections. Connect to the positive side of the load to perform remote sense. See “output voltage protections” section for more details.
24	RT/ DROOP	Operation frequency setting. Internally fixed at 1.240 V it allows programming the switching frequency FSW of each channel. Frequency is programmed according to the Rosc resistor connected from the pin vs. AGND with again of 9 kHz/µA. Leaving the pin floating programs a switching frequency of 200 kHz per phase. The device uses this pin also to enable/disable the droop function. See “droop function“ section for details.
25	IOUT/OCP	Output current indication and over current protection setting. The device sources from this pin a current proportional to the load current [(DCR/Rg)*IOUT)]. Connect a resistor from this pin to AGND to program the over current protection level. This pin is also used as output current indication. Voltage measured at this pin is proportional to the output current. External NTC can be used for temperature compensation of OCP and IOUT readings. See “over current protection “section for details.

Table 2. Pin description (continued)

Pin n°	Name	Description
26	MODE	Phase Number selection pin. The maximum voltage on mode pin has to be limited to 3.6 V. The voltage on MODE pin is used to select the number of phase used during normal operation. The device has an internal resistor divider in order to have 1.7 V on MODE pin when it is left floating. See “phase number selection” section for more details.
27	TCS	Temperature sense input pin. Connecting the PTC network between 5 VCC and AGND in order to generate on TCS pin a voltage proportional to the temperature. The device reads the TCS pin voltage and compare it with two thresholds in order to implements the warning and shutdown temperature action. See “thermal monitoring” section for details.
28	5VCC	5 VCC pin. The pin output is 5 V voltage with a minimum of 20 mAdc. The device supply the 5 VCC if VCC1_IC pin voltage is higher than 8 (typ). Filter the 5 VCC pin with a capacitor (470 nFMIN - 2.2 µF MAX) versus PGND.
29	UGATE3	Channel 3 HS driver output. It must be connected to the HS3 MOSFET gate. A small series resistors helps in reducing device-dissipated power.
30	BOOT3	Channel 3 HS driver supply. Connect through a capacitor (100 nF typ.) to PHASE3 Needed external bootstrap diode. The device implements Vin detections through this pin. see “vin detection” section for details. A small resistor in series to the boot diode helps in reducing Boot capacitor overcharge (see reference schematic).
31	PHASE3	Channel 3 HS driver return path. Connected to the HS3 MOSFET source and provides return path for the HS driver of channel 3.
32	LGATE3	Channel 3 LS driver output. Driver can support 12 V bus voltage. A small series resistor helps in reducing device-dissipated power.
33	VCC2_DR	LS driver supply. Driver can support 12 V bus voltage. Connect to 12 V_BUS and filter with RC network. (Suggested value: R = 2.2 /0805 size; C=2x1 µF MLCC capacitor vs. PGND).
34	UGATE2	Channel 2 HS driver output. It must be connected to the HS2 MOSFET gate. A small series resistors helps in reducing device-dissipated power.
35	BOOT2	Channel 2 HS driver supply. Connect through a capacitor (100 nF typ.) to PHASE2 Needed external bootstrap diode. The device implements Vin detections through this pin. See “vin detection” section for details. A small resistor in series to the boot diode helps in reducing Boot capacitor overcharge (see Reference schematic).
36	PHASE2	Channel 2 HS driver return path. Connected to the HS2 MOSFET source and provides return path for the HS driver of channel 2.
37	LGATE2	Channel 2 LS driver output. Driver can support 12 V bus voltage. A small series resistor helps in reducing device-dissipated power.

Table 2. Pin description (continued)

Pin n°	Name	Description
38	VCC1_IC	Device supply voltage pin. The operative supply voltage is 12 V ± 10%. Connect to 12 V_BUS and filter with RC network (R = 2.2 /0603 size, and C=1x1 µF MLCC capacitor vs. PGND).
39	LGATE1	Channel 1 LS driver output. Driver can support 12 V bus voltage. A small series resistor helps in reducing device-dissipated power.
40	PHASE1	Channel 1 HS driver return path. Connected to the HS1 MOSFET source and provides return path for the HS driver of channel 1.
41	PGND	Power ground pin (LS drivers return path). Connect to power ground plane. Exposed pad connects also the silicon substrate. As a consequence it makes a good thermal contact with the PCB to dissipate the power necessary to drive the external MOSFETs. Connect it to the power ground plane using 4.2x4.2 mm square area on the PCB and with sixteen vias to improve electrical and thermal conductivity.

3 Maximum ratings

3.1 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient (Device soldered on 2s2p PC board)	35	°C / W
R_{thJC}	Thermal resistance junction to case	1	°C / W
T_{MAX}	Maximum junction temperature	150	°C
T_{stg}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	0 to 125	°C

3.2 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC1_IC}, V_{CC2_DR}	To PGNDx	15	V
V_{BOOTx}-V_{PHASEx}	Boot voltage	15	V
V_{UGATEx}-V_{PHASEx}		15	V
	LGATEx to PGND	-0.3 to Vcc+0.3	V
	5VCC to PGND	-0.3 to 7	V
	SCL, SDA to PGND	-0.3 to 5.5	V
	All other pins to PGND	-0.3 to 3.6	V
V_{PHASEx}	Negative peak voltage to PGND; T < 400 ns V_{CC1_IC} = V_{CC2_DR} = 12 V; V_{BOOTx} = 8.5 V	-8	V
	Positive peak voltage to PGND; V_{CC1_IC} = V_{CC2_DR} = 15 V; V_{BOOTx} = 41 V	26	V

4 Electrical specifications

4.1 Electrical characteristics

V_{CC} = 12 V ± 15%, T_J = 25 °C unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply voltages operating conditions						
V_{CC1_IC}	Device supply voltage		10.8	12	13.2	V
V_{CC2_DR}	LS driver supply voltage		10.8	12	13.2	V
Vsuorces (VIN)	Conversion input voltage	Vsource1 = Vsource2	10.8		13.2	V
Vsource1-Vsource2	BOOTx supply current	Max difference between conversion input voltages (static condition)			2.4	V
Supply current and power-on						
I_{CC1_IC}	VCC1_IC supply current	UGATEx and LGATEx OPEN; VCC1_IC=VCC2_DR=VBOOTx=12 V		25		mA
I_{CC2_DR}	VCC2_DR supply current	LGATEx = OPEN; VCC1_IC=VCC2_DR= 12 V		6		mA
I_{BOOTx}	BOOTx supply current	UGATEx = OPEN; PHASEx to PGND; VCC1_IC=VCC2_DR=BOOTx=12 V		2		mA
$UVLO_{VCC_IC}$	VCC1_IC turn-ON threshold	VCC1_IC rising; VCC2_DR = VCC1_IC		7		V
	VCC1_IC turn-OFF threshold	VCC1_IC falling; VCC2_DR = VCC1_IC		5.8		V
$UVLO_{5VCC}$	5VCC turn-ON threshold	5 VCC rising; VCC1_IC=VCC2_DR>7		3		V
	5VCC turn-OFF threshold	5 VCC falling; VCC1_IC=VCC2_DR>7		1		V
Oscillator, soft start time and inhibit						
F_{OSC}	Default value	RT = OPEN		200		kHz
	Programmability range	RT connected to AGND	200		800	kHz
T_{rp}	Soft start time	VCC1_IC = 12 V; 5VCC = 5 V; VOUT=1.350 V; EN rising.		3	5	ms
VR_HOT/EN	ENABLE threshold	Input low			0.7	V
		Input high	1.3			V
	Pull-Up current	VR_HOT/EN to AGND		10		µA
	Voltage at VR_HOT/EN pin during normal operation	$I_{VR_HOT_EN}$ = 50 µA to 150 µA; (current sunk by VR_HOT/EN)		1.5		V
ΔVosc	Ramp amplitude			1.5		V
FAULT	Voltage at pin RT pin	OVP, UVP and OCP avg and thermal shutdown active		3.3		V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Reference and DAC						
V_{OUT}	Output voltage accuracy	V_{OUT} > 0.800 V; R_{IREF}=12.4 kΩ	-2	-	2	%
I_{RX}	R_X source current	R_{IREF} = 12.4 kΩ resistor to AGND.		100		µA
V_{IREF}	IREF pin voltage	R_{IREF} = 12.4 kΩ resistor to AGND.		1.240		V
5VCC	Accuracy	I_{5VCC} = 2 mA to 20 mA; C = 1 µF to PGND.	-2.5		2.5	%
	Maximum output current	C = 1 µF to PGND.	25			mA
VID	VID threshold; PVID mode	Input low			0.7	V
		Input high	1.3			V
	Pull-down current	VIDx to 3.3 V		10		µA
Protections						
OCP_{AVG}	Over current threshold on total output current	IOUT/OCP rising		1.700		V
I_{OCTH}	Over current threshold for each phase	I_{CSX-} rising; R_{IREF} = 12.4 kΩ resistor to AGND.		33		µA
OVP	Over voltage threshold	VSEN rising; % programmed reference voltage		140		%
UVP	Under voltage threshold	VSEN falling; % programmed reference voltage		50		%
Thermal monitor						
V_{TCS}	OT warning	TCS rising		1.500		V
	OT shut down	TCS rising		2.500		V
Soft-start end indicator						
V_{POK}	POK low voltage	I = -4 mA			0.4	V
Error amplifier						
A_O				100		dB
GBWP	Gain bandwidth product			15		MHz
SR	Slew rate	COMP = 10 pF to AGND		2		V/µs
Gate drivers						
I_{UGATEx}	High side source current	BOOTx-PHASEx = 12 V; C_{UGATEx} to PHASEx = 3.3 nF		1.5		A
R_{UGATEx}	High side sink resistance	BOOTx-PHASEx = 12 V;		2		Ω
I_{LGATEx}	Low side source current	VCC1_IC=VCC2_DR = 12 V; C_{LGATEx} to PGND = 5.6 nF		2		A
R_{LGATEx}	Low side sink resistance	VCC1_IC = VCC2_DR = 12 V;		1		Ω

Table 6. GPU table for SVID mode

STEP	VID5	VID4	VID3	VID2	VID1	VID0	VREF
1	0	0	0	0	0	0	1.3500
2	0	0	0	0	0	1	1.3375
3	0	0	0	0	1	0	1.3250
4	0	0	0	0	1	1	1.3125
5	0	0	0	1	0	0	1.3000
6	0	0	0	1	0	1	1.2875
7	0	0	0	1	1	0	1.2750
8	0	0	0	1	1	1	1.2650
9	0	0	1	0	0	0	1.2500
10	0	0	1	0	0	1	1.2375
11	0	0	1	0	1	0	1.2250
12	0	0	1	0	1	1	1.2125
13	0	0	1	1	0	0	1.2000
14	0	0	1	1	0	1	1.1875
15	0	0	1	1	1	0	1.1750
16	0	0	1	1	1	1	1.1650
17	0	1	0	0	0	0	1.1500
18	0	1	0	0	0	1	1.1375
19	0	1	0	0	1	0	1.1250
20	0	1	0	0	1	1	1.1125
21	0	1	0	1	0	0	1.1000
22	0	1	0	1	0	1	1.0875
23	0	1	0	1	1	0	1.0750
24	0	1	0	1	1	1	1.0650
25	0	1	1	0	0	0	1.0500
26	0	1	1	0	0	1	1.0375
27	0	1	1	0	1	0	1.0250
28	0	1	1	0	1	1	1.0125
29	0	1	1	1	0	0	1.0000
30	0	1	1	1	0	1	0.9875
31	0	1	1	1	1	0	0.9750
32	0	1	1	1	1	1	0.9650
33	1	0	0	0	0	0	0.9500

Table 6. GPU table for SVID mode (continued)

STEP	VID5	VID4	VID3	VID2	VID1	VID0	VREF
34	1	0	0	0	0	1	0.9375
35	1	0	0	0	1	0	0.9250
36	1	0	0	0	1	1	0.9125
37	1	0	0	1	0	0	0.9000
38	1	0	0	1	0	1	0.8875
39	1	0	0	1	1	0	0.8750
40	1	0	0	1	1	1	0.8650
41	1	0	1	0	0	0	0.8500
42	1	0	1	0	0	1	0.8375
43	1	0	1	0	1	0	0.8250
44	1	0	1	0	1	1	0.8125
45	1	0	1	1	0	0	0.8000
46	1	0	1	1	0	1	0.7875
47	1	0	1	1	1	0	0.7750
48	1	0	1	1	1	1	0.7650
49	1	1	0	0	0	0	0.7500
50	1	1	0	0	0	1	0.7375
51	1	1	0	0	1	0	0.7250
52	1	1	0	0	1	1	0.7125
53	1	1	0	1	0	0	0.7000
54	1	1	0	1	0	1	0.6875
55	1	1	0	1	1	0	0.6750
56	1	1	0	1	1	1	0.6650
57	1	1	1	0	0	0	0.6500
58	1	1	1	0	0	1	0.6375
59	1	1	1	0	1	0	0.6250
60	1	1	1	0	1	1	0.6125
61	1	1	1	1	0	0	0.6000
62	1	1	1	1	0	1	0.5875
63	1	1	1	1	1	0	0.5750
64	1	1	1	1	1	1	0.5625

Table 7. PVID mode table

VID1 (pin)	VID0 (pin)	Selected dynamic voltage table (DVT) level	Resistor strap
0	0	Level 1	R1
0	1	Level 2	R2
1	0	Level 3	R3
1	1	Level 4	R3

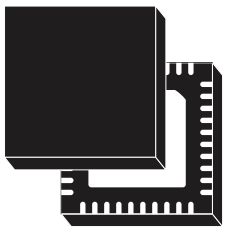
5 Mechanical data and package dimensions

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

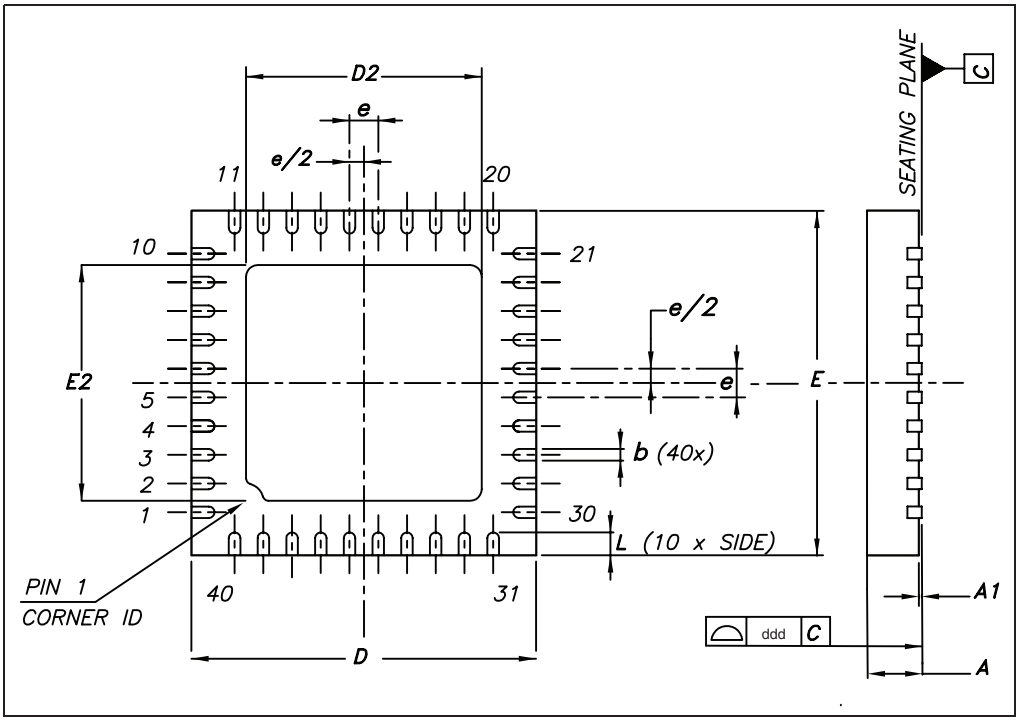
Figure 4. VFQFPN40 package mechanical data

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.800	0.900	1.000	0.031	0.035	0.039
A1		0.020	0.050		0.0008	0.0019
b	0.180	0.250	0.300	0.007	0.009	0.012
D	5.900	6.000	6.100	0.232	0.236	0.240
D2	3.950	4.100	4.200	0.155	0.161	0.165
E	5.900	6.000	6.100	0.232	0.236	0.240
E2	3.950	4.100	4.200	0.155	0.161	0.165
e		0.500			0.020	
L	0.300	0.400	0.500	0.012	0.015	0.018
ddd			0.080			0.003

OUTLINE AND MECHANICAL DATA



VFQFPN40 (6x6x1.0mm)
Very **F**ine **Q**uad **F**lat **P**ackage **N**o lead



6 Revision history

f

Table 8. Document revision history

Date	Revision	Changes
27-Jan-2009	1	Initial release
22-Jul-2009	2	Updated *Figure 2 on page 4*

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