



STD40N2LH5 STU40N2LH5

N-channel 25 V, 0.01 Ω , 40 A, DPAK, IPAK
STripFET™ V Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)} max	I _D
STD40N2LH5	25 V	0.0118 Ω	40 A
STU40N2LH5	25 V	0.0124 Ω	40 A

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses

Application

- Switching applications

Description

This STripFET™ V Power MOSFET technology is among the latest improvements, which have been especially tailored to achieve very low on-state resistance providing also one of the best-in-class figure of merit (FOM).

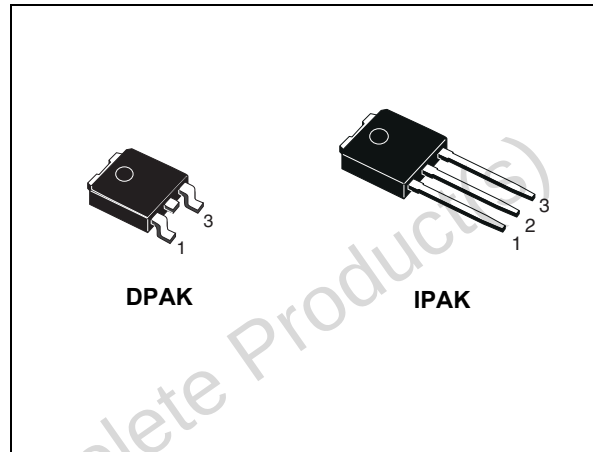


Figure 1. Internal schematic diagram

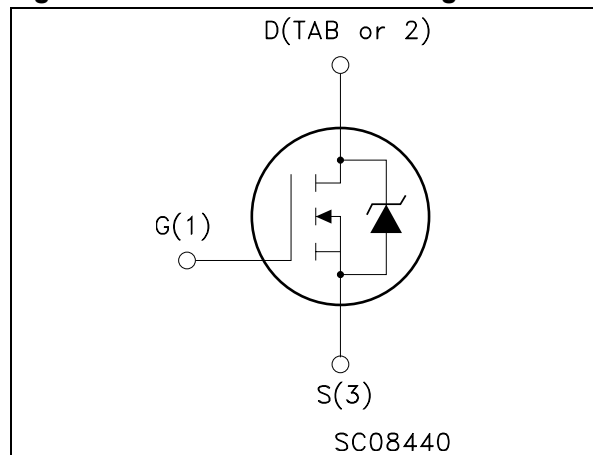


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD40N2LH5	40N2LH5	DPAK	Tape and reel
STU40N2LH5	40N2LH5	IPAK	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS}=0$)	25	V
V_{GS}	Gate-Source voltage	± 22	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	40	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	28	A
$I_{DM}^{(1)}$	Drain current (pulsed)	160	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	35	W
	Derating factor	0.23	W/ $^{\circ}\text{C}$
$E_{AS}^{(2)}$	Single pulse avalanche energy	110	mJ
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	$^{\circ}\text{C}$

1. Pulse width limited by safe operating area

2. Starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = 24\text{ A}$, $V_{DD} = 12\text{ V}$

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	4.3	$^{\circ}\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-case max	100	$^{\circ}\text{C/W}$
T_l	Maximum lead temperature for soldering purpose	275	$^{\circ}\text{C}$

2 Electrical characteristics

($T_{CASE} = 25^{\circ}\text{C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	25			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 25\ \text{V}$ $V_{DS} = 25\ \text{V}$, $T_C = 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 22\ \text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\ \text{V}$, $I_D = 20\ \text{A}$ SMD version		0.01	0.0118	Ω
		$V_{GS} = 10\ \text{V}$, $I_D = 20\ \text{A}$		0.0106	0.0124	Ω
		$V_{GS} = 5\ \text{V}$, $I_D = 20\ \text{A}$ SMD version		0.0135	0.0155	Ω
		$V_{GS} = 5\ \text{V}$, $I_D = 20\ \text{A}$		0.0141	0.0161	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 20\ \text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0$	-	700	-	pF
C_{oss}	Output capacitance			160		pF
C_{rss}	Reverse transfer capacitance			27		pF
Q_g	Total gate charge	$V_{DD} = 15\ \text{V}$, $I_D = 40\ \text{A}$	-	6.3	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 5\ \text{V}$		2.4		nC
Q_{gd}	Gate-drain charge	(Figure 14)		2.7		nC

Table 6. Switching on/off (resistive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 10\ \text{V}$, $I_D = 20\ \text{A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\ \text{V}$ (Figure 13 and Figure 18)	-	4.8	-	ns
t_r	Rise time			13.6		ns
$t_{d(off)}$	Turn-off delay time	$V_{DD} = 10\ \text{V}$, $I_D = 20\ \text{A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\ \text{V}$ (Figure 13 and Figure 18)	-	17.6	-	ns
t_f	Fall time			3.5		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		40	A
I_{SDM}	Source-drain current (pulsed) ⁽¹⁾		-		160	A
V_{SD}	Forward on voltage	$I_{SD} = 20\text{ A}$, $V_{GS} = 0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 40\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 20\text{ V}$, $T_j = 25\text{ °C}$ (Figure 15)	-	17.6		ns
Q_{rr}	Reverse recovery charge			9.2		nC
I_{RRM}	Reverse recovery current			1		A

1. Pulsed: pulse duration = 300 μ s, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

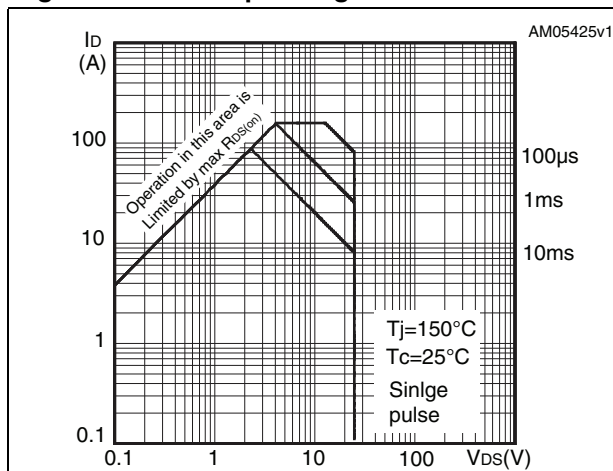


Figure 3. Thermal impedance

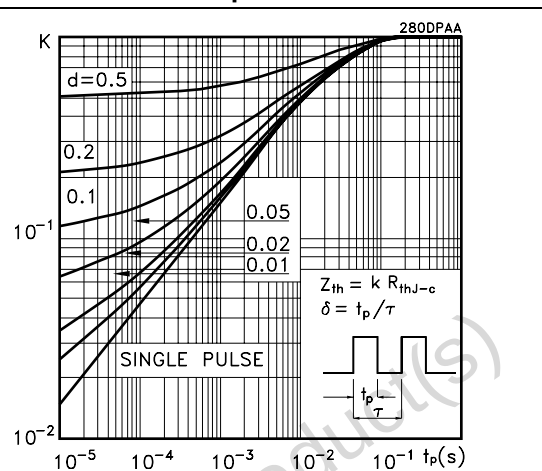


Figure 4. Output characteristics

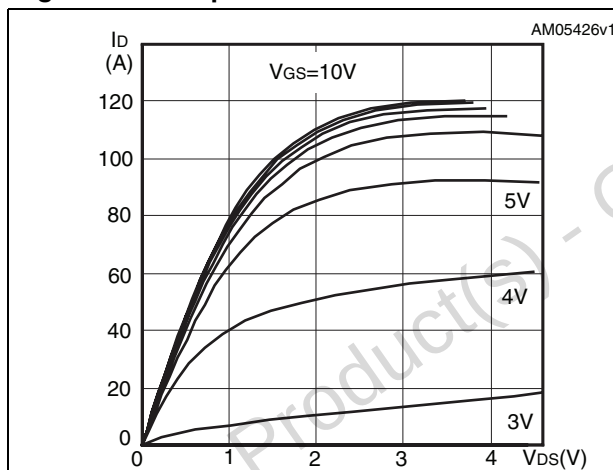


Figure 5. Transfer characteristics

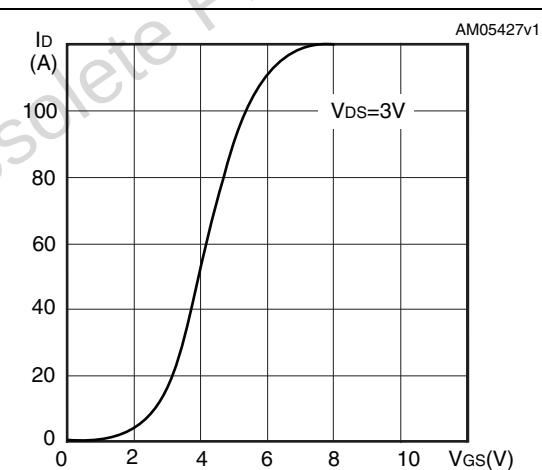
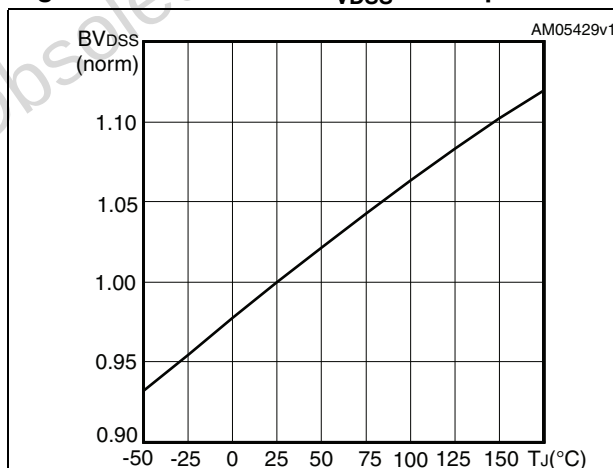
Figure 6. Normalized $B_{V_{DS}}$ vs temperature

Figure 7. Static drain-source on resistance

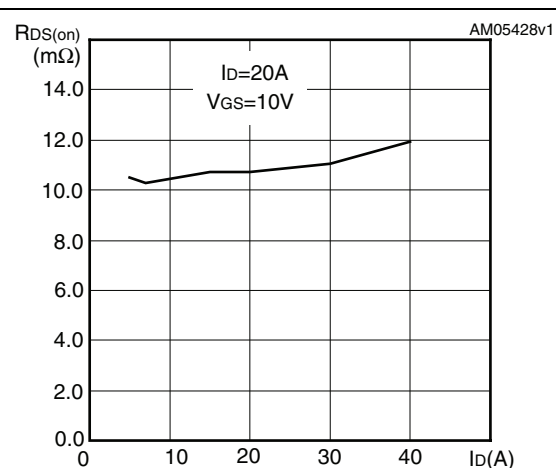


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

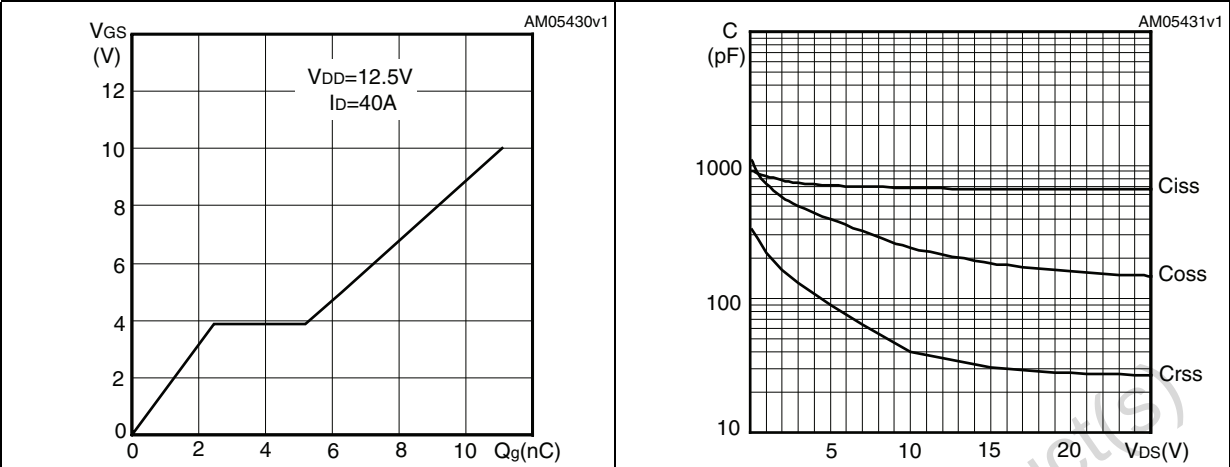


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

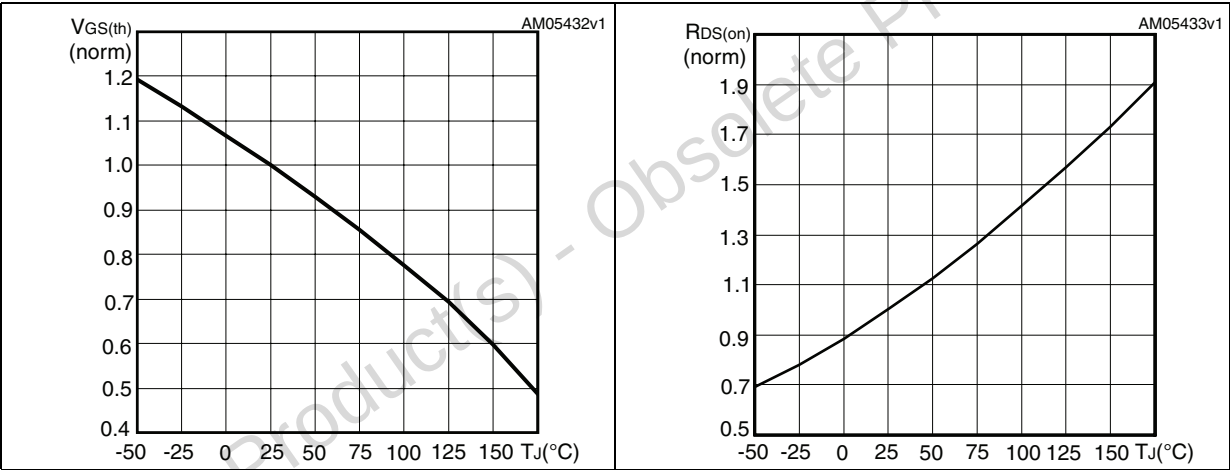
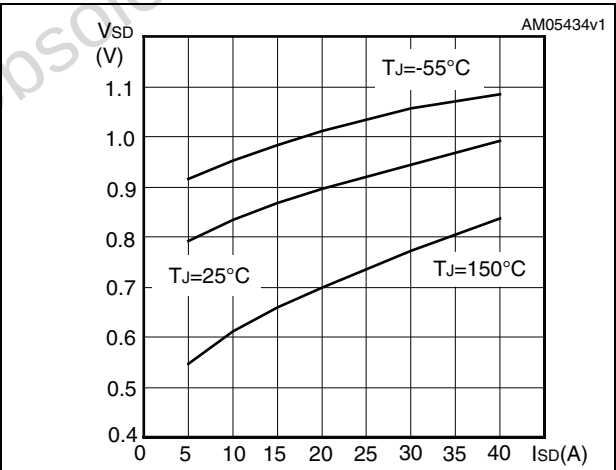


Figure 12. Source-drain diode forward characteristics



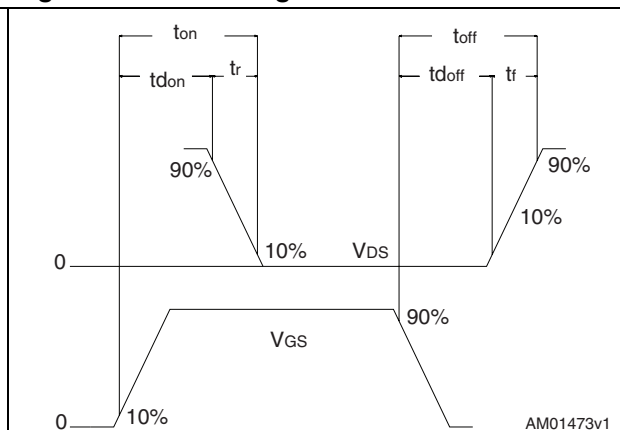
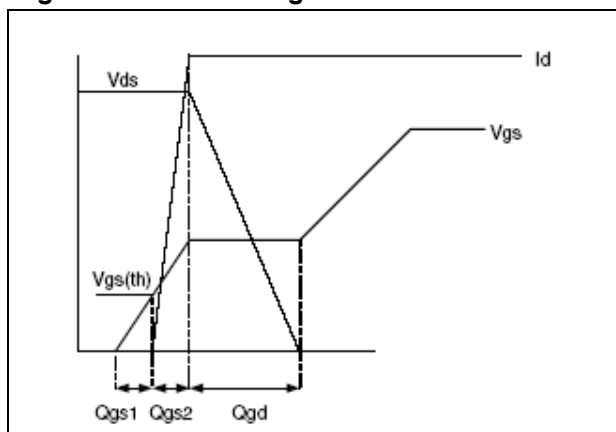


Figure 19. Gate charge waveform



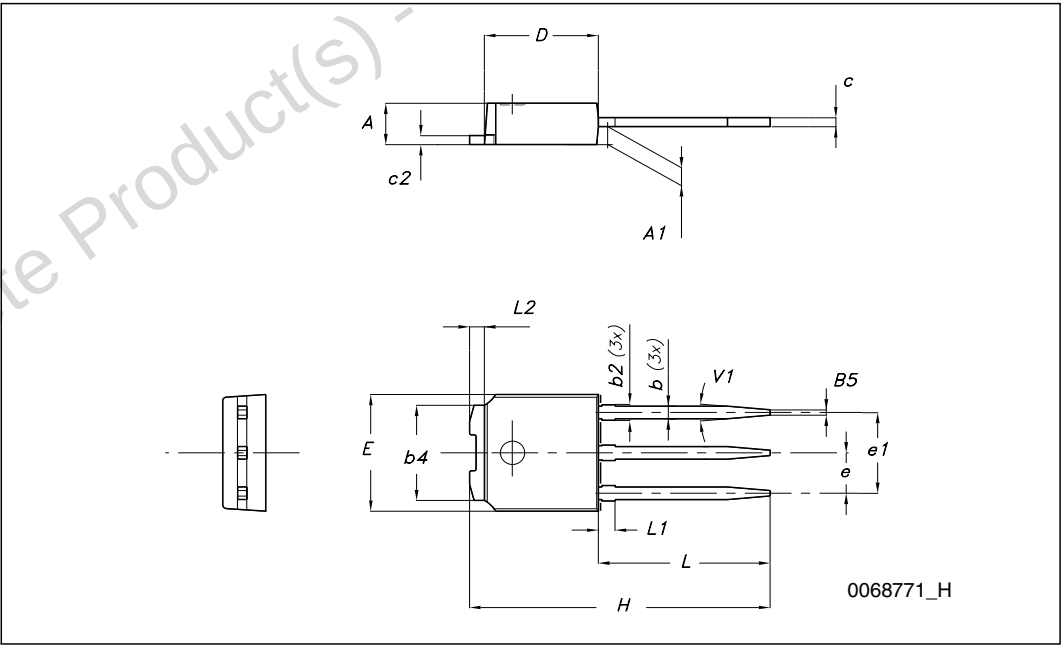
4 Package mechanical data

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Obsolete Product(s) - Obsolete Product(s)

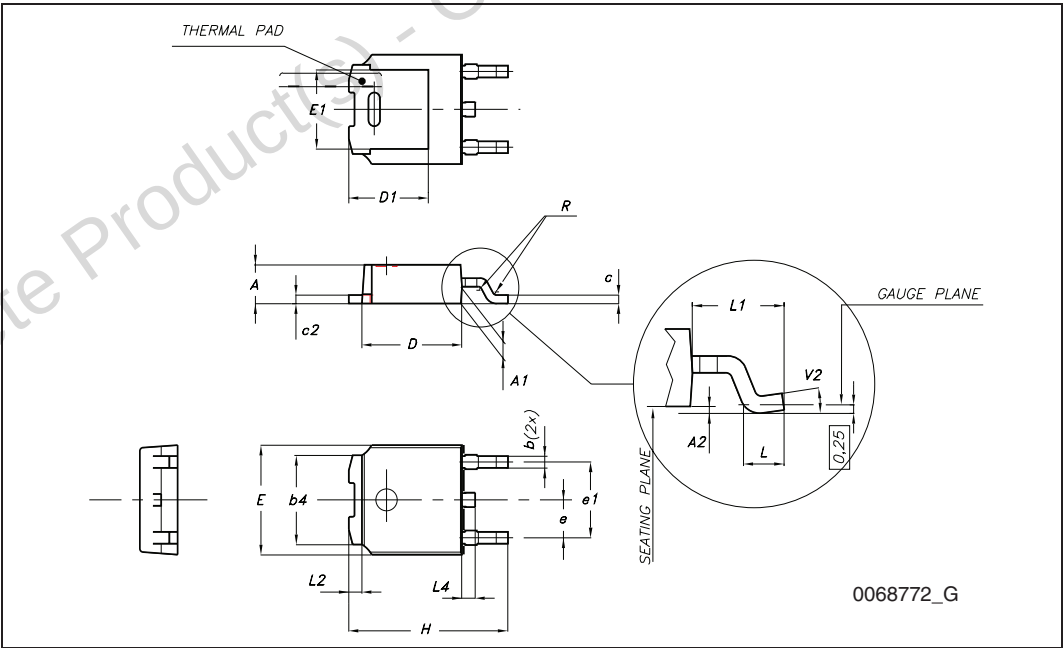
TO-251 (IPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
(L1)	0.80		1.20
L2		0.80	
V1		10°	



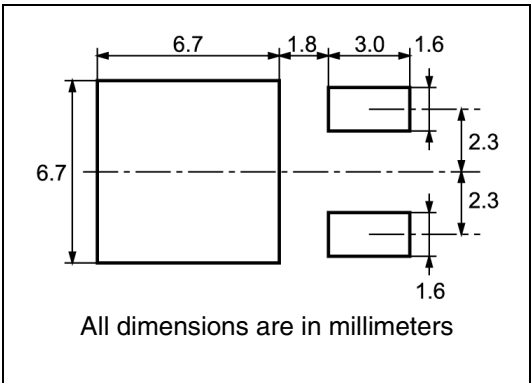
TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0 °		8 °

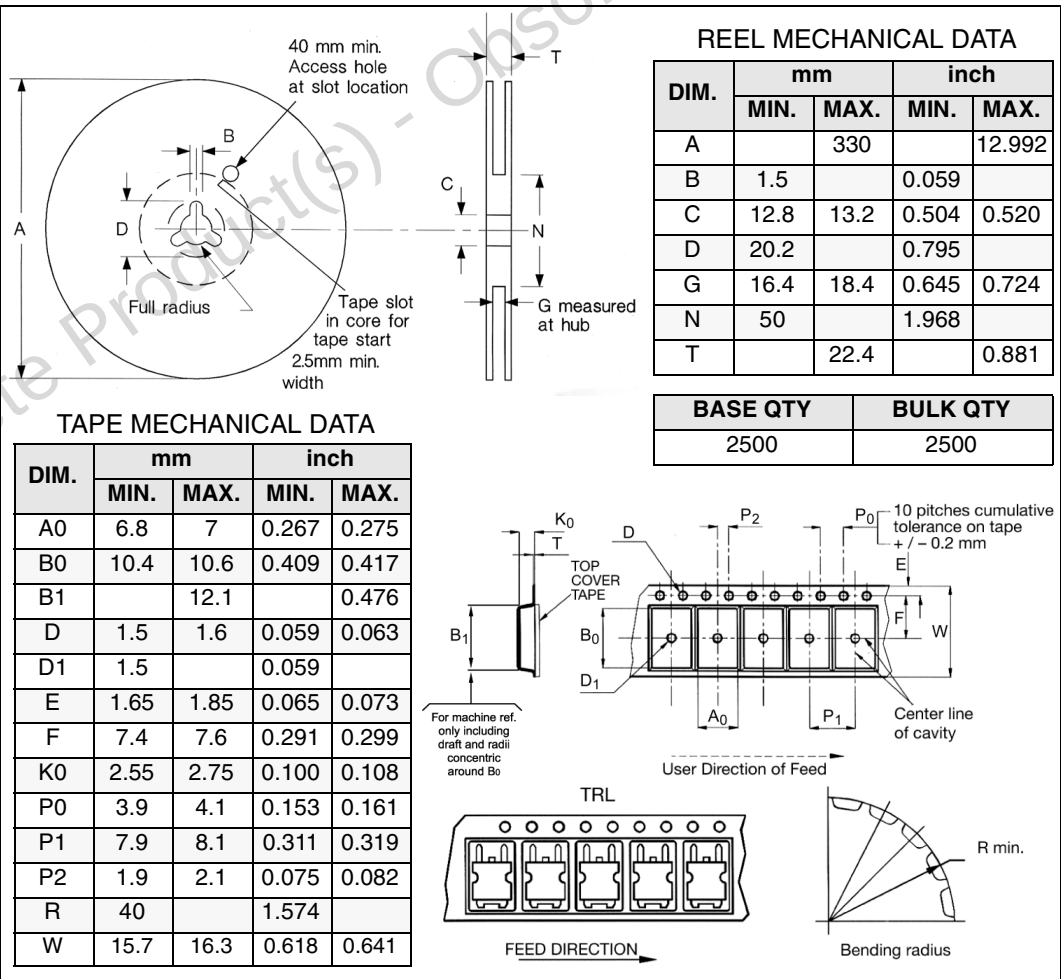


5 Packaging mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 8. Document revision history

Date	Revision	Changes
24-Jul-2008	1	Initial release
23-Sep-2008	2	V _{GS} value has been changed on Table 2 and Table 5
10-Sep-2009	3	Document status promoted from preliminary data to datasheet.

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